NC State University

Department of Electrical and Computer Engineering

ECE 463/563: Fall 2018 (Rotenberg)

Project #1: Cache Design, Memory Hierarchy Design

by

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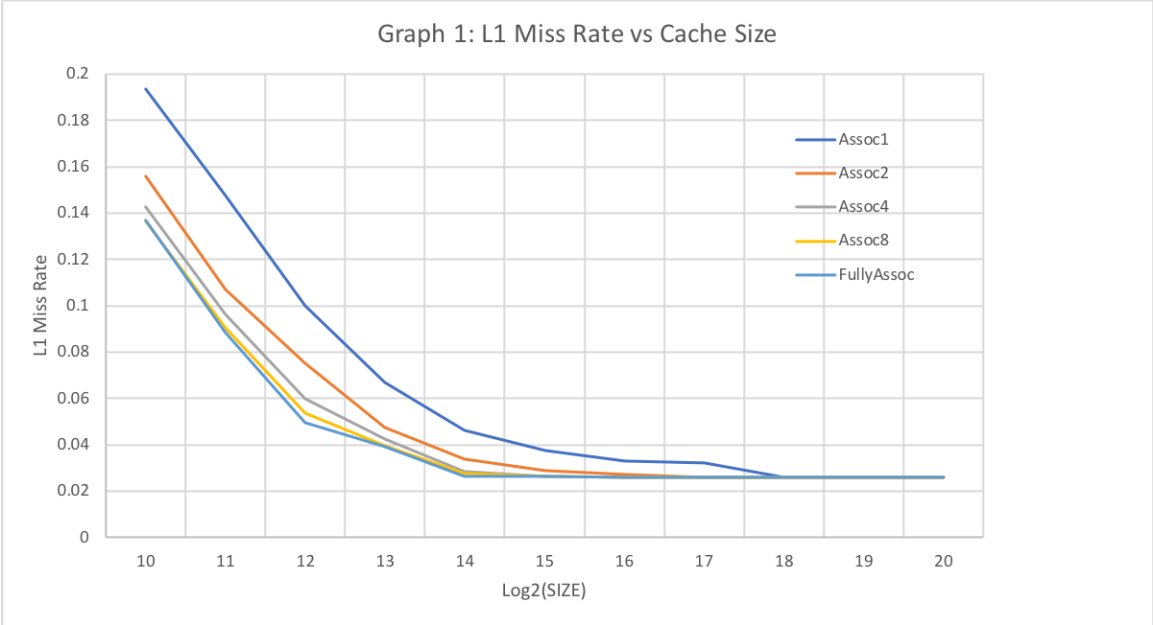
NCSU Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

Student's electronic signature: _____Vishal Ganesh Shitole_____
(sign by typing your name)

Course number: ____563___
(463 or 563 ?)

1. Graph 1



Discussion:

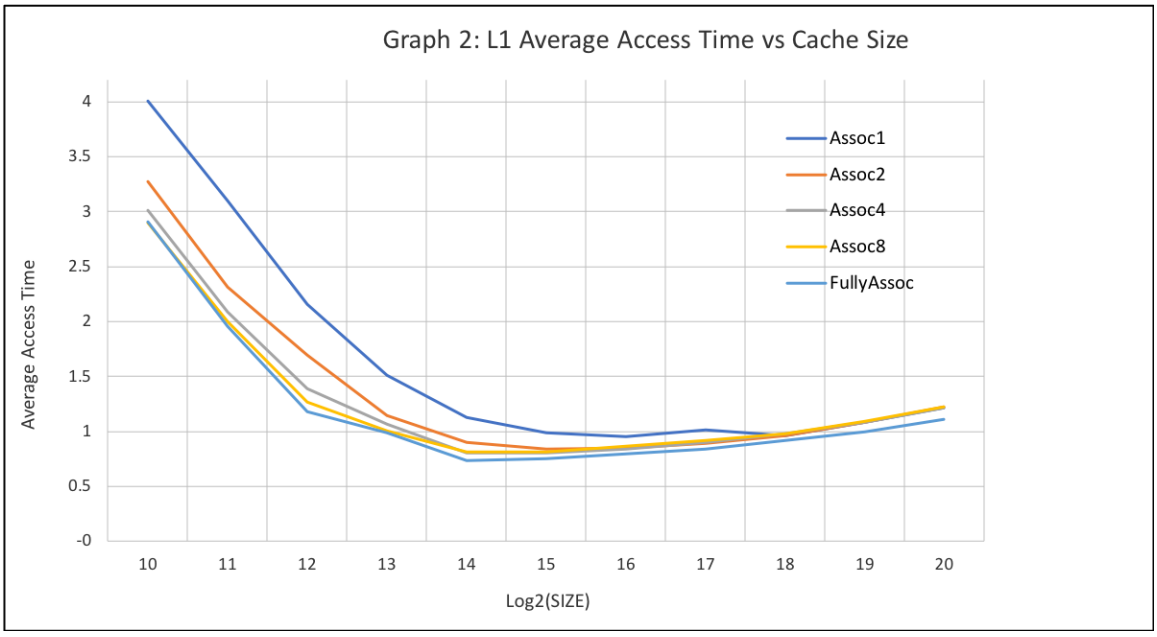
i. For a given associativity the increase in Cache Size leads to decrease in Miss Rate. This is obvious to the fact that as we make more data available in the cache we get more hits and hence decrease in Miss Rate.
We also see from the graph that an increase in associativity leads to decrease in miss rate.

ii. The part where Despite of Increasing the Cache Size we Keep getting miss rate is Compulsory Miss Rate. Thus, we see the compulsory miss rate for this system to be 0.0258

iii. The capacity miss rate for any cache size would be the miss rate of fully associative cache minus the compulsory miss rate (0.0258ns). For cache size 1Kb: Capacity Miss Rate is → 0.137-0.0258 = 0.1112.

   a. For Assoc1, the Conflict Miss Rate would be
   0.1935 – 0.137 = **0.0565,** Total Miss Rate → 0.1935
   b. For Assoc2, the Conflict Miss Rate would be
   0.1560 – 0.137 = **0.0190,** Total Miss Rate → 0.1560
   c. For Assoc4, the Conflict Miss Rate would be
   0.1427 – 0.137 = **0.0057,** Total Miss Rate → 0.1427
   d. For Assoc8, the Conflict Miss Rate would be
   0.1363 – 0.137 = **-0.0007,** Total Miss Rate → 0.1363
   Therefore no Conflict Misses
   e. For Fully Associative, the Conflict Miss Rate would be
   0.137 – 0.137 = **0.0000,** Total Miss Rate → 0.137

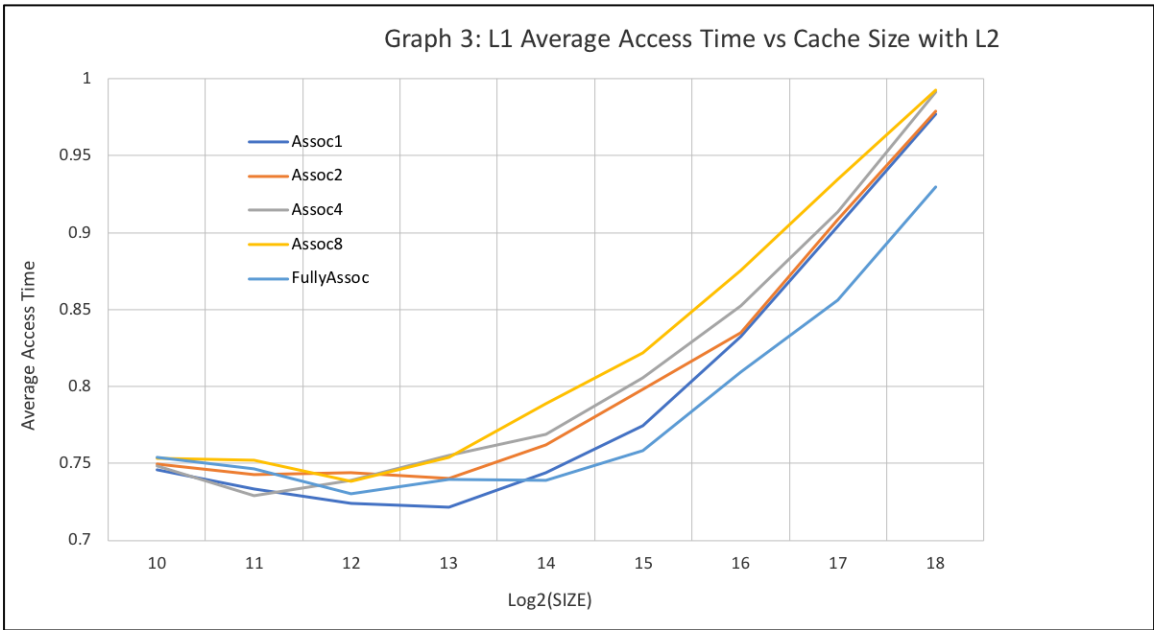
2. Graph 2



Discussion:

i. A cache size of 16Kb that is Full Associative shows the minimum Access time → 0.734238 ns

3. Graph 3



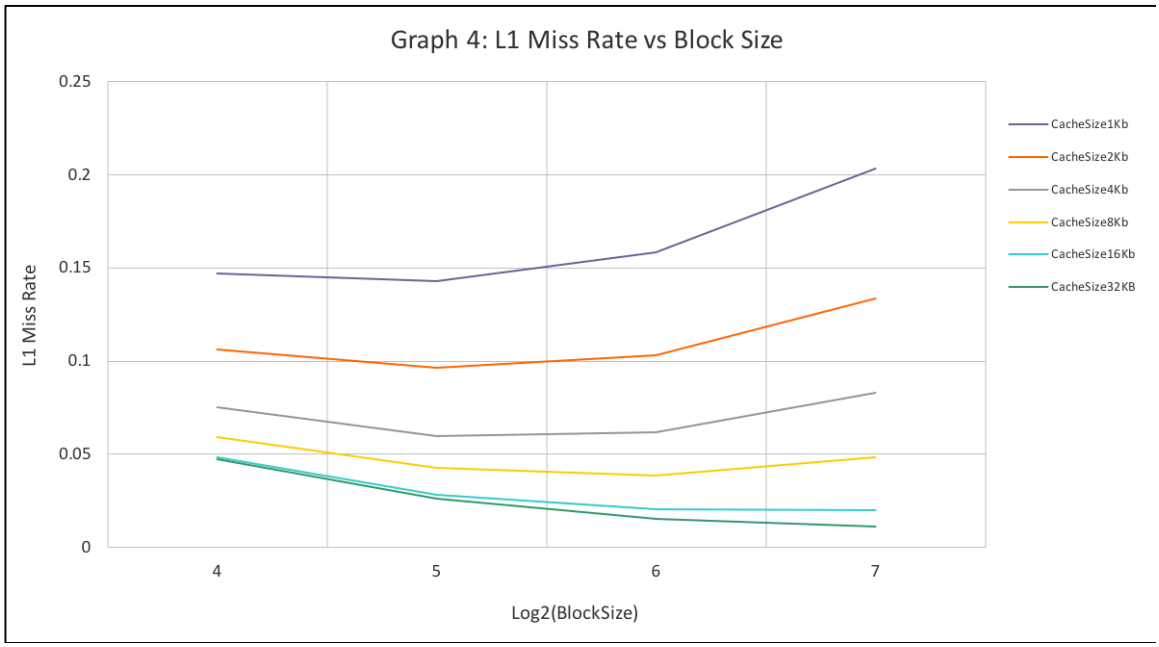
Discussion:

i. A directly mapped Cache 1 with size 4kB Fully associativity Cache shows the AAT close to the AAT of best point in Graph2 with value 0.730135

ii. The best AAT with Cache 2 is yield by the config, Cache 1 8kB directly mapped and the AAT value is 0.721586 ns and is lower by 1.72 %.

iii. The Total Area for this Config is 0.053293238 mm^2 + 2.640142073 mm^2. Whereas the Total Area for Optimal Solution in Graph 2 is 0.063446019 mm^2. There is a huge increase in total area.

4. Graph 4

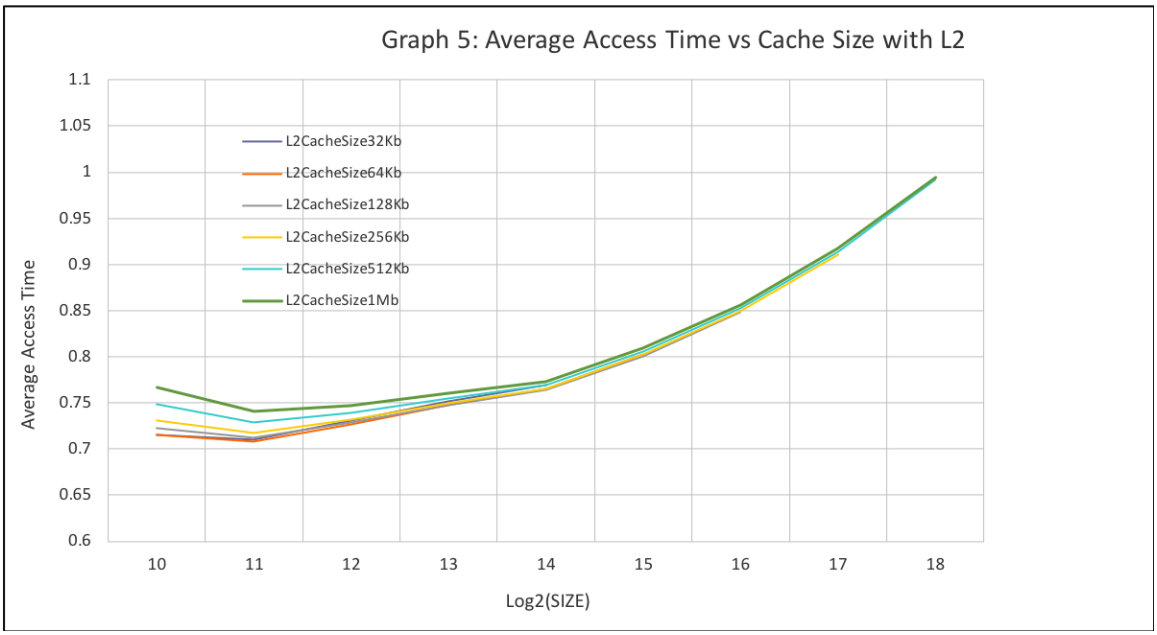


Discussion:

i. It is evident from the graph that Smaller Caches Prefer Smaller Block Sizes. We see a rate of increase in Miss Rate due to increase in block size. Also, we can see that larger block sizes prefer slightly larger block sizes. This is a result of cache pollution.

Cache pollution describes situations where an executing computer program loads data into CPU cache unnecessarily, thus causing other useful data to be evicted from the cache into lower levels of the memory hierarchy, degrading performance
The balance between increasing spatial locality versus increasing cache pollution is evident is evident from the graph and the tradeoff does shift with increase in cache sizes.

5. Graph 5

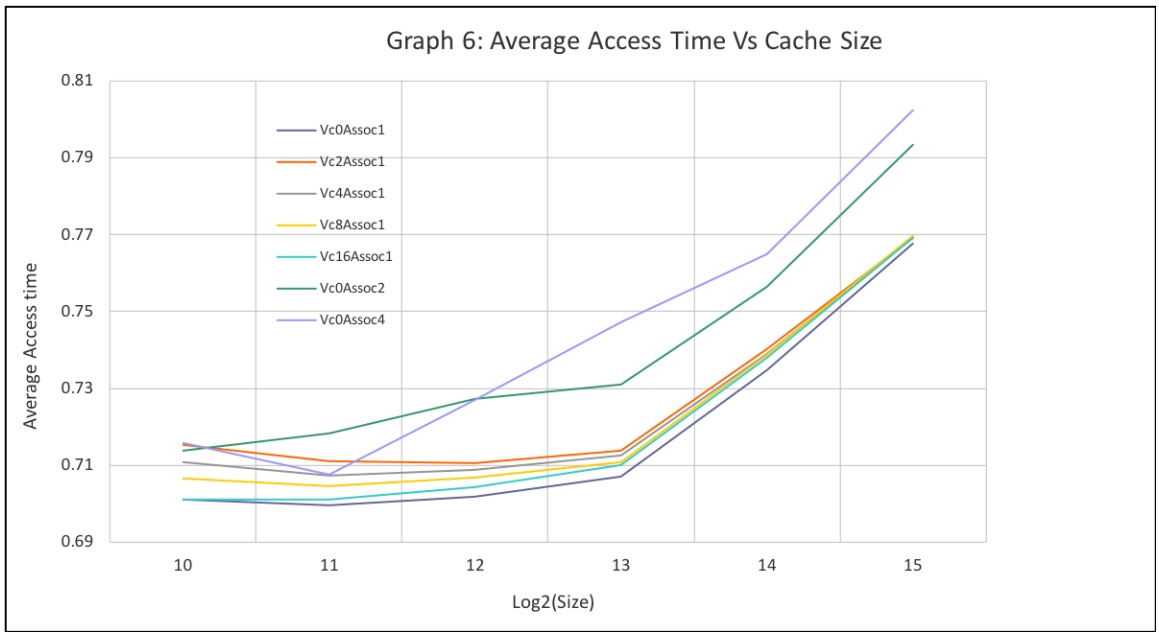


Discussion:

i. The Lowest AAT is observed for the Cache Configuration: Cache 1 : 2Kb and Cache 2: 64kb with Lowest AAT value being: 0.707657.

ii. The Lowest Area for AAT 5% range comes for the configuration L1 Cache 1kb and L2 cache is 32kb. The Lowest Area = 0.01511495(L1) + 0.24217064(L2) → **0.25728558** with the AAT Value = 0.7157522

6. Graph 6



Discussion:

i. Adding a victim cache is beneficial in comparison to Increasing Associativity. This is seen in the graph at Cache Size 2Kb(11) where Victim Cache entry is 2 the AAT is greater than Cache with Associativity 2. However for Cache Size 1Kb we see that 2 way associativity has Lower AAT than Victim Cache with 2 entries.

ii. Memory hierarchy with Cache Size 2kb and Associativity 1 Without Victim Cache has the lowest AAT = 0.699615 ns

iii. With 5% tolerance the configuration with lowest area is No victim Cache Associativity 4 and Cache Size 1kb with AAT Value 0.707657 ns