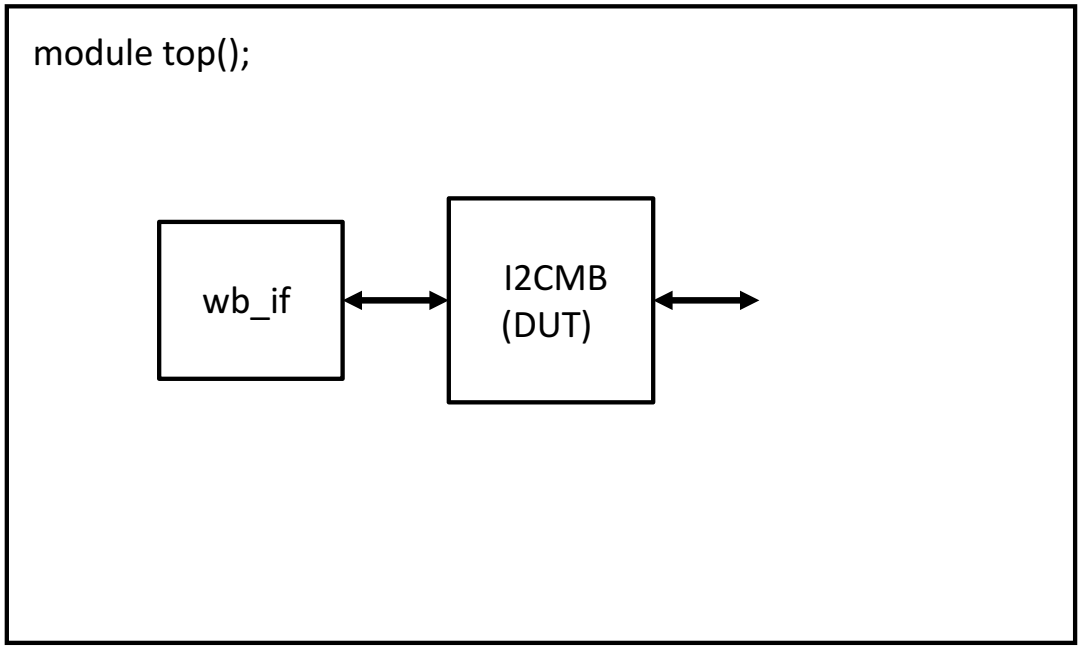
ECE 745

ASIC Verification

Lab 1 Assignment – I2CMB With Wishbone Interface (10 points of Project 1 grade)



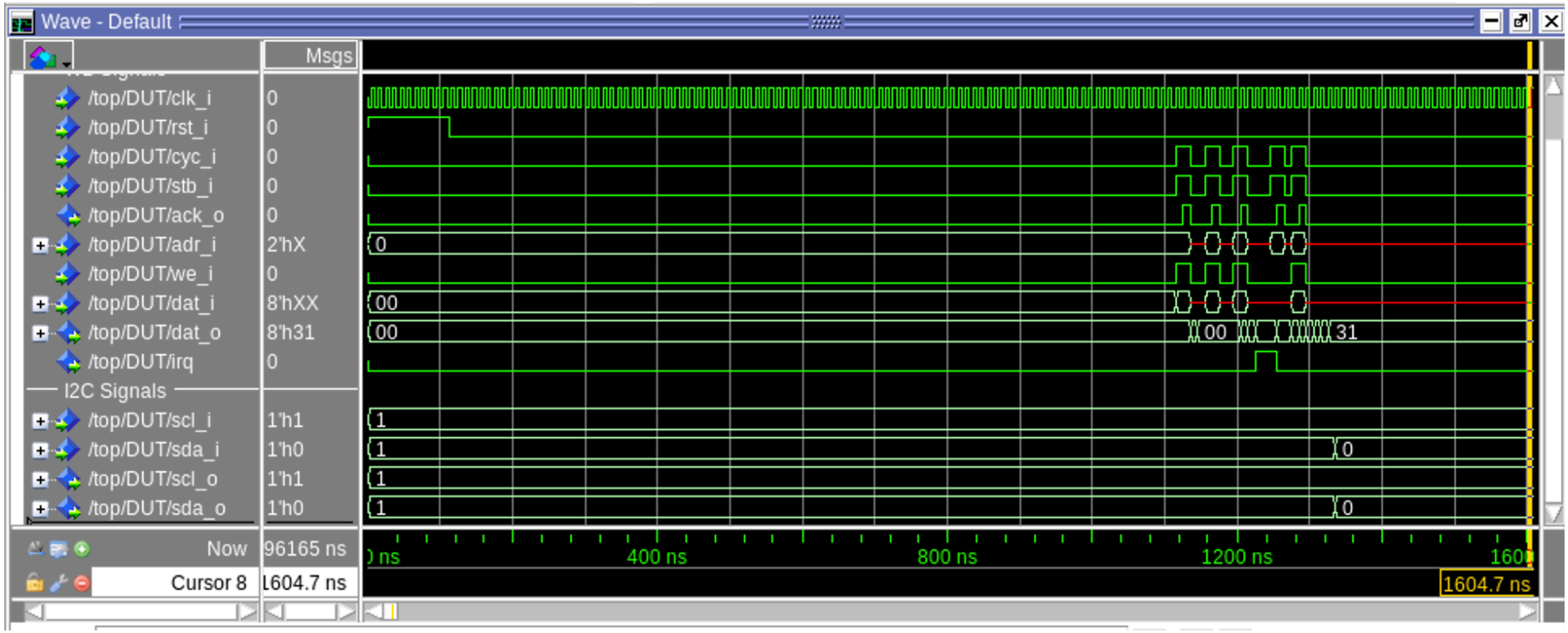
Provided in Assignment

- Directory structure
- Design Specification
- Top level module that Instantiates:
  - DUT: I2CMB
  - Wishbone Interface, wb_if
- Makefile for compilation and simulation
- Waveform format file, wave.do

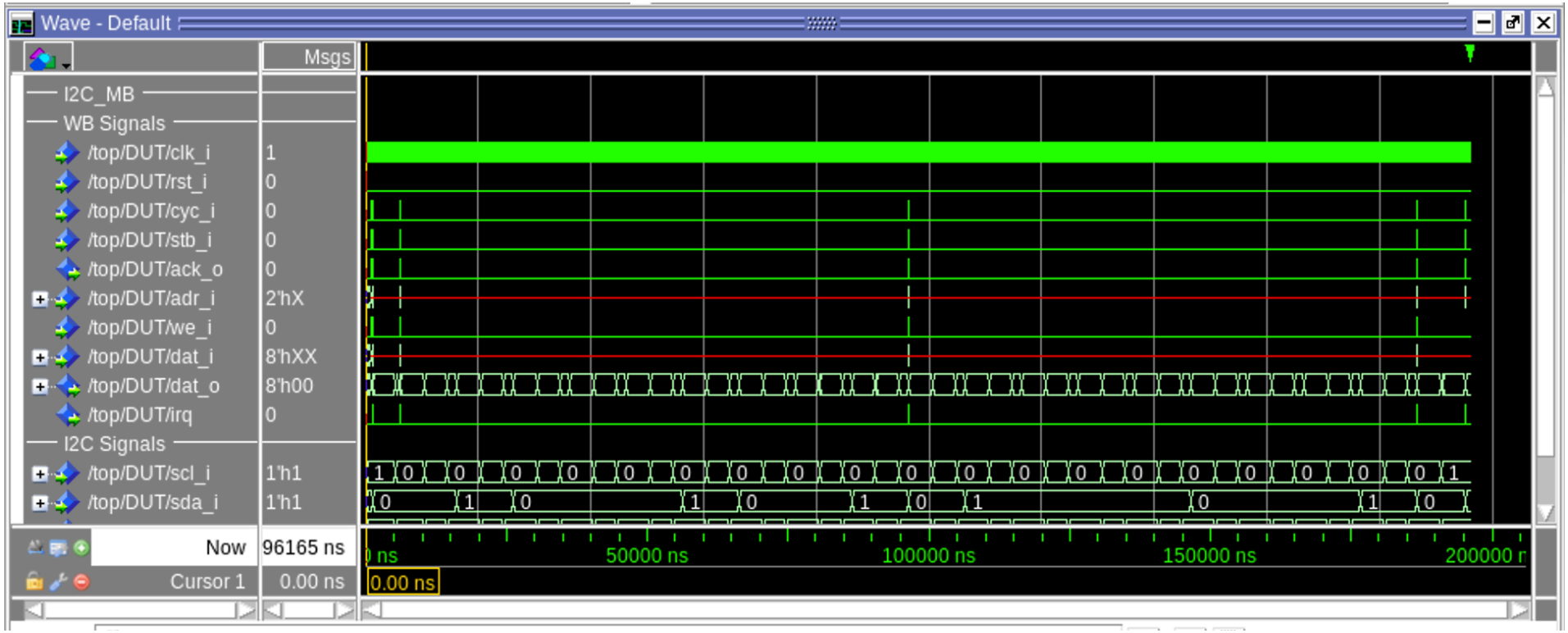
Project Instructions

- Copy ece745_projects directory from common locker to your locker
- Cd into ece745_projects/project_benches/lab_1/sim directory
- Run simulation using ‘make debug’
- Add initial block named clk_gen that generates a 10ns clock
- Add initial block named rst_gen that generates a 113ns reset
- Add initial block named wb_monitoring that
  - Calls master_monitor task within wb_if
  - Uses $display to print observed transfers in transcript
- Add initial block named test_flow that performs the steps in example one and example three of the design specification examples in chapter six

Lab Result Signaling – Zoomed In



Lab Result Signaling – Zoomed Out



Project Submission

- Submit by 11:59pm on Friday, January 25th
- Single tar file
  - Containing: ece745_projects directory and all sub-directories
  - Named: <unityId>_l1.tar
  - Execute ‘make clean’ in sim directory before creating tar file