A 20MS/s 5.6 mW 6b asynchronous ADC in 0.6μm CMOS

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Abstract

The design of an N-comparator based asynchronous Successive Approximation Analog-to-Digital Converter (SAR ADC) is described (with $N = 6$) working at 20 MS/s and consuming only 5.6 mW for low power high speed applications like communication systems. Resetting the comparators in each conversion cycle is avoided (reducing power consumption compared to [1]) and only N latches are used overall (incl. comparator latches) for the output code. Further using only N comparators instead of $2^N - 1$ as in [2], leads to huge savings in terms of area at comparable power consumption. For example, a saving of $\sim$90% comparator area is achieved for the 6 bit ADC design when compared to the design in [2].

1. Introduction

There is a constant need for high speed data converters ([3],[4]) in communication systems with low power consumption also being a major concern. The resolutions demanded are about 4-8 bits (e.g., UWB applications [5] & [6]). Asynchronous ADC (Analog to Digital Converter) design seems to be a promising way to meet this goal and has been pursued actively in the past few years ([7],[8],[9]). Of particular interest are those architectures which evolve from the SAR (Successive Approximation) scheme as in [1] and [2]. Exploring asynchronous conversion in this scheme has the advantage of retaining some of its simplistic features and at the same time one can design a class of ADCs whose performance matches the flash or the folding flash versions. A flash ADC requires as many comparators in a conversion operation as the number of quantization levels and thus taxes area and power exponentially with increasing resolution.

In this paper, an N-comparator based asynchronous SAR ADC is proposed which strikes a balance between single comparator [1] and $2^N - 1$ comparator [2] based asynchronous designs. The single comparator based ADC needs its comparator to be reset after every comparison requiring a complex clock generation block and extra resetting time as a result. The $2^N - 1$ comparator based design requires calibration and trimming to achieve all $(2^N - 1)$ embedded thresholds at its comparators and its resolution cannot be increased without an accompanying exponential increase in area. On the other hand, the N comparator based ADC proposed here doesn't require resetting of the comparators and thus can be much faster in operation. Also, this asynchronous design scales linearly with resolution facing only the same problems as a regular SAR ADC. It offers comparable performance benefits as the $2^N - 1$ design without having to lose much area. The proposed design makes use of minimal number of latches and doesn't need an encoder to output the codes. Note that the maximum input clock rate required will be the same as the conversion rate, reducing power and complexity when compared to similar synchronous designs.

In Section 2, the new asynchronous architecture along with the single and $2^N - 1$ comparator architectures is explained. Section 3 provides the implementation details of the proposed architecture for $N = 6$. Simulation results are briefed in Section 4 and finally Section 5 presents the concluding remarks.

2. Asynchronous ADC

An N bit synchronous SAR ADC which has a conversion rate of M samples/second generally needs a clock of at least $(N + 1) * M$ Hz. It works in two phases: signal track and conversion phases. In the signal track phase (1 cycle), the input is applied to the ADC. In the succeeding conversion phase (N cycles), each bit of the output code is resolved in a binary fashion mapping to one of the $2^N - 1$ quantization levels. It generally has one comparator which is reused in each of the N comparison cycles of the conversion phase. At least once in each conversion phase (i.e. in each ADC operation), the inputs to the comparator will be so close that they will cause a high resolving time. To ensure proper functioning, the cycle of the system clock

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($((N+1)*M$ Hz) should be greater than this time for minimum resolving. This clock period has to be maintained even if some of the comparisons have settled beforehand (this happens when the input difference is large) thus losing potential time savings. This limitation is done away with in an asynchronous approach, where as soon as each comparison resolves one bit of the output code, it triggers the execution of the next comparison thereby saving time. A first order upper and lower limit on the time savings when such a configuration of dynamic comparators is used is shown in [1] and elaborated in Section 2.2 where it can be seen that the order of the savings is almost $1.5-2$ times. The asynchronous approach also doesn't require an input clock greater than the conversion rate (M) itself. A start signal is still required for the entire analog to digital conversion process to begin in both asynchronous and synchronous cases. This can be the input clock edge itself in the asynchronous case.

A flash is a true asynchronous ADC since it generates the output code in one clock span. But due to the thermometric structure where input is compared with all the 2^N-1 reference levels, it consumes more power than a SAR ADC which does N comparisons over a period of N cycles (in the synchronous case). Two completely different variations of the SAR scheme retaining the N sequential comparisons/sample feature implemented in an asynchronous way are reported in [1] and [2]. We also report an architecture falling into this class. A comparison of [1] and [2] with the proposed architecture is done next. Such a comparison is justified even though their architectures might differ in some aspects because they still take similar times to perform the conversion (with N sequential comparisons) assuming all else being same.

2.1. Single, N and 2^N-1 comparator Architectures

Figure 1 shows the asynchronous SAR ADC proposed in [1]. In addition to the standard charge-redistribution DAC, SAR logic block and a comparator, it also has a ready signal generator, a multi-phase clock generator and additional latches. Each comparison output is stored in the additional latches, and a ready signal is generated simultaneously. This drives the multi-clock generator which apart from resetting the comparator also generates the signals used to control the SAR logic block and prepares the system for the next comparison.

In [2], the limitation of using a single comparator is overcome by employing a binary tree of 2^N-1 comparators with embedded threshold as shown in Figure 2. Input is applied to all the comparators all the time. The root comparator is turned on by the external start signal (same as the input clock). Depending on the comparison it enables either the

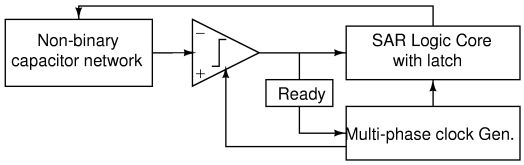

Figure 1. Single comparator asynchronous SAR ADC architecture

left child comparator or the right child comparator. Once one of the child comparators in the tree is turned on, it starts doing the next comparison making use of the embedded thresholds and then triggers one of its children. Embedded threshold in each of the 2^N-1 comparators is achieved by using intentional transistor mismatch and loading capacitor mismatch ([5],[10]). The N comparators which are turned on during the conversion phase are reset together at the start of the succeeding signal track phase (i.e. next input clock edge).

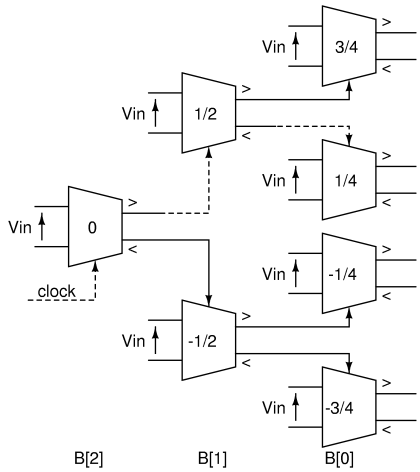

Figure 2. 2^N-1 comparator asynchronous SAR ADC architecture

The architecture proposed in this paper consists of a self clocked chain of N comparators and a standard charge-redistribution DAC as shown in Figure 3 (where $N=3$). The DAC is controlled by a latchless SAR logic core. The input is applied to all the comparators simultaneously and the first comparator is turned on by the external start signal (again same as the input clock). Once this comparator resolves, it generates a next-state trigger signal which turns on the succeeding comparator in the chain. It also causes a change in the combinational SAR logic and steers the charge redistribution DAC accordingly. The output of each dynamic comparator gives one bit of the digital code

and no further encoders or additional latches are necessary. The design thus does not require high complexity calibrations to set voltage thresholds as in the $2^N - 1$ case ([2]). Since it also doesn't require its comparators to be reset right after their comparisons are done, no additional resetting logic needs to be incorporated along with saving of resetting time. In [2], power consumption is made the same as that required by a typical SAR ADC by turning on only N comparators out of the $2^N - 1$ in each analog-to-digital conversion cycle. Though in this case power scales linearly with resolution, area on the other hand still scales exponentially. In the proposed N-comparator architecture however, both power and area scale linearly with resolution. Note that the ADC in [2] looks closer to a flash configuration than a SAR configuration at a first glance. Nonetheless, use of embedded thresholding seems to be the only diversion from a conventional SAR design too. All the three configurations described and compared here take a sum of N comparison times ($\sum_{i=0}^{N-1}(t_{i^{th}comparison})$) to do a conversion unlike the flash architecture where conversion rate is determined by the slowest comparison time ($max_{i=0,\ldots,2^N-1}\{t_{i^{th}comparison}\}$).

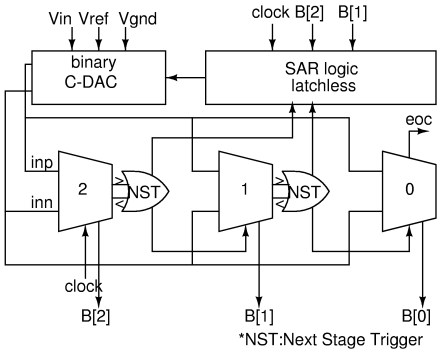

Figure 3. Proposed N comparator asynchronous SAR ADC architecture

2.2 Conversion times

If the relation between input voltage V_{diff} ($= inp - inn$) to a comparator and the resolving time T_c is given as ([1]):

$$T_c = K * ln\frac{V_{FS}}{V_{diff}} \tag{1}$$

Where V_{FS} is the full scale voltage at input, then, one can write the synchronous and asynchronous conversion times (T_{syn} and T_{asyn}) as:

$$T_{syn} = N * K * ln\frac{V_{FS}}{min(V_{diff}(i))} \tag{2}$$

$$T_{asyn} = \sum_{i=0}^{N-1} K * ln\frac{V_{FS}}{V_{diff}(i)} \tag{3}$$

Their ratio for the best case input (staircase like convergence in each step) can be shown to be

$$\frac{T_{asyn}}{T_{syn}} = \frac{1}{2} + \frac{1}{N+1} \tag{4}$$

which means that, for high conversion steps (resolution N), the speed up is almost 2 times theoretically. For N = 4, 5 and 6 this value is 0.70, 0.67 and 0.64 respectively. From a different viewpoint, this is same a saying that in the best case for 4 bits, asynchronous SAR ADCs are only 2.8 times slower than a flash ADC rather than 4 times like a synchronous SAR. Worst case and average speed up can also be worked out similarly.

3. Circuit Implementation Details

The asynchronous ADC proposed here is designed for $N = 6$. It consists of a passive T/H followed by a charge-redistribution capacitive DAC. The top plate of the capacitor array is connected to one input port of all the 6 comparators and the bottom plates of the individual capacitors are connected to three switches each (which in turn are connected to the output of the T/H (v_{in}), v_{ref} and v_{gnd}). The next stage triggering signal is generated from the *'less than'* and *'greater than'* outputs of each comparator using a NOR gate. In addition to enabling the succeeding comparator, this trigger signal is fed into the combinational SAR logic. Bitlines are resolved using the *'less than'* and *'greater than'* signals and serve as the only 'registers' in this SAR scheme as shown in Figure 3 (example with $N = 3$).

3.1. Comparator and Next-Stage Trigger

Each comparator triggers a succeeding comparator in the chain as soon as it resolves a bit as shown in Figure 4 for the actual design with $N = 6$. A capacitive DAC (see 3.2) connects to the inp and inn terminals of each of the comparators. Note that, the input load capacitance is reduced from being $\propto 2^N - 1$ to N from the design of [2]. All the comparators are dynamic with cross-coupled inverters. A pmos driven implementation is chosen similar to [2],[11] and [12] with a few variations. The comparator circuit diagram is shown in Figure 6. When the enabling signal ϕ is HI, both the latch outputs are pulled down to ground. An nmos is kept at the top of the comparator as in [2] to pull that node to a deterministic value and also to linearize the input capacitance. The pmos pair is kept matched and embedded thresholding is completely done away with. Embedded thresholding is incompatible with the proposed architecture and necessitates the use of $2^N - 1$ comparators

like a flash ([5]) or 2^{N-1} comparators as in folding flash schemes ([13],[14]). When 'ϕ' goes LO, the pmos at the top is turned on enabling the latch in the process. Further, because of the imbalance at the input terminals the currents through the two branches in the comparator change, and the latch resolves to a logic state. The comparator in [1] is accompanied by a preamplifier which has been dispensed with in this design, lowering power consumption further. The Next-Stage Trigger is a logic signal which can differentiate between the outputs (LO,LO) in the reset phase with any other state. Note that, if the comparator doesn't go into metastable state, its latch outputs will resolve into either (HI,LO) or (LO,HI) depending on the input voltage imbalance. Even when they have entered into a metastable state as shown in Figure 5, the input common mode voltage ensures that both the outputs of the latch rise from (LO,LO) to some value above LO determined by circuit conditions. A NOR gate with input threshold below this value helps in giving out a trigger signal in this case along with the normal cases (this is similar to NAND used in [1]). The comparator may remain unresolved but is prevented from stalling the chain. The bitline will reflect a previously resolved bit till the comparator makes a decision. This decision might not be the same as the decision which was assumed just before triggering the next comparator ($\sim 50\%$ of the times). The comparator which was sensed to be in metastable state thus needs to be disabled from taking a decision. This can easily be done using an additional logic gate (not shown here).

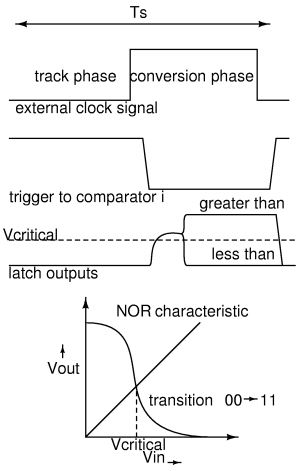

Figure 5. A timing diagram showing the operating principle of next stage triggering

There are high threshold buffers at the two outputs of the comparator depicted in Figure 6 to drive the bitline as well as the succeeding comparator through the NOR gate. High threshold avoids bus contention or instances where both the 'bitline nmos transistors' get turned on. [2] uses additional OR encoders to get the final bitline (since there are $2^N - 1$ comparators and only N final bitlines corresponding to a N bit output code). For a 6 bit design of this type, the OR encoder ties up 32 bitline nmos transistor pairs of the 32 (2^{N-1}) comparators together at the LSB stage. And only one comparator's bitline nmos transistor (either the top or the bottom one which got switched on) has to drive all the other 63 transistors (or equivalent load capacitances). This issue has been avoided in the present architecture since exactly N bitlines are present.

The output code is preserved till the beginning of the next ADC conversion phase irrespective of resetting because resetting the comparators in the signal track phase will make the bitlines float and keep the voltage value unchanged. Note that the comparator next in the chain is triggered by the one before it after a delay as shown in Figure 7. This delay is to account for DAC settling and the speed of the combinational SAR logic core.

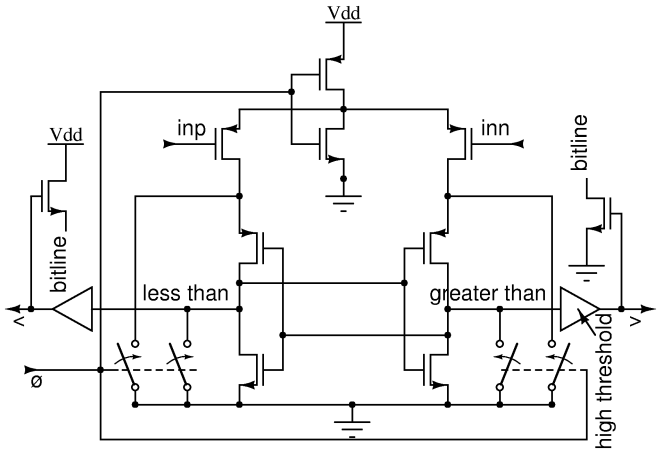

Figure 6. Circuit schematic of the comparator

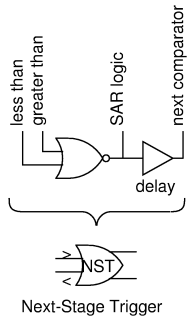

Figure 7. Next stage trigger

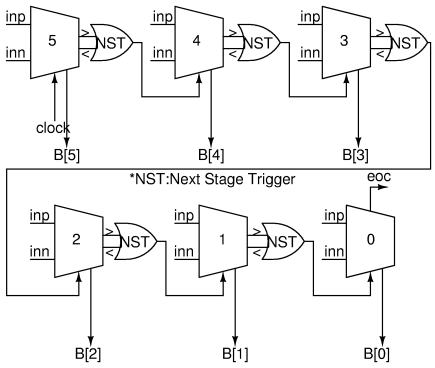

Figure 4. The N comparators connected as a chain

3.2. Binary C-DAC (Capacitor based Digital to Analog Converter)

Switched capacitor (or charge-redistribution) DAC ([15]) has been used in a straight forward manner here. The advantage w.r.t a resistive one is that the accuracy and linearity of the DAC (and in turn of the ADC) is achieved by default by the high-accuracy photolithography process (which controls the capacitor plate area and capacitance matching). For higher resolutions however, binary weighted capacitor array becomes too large for switching. One might have to go for modified DACs and switching sequences (for example, by using a multi-stage network [16] or a coupling capacitor). A dummy capacitor array is connected to the second input of the comparators to neutralize loading effects when the input is applied and removed on the bottom plates of the capacitor array connected to the first input. Input capacitance depends on the unit capacitance one uses, multiples of which will constitute the capacitive DAC. Since this portion has been implemented in a conventional manner with little optimization in an analog 0.6μm technology, the total input capacitance turns out to be high (see Section 4 and Table 2).

3.3. Digital Core without Latches

Significant power gains have been achieved by removing redundant latches/registers in the SAR logic core. The only latches present are those in the dynamic comparators which directly set the bitlines. Loading effects on the C-DAC switch driving lines differ and have been taken into consideration. For the 6 bit design, 40 basic gates constitute the SAR logic as listed in Table 1.

Gate	Count
And	18
Inverter	15
Or	5
Nand	2
Total	40

Table 1. Gates used in SAR Logic

4. Results

The 6 bit design was simulated in a 0.6μm $5V$ analog CMOS process with a full scale voltage of $2.5V$. Power consumption and other features are listed in Table 2 along with those reported in the literature. The important difference is that the other two implementations are in digital $\sim 1V$ CMOS thus giving better performances (e.g., power). Nonetheless, the performance results of the design using the 0.6μm 5V analog CMOS process (this technology is preferred for high resolution SAR ADCs) suggest that significant gains can further be made by voltage and technology scaling. No specific effort has been made to reduce the input capacitance (which will require a change in the DAC structure). The offsets of the comparators due to size mismatch and loading mismatch limits the resolution of the present scheme, among other things. Note that the difference in the offsets of different comparators is avoided in [1], and at the same time, is purposefully introduced and indispensable to the working of the state-of-the-art Asynchronous ADC in [2]. SFDR (Spurious-Free Dynamic Range) and PSD plots at simulation stage are not very relevant as post fabrication metrics can significantly differ and hence have not been shown here. [1] presents a time interleaved (TI) ADC housing two single-comparator sub-units and hence its performance metrics are slightly different (refer Table 2). Time interleaving has not been done here since it is a standard concept and requires considering analog or digital calibration to counter offset mismatch, gain mismatch and phase skew across channels.

Architecture (comparators)	Single ([1])	$2^N - 1$ ([2])	N (proposed)
Resolution	6	7	6
Process (CMOS)	130nm 1.2V digital	90nm 1V digital	**600nm 5V** analog
Input Cap.(pF)	0.09	0.25	3.2
Conv. Rate (MS/s)	600 (TI)	150	20
Peak SNDR (dB)	34	40	35.2
Efficiency (pJ/step)	0.22	0.01	5.985
Power(mW)			
Analog	1.2	0.089	0.75
Digital	4.1	0.044	4.84

Table 2. Comparison of the three asynchronous SAR architectures. Note that [1] is Time Interleaved.

5. Conclusion

Design of an asynchronous ADC which takes advantage of faster comparison cycles to perform the conversion has been detailed. With clock requirement equal to the sampling rate (unlike synchronous SARs), its area and power consumption scale linearly with resolution. Comparison with two other similar architectures has been done and a 6bit version has been simulated which works at 20MS/s. The limitation on the the clocking in synchronous case was governed by the slowest resolving time. Here, this bottleneck has been done away with. This ADC is faster than synchronous SAR ADCs and can be increasingly relevant in non-uniform sampling systems in areas like communication and imaging (e.g. MRI). When compared with a 4 bit flash for example, such an ADC is about 2.8 times slower instead of being 4 times slower like a synchronous SAR (see Section 2.2).

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