CHAPTER 9

LATCHES AND FLIP-FLOPS

9.1 Introduction

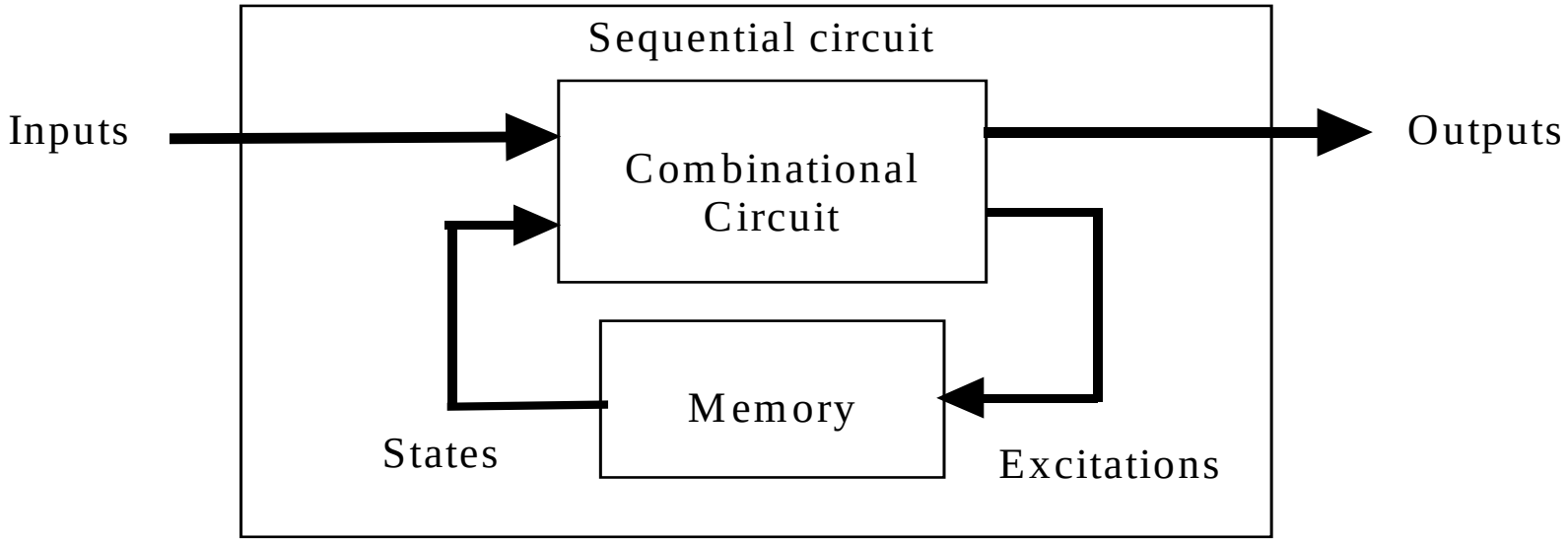


Figure 9.1 Structure of a sequential circuit.

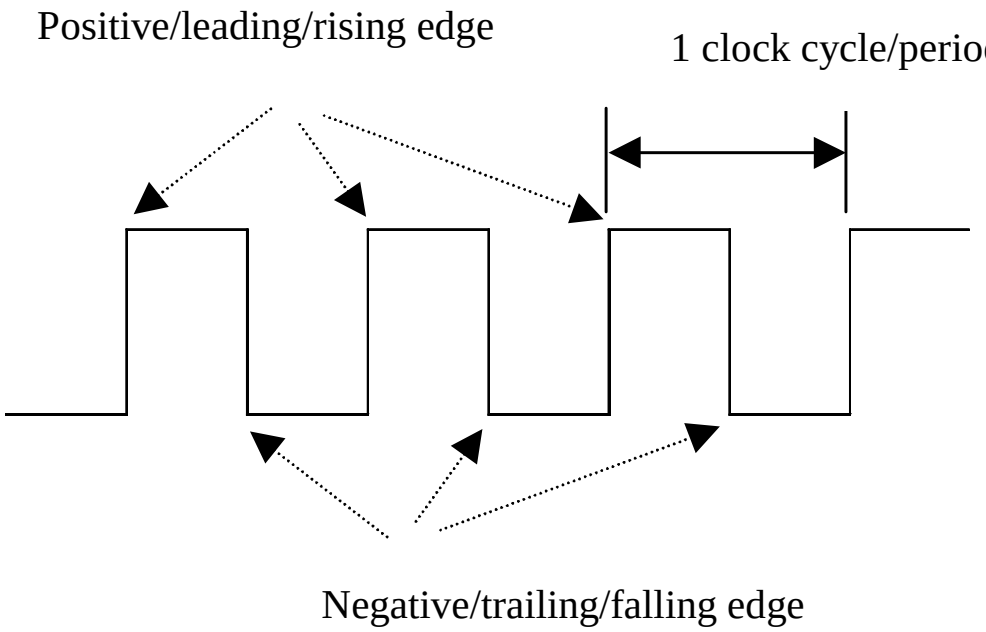


Figure 9.2 Clock for a synchronous sequential circuit.

9.2 SR Latch

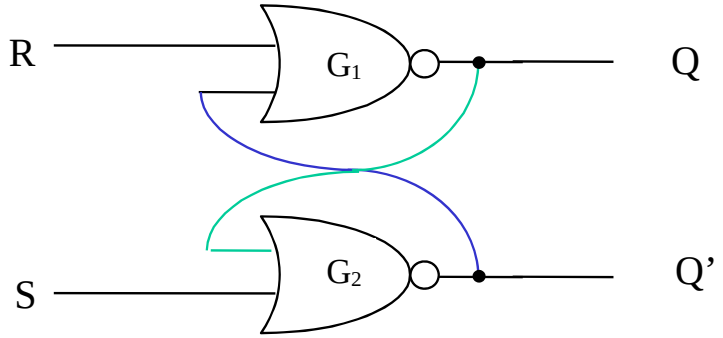


Figure 9.3 A cross-coupled NOR SR latch.

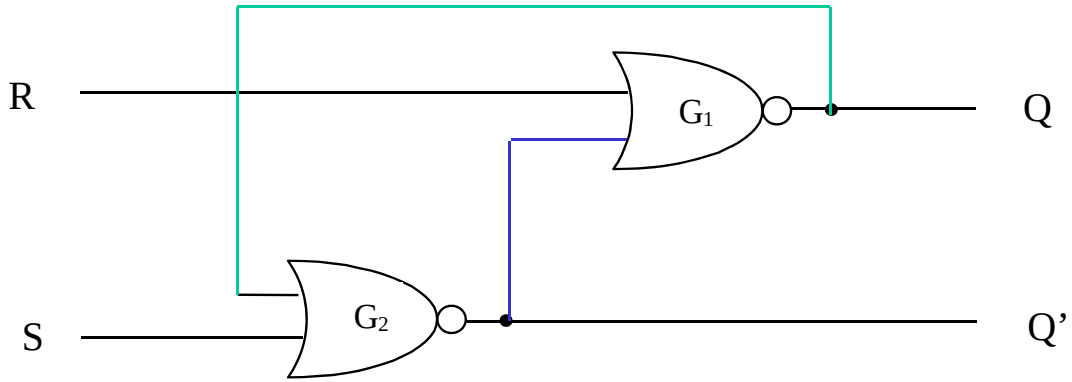


Figure 9.4 Timing diagrams for the cross-coupled NOR SR latch.

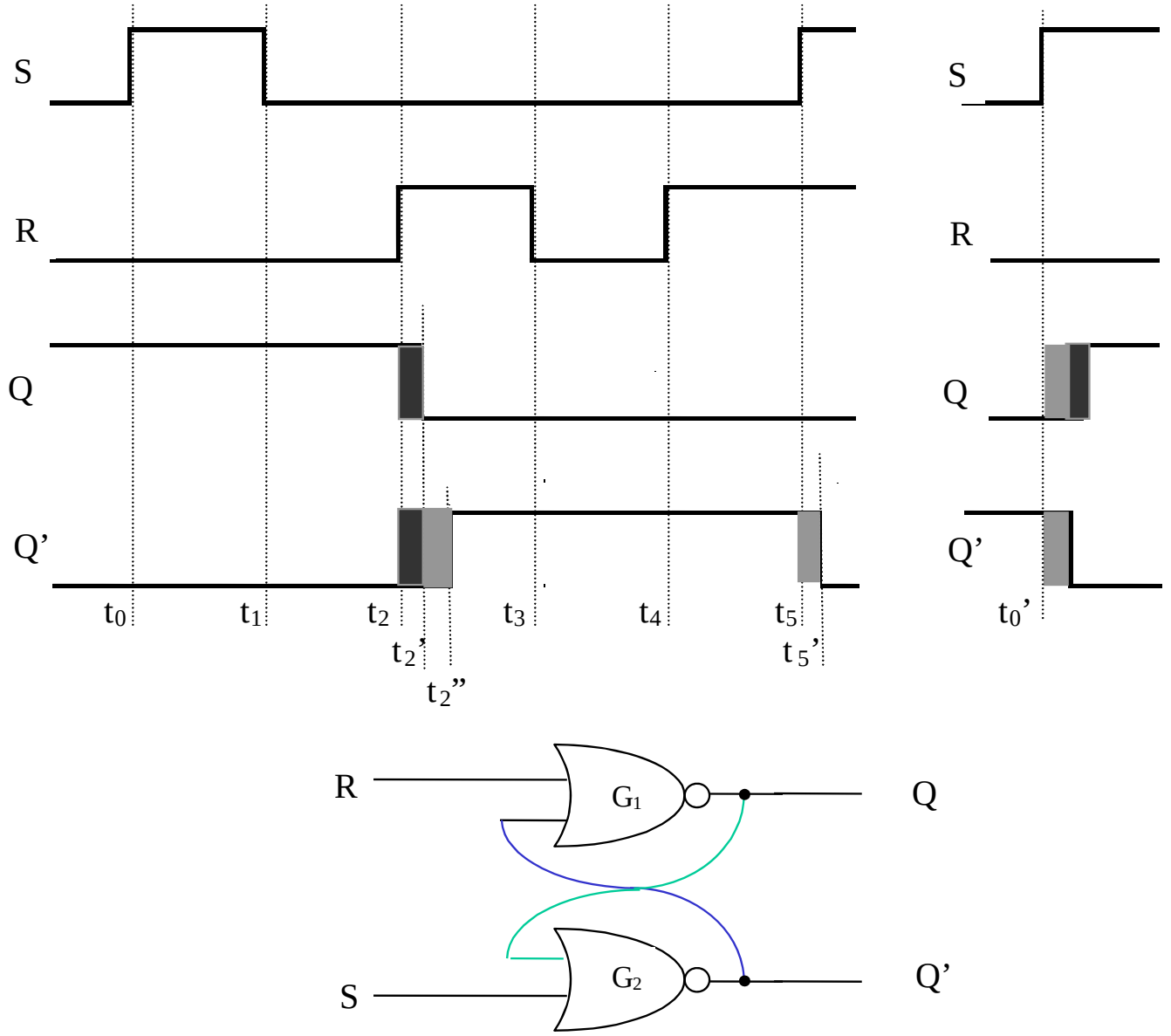
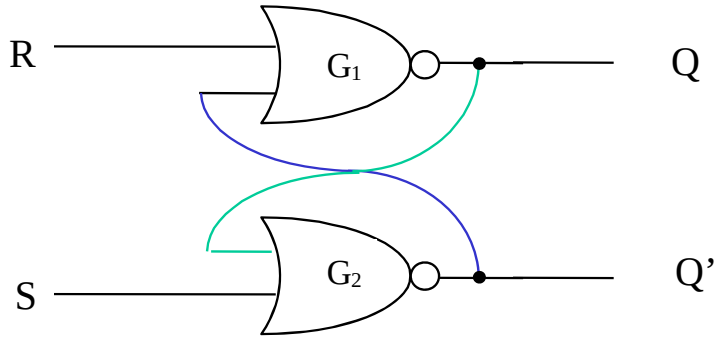


Table 9.1 Characteristic table for SR latch.

Present inputs S R	Present state Q	Next state Q^+	Function	
0 0	0	0	Hold (No change)	t_3
0 0	1	1		t_1
0 1	0	0	Reset	t_4
0 1	1	0		t_2,
1 0	0	1	Set	t_0,
1 0	1	1		t_0
1 1	0	d	Prohibited	t_5
1 1	1	d		



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1 0	0	1	Set	t_0’
1 0	1	1		t_0
1 1	0	d	Prohibited	t_5
1 1	1	d		

Characteristic equation: $Q^+ = S + R'Q$ $SR = 0$

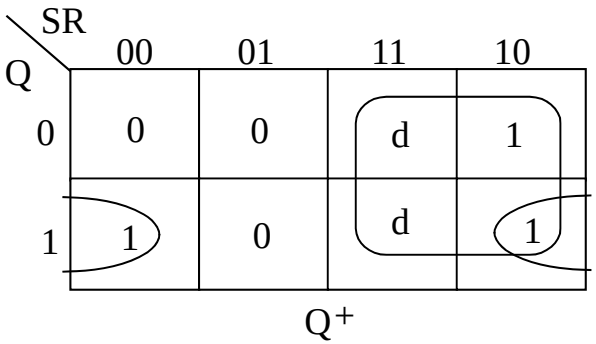


Figure 9.5 Next-state map for SR latch.

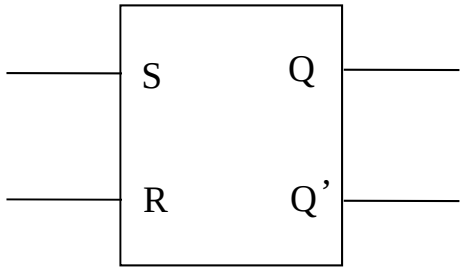


Figure 9.6 Logic symbol for SR

Gated SR Latch

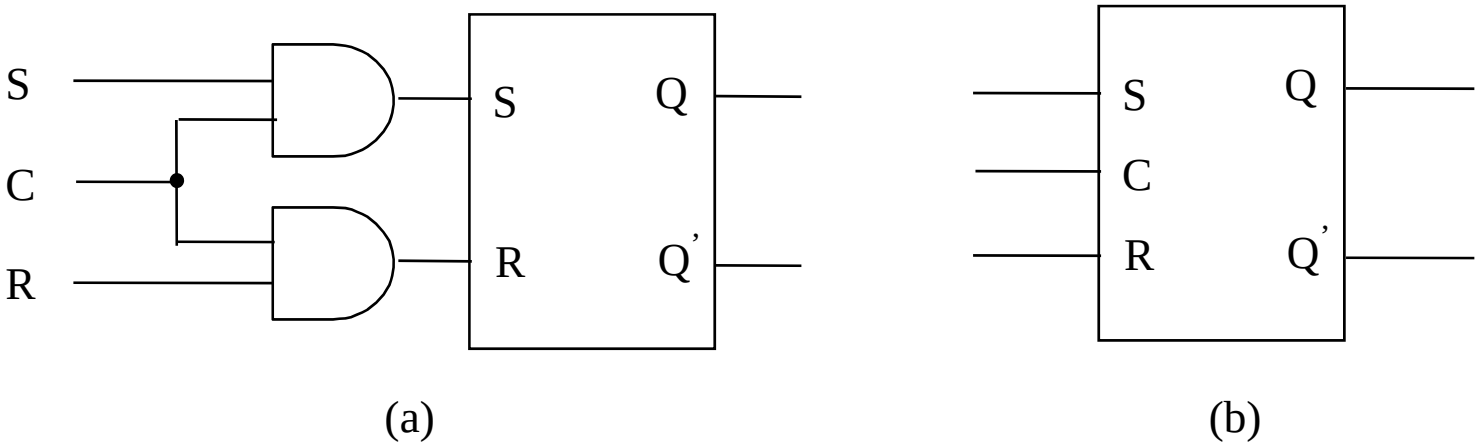


Figure 9.7 Gated SR latch. (a) Circuit structure. (b) Logic symbol.

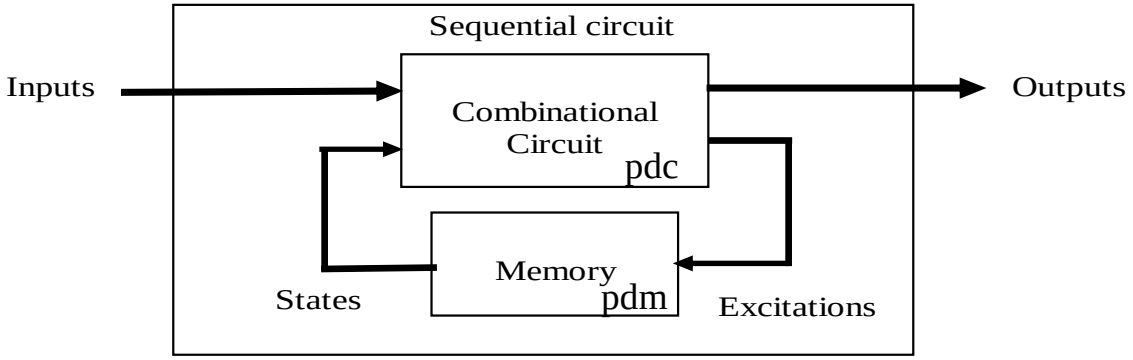


Figure 9.1 Structure of a sequential circuit.

9.3 Flip-flops

9.3.1 Gated latch as Flip-flop

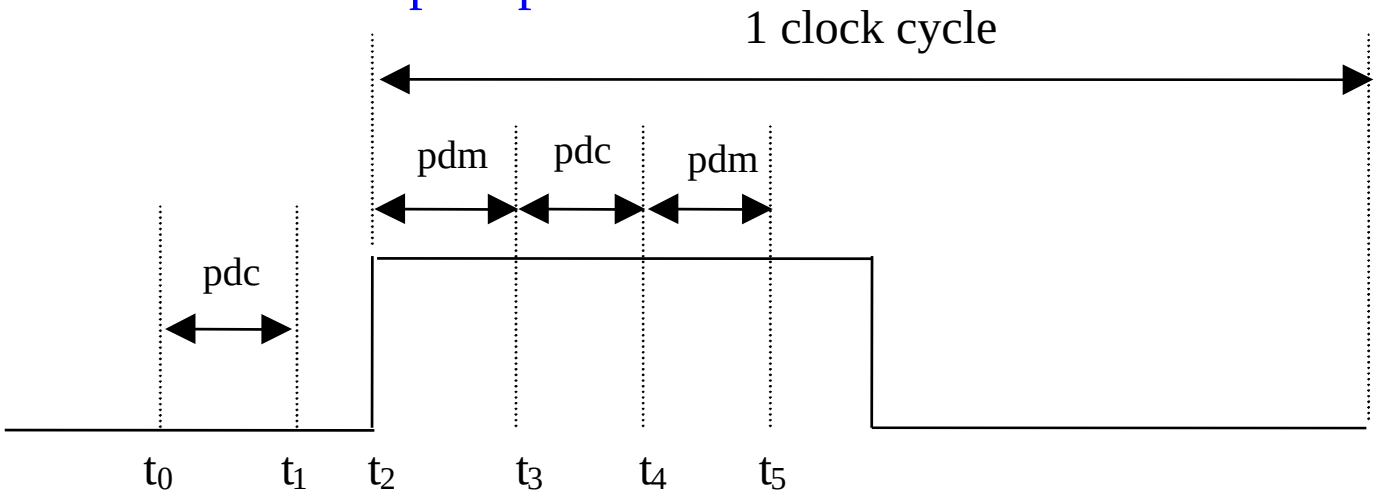


Figure 9.8 Timing diagram for a gated SR latch as a flip-flop.

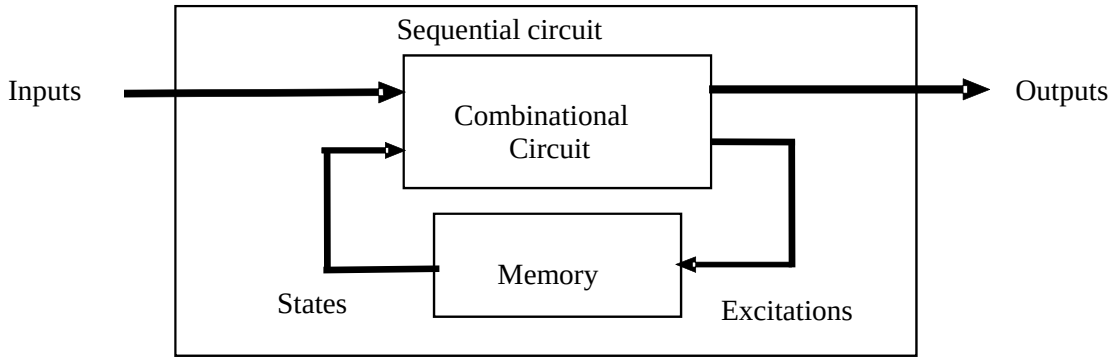


Figure 9.1 Structure of a sequential circuit.

9.3.2 Flip-flops

Master-slave SR flip-flop

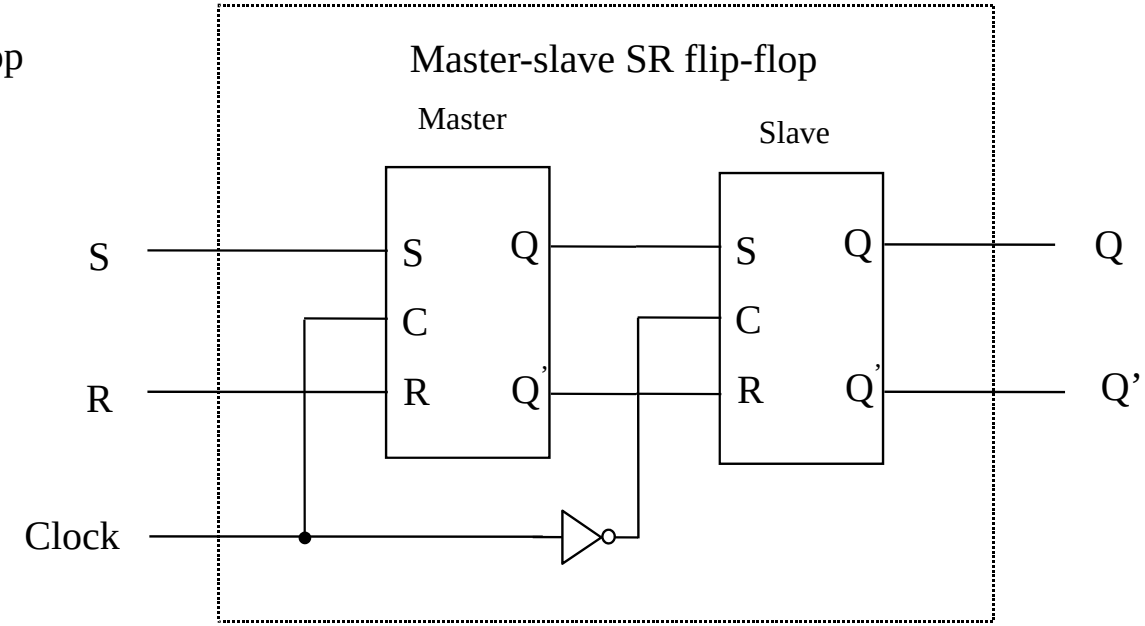


Figure 9.9 Master-slave SR flip-flop.

9.3.2 Flip-flops

Master-slave SR flip-flop

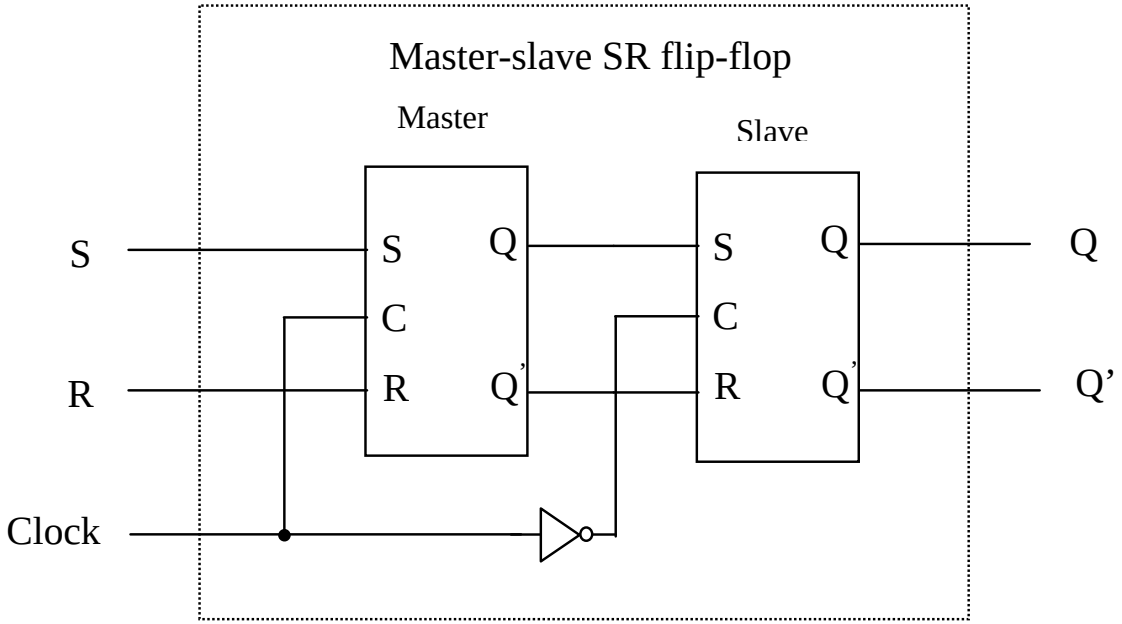


Figure 9.9 Master-slave SR flip-flop.

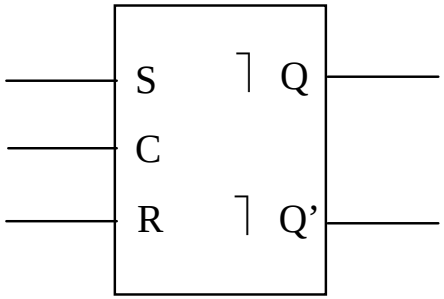


Figure 9.10 Logic symbol for SR flip-flop.

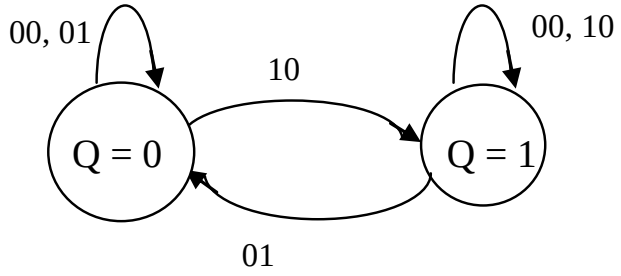
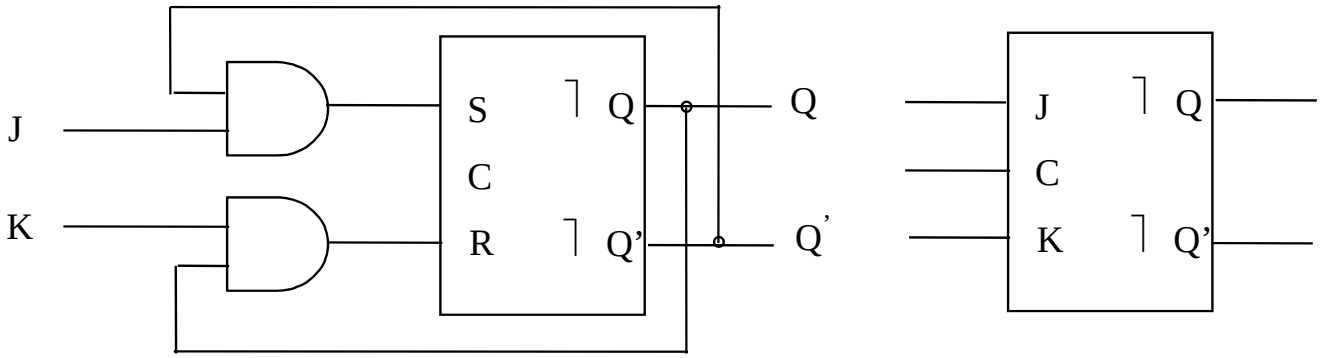


Figure 9.11 State diagram for SR flip-flop.

JK Flip-flop



(a) (b)

Figure 9.12 JK flip-flop. (a) Circuit structure. (b) Logic symbol.

Table 9.2 Characteristic table for JK flip-flop.

Present inputs J K	Present state Q	S = JQ'	R = KQ	Next state Q^+	Function
0 0	0	0	0	0	Hold (No change)
0 0	1	0	0	1	
0 1	0	0	0	0	Reset
0 1	1	0	1	0	
1 0	0	1	0	1	Set
1 0	1	0	0	1	
1 1	0	1	0	1	Toggle
1 1	1	0	1	0	

Characteristic equation: $Q^+ = JQ' + K'Q$

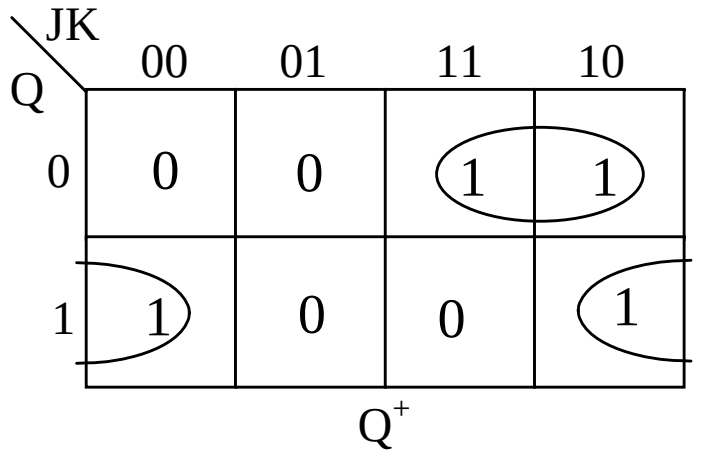


Figure 9.13 Next-state map for JK flip-flop.

D flip-flop

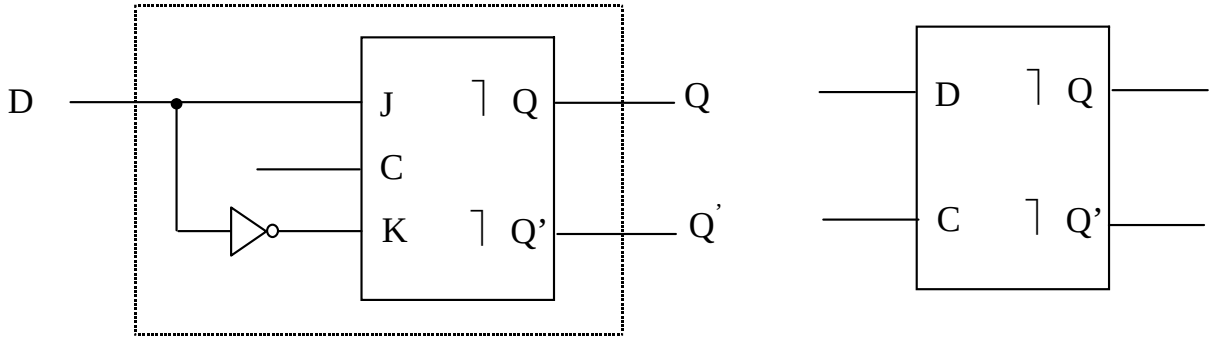


Figure 9.14 D flip-flop. (a) Circuit structure. (b) Logic symbol.

Table 9.3 Characteristic table for D flip-flop.

Present input D	Present state Q	J = D	K = D'	Next state Q^+
0	0	0	1	0
0	1	0	1	0
1	0	1	0	1
1	1	1	0	1

Characteristic equation $Q^+ = D$

T flip-flop

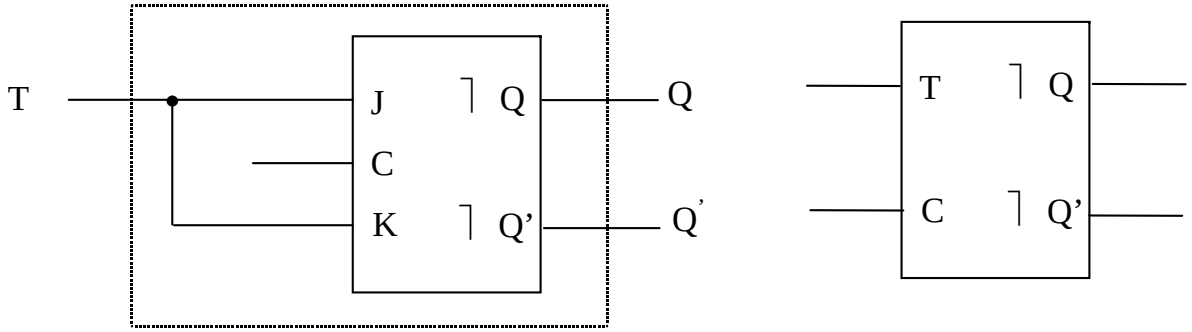


Figure 9.15 T flip-flop. (a) Circuit structure. (b) Logic symbol.

Table 9.4 Characteristic table for T flip-flop.

Present input T	Present state Q	J = T	K = T	Next state Q^+
0	0	0	0	0
0	1	0	0	1
1	0	1	1	1
1	1	1	1	0

Characteristic equation $Q^+ = T \oplus Q$

9.3.3 Edge-triggered Flip-flops

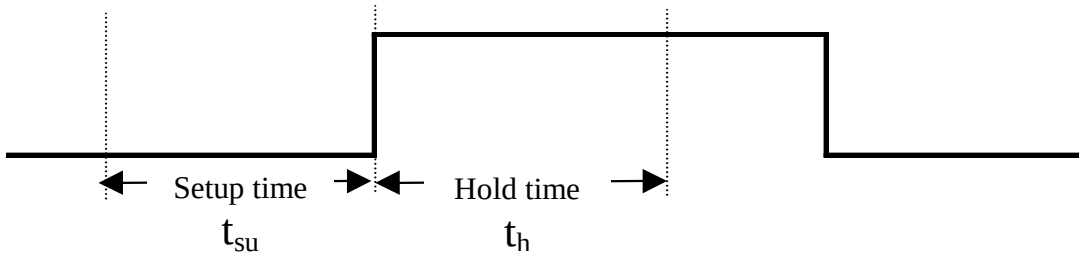


Figure 9.16 Timing constraint of positive-edge triggered flip-flop.

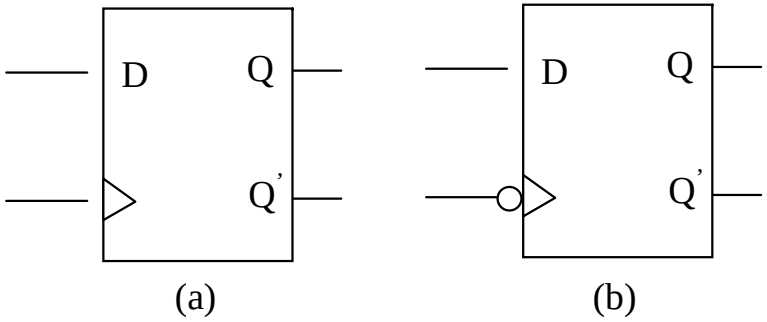


Figure 9.17 Logic symbols for edge-triggered flip-flop.
(a) positive edge. (b) Negative edge.

9.3.4 Asynchronous Preset and Clear

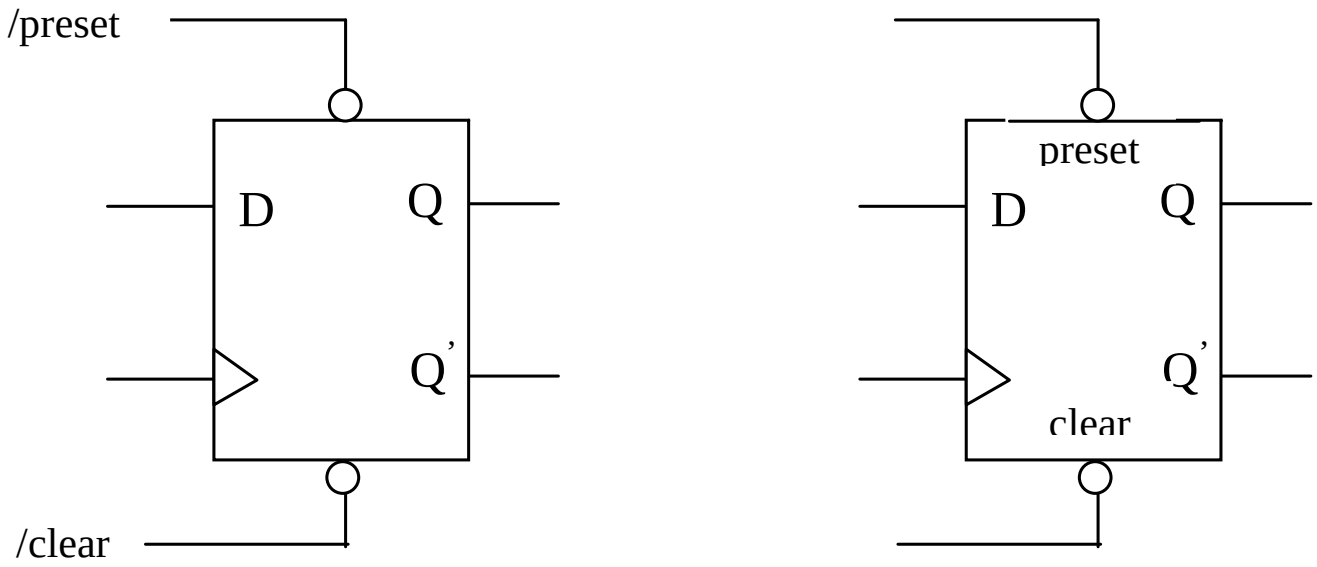


Figure 9.18 Logic symbols for flip-flops with asynchronous preset and clear.

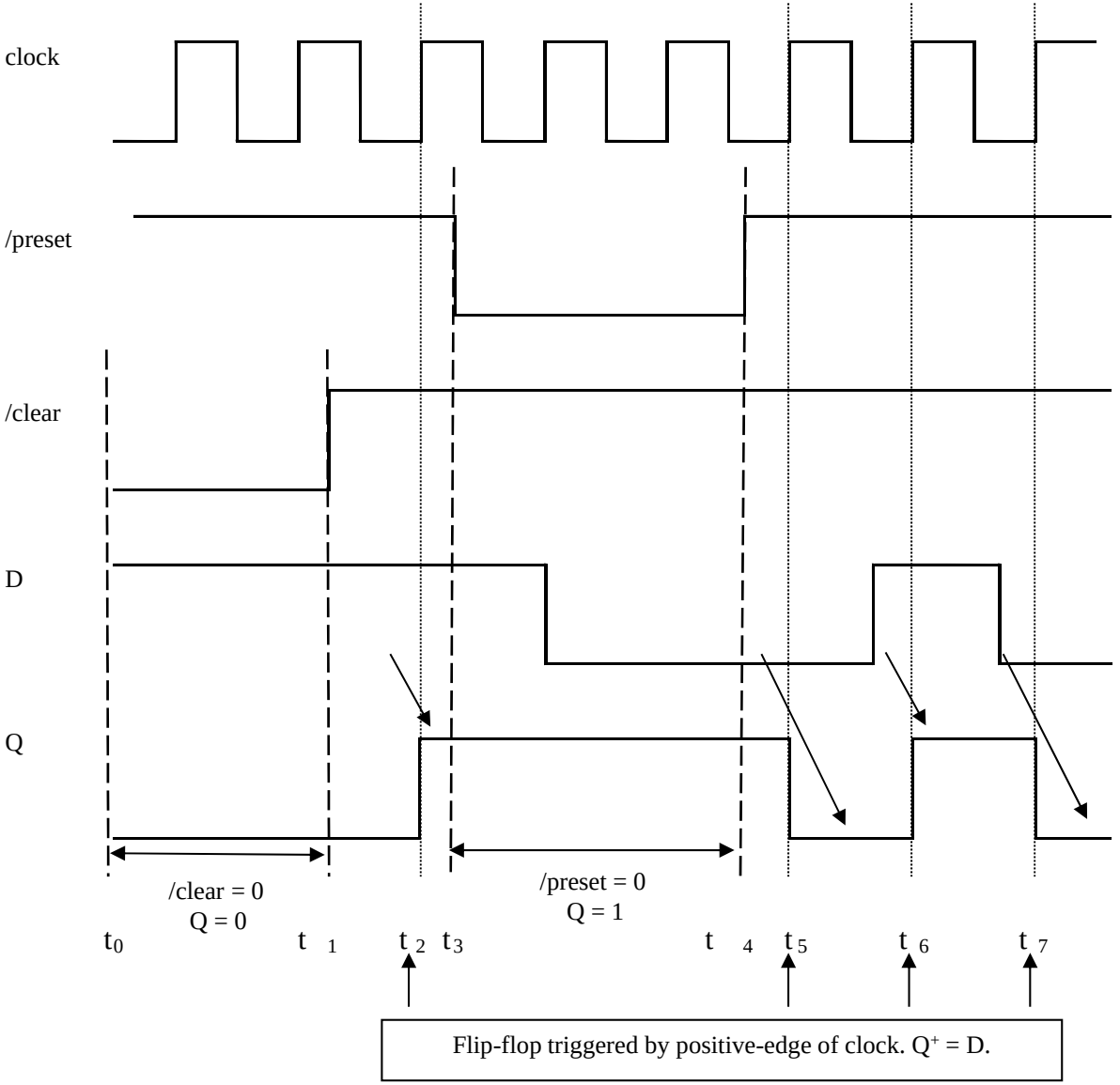


Figure 9.19 Timing diagrams for a positive edge-triggered D flip-flop with asynchronous preset and clear.