## Experiment 3 Design with Decoders and Multiplexers

1 Objective

(1) To expand the knowledge of decoders and multiplexers.
(2) To learn the implementation of functions with decoders.
(3) To learn the implementation of functions with multiplexers.

2 Design description

Five Boolean functions are to be implemented using multiplexers and decoders. The functions must be implemented as specified below:

(1) Implement $F_1(x,y,z)$ and $F_2(x,y,z)$ using a 3-to-8 decoder and added gates. The 3-to-8 decoder should be built from the two 2-to-4 decoders in a type 74155IC before implementing the functions.
(2) Implement $F_3(w,x,y,z)$ with an 8-to-1 multiplexer which should be constructed from the two 4-to-1 multiplexers in a type 74153 IC . The control signals are w, y, and z.
(3) Implement each of the remaining two functions, $F_4(w,x,y,z)$ and $F_5(w,x,y,z)$, using a 4-to-1 multiplexer and added gates. Note that the two multiplexers in 74153 have common selects. The variables which are chosen as control signals (selects) are the same for both $F_4$ and $F_5$.

Ten sets of Boolean functions are given below. You need to implement just one and only one of the ten sets. The Boolean function set assigned to you is given on pages 19-25.

Boolean function set 1

$F_1(x,y,z) = 1 \oplus x'z \oplus y'$
$F_2(x,y,z) = x' \oplus y \oplus z \oplus xyz'$
$F_3(w,x,y,z) = w\,(x + yz') + w'\,(xy'z + x'yz')$
$F_4(w,x,y,z) = \Sigma\, m(0,5,6,9,13,15) + d(1,2,8,10)$
$F_5(w,x,y,z) = (y+z)(w+x'+z)(x+y'+z')(w'+y'+z')$

Boolean function set 2

$F_1(x,y,z) = 1 \oplus xy \oplus z'$
$F_2(x,y,z) = x \oplus y' \oplus z \oplus x'yz$
$F_3(w,x,y,z) = y\,(w + xz') + y'\,(wxz' + w'x'z)$
$F_4(w,x,y,z) = \Sigma\, m(1,3,7,8,11,14) + d(4,6,12,15)$
$F_5(w,x,y,z) = (w+y')(x'+y'+z)(w'+x+y)(w'+y+z')$

Boolean function set 3

$F_1(x,y,z) = 1 \oplus x'y' \oplus z$
$F_2(x,y,z) = x \oplus y \oplus z' \oplus xyz'$
$F_3(w,x,y,z) = z'\,(x' + wy') + z\,(wx'y' + w'xy)$
$F_4(w,x,y,z) = \Sigma\, m(1,3,5,9,10,12) + d(4,6,13,14)$

$F_5(w,x,y,z) = (y+z')(w'+x+y)(w+y'+z)(x'+y'+z)$

Boolean function set 4

$F_1(x,y,z) = 1 \oplus xy' \oplus z'$
$F_2(x,y,z) = x' \oplus y' \oplus z \oplus xyz$
$F_3(w,x,y,z) = y\,(w' + xz) + y'\,(w'xz + wx'z')$
$F_4(w,x,y,z) = \Sigma\, m(3,6,9,11,12,15) + d(0,2,4,7)$
$F_5(w,x,y,z) = (w+y)(w+x'+z)(w'+x+y')(w'+y'+z')$

Boolean function set 5

$F_1(x,y,z) = 1 \oplus xy' \oplus z$
$F_2(x,y,z) = x' \oplus y \oplus z' \oplus x'y'z$
$F_3(w,x,y,z) = z\,(x + wy') + z'\,(wxy' + w'x'y)$
$F_4(w,x,y,z) = \Sigma\, m(1,2,5,7,8,13) + d(9,10,12,14)$
$F_5(w,x,y,z) = (y'+z)(w+x'+y')(x+y+z')(w'+y+z')$

Boolean function set 6

$F_1(x,y,z) = 1 \oplus x'y \oplus z$
$F_2(x,y,z) = x \oplus y' \oplus z' \oplus xy'z'$
$F_3(w,x,y,z) = z'\,(x' + w'y) + z\,(w'x'y + wxy')$
$F_4(w,x,y,z) = \Sigma\, m(0,3,5,7,10,15) + d(8,11,12,14)$
$F_5(w,x,y,z) = (w'+x)(w'+y'+z)(w+x'+y)(w+x'+z')$

Boolean function set 7

$F_1(x,y,z) = 1 \oplus xz \oplus y'$
$F_2(x,y,z) = x' \oplus y \oplus z' \oplus x'y'z$
$F_3(w,x,y,z) = x\,(w' + yz') + x'\,(w'y'z + wyz')$
$F_4(w,x,y,z) = \Sigma\, m(2,4,7,11,13,15) + d(0,3,8,10)$
$F_5(w,x,y,z) = (w+y)(w+x+z')(w'+y'+z)(w'+x'+y')$

Boolean function set 8

$F_1(x,y,z) = 1 \oplus xz' \oplus y$
$F_2(x,y,z) = x' \oplus y \oplus z \oplus x'y'z'$
$F_3(w,x,y,z) = w\,(x'+ y'z) + w'\,(x'yz' + xy'z)$
$F_4(w,x,y,z) = \Sigma\, m(0,6,9,10,14,15) + d(1,2,4,5)$
$F_5(w,x,y,z) = (w'+y')(x'+y'+z)(w+x+y)(w+y+z')$

Boolean function set 9

$F_1(x,y,z) = 1 \oplus x'y \oplus z'$
$F_2(x,y,z) = x \oplus y \oplus z' \oplus xy'z$

$F_3(w,x,y,z) = y' (w + xz) + y (wxz + w'x'z')$
$F_4(w,x,y,z) = \Sigma\, m(1,2,6,7,8,14) + d(9,10,12,13)$
$F_5(w,x,y,z) = (w'+y)(x'+y+z')(w+x+y')(w+y'+z)$

Boolean function set 10

$F_1(x,y,z) = 1 \oplus xy \oplus z$
$F_2(x,y,z) = x \oplus y \oplus z' \oplus xy'z$
$F_3(w,x,y,z) = y' (w' + xz') + y (w'xz' + wx'z)$
$F_4(w,x,y,z) = \Sigma\, m(1,4,9,11,13,14) + d(0,2,5,6)$
$F_5(w,x,y,z) = (y+z)(w'+x+z)(w+y'+z')(x'+y'+z')$

## 3 IC Requirements

Other than one 74155 IC and two 74153 ICs, other ICs that can be used in the design must be from the following list:

| | |
|---|---|
| Two | IC type 7400 (quadruple 2-input NAND gates) |
| One | IC type 7402 (quadruple 2-input NOR gates) |
| One | IC type 7420 (dual 4-input NAND gates) |
| One | IC type 7486 (quadruple 2-input XOR gates) |

Although the maximum number of ICs that can be used is eight, minimizing the number of ICs and gates used in your design is required.

## 4 Description of 74155 and 74153

As shown in Figure 1, 74155 is an IC which consists of two 2-to-4 decoders. They can also be used as de-multiplexers. The features are listed below when used as decoders..

Top decoder

G (Pin 14) : Active-low enable/strobe
C (Pin 15) : Active-low enable/strobe
Y0, Y1, Y2, Y3 (Pins 9, 10, 11, 12): Active low outputs.

Bottom decoder

G (Pin 2) : Active-low enable/strobe
C (Pin 1) : Active-high enable/strobe
Y0, Y1, Y2, Y3 (Pins 7, 6, 5, 4): Active low outputs.

Both decoders have the same address bits. They are

B (pin 3, most significant) and A (pin 13, least significant)

To enable a decoder, both G and C must be asserted. De-asserting either G or C or both will disable a decoder. When both C's (Pin 1 and Pin 15) are connected together, one of the two decoders is always disabled. This input connection can be used as a

third address bit to convert 75155 to a 3-to-8 decoder. The two G's can be connected to become a single enable/strobe for the 3-to-8 decoder.

When 74155 is used as de-multiplexers, the active-low C (Pin 15) and the active-high C (Pin 1) are the data inputs for the top and bottom de-multiplexers respectively. When a data input is asserted (de-asserted), the corresponding output to which the data is routed to must be asserted (de-asserted), the other three outputs are all de-asserted.

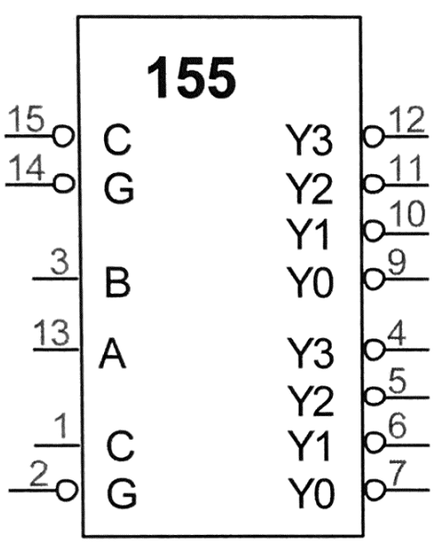


Figure 1 Diagram for 74155: dual decoders/de-multiplexers.

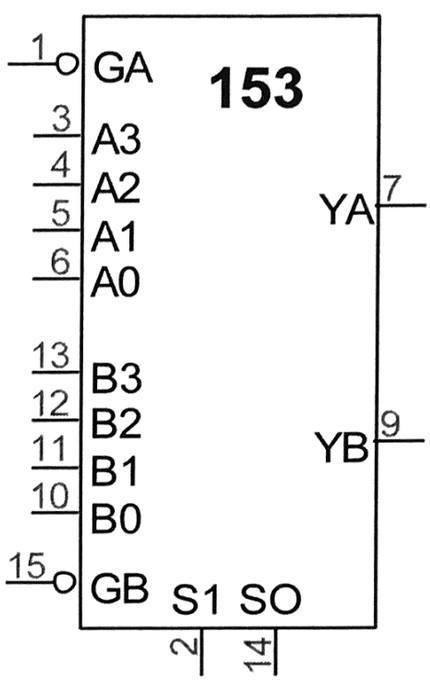


Figure 2 Diagram for 74153: dual 4-to-1 multiplexers.

For the two 4-to-1 multiplexers contained in a 74153 IC as shown in Figure 2, they have common selects but separate strobes. The two separate strobes allow one multiplexer to be activated and the other to be disabled. For the two control signals, S1 is the most significant and S0 is the least significant. The two 4-to-1 multiplexers can be connected to form an 8-to-1 multiplexers. Since a multiplexer has only one output, an external gate may have to be added in the conversion of two multiplexer outputs to one.