CHAPTER 8

PROGRAMMABLE LOGIC DEVICES

8.1 Introduction

Programmable Logic Devices (PLD):

- Read-only memory (ROM)
- Programmable logic array (PLA)
- Programmable array logic (PAL)

Each of the PLDs comprises of two arrays of gates:

an AND gate array and an OR gate array.

8.2 Notations

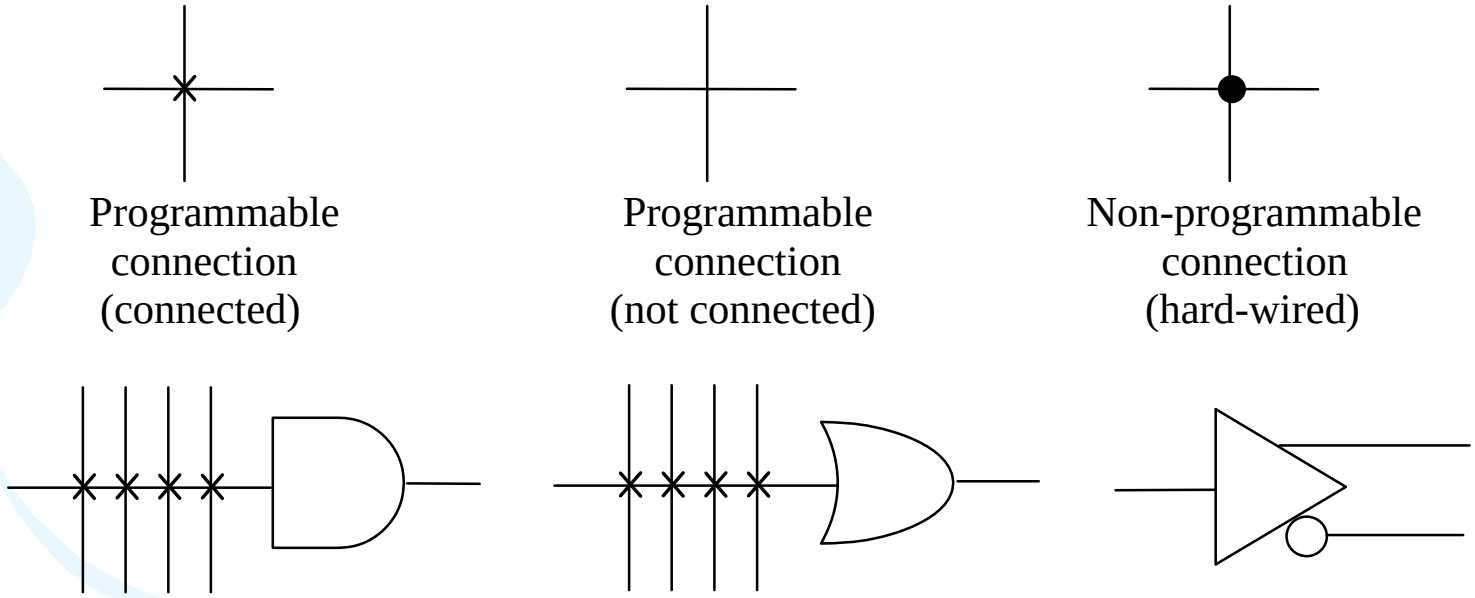


Figure 8.1 PLD notations

8.3 Read-Only Memory (ROM)

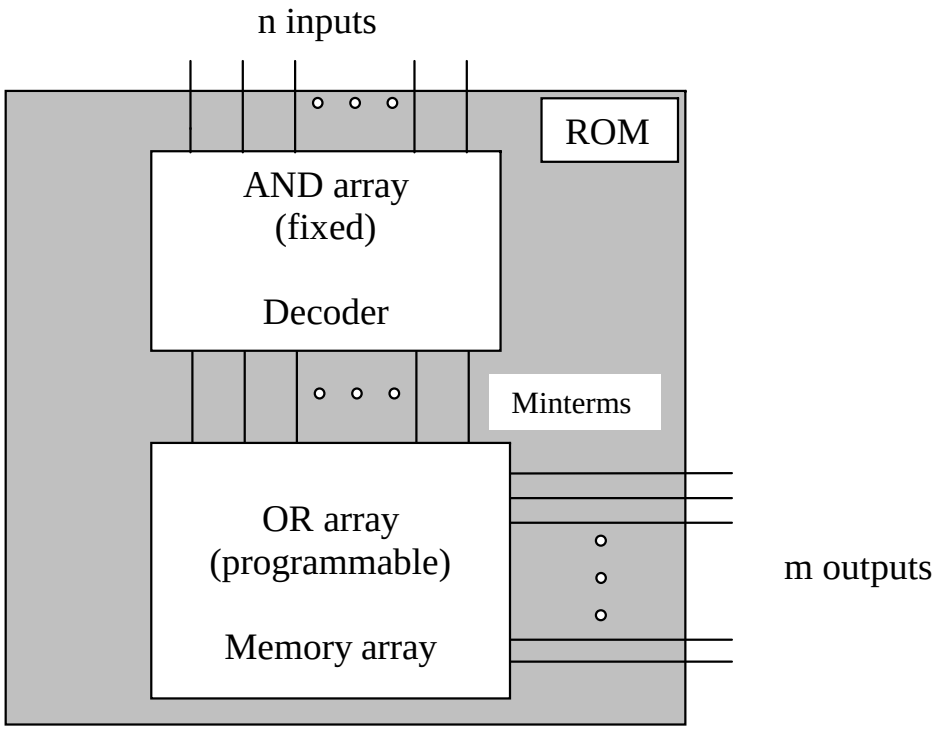


Figure 8.2 Structure of ROM.

Example 8.1

$f_1(A, B, C) = \Sigma\, m(0, 2, 3, 4)$
$f_2(A, B, C) = \Sigma\, m(1, 2, 3, 5, 6)$
$f_3(A, B, C) = \Sigma\, m(2, 6, 7)$
$f_4(A, B, C) = \Sigma\, m(2, 3, 5)$

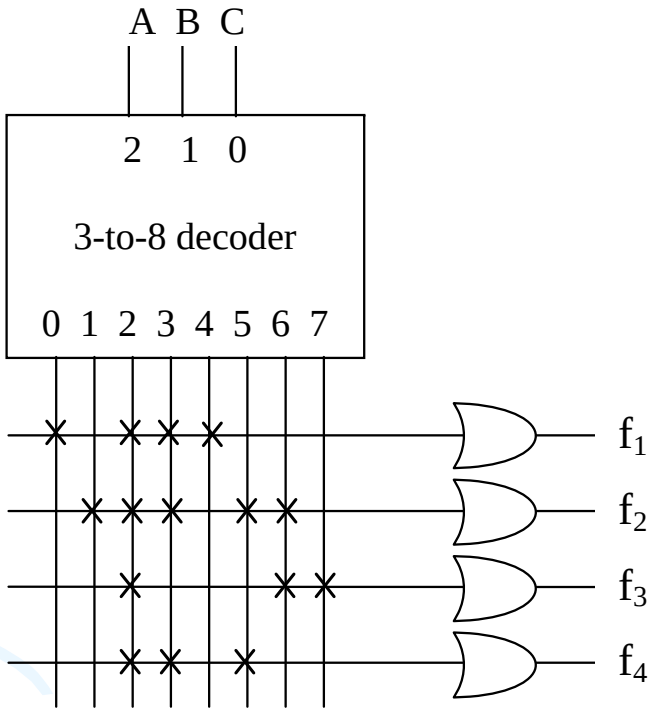
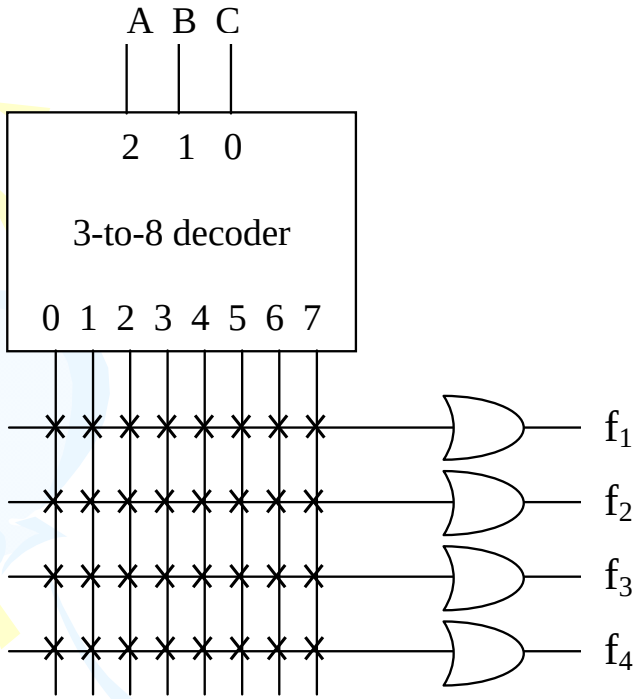
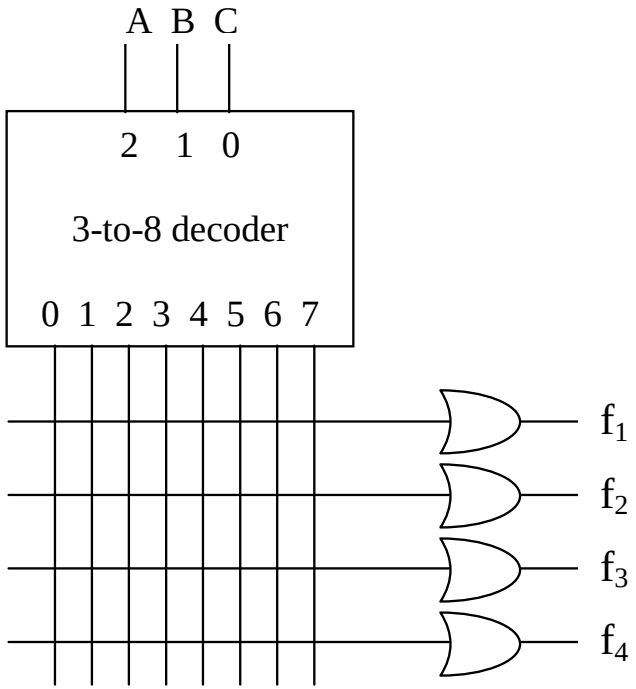


Figure 8.3 Implementation of functions by ROM.


A B C
2 1 0
3-to-8 decoder
0 1 2 3 4 5 6 7
f1
f2
f3
f4


A B C
2 1 0
3-to-8 decoder
0 1 2 3 4 5 6 7
f1
f2
f3
f4

Example 8.2 Seven-segment display

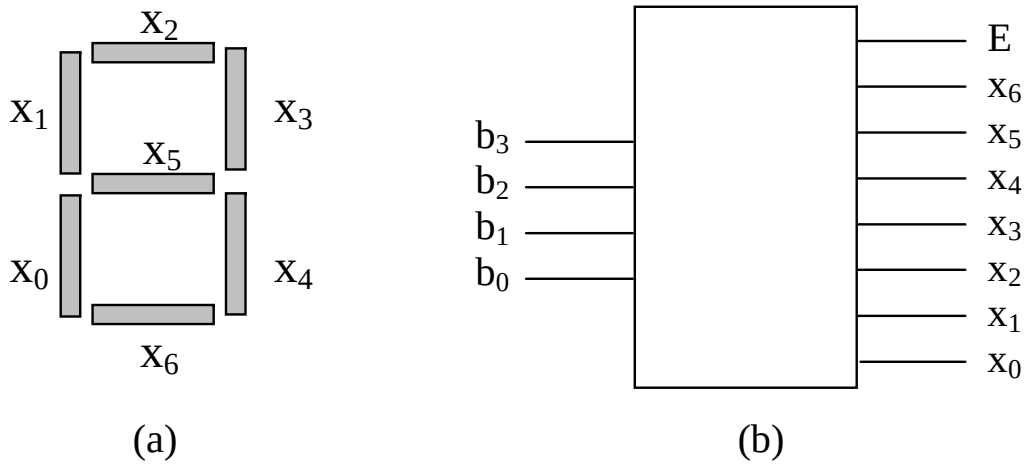


Figure 8.4 (a) Structure of 7-segment display. (b) Bock diagram for a 7-segment display circuit.

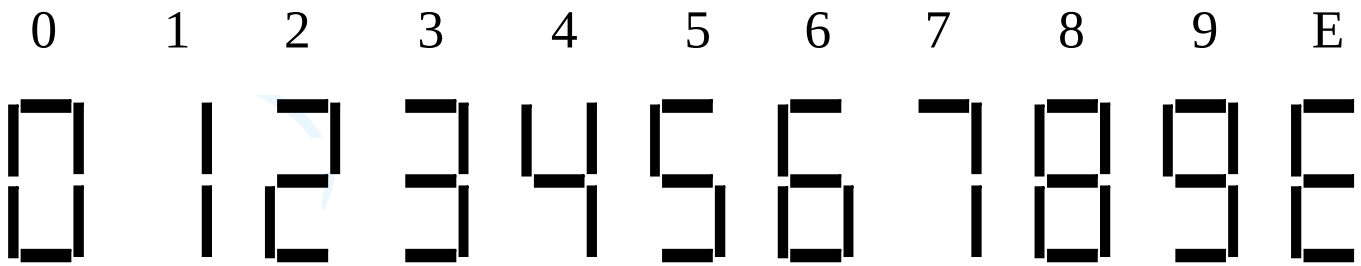


Figure 8.5 Seven-segment display of decimal digits and the letter E.

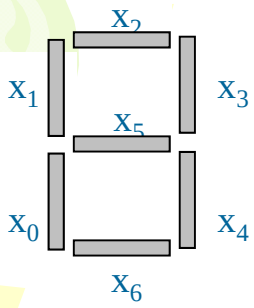


Table 8.1 Truth table for 7-segment display circuit.

Decimal digit	$b_3\ b_2\ b_1\ b_0$	$E\ x_6\ x_5\ x_4\ x_3\ x_2\ x_1\ x_0$
0	0 0 0 0	0 1 0 1 1 1 1 1
1	0 0 0 1	0 0 0 1 1 0 0 0
2	0 0 1 0	0 1 1 0 1 1 0 1
3	0 0 1 1	0 1 1 1 1 1 0 0
4	0 1 0 0	0 0 1 1 1 0 1 0
5	0 1 0 1	0 1 1 1 0 1 1 0
6	0 1 1 0	0 1 1 1 0 1 1 1
7	0 1 1 1	0 0 0 1 1 1 0 0
8	1 0 0 0	0 1 1 1 1 1 1 1
9	1 0 0 1	0 1 1 1 1 1 1 0
Invalid	1 0 1 0	1 1 1 0 0 1 1 1
Invalid	1 0 1 1	1 1 1 0 0 1 1 1
Invalid	1 1 0 0	1 1 1 0 0 1 1 1
Invalid	1 1 0 1	1 1 1 0 0 1 1 1
Invalid	1 1 1 0	1 1 1 0 0 1 1 1
Invalid	1 1 1 1	1 1 1 0 0 1 1 1

Table 8.1 Truth table for 7-segment display circuit.

Decimal digit	$b_3\ b_2\ b_1\ b_0$	$E\ x_6\ x_5\ x_4\ x_3\ x_2\ x_1\ x_0$
0	0 0 0 0	0 1 0 1 1 1 1 1
1	0 0 0 1	0 0 0 1 1 0 0 0
2	0 0 1 0	0 1 1 0 1 1 0 1
3	0 0 1 1	0 1 1 1 1 1 0 0
4	0 1 0 0	0 0 1 1 1 0 1 0
5	0 1 0 1	0 1 1 1 0 1 1 0
6	0 1 1 0	0 1 1 1 0 1 1 1
7	0 1 1 1	0 0 0 1 1 1 0 0
8	1 0 0 0	0 1 1 1 1 1 1 1
9	1 0 0 1	0 1 1 1 1 1 1 0
Invalid	1 0 1 0	1 1 1 0 0 1 1 1
Invalid	1 0 1 1	1 1 1 0 0 1 1 1
Invalid	1 1 0 0	1 1 1 0 0 1 1 1
Invalid	1 1 0 1	1 1 1 0 0 1 1 1
Invalid	1 1 1 0	1 1 1 0 0 1 1 1
Invalid	1 1 1 1	1 1 1 0 0 1 1 1

$E(b_3, b_2, b_1, b_0) = \Sigma\ m(10 - 15)$
$x_6(b_3, b_2, b_1, b_0) = \Sigma\ m(0, 2, 3, 5, 6, 8 - 15)$
$x_5(b_3, b_2, b_1, b_0) = \Sigma\ m(2 - 6, 8 - 15)$
$x_4(b_3, b_2, b_1, b_0) = \Sigma\ m(0, 1, 3 - 9)$
$x_3(b_3, b_2, b_1, b_0) = \Sigma\ m(0 - 4, 7 - 9)$
$x_2(b_3, b_2, b_1, b_0) = \Sigma\ m(0, 2, 3, 5 - 15)$
$x_1(b_3, b_2, b_1, b_0) = \Sigma\ m(0, 4 - 6, 8 - 15)$
$x_0(b_3, b_2, b_1, b_0) = \Sigma\ m(0, 2, 6, 8, 10 - 15)$

$E(b_3, b_2, b_1, b_0) = \Sigma\, m(10 - 15)$

$x_6(b_3, b_2, b_1, b_0) = \Sigma\, m(0, 2, 3, 5, 6, 8 - 15)$

$x_5(b_3, b_2, b_1, b_0) = \Sigma\, m(2 - 6, 8 - 15)$

$x_4(b_3, b_2, b_1, b_0) = \Sigma\, m(0, 1, 3 - 9)$

$x_3(b_3, b_2, b_1, b_0) = \Sigma\, m(0 - 4, 7 - 9)$

$x_2(b_3, b_2, b_1, b_0) = \Sigma\, m(0, 2, 3, 5 - 15)$

$x_1(b_3, b_2, b_1, b_0) = \Sigma\, m(0, 4 - 6, 8 - 15)$

$x_0(b_3, b_2, b_1, b_0) = \Sigma\, m(0, 2, 6, 8, 10 - 15)$

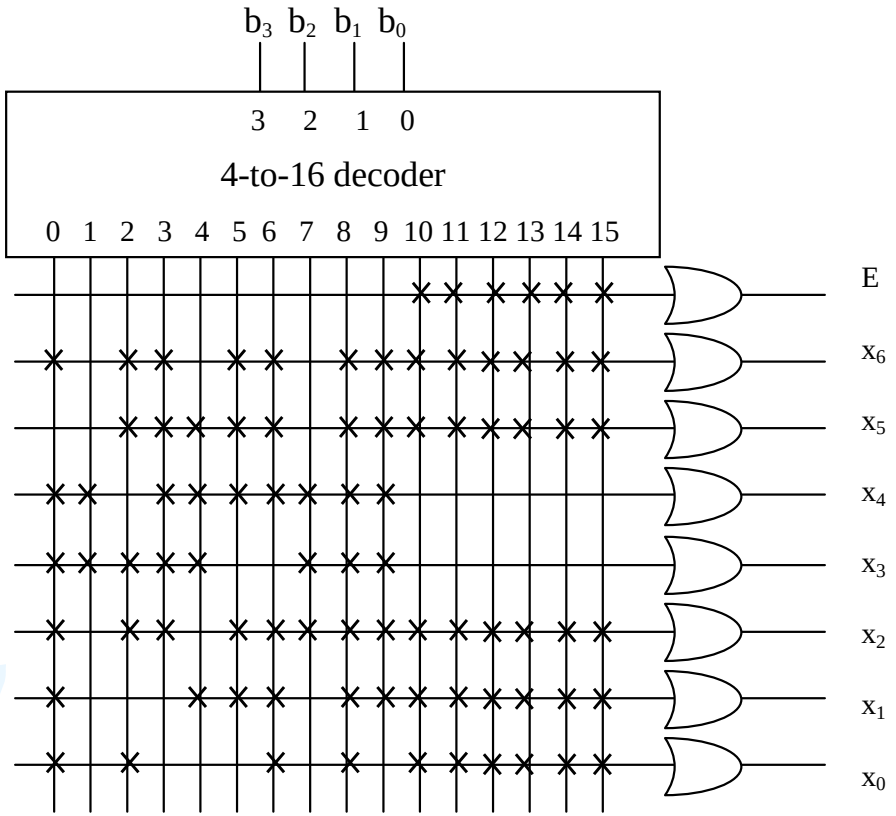


Figure 8.6 Implementation of a 7-segment display circuit using ROM.

8.4 Programmable Logic Array (PLA)

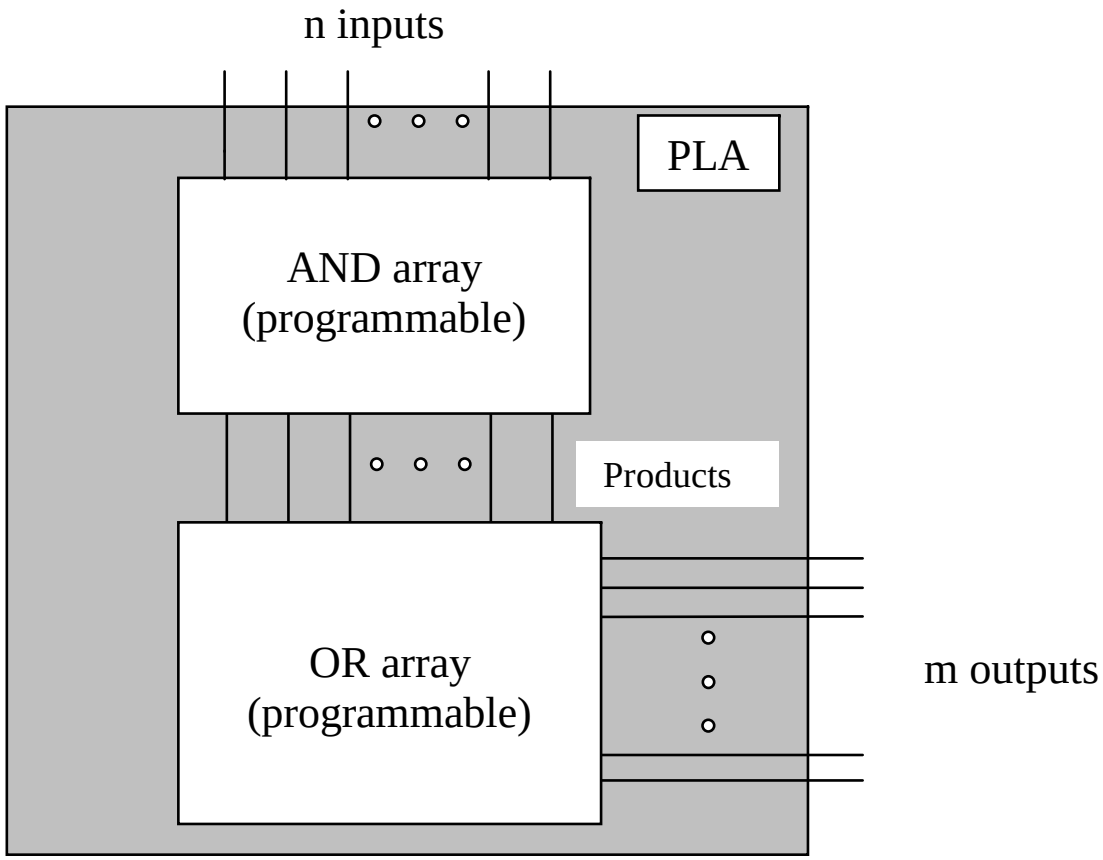


Figure 8.7 Structure of PLA.

Example 8.3

$f_1(A, B, C) = \Sigma\, m(0, 2, 3, 4) = B'C' + A'B$
$f_2(A, B, C) = \Sigma\, m(1, 2, 3, 5, 6) = BC' + B'C + A'B$
$f_3(A, B, C) = \Sigma\, m(2, 6, 7) = BC' + AB$
$f_4(A, B, C) = \Sigma\, m(2, 3, 5) = A'B + AB'C$

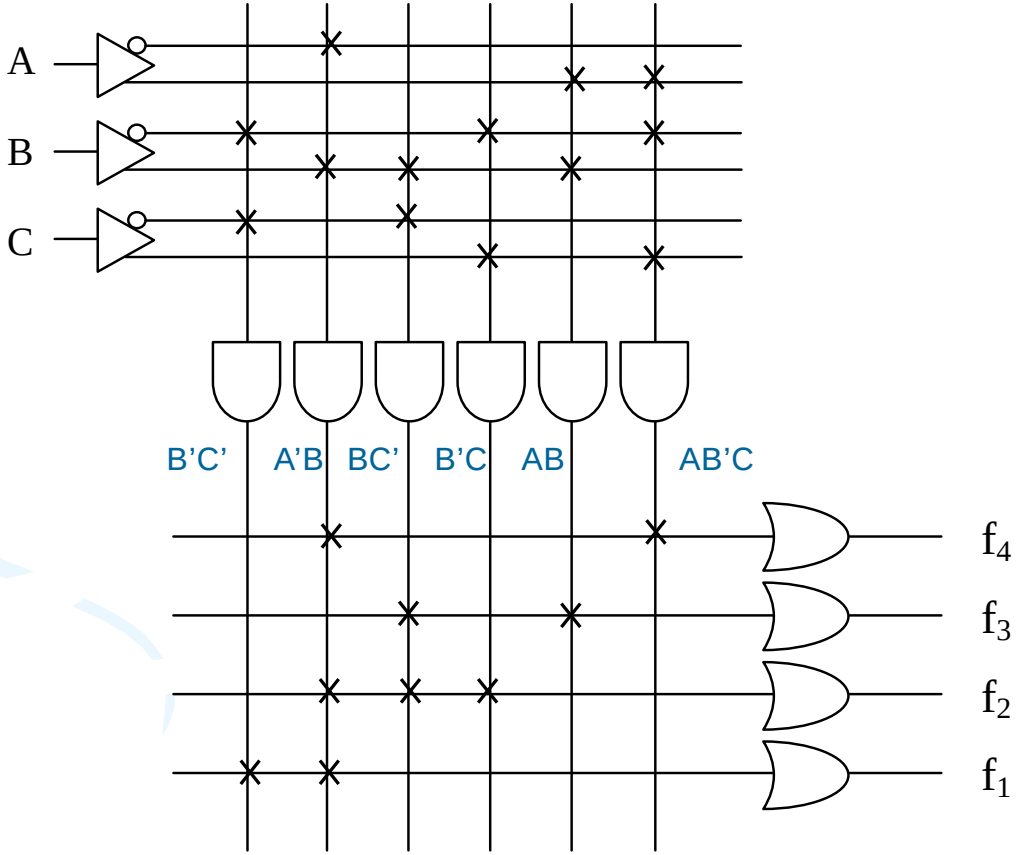


Figure 8.8 Implementation of functions by PLA.

8.5 Programmable Array Logic (PAL)

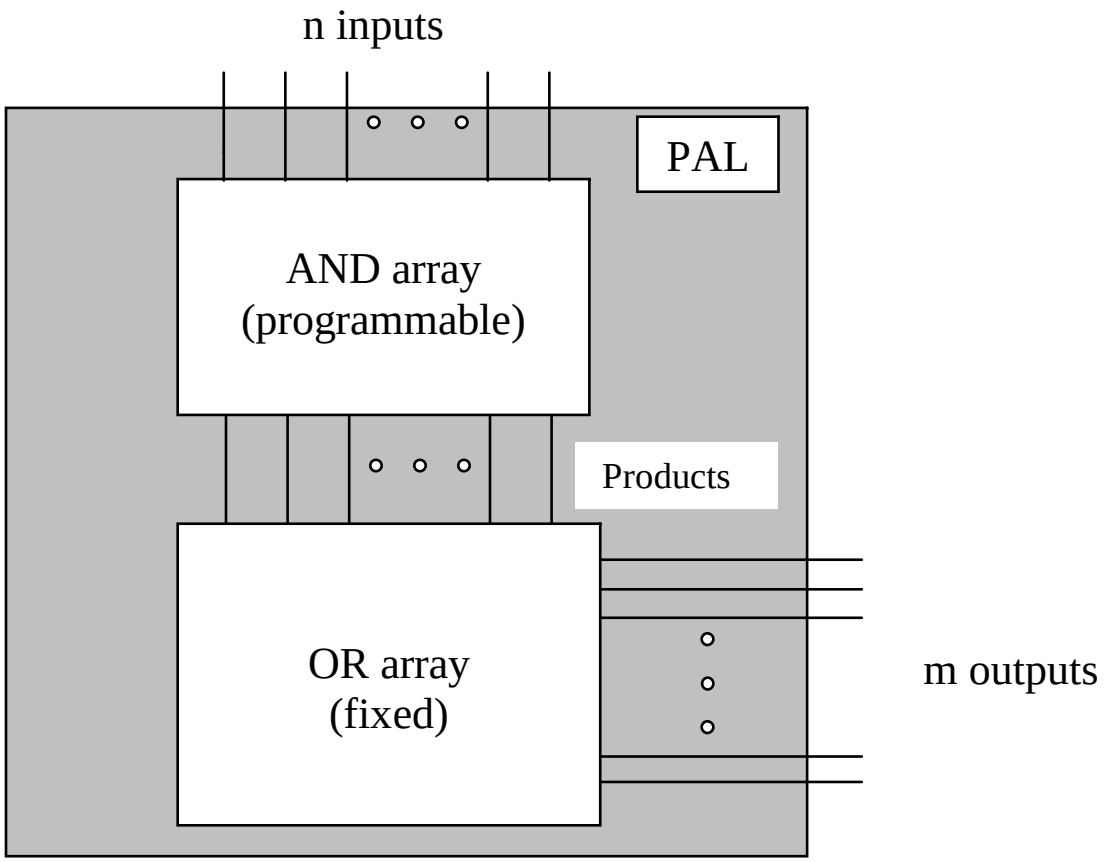


Figure 8.9 Structure of PAL.

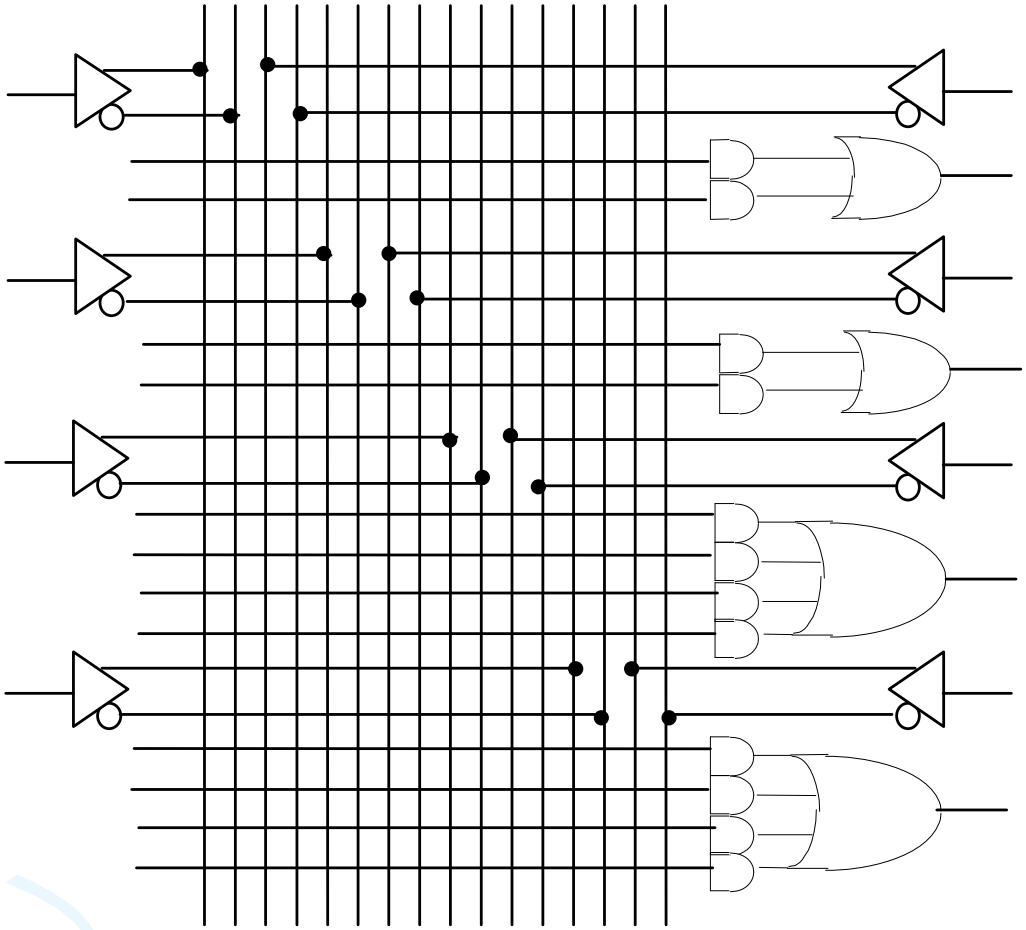


Figure 8.10

Example 8.4

X = A’C + C’D

Y = A’C’D’ + AD + AB’C

Z = BD + A’C + A’B’D’ + ABC’ + ACD

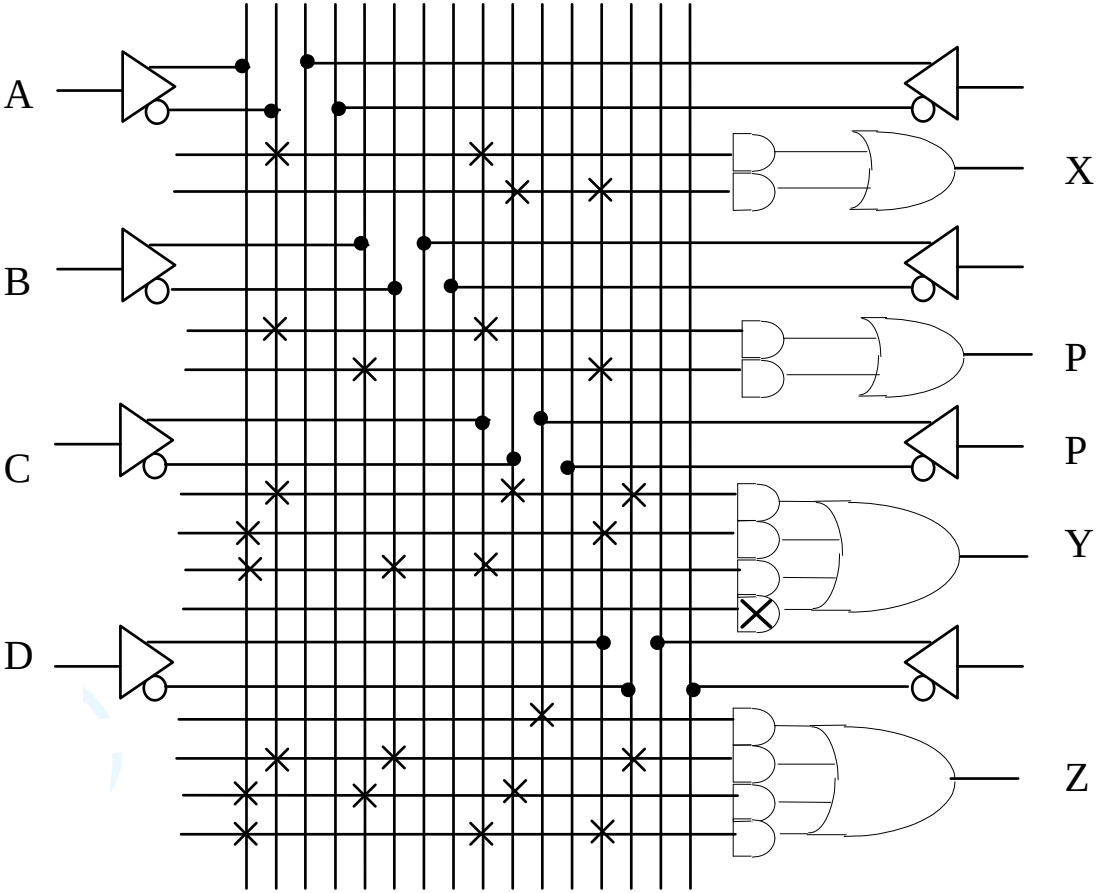


Figure 8.10 Implementation of functions using PAL.