Student Logic Number	Experiment 1	Experiment 2		Experiment 3	Experiment 4	Experiment 5
	Circuit number	Input (reflected) code	Output (weighted) code	Boolean function set number	Counter sequence S_0 S_1 S_2 S_3 S_4 S_5	Arithmetic function set number
136	6	1	(6,4,1,-2)	9	134276	8
137	7	1	(6,4,-1,-2)	10	134576	9
138	8	1	(7,5,-1,-3)	1	134672	10
139	9	2	(5,3,1,-2)	2	134702	11
140	10	2	(5,4,2,-1)	3	134760	12
141	1	2	(5,4,-1,-2)	4	135042	13
142	2	2	(6,4,1,-2)	5	135046	14
143	3	2	(6,4,-1,-2)	6	135276	1
144	4	2	(7,5,-1,-3)	7	136407	2
145	5	1	(5,3,1,-2)	8	136527	3
146	6	1	(5,4,-1,-2)	9	136570	4
147	7	1	(6,4,1,-2)	10	136704	5
148	8	1	(6,4,-1,-2)	1	137250	6
149	9	1	(7,5,-1,-3)	2	137254	7
150	10	2	(5,3,1,-2)	3	137504	8
151	1	2	(5,4,2,-1)	4	140265	9
152	2	2	(5,4,-1,-2)	5	140276	10
153	3	2	(6,4,1,-2)	6	140375	11
154	4	2	(6,4,-1,-2)	7	140567	12
155	5	2	(7,5,-1,-3)	8	140675	13
156	6	1	(5,3,1,-2)	9	142573	14
157	7	1	(5,4,-1,-2)	10	143027	1
158	8	1	(6,4,1,-2)	1	143625	2
159	9	1	(6,4,-1,-2)	2	143672	3
160	10	1	(7,5,-1,-3)	3	143706	4
161	1	2	(5,3,1,-2)	4	145067	5
162	2	2	(5,4,2,-1)	5	145273	6
163	3	2	(5,4,-1,-2)	6	145376	7
164	4	2	(6,4,1,-2)	7	145703	8
165	5	2	(6,4,-1,-2)	8	145736	9
166	6	2	(7,5,-1,-3)	9	146037	10
167	7	1	(5,3,1,-2)	10	146052	11
168	8	1	(5,4,-1,-2)	1	146072	12
169	9	1	(6,4,1,-2)	2	146307	13
170	10	1	(6,4,-1,-2)	3	146327	14
171	1	1	(7,5,-1,-3)	4	146352	1
172	2	2	(5,3,1,-2)	5	146370	2
173	3	2	(5,4,2,-1)	6	146520	3
174	4	2	(5,4,-1,-2)	7	146530	4
175	5	2	(6,4,1,-2)	8	146702	5

16.265 Logic Design	
Student Logic Number	140
Name	Dangnhi Ngo
E-mail address (print)	Nhi_Ngo@student.uml.edu
Experiment Number	3
Date	11/08/2017

For grader use	
Schematic diagram submitted is different from the one in the report. (Need to re-submit the schematic diagram in the report or will be graded based on a maximum of 50 points.)	5 points deduction
Cannot open file	
File is not readable	
Date student is notified to re-submit a schematic file by e-mail	
Date schematic file received	

Report will be graded based on a maximum of 50 (out of 100 points) if a schematic diagram is not received within three calendar days of notification or the re-submitted schematic file still cannot be opened or is not readable.

Grade: 100

Experiment 3 Design with Decoders and Multiplexers

1. **Function Set Assignment**

   Function set number _3____

   $F_1(x,y,z) = 1 \oplus x'y' \oplus z$

   $F_2(x,y,z) = x \oplus y \oplus z' \oplus xyz'$

   $F_3(w,x,y,z) = z'(x' + wy') + z(wx'y' + w'xy)$

   $F_4(w,x,y,z) = \sum m(1,3,5,9,10,12) + d(4,6,13,14)$

   $F_5(w,x,y,z) = (y+z')(w'+x+y)(w+y'+z)(x'+y'+z)$

2. **Design Procedures**

   <u>Express all the functions in minterm list form</u>

   $F_1(x,y,z) = \Sigma m\,(1,2,4,6)$

   $F_2(x,y,z) = \Sigma m\,(0,3,5)$

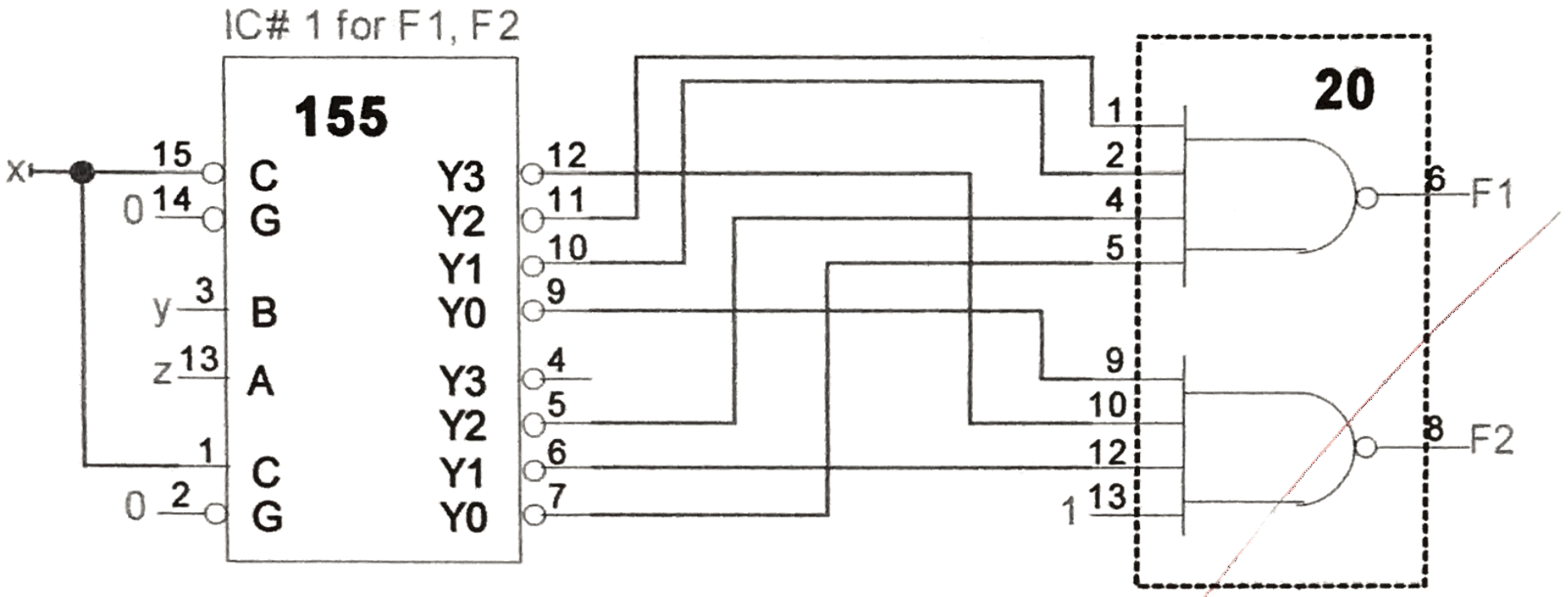
   $F_3(w,x,y,z) = \Sigma m\,(0,2,7,8,9,10,12)$

   $F_4(w,x,y,z) = \Sigma m\,(1,3,5,9,10,12) + d(4,6,13,14)$

   $F_5(w,x,y,z) = \Sigma m\,(0,3,4,7,10,11,12,15)$

Design for F_1 and F_2

(Show the implementation of F_1 and F_2 by a 74155 IC and some external gates. Draw a circuit diagram.)



Design for F_3

Draw the sub-function K-maps for F_3 with w, x, z as expansion variables.

y	$F_{wxz} = 000$	$F_{wxz} = 001$	$F_{wxz} = 010$	$F_{wxz} = 011$	$F_{wxz} = 100$	$F_{wxz} = 101$	$F_{wxz} = 110$	$F_{wxz} = 111$
0	1	0	0	0	1	1	1	0
1	1	0	0	1	1	0	0	0

Based on the sub-function K-maps, the data inputs to the 8-to-1 multiplexers are as follows:

$I_0 = 1$
$I_1 = 0$
$I_2 = 0$
$I_3 = y$
$I_4 = 1$
$I_5 = y'$
$I_6 = y'$
$I_7 = 0$

Design for F_4 and F_5

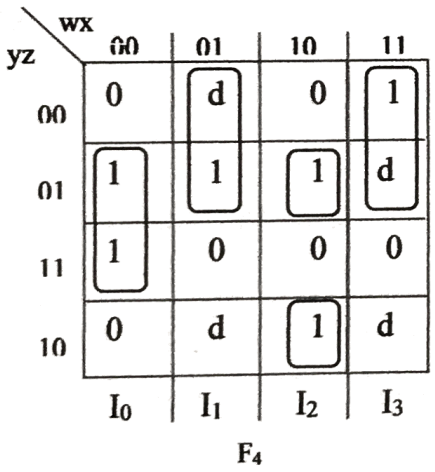
yz \ wx	00	01	11	10
00	0	d	1	0
01	1	1	d	1
11	1	0	0	0
10	0	d	d	1

K-map for F_4

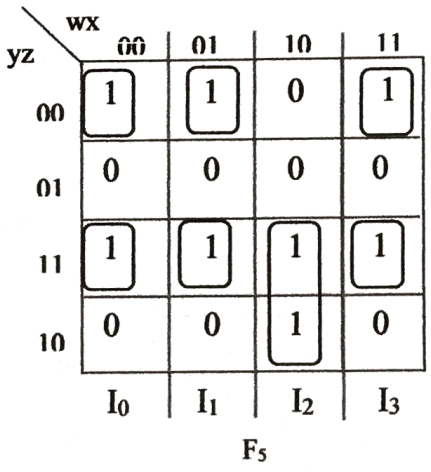
yz \ wx	00	01	11	10
00	1	1	1	0
01	0	0	0	0
11	1	1	1	1
10	0	0	0	1

K-map for F_5

(i) Partition the K-maps with w and x as control signals.



F_4



F_5

The data inputs are as follows:

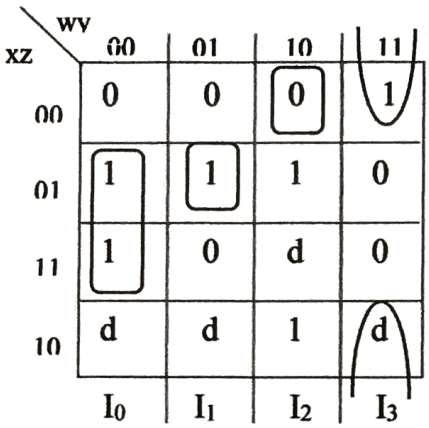
For F_4

$I_0 = z$
$I_1 = y'$
$I_2 = y \oplus z$
$I_3 = y'$

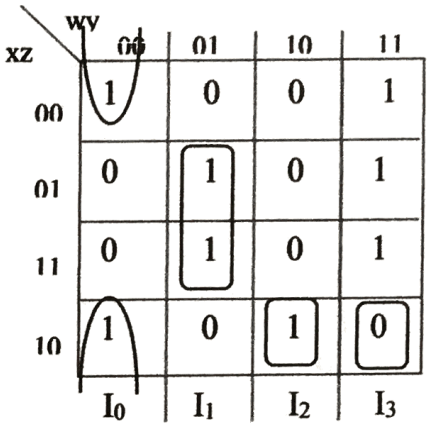
For F_5

$I_0 = y' \oplus z$
$I_1 = y' \oplus z$
$I_2 = y$
$I_3 = y' \oplus z$

(ii) Partition the K-maps with w and y as control signals.



F4



F5

The data inputs are as follows:

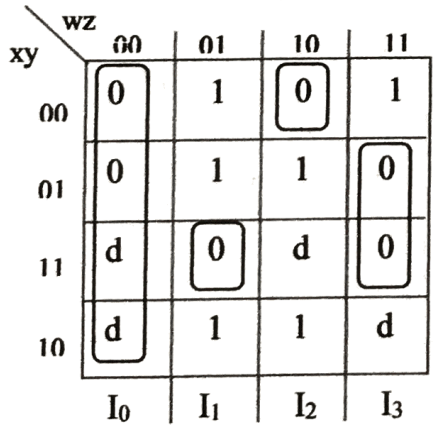
For F_4

$I_0 = z$
$I_1 = x'z$
$I_2 = x + z$
$I_3 = z'$

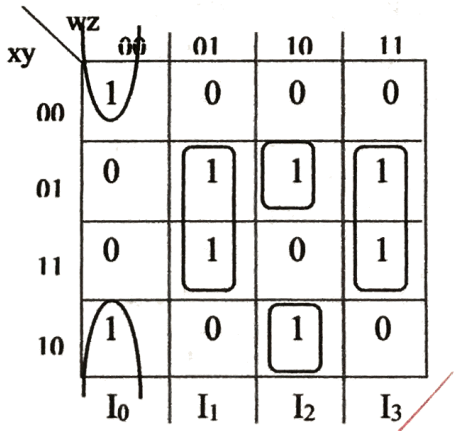
For F_5

$I_0 = z'$
$I_1 = z$
$I_2 = xz'$
$I_3 = x' + z$

(iii)Partition the K-maps with w and z as control signals.



F4



F5

The data inputs are as follows:

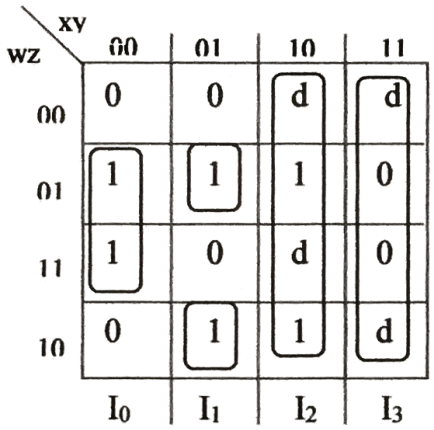
For F_4

$I_0 = 0$
$I_1 = x' + y'$
$I_2 = x + y$
$I_3 = y'$

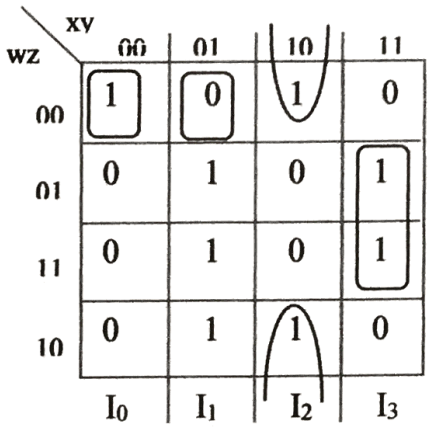
For F_5

$I_0 = y'$
$I_1 = y$
$I_2 = x \oplus y$
$I_3 = y$

(iv) Partition the K-maps with x and y as control signals.



F4



F5

The data inputs are as follows:

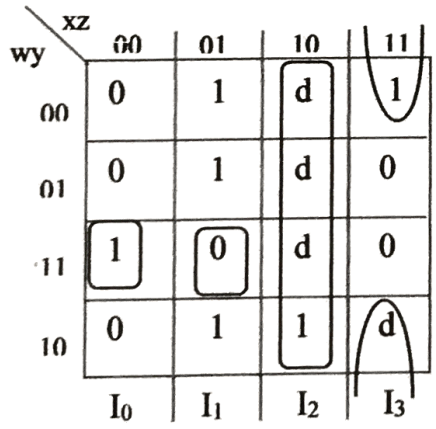
For F4

$I_0 = z$
$I_1 = w \oplus z$
$I_2 = 1$
$I_3 = 0$

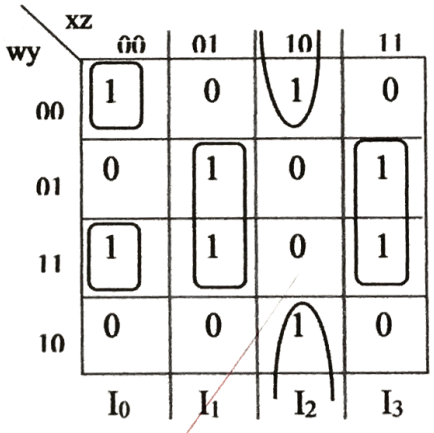
For F5

$I_0 = w'z'$
$I_1 = w + z$
$I_2 = z'$
$I_3 = z$

(v) Partition the K-maps with x and z as control signals.



F4



F5

The data inputs are as follows:

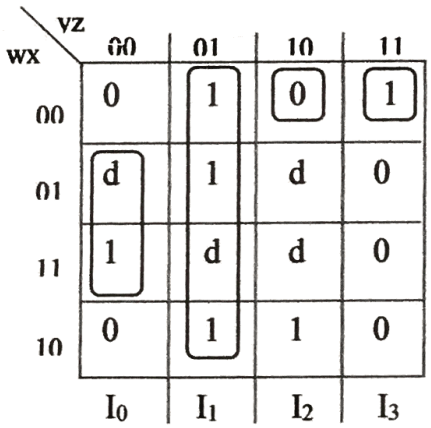
For F4

$I_0 = wy$
$I_1 = w' + y'$
$I_2 = 1$
$I_3 = y'$

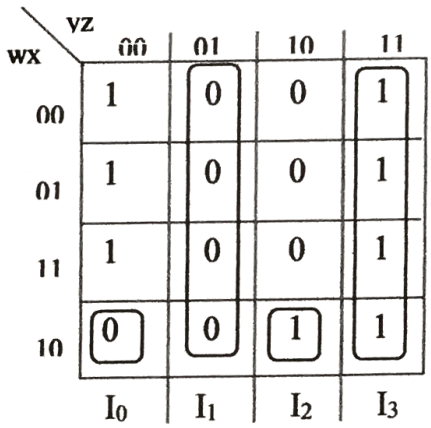
For F5

$I_0 = w' \oplus y$
$I_1 = y$
$I_2 = y'$
$I_3 = y$

(vi) Partition the K-maps with y and z as control signals.



F_4



F_5

The data inputs are as follows:

For F_4

$I_0 = x$
$I_1 = 1$
$I_2 = w + x$
$I_3 = w'x'$

For F_5

$I_0 = w' + x$
$I_1 = 0$
$I_2 = wx'$
$I_3 = 1$

By comparing the six different combinations for control signals, the best selection is __(i)_____.

3. List of ICs and unused gates

IC number	Type number	Function	Unused gates
1	74155	Dual 2-to-4 decoders	None
2	74153	Dual 4-to-1 multiplexers	None
3	74153	Dual 4-to-1 multiplexers	None
4	7400	Quad 2-input NAND	4
5	7400	Quad 2-input NAND	4
6	7402	Quad 2-input NOR	None
7	7420	Dual 4-input NAND	None
8	7486	Quad 2-input XOR	2

4. Simulation results

Table for simulation results

(Place a check mark in the column "Incorrect results" for each simulation value that is different from the value listed in the truth table in Section 2. All don't-care terms should have values of either 0 or 1.)

Inputs	Simulation results					Incorrect results				
w x y z	F_1	F_2	F_3	F_4	F_5	F_1	F_2	F_3	F_4	F_5
0 0 0 0	0	1	1	0	1					
0 0 0 1	1	0	0	1	0					
0 0 1 0	1	0	1	0	0					
0 0 1 1	0	1	0	1	1					
0 1 0 0	1	0	0	1	1					
0 1 0 1	0	1	0	1	0					
0 1 1 0	1	0	0	0	0					
0 1 1 1	0	0	1	0	1					
1 0 0 0	0	1	1	0	0					
1 0 0 1	1	0	1	1	0					
1 0 1 0	1	0	1	1	1					
1 0 1 1	0	1	0	0	1					
1 1 0 0	1	0	1	1	1					
1 1 0 1	0	1	0	1	0					
1 1 1 0	1	0	0	0	0					
1 1 1 1	0	0	0	0	1					

5. Schematic diagram

Schematic diagram for the 4-input 5-output circuit

Attach a complete schematic diagram including the title box.

16.265 Logic Design
Experiment 3: Design with Decoders and Multiplexers
Name: Dangnhi Ngoc Ngo
Student Logic Number: 140
Function Set Number: 3