UNIVERSITY OF MASSACHUSSETS LOWELL
Department of Electrical & Computer Engineering
Course Syllabus for EECE 2650 Logic Design
Spring 2018

I. General Information: Instructors and Course

Sections 201 Instructor:	Prof. Tricia Chigan
Office Location:	BL 401
Office hours:	Monday, Wednesday 10:30am – 12:00pm
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Section 202 & 203 Instructor:	Prof. Jianxin Tang
Office Location:	BL 311
Office hours:	Monday, Wednesday, 2:00pm – 3:30pm
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Lecture meeting time & location:	Monday, Wednesday, Friday 1:00 p.m.-1:50 p.m. Section 201 in Ball Hall 208 Section 202 in Kitson 305 Monday, Wednesday, Friday 11:00 a.m.-11:50 a.m. Section 203 in Ball Hall 314

Pre-requisites: (1) 92.132 Calculus II with a grade of C or better.
OR (2) 91.102 Computing II.

Students for whom the course is intended:
This is a required course for all Electrical & Computer Engineering, Computer Science, and Mechanical Engineering (Robotics option) majors. Students in the Electrical Engineering and Computer Engineering graduate programs can also take this course to make up deficiency.

Course web-page: http://faculty.uml.edu/Tricia_Chigan/Courses/16_265/LogicDesign.html

II. Textbook, Notes, Reference, Software

1. Anh Tran, "Fundamentals of Logic Design, 2nd Edition", ISBN 978-0-470-19044-9, John Wiley Custom Publishing, 2008 (Electronic version is available online, to be announced in class)
2. Anh Tran, "Experiments in Logic Design", 2014 (To be handed out in week 4)
3. Capilano Computing Systems Ltd., "LogicWorks 5: Interactive Circuit Design Software", Addison Wesley, 2004.

III. Course Structure and Goals

Structure: There are three 50-minute lectures each week. There is also a laboratory component of five analysis/designs with software simulation and circuit wiring. Homework exercises will also be assigned but not collected/graded.

Goals: This is an introductory course, which covers the basics of digital circuit design in both theory and practice. Upon completion of the course, students are expected to be able to:

1. analyze combinational and sequential circuits,
2. design/synthesize combinational circuits using SSI and MSI circuits and programmable logic devices,
3. design/synthesize synchronous sequential circuits,
4. apply the design techniques of combinational and sequential circuits to the design of more complex circuits using register level logic.

IV. Content Outline

The contents of the course are partitioned into four parts: fundamentals, combinational logic, sequential logic, and register level logic. How they are related to each other and the topics in each part are outlined in the chart on p.3. It also shows where the experiments are incorporated into the course.

V. Course Objectives

A. Fundamentals

1. Convert numbers between two systems.
2. Convert numbers to computer codes or vice versa.
3. Generate parity check bits for error detection.
4. Find the 2's complement of signed numbers.
5. Subtract two signed numbers using 2's complement arithmetic.
6. Prove the validity of Boolean equations.
7. Convert and simplify Boolean expressions to SOP and POS by algebraic methods.
8. Minimize the number of literals of a Boolean function.
9. Find the complement and dual of Boolean expressions.
10. Expansion of Boolean functions into sub-functions.
11. Construction of Boolean functions from sub-functions.
12. Represent Boolean functions by binary trees.

B. Combinational Logic

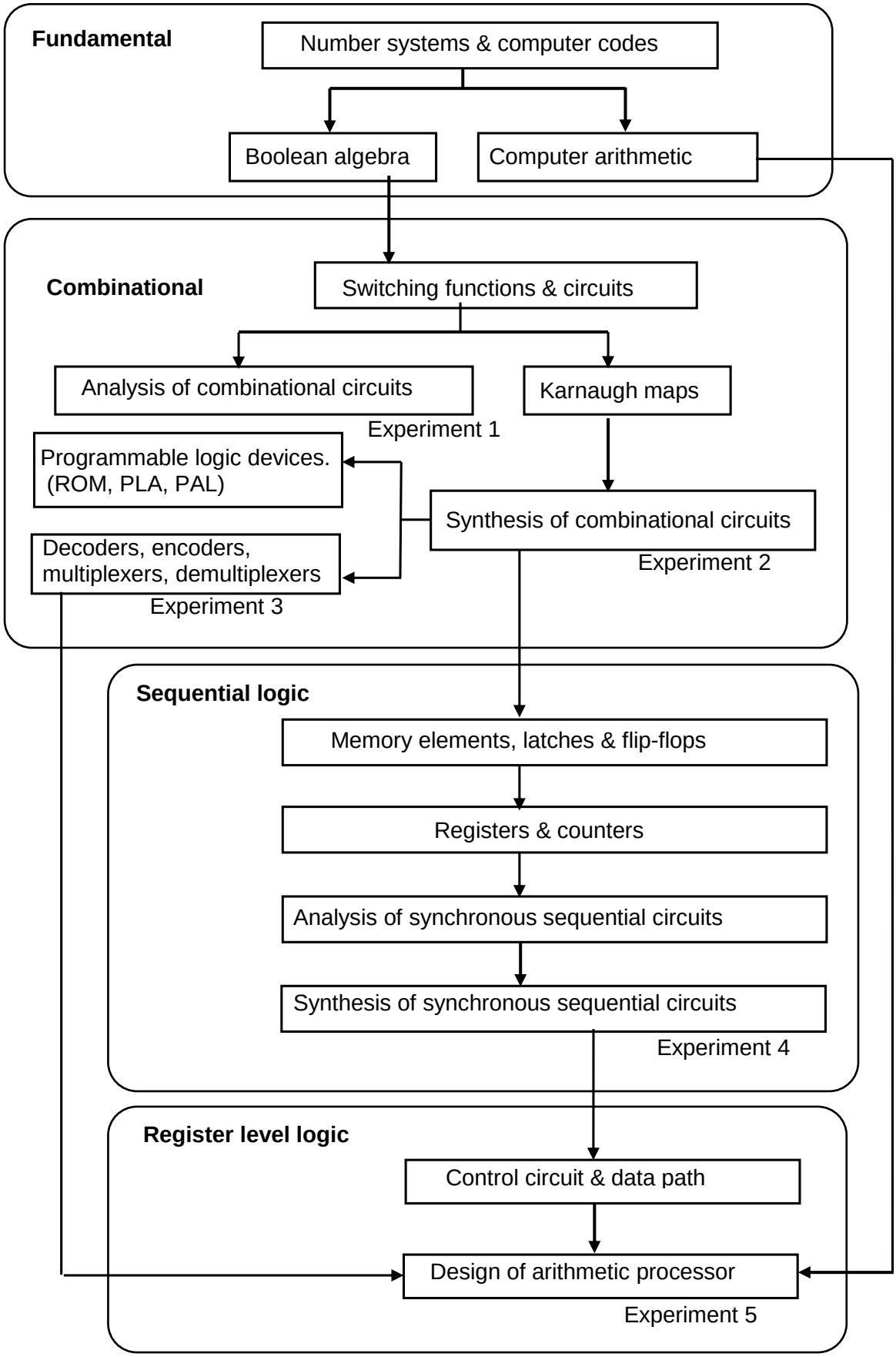
1. Convert Boolean functions to minterm, maxterm, standard SOP & POS forms.
2. Apply active-high and active-low signal levels to circuit inputs and outputs.
3. Apply DeMorgan's theorem to circuit diagrams without using Boolean algebra.
4. Construct the Karnaugh map for a Boolean function.
5. Use Karnaugh maps to find the simplest SOP & POS for a Boolean function.
6. Recognize the exclusive-OR patterns on a K-map.
7. Partition Karnaugh maps into sub-function maps.
8. Express word problems by truth tables and Boolean functions.
9. Implement a Boolean function as various 2-level circuits.
10. Convert two-level circuits to multi-level circuits
11. Design combinational circuits using NAND, NOR, AND, OR, XOR.
12. State the functions of decoders, encoders, multiplexers, and demultiplexers.
13. Construct large-size decoders from smaller size decoders
14. Implement Boolean functions using decoders.
15. Construct large-size decoders from smaller size decoders.
16. Implement Boolean functions using multiplexers.
17. Describe the structures and characteristics of ROM, PLA, & PAL.
18. Implement Boolean functions using programmable logic devices.

C. Sequential Logic

1. Derive the characteristics of SR latches. and flip-flops.
2. Derive the characteristic tables, characteristic equations, and state diagrams of various types of flip-flops.
3. State the operations of master-slave flip-flops and edge-triggered flip-flops.
4. Describe the operations of shift registers and counters.
5. Design universal shift registers, self-correcting counters, and ring counters.
6. Describe the difference between the Moore model and the Mealy model of synchronous sequential circuits.
7. Draw the timing diagrams for synchronous sequential circuits.
8. Derive the state diagram of a synchronous sequential circuit by following the analysis procedure.
9. Construct the state diagram of a synchronous sequential circuit.
10. Convert state diagrams to transition tables and next state maps.
11. Derive excitations to flip-flops from next state maps.
12. Design synchronous sequential circuits by following the synthesis procedures.

D. Register Level Logic

1. Partition a more complex circuit into a data path and a control circuit.
2. Describe the operations carried out by a data path.
3. Describe the operations of an algorithmic state machine (ASM) chart.
4. Convert state diagrams to ASM charts.
5. Design using one flip-flop per state.
6. Design state generators.
7. Design the control circuit.
8. Determine the functions performed by an arithmetic processor.


Fundamental
Number systems & computer codes
Boolean algebra
Computer arithmetic
Combinational
Switching functions & circuits
Analysis of combinational circuits
Karnaugh maps
Experiment 1
Programmable logic devices.
(ROM, PLA, PAL)
Synthesis of combinational circuits
Experiment 2
Decoders, encoders,
multiplexers, demultiplexers
Experiment 3
Sequential logic
Memory elements, latches & flip-flops
Registers & counters
Analysis of synchronous sequential circuits
Synthesis of synchronous sequential circuits
Experiment 4
Register level logic
Control circuit & data path
Design of arithmetic processor
Experiment 5

VI. Laboratory Structure:

There are five experiments in this course. Circuit(s) designed in each experiment are simulated by using the software package LogicWorks 4 or LogicWorks 5.0. Circuits can be designed at home or in the computer laboratory (Ball 420) where LogicWorks 4 is available. **LogicWorks 4 is also available on vlabs.uml.edu.** You can log in with your school credentials. A report is required for each experiment. Students are also required to wire a given combinational circuit in the laboratory using SSI circuits.

Policies:

1. All experiments in this course should be done independently. No collaboration or copying is allowed. Punishments for violating this rule are listed below.
   (i) Report: No credit for the experiment.
   (ii) Design: The letter course grade will be reduced by two levels. For example, a grade of "A" will be reduced to "B+", "C+" will become "C–".
   (iii) A letter will be sent to the student's advisor/department chair/program director. Punishment also applies to those who are copied. Therefore safeguard your reports and designs. Do not leave them in public domain.
2. Reports are due before 2:00 p.m. of the due date. There is a grace period of 48 hours. If the end of the grace period is not on a school day, the grace period is extended to 2:00 p.m. of the next school day. No report will be accepted after the grace period. Exceptions may be granted only by the course instructor under unusual circumstances beyond the control of the student.
3. Circuits that are not designed according to requirements will not be accepted.
4. Additional report and design requirements are described in the laboratory notes.

   The wiring of circuits is scheduled after Spring Break. Each student may sign up a slot not in conflict with their class schedule in advance.

VII. Calendar and Lecture Topics

The course calendar and lecture topics are given on page 5. Note that (a) lecture topics do not necessarily follow the order of the course contents outlined in Section IV, (b) the coverage of each topic may need more or less time than what is allocated. Thus it is the responsibility of students to attend classes and find out the exact coverage of the course materials in each class.

When class is cancelled or school is closed due to adverse weather or any other reasons, the make-up schedules for examinations will be announced separately.
In such cases, the due day for experiments will be extended to the next school day. The wiring of circuits will be re-scheduled.

You may call 978-934-2121 for a recorded announcement of class cancellation.

VIII. Course Grade

The distribution of grades is given below. The grade policies for laboratory are described separately in Section VI.

Laboratory	Circuit wiring	2%
	Experiments 1 & 5	10%
	Experiments 2, 3, & 4	18%
Examinations 1		20%
Examinations 2		20%
Final Exam		25%
Class attendance		5%

A minimum standard of 60% in the combined experiment and examination grades is used as a measure for the passing of the course. Assignments of course (letter) grades other than "F" depend on class distributions, which usually start with a minimum of 90% for "A".

A course grade of F will be assigned for cheating in exams. A letter will be sent to the student's advisor/department chair/program director.

Calendar and Lecture Topics

Week	Dates	Lecture Topics (Chapter)	Laboratory/Remark
1	01/22 (M) 01/24 (W) 01/26 (F)	Introduction to digital systems. (1) Number systems. (2)	
2	01/29 (M) 01/31 (W) 02/02 (F)	Number systems and codes. (2) Boolean algebra. (3)	
3	02/05 (M) 02/07 (W) 02/09 (F)	Boolean algebra (3)	
4	02/12 (M) 02/14 (W) 02/16 (F)	Boolean functions and digital circuits (4)	Experiments handouts distributed
5	02/20 (T) 02/21 (W) 02/23 (F)	Boolean functions and digital circuits (4) **Examination 1 (Friday 02/23, 6:30 pm – 8:00 pm)**	*02/19 President Day*
6	02/26 (M) 02/28 (W) 03/02 (F)	Karnaugh maps (5)	**Experiment 1 due Wednesday., 02/28**
7	03/05 (M) 03/07 (W) 03/09 (F)	Synthesis of combinational circuits (6) Decoders and encoders (7)	Circuit Wiring
8		**Spring Break**	
9	03/19 (M) 03/21 (W) 03/23 (F)	Multiplexers and de-multiplexers (7)	**Experiment 2 due Wednesday, 03/21**
10	03/26 (M) 03/28(W) 03/30 (F)	Latches and flip-flops (9) Shift registers & counters (10)	
11	04/02 (M) 04/04 (W) 04/06(F)	Analysis and synthesis of sequential circuits (10)	**Experiment 3 due Monday, 04/02**
12	04/09 (M) 04/11 (W) 04/13 (F)	Adder. Signed numbers. ASM charts (11). **Examination 2 (Friday 04/13, 6:30 – 8:00 pm)**	04/09- Last day to withdraw with "W"
13	04/18 (W) 04/20 (F)	Control circuit and data path (11)	*04/16 Patriot's Day* **Experiment 4 due Wednesday, 04/18**
14	04/23 (M) 04/25 (W) 04/27 (F)	Design of an arithmetic processor (11)	
15	04/30 (M) 05/02 (W)	Design with ROM, PLA, & PAL (8) Review	**Experiment 5 due Monday, 04/30**
16	**Final Examination**	**Date, time, and room to be announced**	

(a) Lecture topics do not necessarily follow the order of the course contents outlined in Section IV.
(b) The coverage of each topic may need more or less time than what is allocated.