16.265 Logic Design	
Student Logic Number	140
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Experiment Number	4
Date	11/27/2017

For grader use	
Schematic diagram submitted is different from the one in the report. (Need to re-submit the schematic diagram in the report or will be graded based on a maximum of 50 points.)	5 points deduction
Cannot open file	—
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Date student is notified to re-submit a schematic file by e-mail	—
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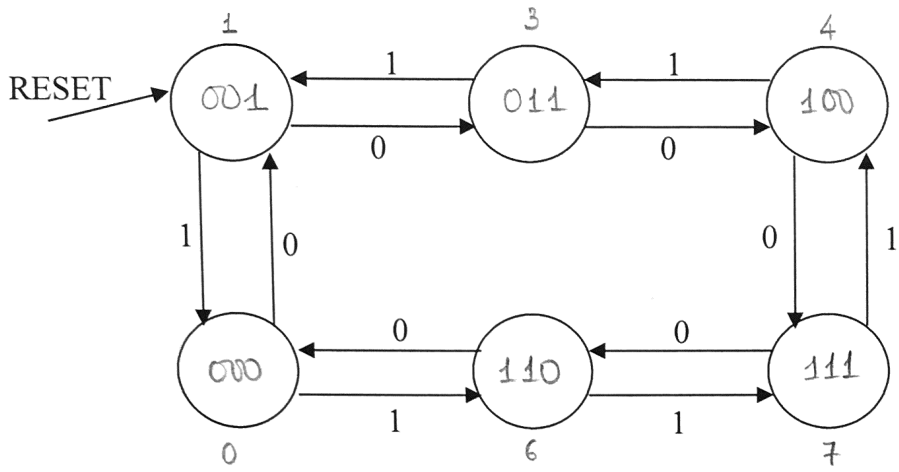
Report will be graded based on a maximum of 50 (out of 100 points) if a schematic diagram is not received within three calendar days of notification or the re-submitted schematic file still cannot be opened or is not readable.

Grade: 100

Experiment 4 Six-State Up-Down Counter

1. Sequence assignment



2. Next-state maps

Construction of transition table

Present state $Q_2\,Q_1\,Q_0$	Next state $Q^+_2\,Q^+_1\,Q^+_0$	
	C = 0	C = 1
0 0 0	001	110
0 0 1	011	000
0 1 0	ddd	ddd
0 1 1	100	001
1 0 0	111	011
1 0 1	ddd	ddd
1 1 0	000	111
1 1 1	110	100

Convert the transition table to next-state maps.

CQ_0 \ Q_2Q_1	00	01	11	10
00	0	d	0	1
01	0	1	1	d
11	0	0	1	d
10	1	d	1	0

Q_2^+

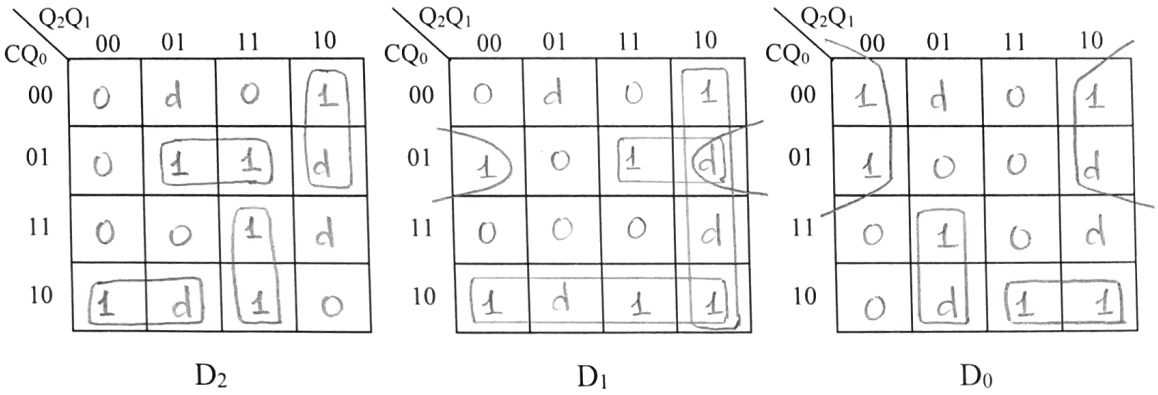
CQ_0 \ Q_2Q_1	00	01	11	10
00	0	d	0	1
01	1	0	1	d
11	0	0	0	d
10	1	d	1	1

Q_1^+

CQ_0 \ Q_2Q_1	00	01	11	10
00	1	d	0	1
01	1	0	0	d
11	0	1	0	d
10	0	d	1	1

Q_0^+

3. Design using D flip-flops



Determine the excitation functions from the next state maps.

$D_2 = C'(Q_1Q_0 + Q_2Q_1') + C(Q_2Q_1 + Q_2'Q_0')$

$D_1 = CQ_0' + Q_2Q_1' + (Q_1' + Q_2)C'Q_0$

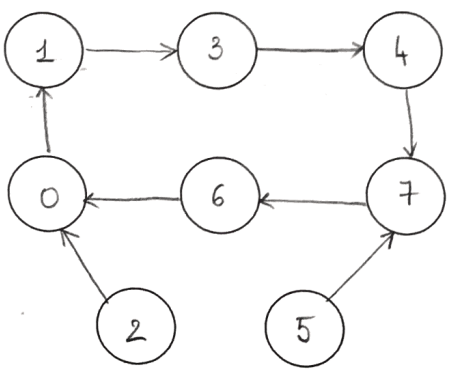
$D_0 = Q_1'C' + (Q_2Q_0' + Q_2'Q_1)C$

List of ICs and unused gates for design using D flip-flops

IC number	Type number	Function	Unused gates
1	7474	Dual D type flip-flops	None
2	7474	Dual D type flip-flops	1 D flip-flop
3	7400	2 Input NAND Gates	None
4	7400	2 Input NAND Gates	None
5	7400	2 Input NAND Gates	None
6	7400	2 Input NAND Gates	None
7	7410	3 Input NAND Gates	None
8			

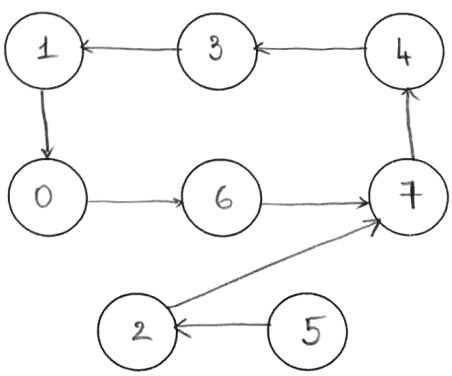
Simulation results for design using D flip-flops

C = 0



Unused states

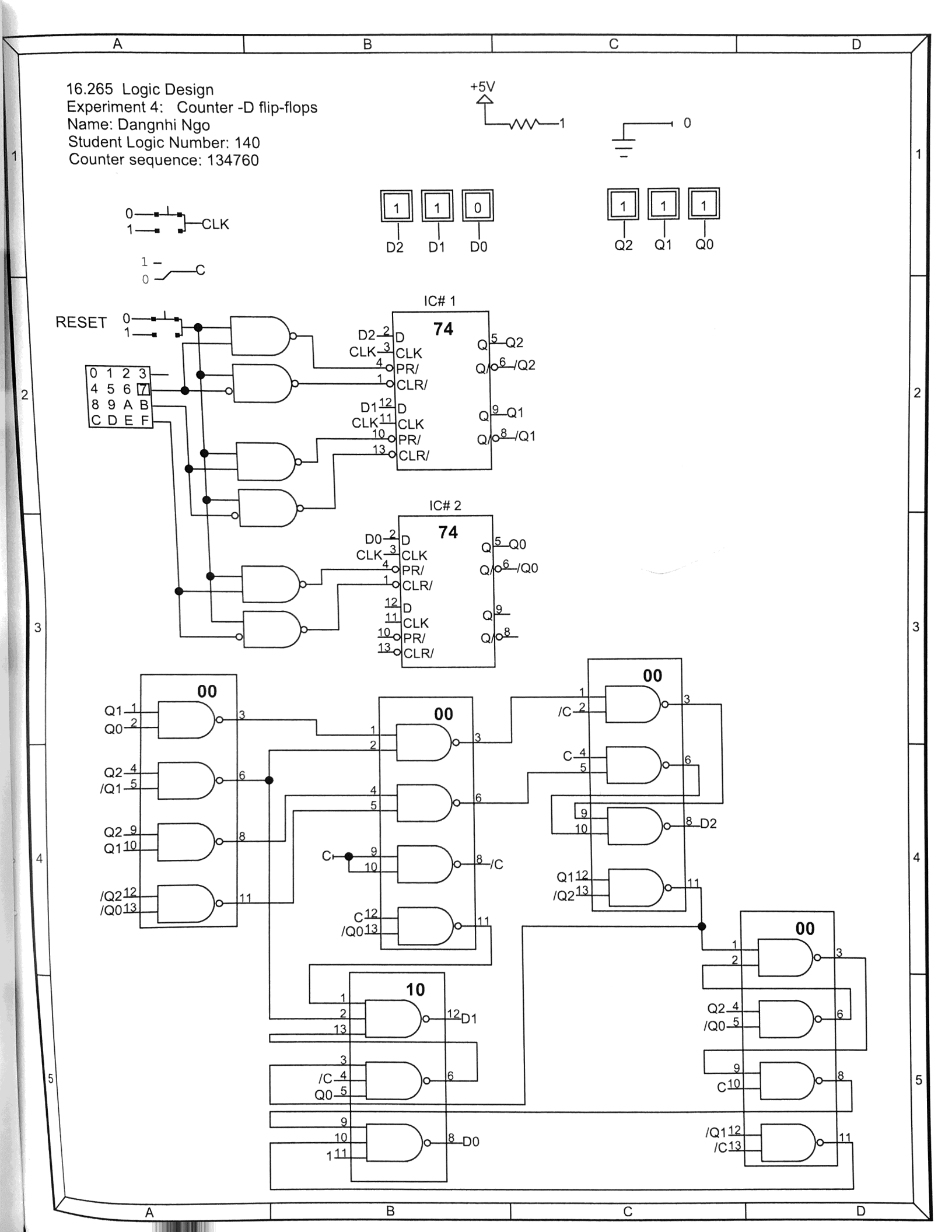
C = 1



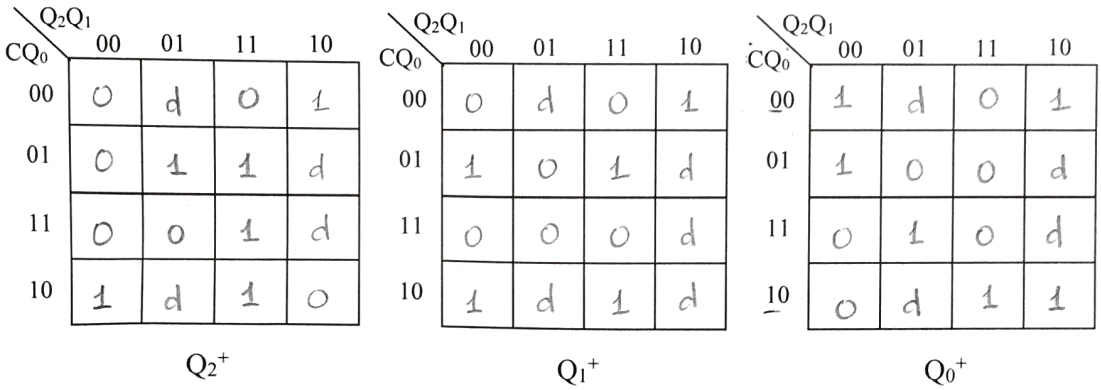
Unused states

Draw the schematic diagrams for the counter using D flip-flops.
Insert a complete schematic diagram including the title box.

16.265 Logic Design
Experiment 4: Counter -D flip-flops
Name: Dangnhi Ngo
Student Logic Number: 140
Counter sequence: 134760



4. Design using JK flip-flops



CQ_0 \ Q_2Q_1	00	01	11	10
00	0	d	0	1
01	0	1	1	d
11	0	0	1	d
10	1	d	1	0

Q_2^+

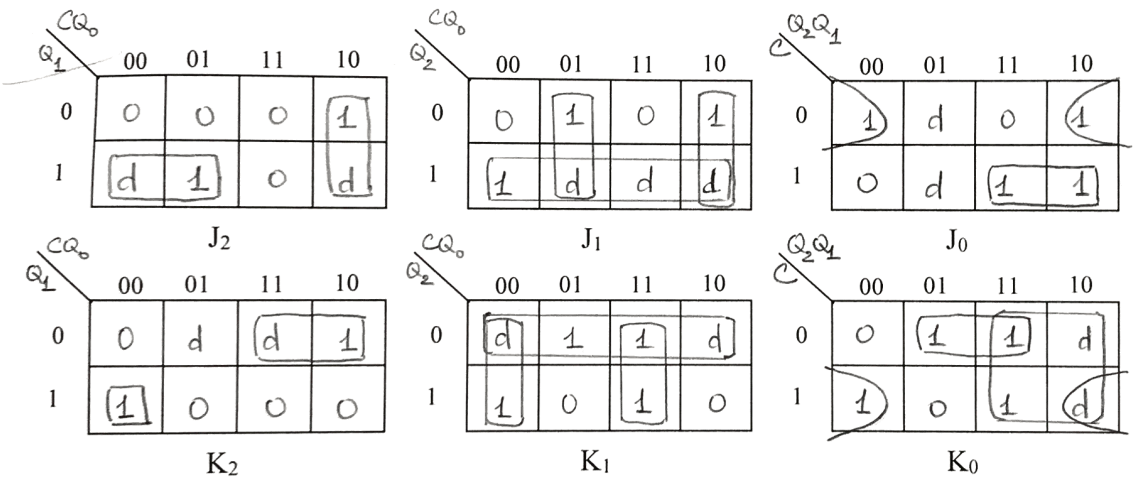
CQ_0 \ Q_2Q_1	00	01	11	10
00	0	d	0	1
01	1	0	1	d
11	0	0	0	d
10	1	d	1	d

Q_1^+

CQ_0 \ Q_2Q_1	00	01	11	10
00	1	d	0	1
01	1	0	0	d
11	0	1	0	d
10	0	d	1	1

Q_0^+

Partition the next state maps into K-maps for the excitation functions.
(Don't forget to label the variables at the upper left corner of each K-map.)



Q_1 \ CQ_0	00	01	11	10
0	0	0	0	1
1	d	1	0	d

J_2

Q_2 \ CQ_0	00	01	11	10
0	0	1	0	1
1	1	d	d	d

J_1

C \ Q_2Q_1	00	01	11	10
0	1	d	0	1
1	0	d	1	1

J_0

Q_1 \ CQ_0	00	01	11	10
0	0	d	d	1
1	1	0	0	0

K_2

Q_2 \ CQ_0	00	01	11	10
0	d	1	1	d
1	1	0	1	0

K_1

C \ Q_2Q_1	00	01	11	10
0	0	1	1	d
1	1	0	1	d

K_0

Determine the excitation functions from the six K-maps.

$J_2 = C'Q_1 + CQ_0'$
$J_1 = Q_2 + (C \oplus Q_0)$
$J_0 = Q_1'C' + Q_2C$

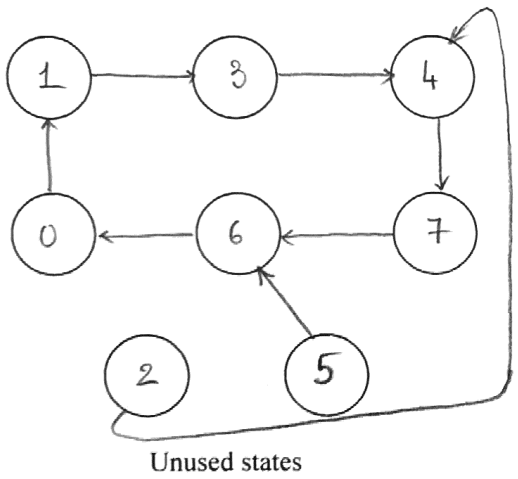
$K_2 = CQ_1' + C'Q_0'Q_1$
$K_1 = Q_2' + CQ_0 + C'Q_0'$
$K_0 = Q_2 + (Q_1 \oplus C)$

List of ICs and unused gates for design using JK flip-flops

IC number	Type number	Function	Unused gates
1	7476	Dual JK type flip-flops	None
2	7476	Dual JK type flip-flops	1 JK flip-flop
3	7400	2 Input NAND Gates	None
4	7400	2 Input NAND Gates	None
5	7400	2 Input NAND Gates	None
6	7400	2 Input NAND Gates	1
7	7410	3 Input NAND Gates	1
8	7486	2 Input XOR Gates	2

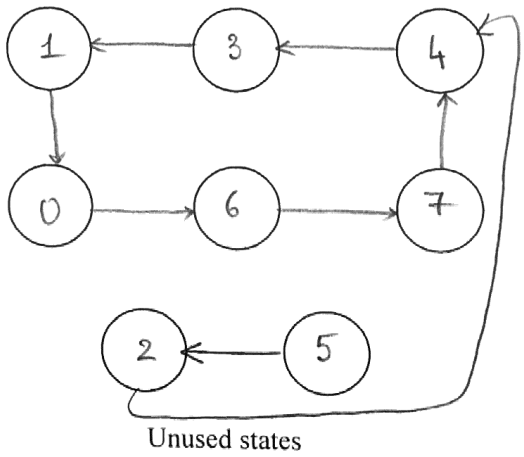
Simulation results for design using JK flip-flops

C = 0



Unused states

C = 1



Unused states

Draw the schematic diagrams for the counter using JK flip-flops.
Insert a complete schematic diagram including the title box.

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