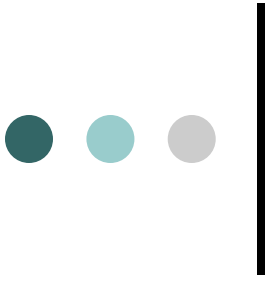


CHAPTER 6

SYNTHESIS OF COMBINATIONAL CIRCUITS



Single-rail and double-rail signals

Single-rail variable or input : Available in only one form

Double-rail variable or input : Available in both true and complemented forms

Fan-in and fan-out limits

Fan-in limit : A constraint on the number of inputs to a gate.

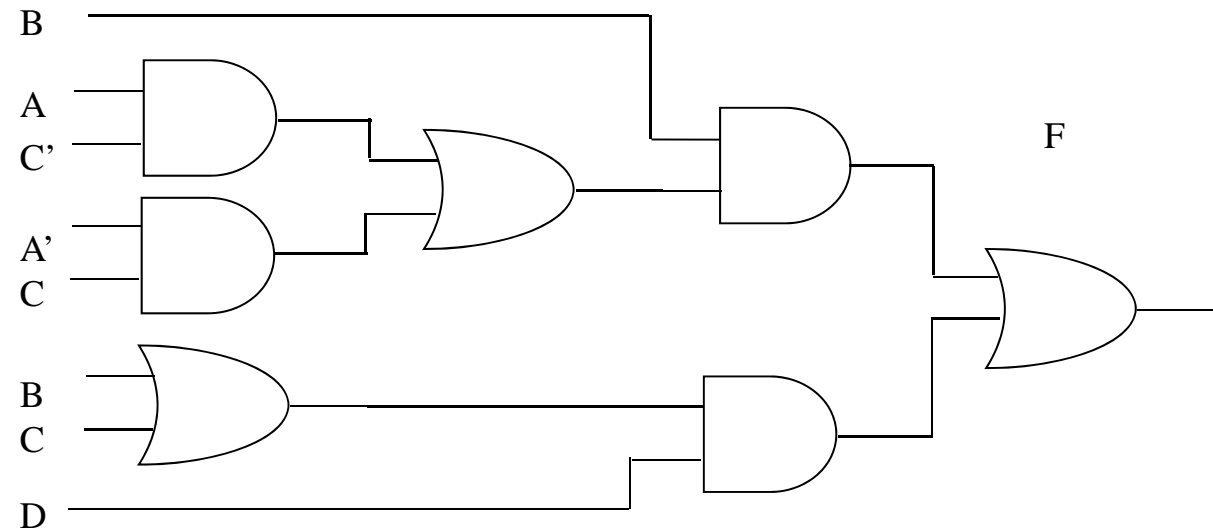
Fan-out limit : The limit to the number of gate inputs that a gate output can be connected to is called.

Level of digital circuits

A circuit is called an n-level circuit. If n is the number of gates in the path with the longest delay (most gates) in a circuit.



4-level Circuit



$$F(A,B,C,D) = \Sigma m(4, 5, 7, 9, 11, 13, 15)$$

$$\begin{aligned} F(A,B,C,D) &= A'BC' + BCD + AD \\ &= (A + B)(A' + D)(C' + D) \end{aligned}$$

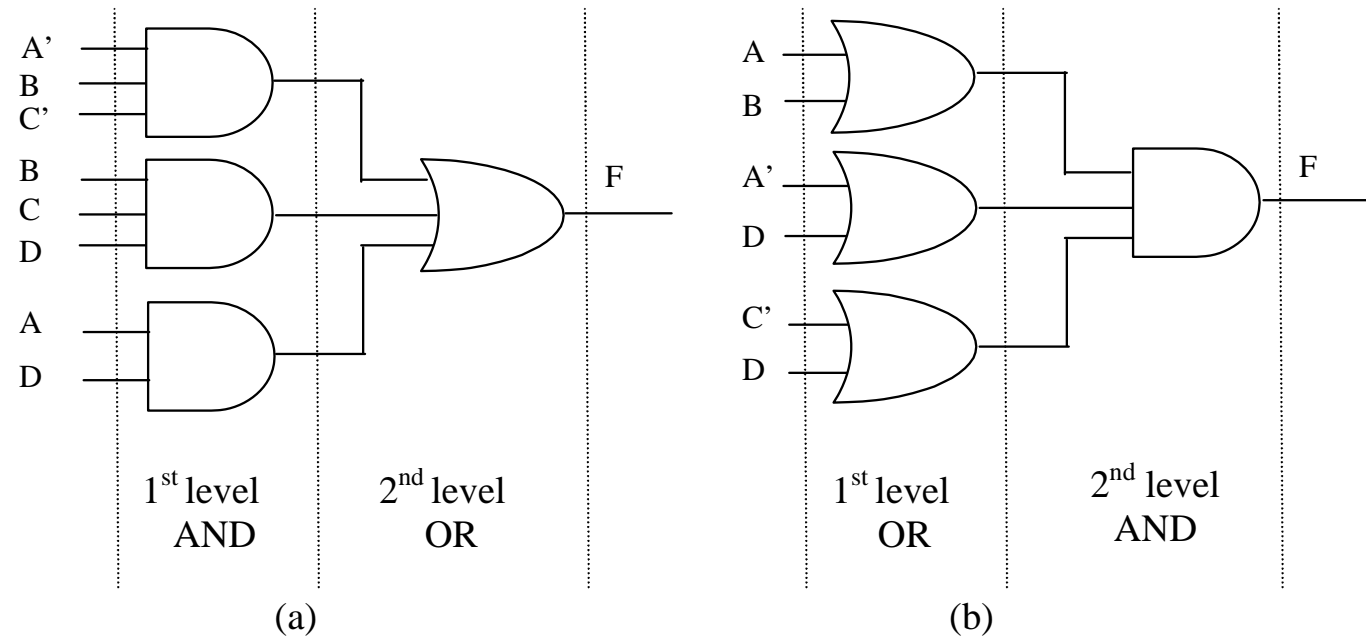
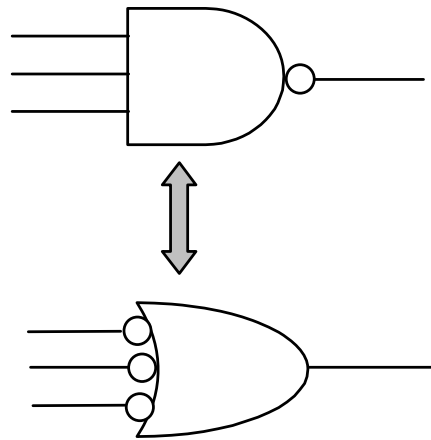
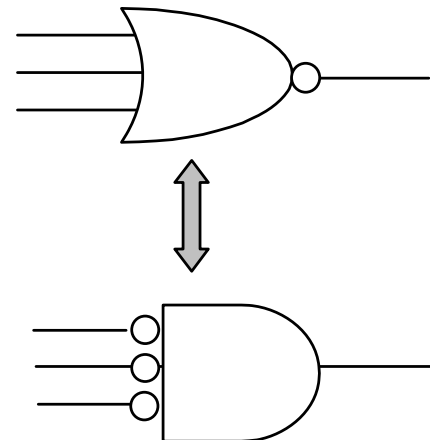


Figure 6.1 (a) 2-level AND-OR circuit. (b) 2-level OR-AND circuit.

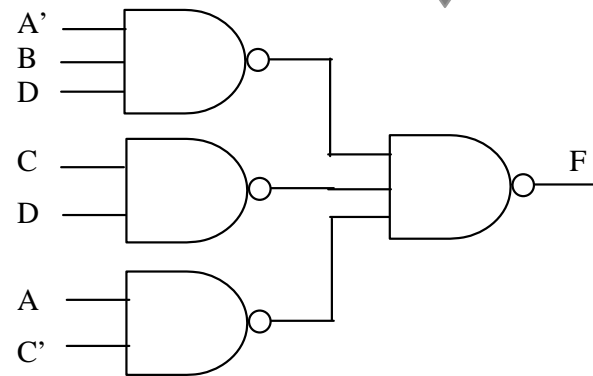
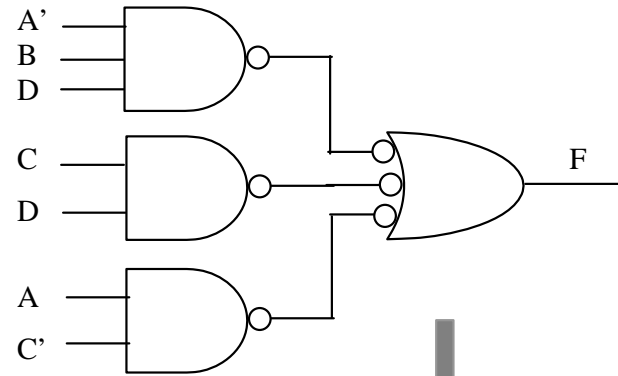
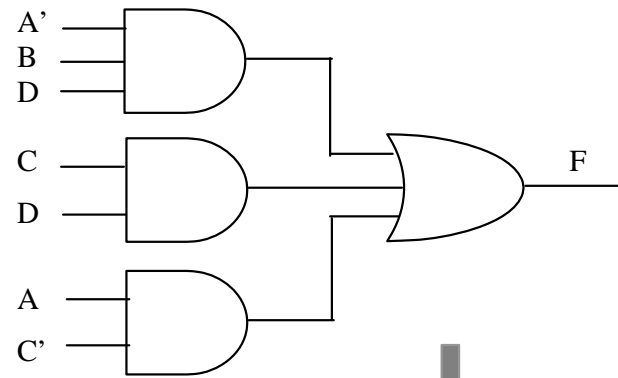
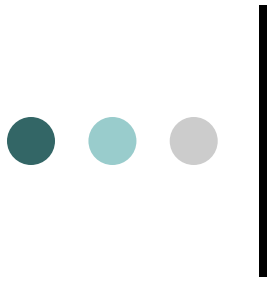


(a)

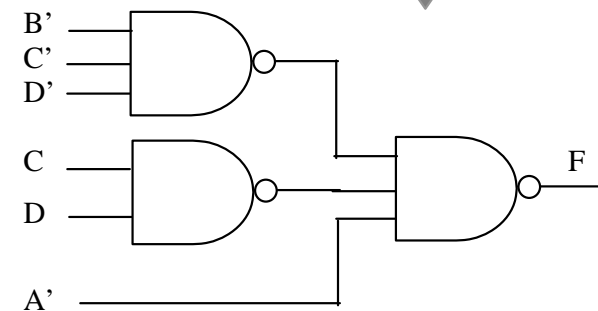
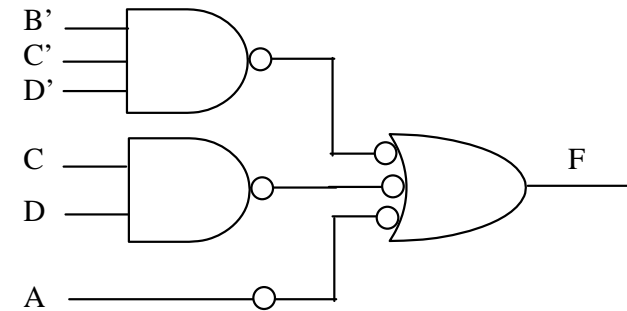
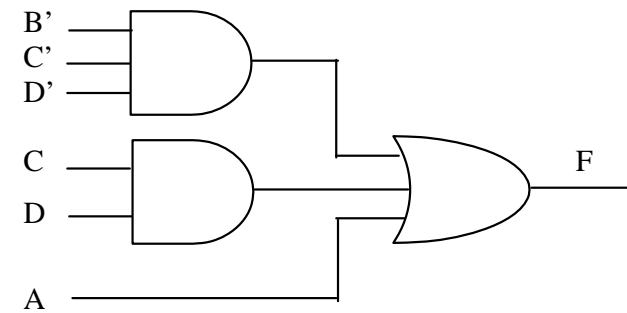


(b)

Figure 6.2 (a) Equivalence between OR with inverted inputs and NAND.
(b) Equivalence between AND with inverted inputs and NOR.

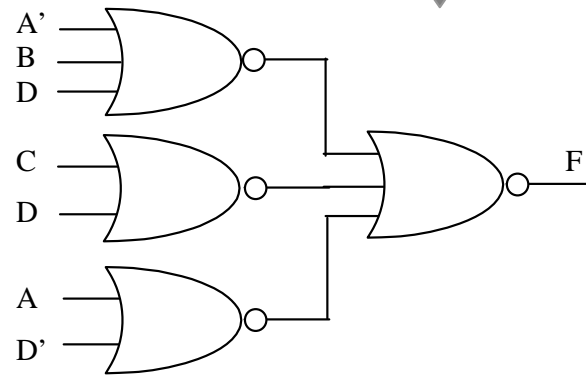
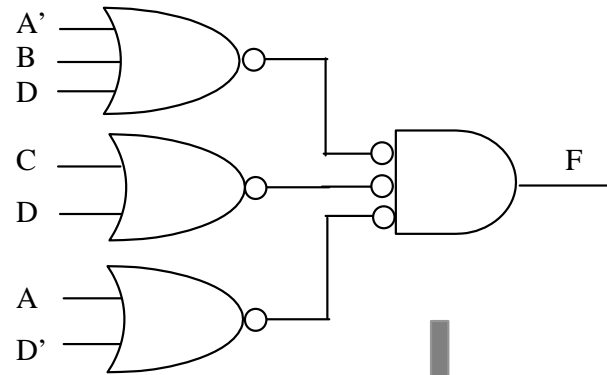
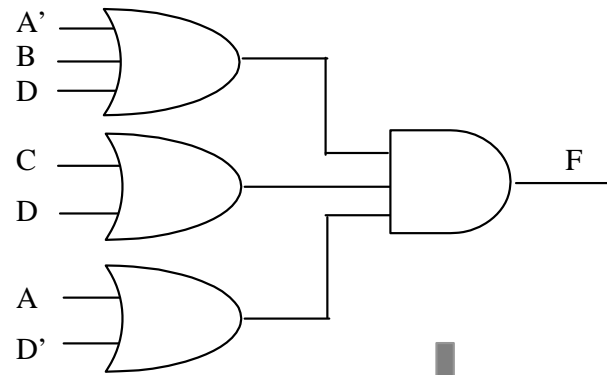
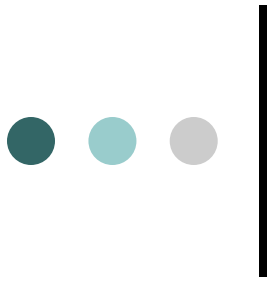


(a)

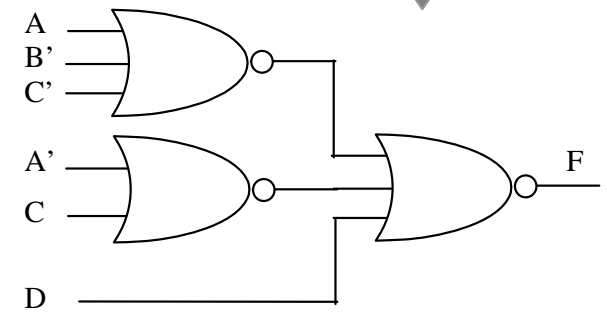
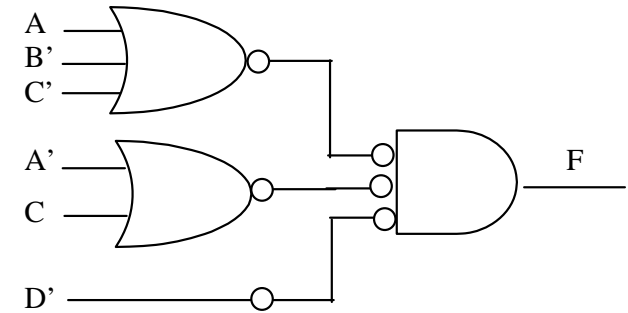
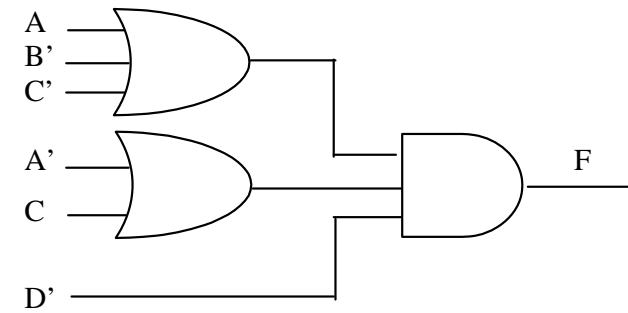


(b)

Figure 6.3 Conversion between 2-level AND-OR and 2-level NAND-NAND circuits.



(a)



(b)

Figure 6.4 Conversion between 2-level OR-AND and 2-level NOR-NOR circuits.

AND-NOR (AOI) Circuit

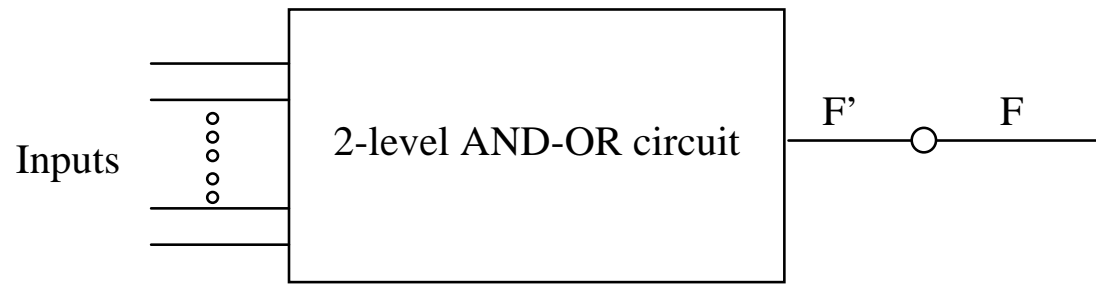


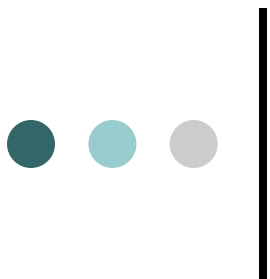
Figure 6.5 Synthesis of 2-level AND-NOR circuit.

❖ Example 6.1

$$F(A,B,C,D) = \Sigma m(2, 3, 4, 5, 7, 10, 11, 15)$$

$$F'(A,B,C,D) = \Sigma m(0, 1, 6, 8, 9, 12, 13, 14)$$

$$F'(A,B,C,D) = BCD' + AC' + B'C'$$



$$F'(A,B,C,D) = \Sigma m(0, 1, 6, 8, 9, 12, 13, 14)$$

$$F'(A,B,C,D) = BCD' + AC' + B'C'$$

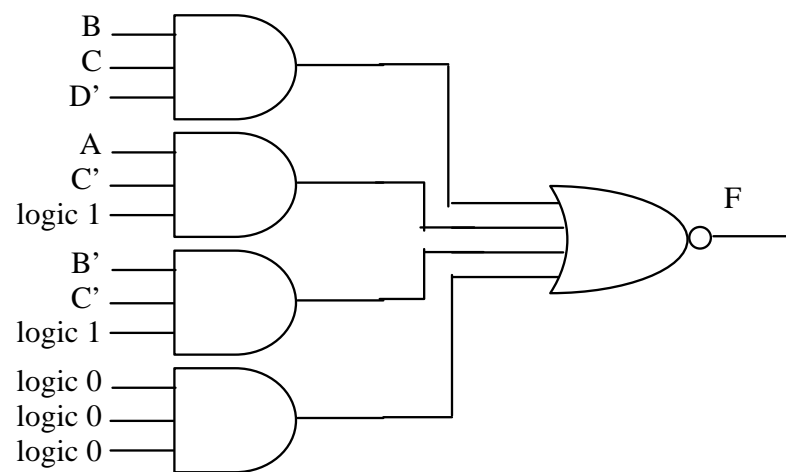


Figure 6.6 Realization of the function in Example 6.1 as an AND-NOR circuit.



Multi-Level Circuits

❖ Example 6.2

$$F(A,B,C,D) = BD + CD + A'BC + ABC'$$

$$F(A,B,C,D) = D(B + C) + B(A'C + AC')$$

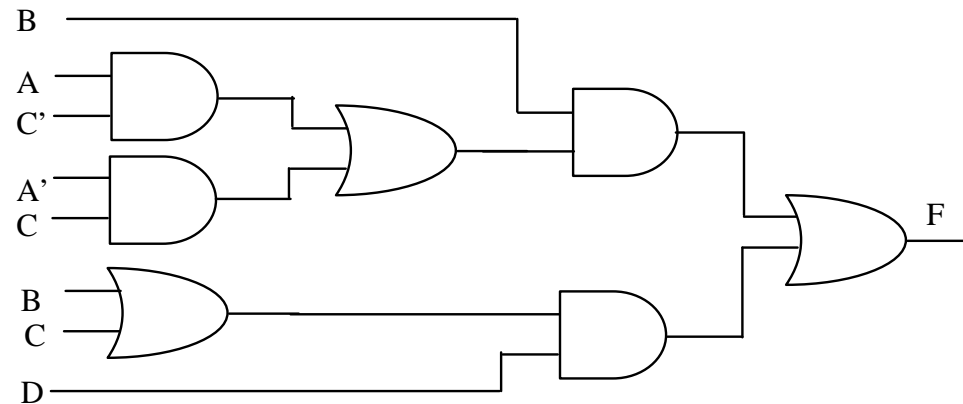


Figure 6.7 4-level circuit for Example 6.2.

❖ Example 6.3

$$F(A,B,C,D,E) = \Sigma m(0, 1, 2, 3, 11, 16 - 23, 27, 31)$$

Simplest sum-of products and product-of-sums expressions

$$AB' + ADE + B'C' + C'DE$$

$$(A + C')(B' + D)(B' + E)$$

Product-of-sums expression is better

$$(A + C')(B' + DE)$$

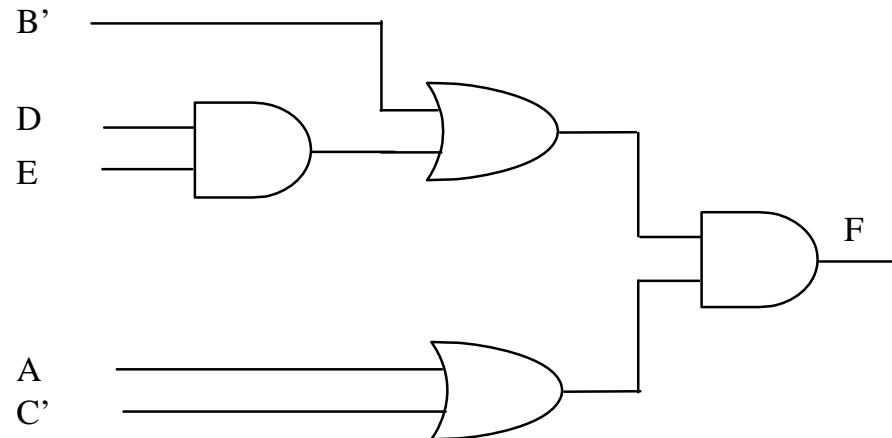


Figure 6.8 3-level circuit for F in Example 6.3.

All-NAND and All-NOR Circuits

❖ Example 6.4

$$F(A,B,C,D) = \Sigma m(3, 5, 6, 7, 12, 13, 14, 15)$$

SOP: $AB + BC + BD + A'CD \Rightarrow B(A + C) + D(B + A'C)$

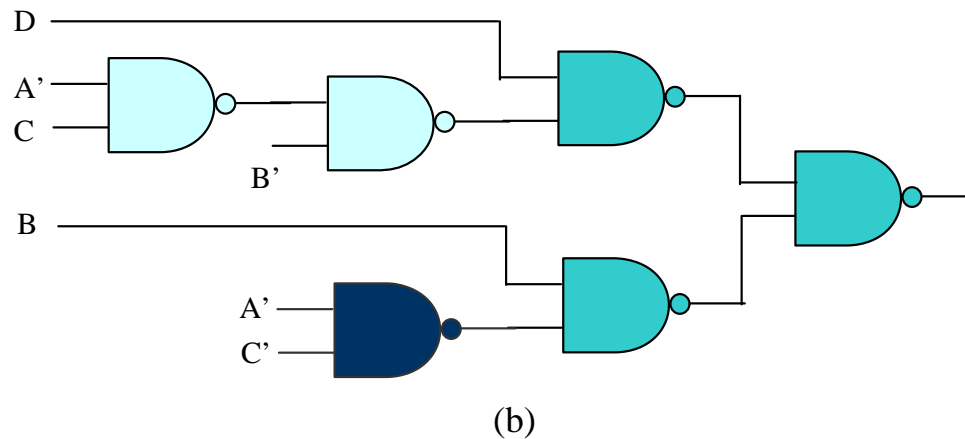
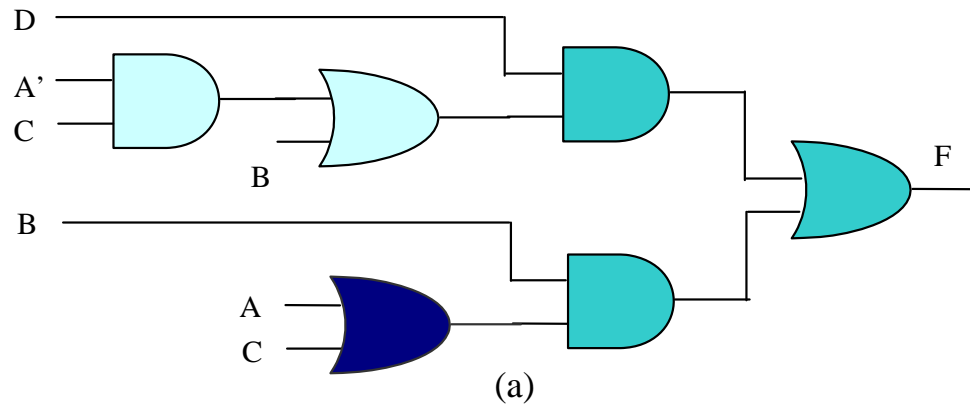
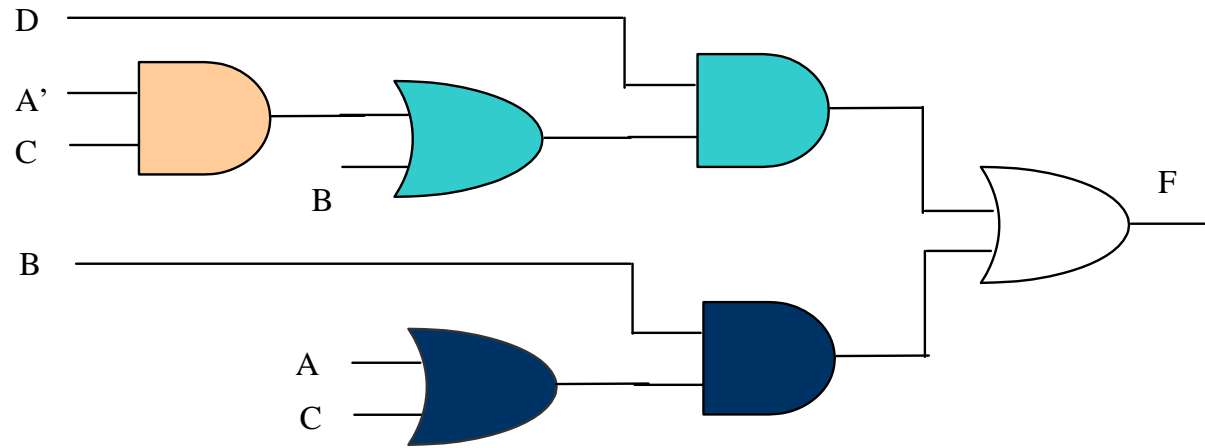
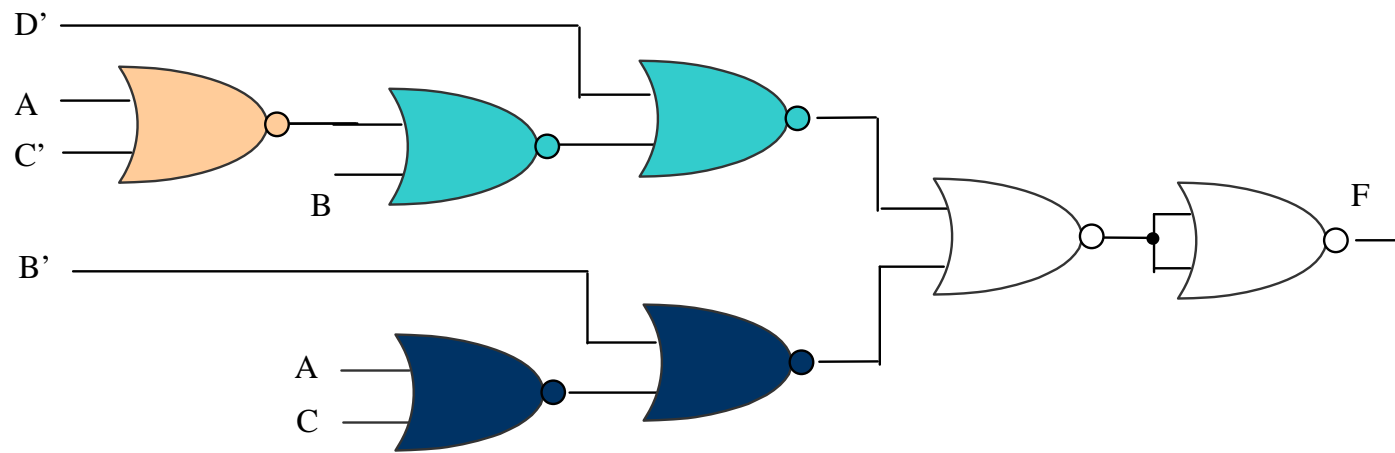


Figure 6.9 Conversion of a multi-level circuit to an all-NAND circuit.



(a)



(b)

Figure 6.10 Conversion of a multi-level circuit to an all-NOR circuit.



POS: $(B + D) (B + C) (A' + B) (A + C + D)$
 $\Rightarrow [D + B(A + C)] [B + A'C]$

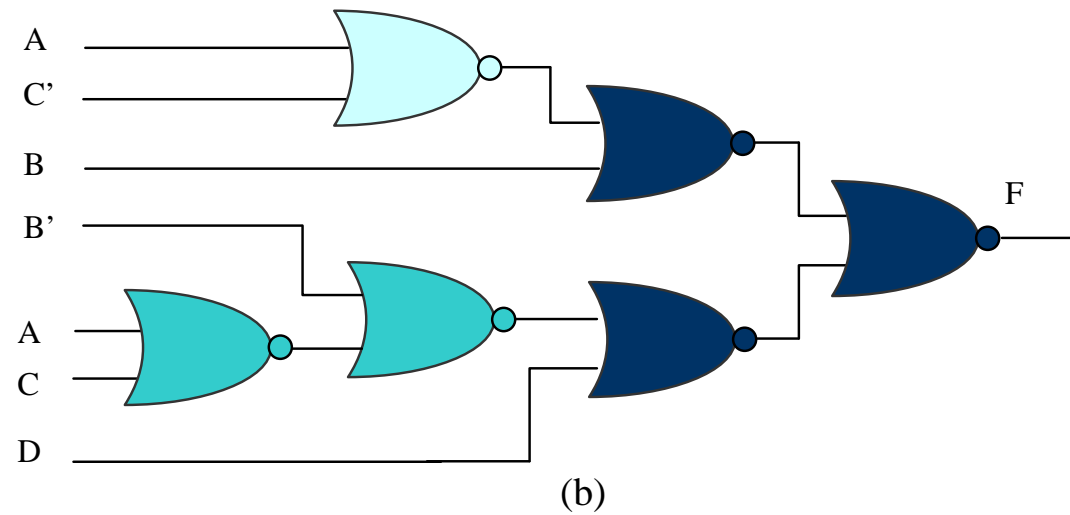
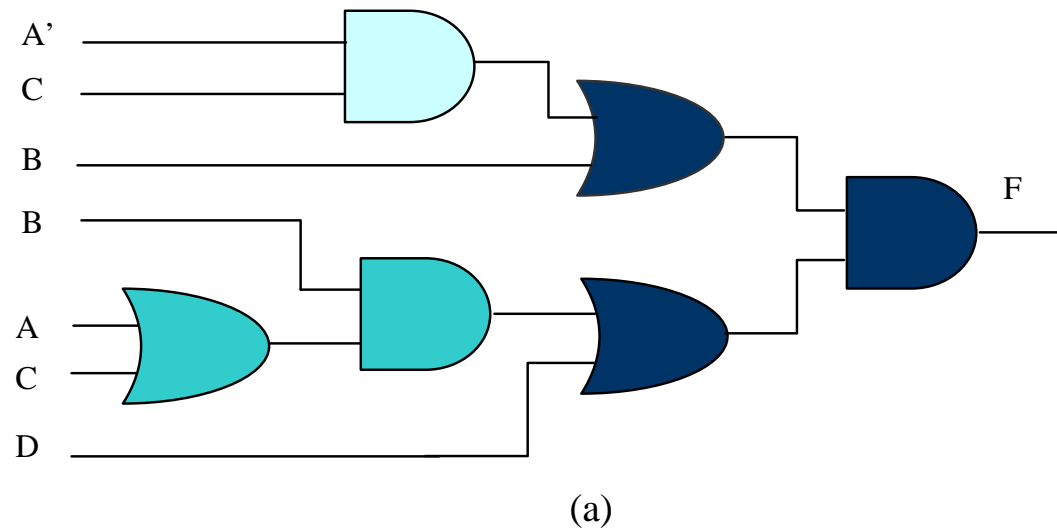


Figure 6.11 A different all-NOR implementation from Figure 6.10.