Instruction set of the Mic1 Macro Language

Binary	Mnemonic	Instruction	Meaning
0000xxxxxxxxxxxx	LODD	Load direct	$ac := m[x]$
0001xxxxxxxxxxxx	STOD	Store direct	$m[x] := ac$
0010xxxxxxxxxxxx	ADDD	Add direct	$ac := ac + m[x]$
0011xxxxxxxxxxxx	SUBD	Subtract direct	$ac := ac - m[x]$
0100xxxxxxxxxxxx	JPOS	Jump positive	**if** $ac \geq 0$ **then** $pc := x$
0101xxxxxxxxxxxx	JZER	Jump zero	**if** $ac = 0$ **then** $pc := x$
0110xxxxxxxxxxxx	JUMP	Jump	$pc := x$
0111xxxxxxxxxxxx	LOCO	Load constant	$ac := x\ (0 \leq x \leq 4095)$
1000xxxxxxxxxxxx	LODL	Load local	$ac := m[sp + x]$
1001xxxxxxxxxxxx	STOL	Store local	$m[x + sp] := ac$
1010xxxxxxxxxxxx	ADDL	Add local	$ac := ac + m[sp + x]$
1011xxxxxxxxxxxx	SUBL	Subtract local	$ac := ac - m[sp + x]$
1100xxxxxxxxxxxx	JNEG	Jump negative	**if** $ac < 0$ **then** $pc := x$
1101xxxxxxxxxxxx	JNZE	Jump nonzero	**if** $ac \neq 0$ **then** $pc := x$
1110xxxxxxxxxxxx	CALL	Call procedure	$sp := sp - 1; m[sp] := pc; pc := x$
1111000000000000	PSHI	Push indirect	$sp := sp - 1; m[sp] := m[ac]$
1111001000000000	POPI	Pop indirect	$m[ac] := m[sp]; sp := sp + 1$
1111010000000000	PUSH	Push onto stack	$sp := sp - 1; m[sp] := ac$
1111011000000000	POP	Pop from stack	$ac := m[sp]; sp := sp + 1$
1111100000000000	RETN	Return	$pc := m[sp]; sp := sp + 1$
1111101000000000	SWAP	Swap ac, sp	$tmp := ac; ac := sp; sp := tmp$
11111100yyyyyyyy	INSP	Increment sp	$sp := sp + y\ (0 \leq y \leq 255)$
11111110yyyyyyyy	DESP	Decrement sp	$sp := sp - y\ (0 \leq y \leq 255)$

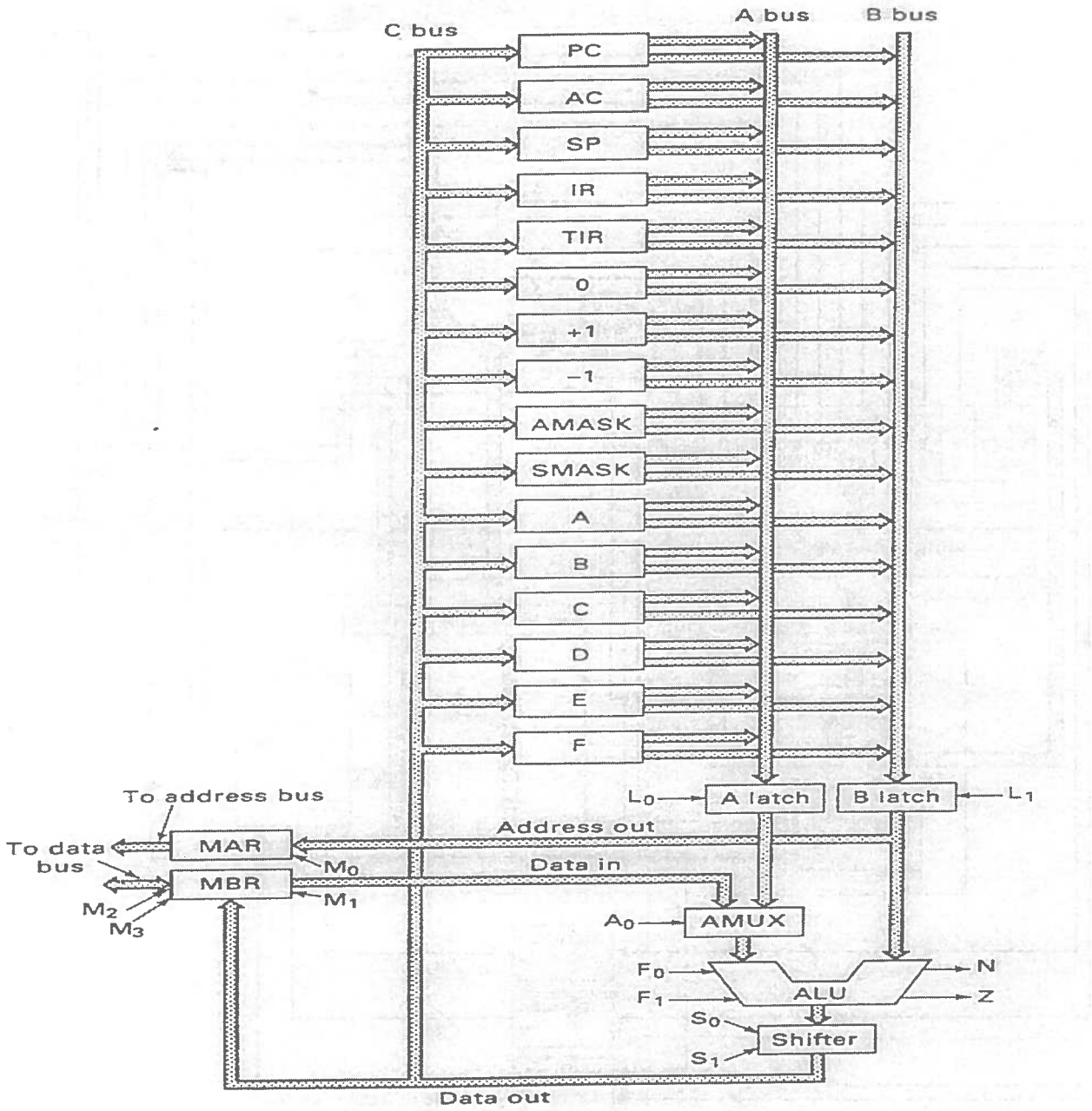
xxxxxxxxxxxx is a 12-bit machine address; in column 4 it is called x.
yyyyyyy is an 8-bit constant; in column 4 it is called y.

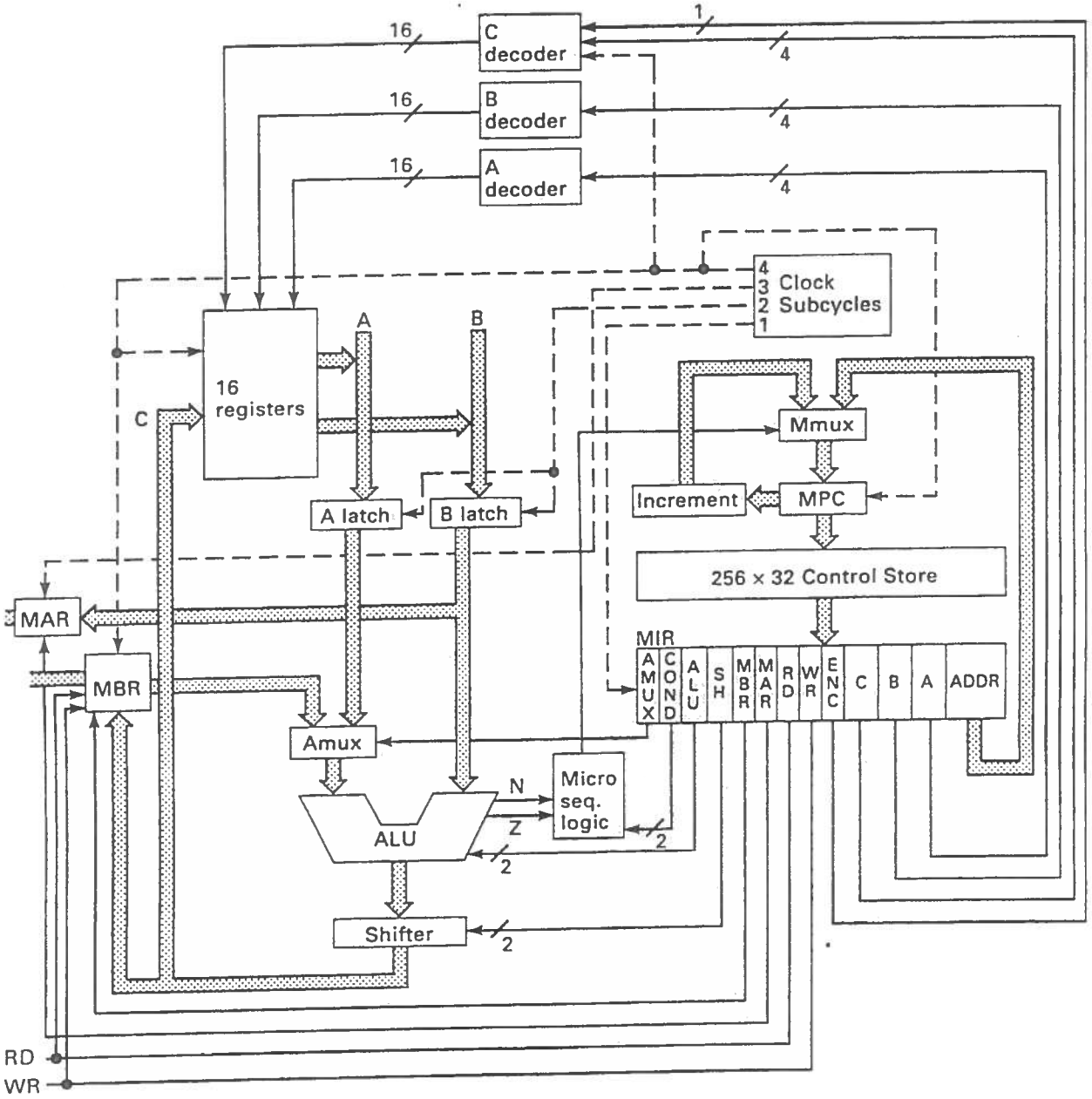
Powers of 2:

2 to the 10^{th} : 1024
2 to the 11^{th} : 2048
2 to the 12^{th} : 4096
2 to the 13^{th} : 8192
2 to the 14^{th} : 16384
2 to the 15^{th} : 32768
2 to the 16^{th} : 65536

Floating Point Formats:

IEEE 754 Single Precision: 1 Sign bit, 8 bits Base 2 Exponent, 23 bits Mantissa
IEEE 754 Double Precision: 1 Sign bit, 11 bits Base 2 Exponent, 52 bits Mantissa
IBM Single Precision: 1 Sign bit, 7 bits Base 16 Exponent, 24 bits Mantissa


C bus
A bus
B bus
PC
AC
SP
IR
TIR
0
+1
−1
AMASK
SMASK
A
B
C
D
E
F
To address bus
To data bus
MAR
MBR
M0
M1
M2
M3
Address out
Data in
L0
A latch
B latch
L1
A0
AMUX
F0
F1
ALU
N
Z
S0
S1
Shifter
Data out


C decoder
B decoder
A decoder
16
4
1
Clock
Subcycles
16 registers
A
B
C
A latch
B latch
Mmux
Increment
MPC
256 x 32 Control Store
MIR
AMUX
COND
ALU
SH
MBR
MAR
RD
WR
ENC
C
B
A
ADDR
MAR
MBR
Amux
ALU
N
Z
Micro seq. logic
Shifter
2
RD
WR