CHAPTER 7

MODULAR CIRCUITS

Decoder

Encoder

Multiplexer

Demultiplexer

7.1.1 Decoder Structure

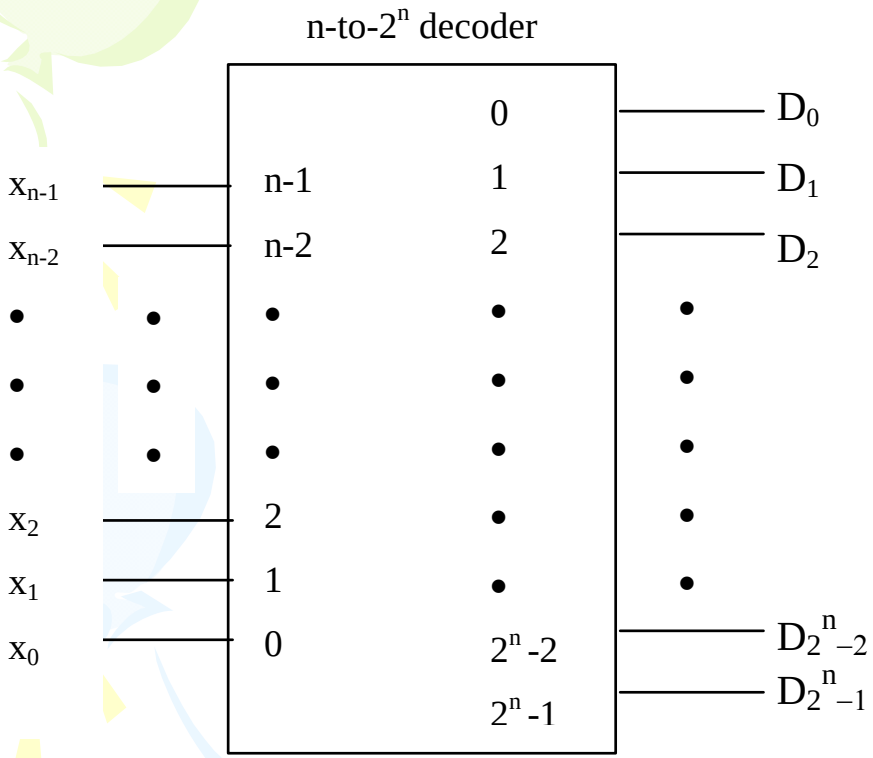


Figure 7.1 n-to-2^n decoder.

Table 7.1 Truth table for a 3-to-8 decoder.

x_2 x_1 x_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0 0 0	1	0	0	0	0	0	0	0
0 0 1	0	1	0	0	0	0	0	0
0 1 0	0	0	1	0	0	0	0	0
0 1 1	0	0	0	1	0	0	0	0
1 0 0	0	0	0	0	1	0	0	0
1 0 1	0	0	0	0	0	1	0	0
1 1 0	0	0	0	0	0	0	1	0
1 1 1	0	0	0	0	0	0	0	1

7.1.2 Decoders with Active-Low Outputs

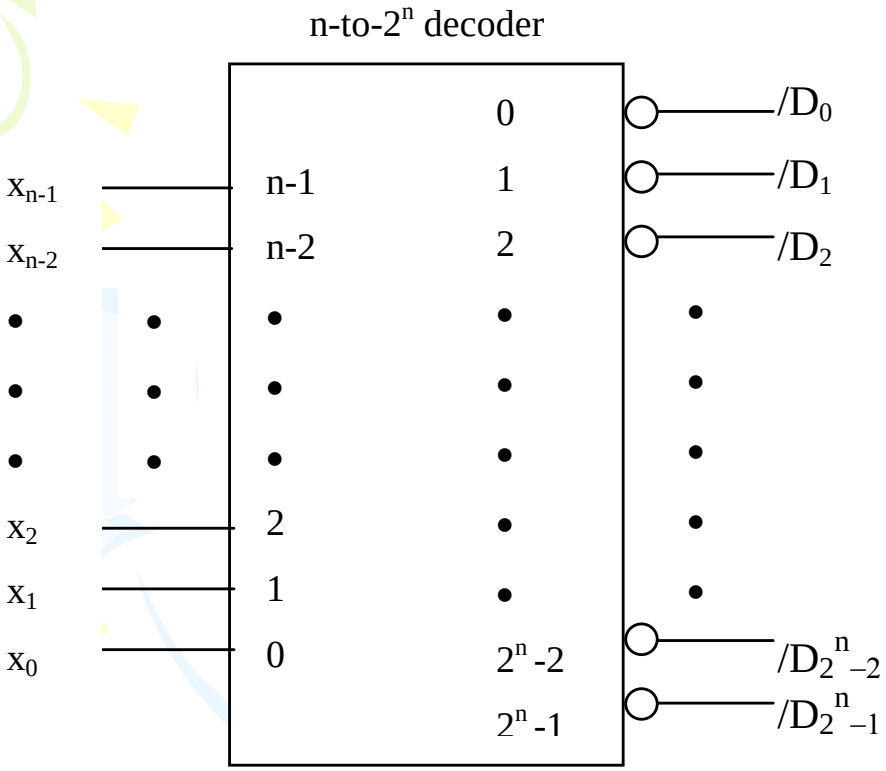


Figure 7.2 n-to-2^n decoder with active-low outputs.

Table 7.2 Truth table for a 3-to-8 decoder with active-low output.

x_2 x_1 x_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0 0 0	0	1	1	1	1	1	1	1
0 0 1	1	0	1	1	1	1	1	1
0 1 0	1	1	0	1	1	1	1	1
0 1 1	1	1	1	0	1	1	1	1
1 0 0	1	1	1	1	0	1	1	1
1 0 1	1	1	1	1	1	0	1	1
1 1 0	1	1	1	1	1	1	0	1
1 1 1	1	1	1	1	1	1	1	0

$$D_i = M_i$$

7.1.3 Decoders with Enable Control

$$D_0 = EN\ (x_1' x_0')$$
$$D_1 = EN\ (x_1' x_0)$$
$$D_2 = EN\ (x_1 x_0')$$
$$D_3 = EN\ (x_1 x_0)$$

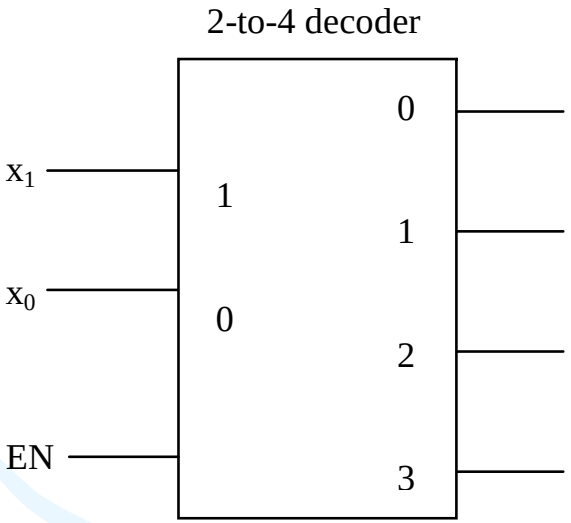


Figure 7.3 2-to-4 decoder with enable control.

Table 7.3 Truth table for Figure 7.7.

EN	x_1	x_0	D_0	D_1	D_2	D_3
0	d	d	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

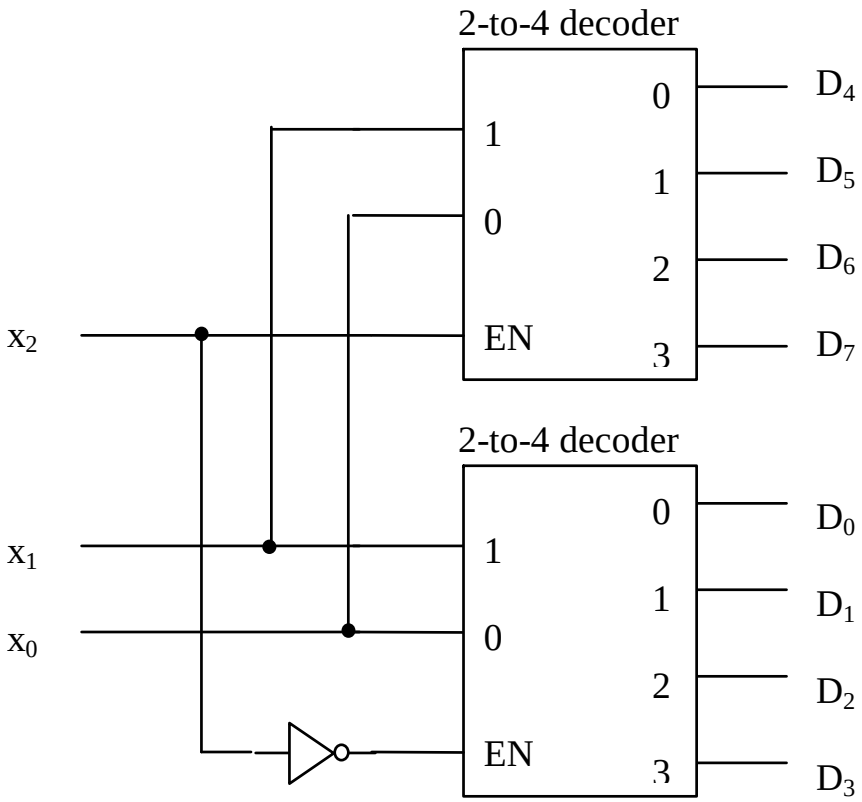


Figure 7.4 Realization of 3-to-8 decoder by 2-to-4 decoders.

(b)

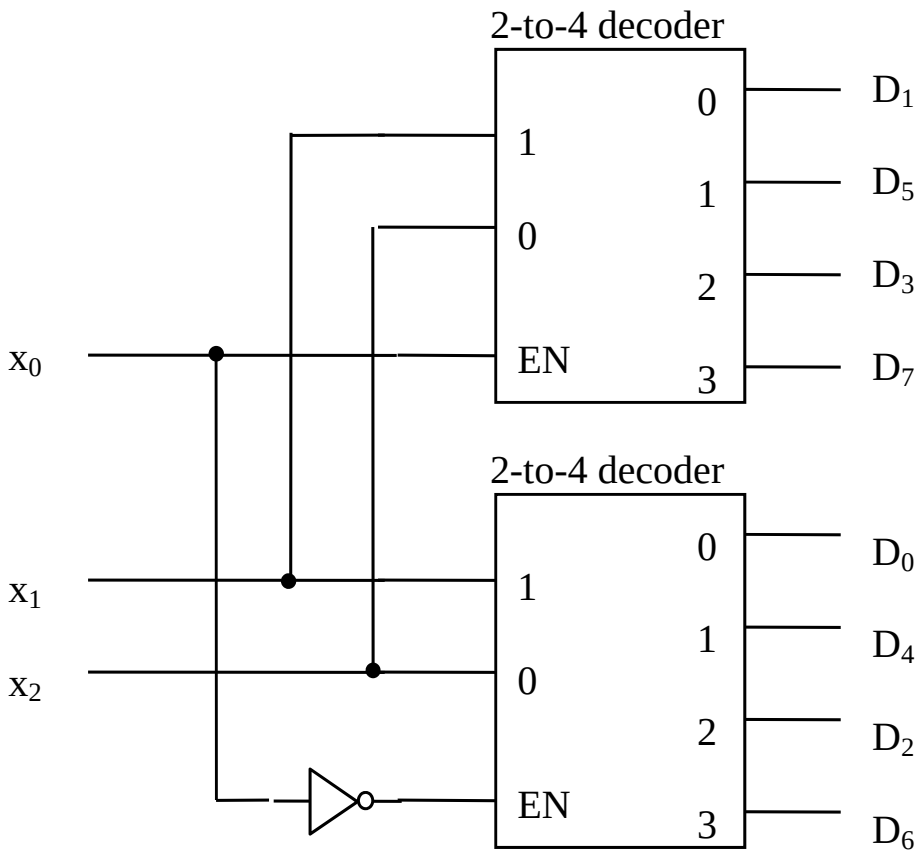
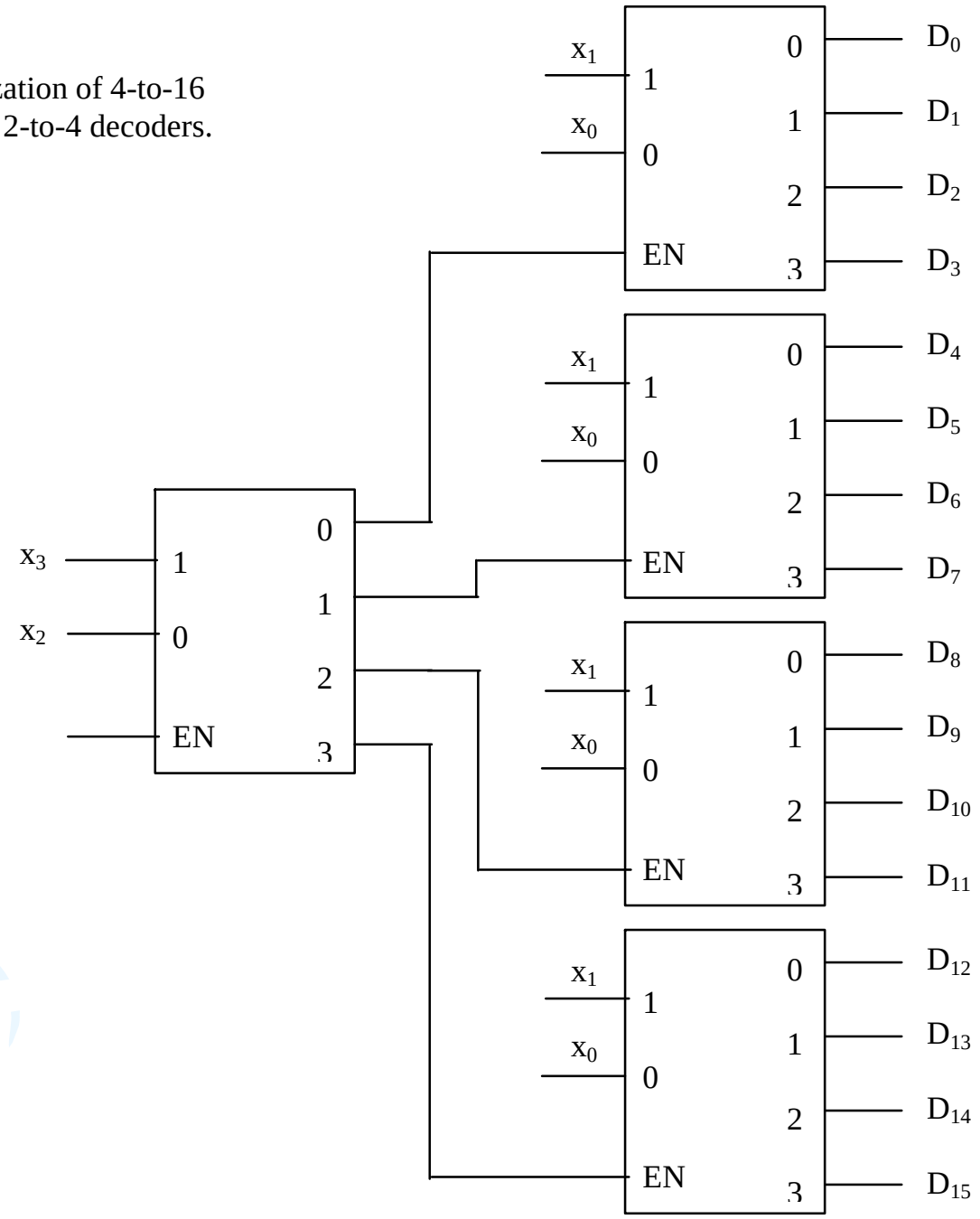


Figure 7.4 Realization of 3-to-8 decoder by 2-to-4 decoders.

Figure 7.5 Realization of 4-to-16 decoder by 2-to-4 decoders.



7.1.5 Implementation of Functions Using Decoders

$$F(A, B, C) = \Sigma\, m(0, 3, 5)$$

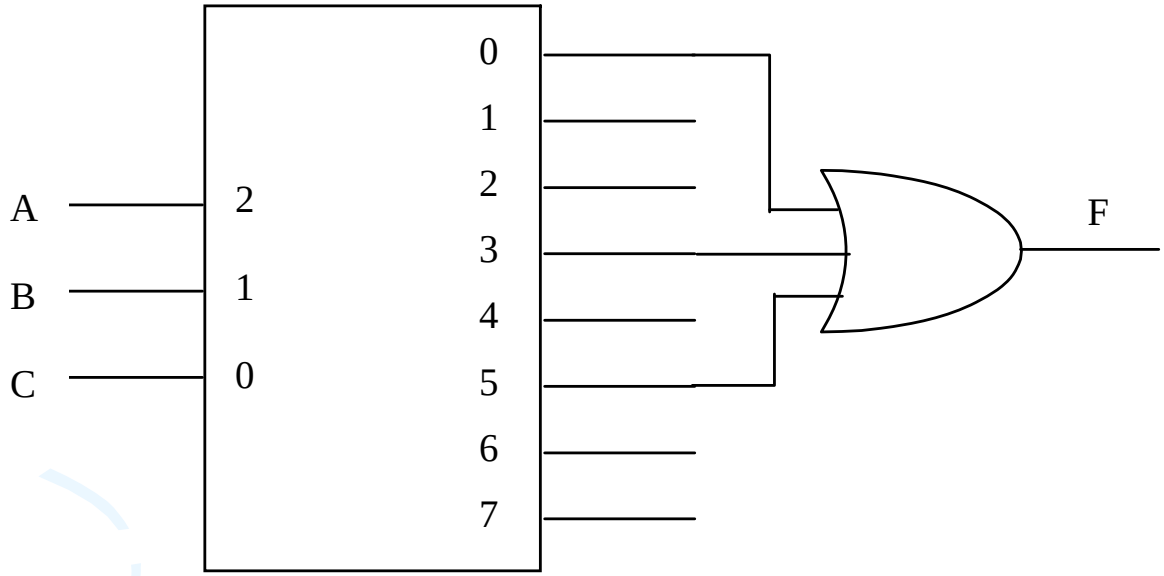


Figure 7.6 Function realization using decoder and OR gate.

$$F(A, B, C) = \Sigma\, m(0, 3, 5)$$

$$F'(A,B,C) = \pi\, M(0, 3, 5) = \Sigma\, m(1, 2, 4, 6, 7)$$

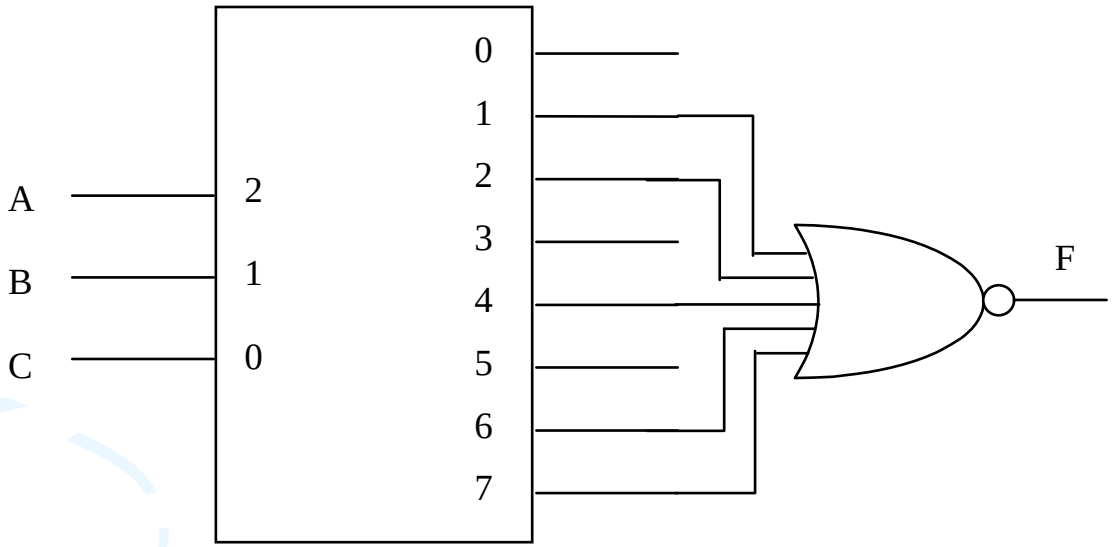


Figure 7.7 Function realization using decoder and OR gate.

$$F = \Sigma\, m(0, 3, 5) = \pi\, M(1, 2, 4, 6, 7)$$

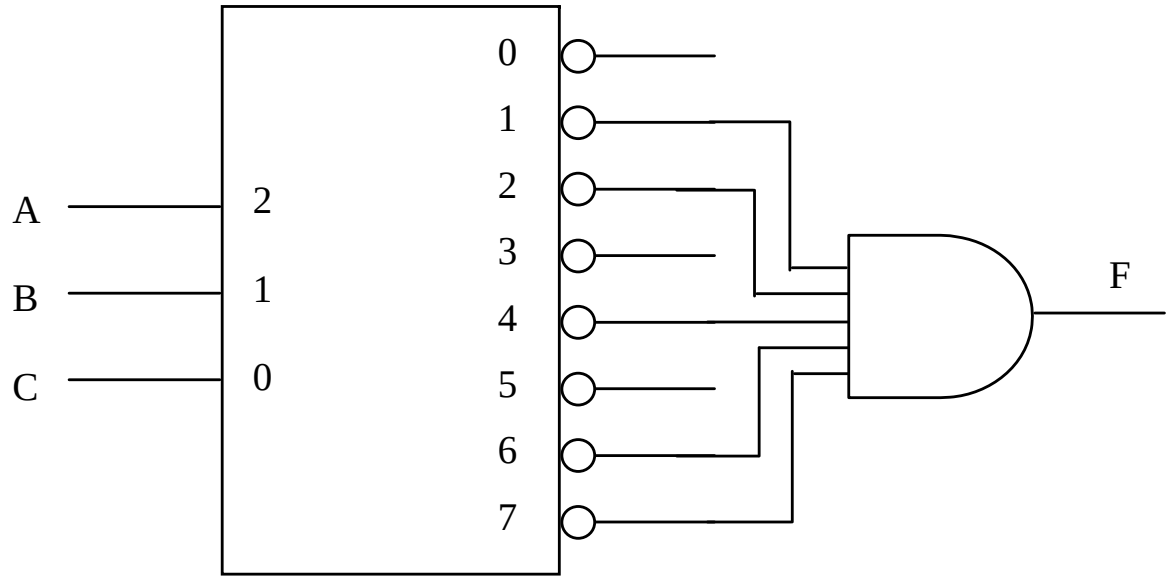


Figure 7.8 Function realization using decoder with inverted output and AND gate.

$$F = \Sigma\, m(0, 3, 5) = \pi\, M(1, 2, 4, 6, 7)$$

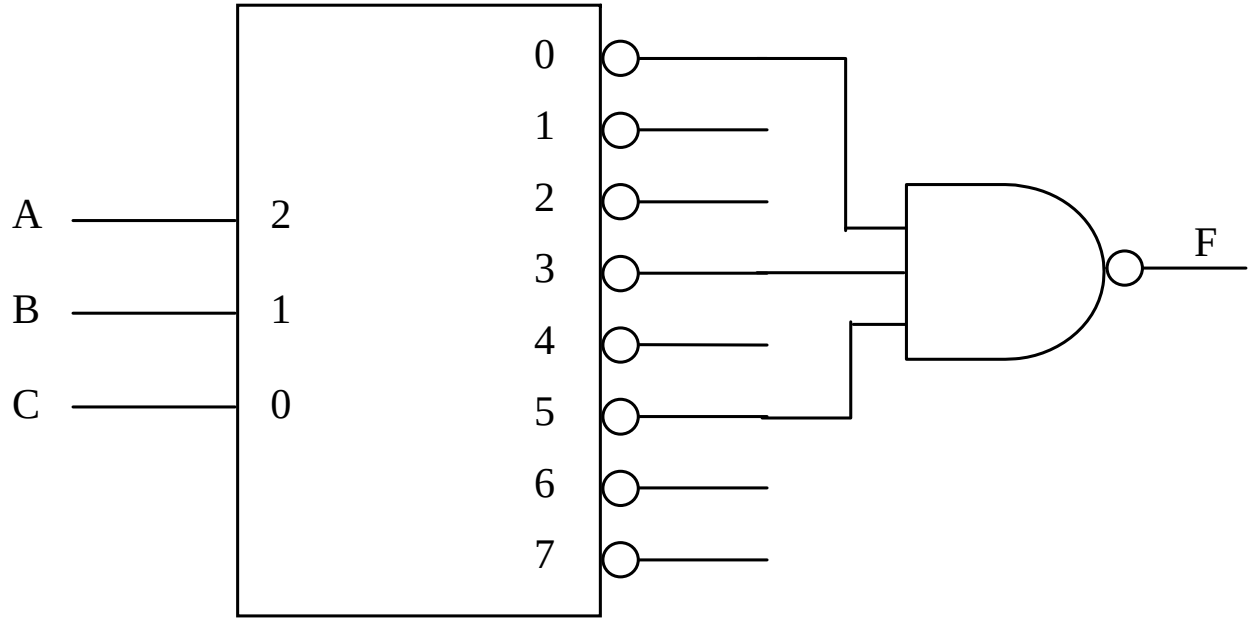


Figure 7.9 Function realization using decoder with inverted output and NAND gate.

7.2.1 Encoder Structure

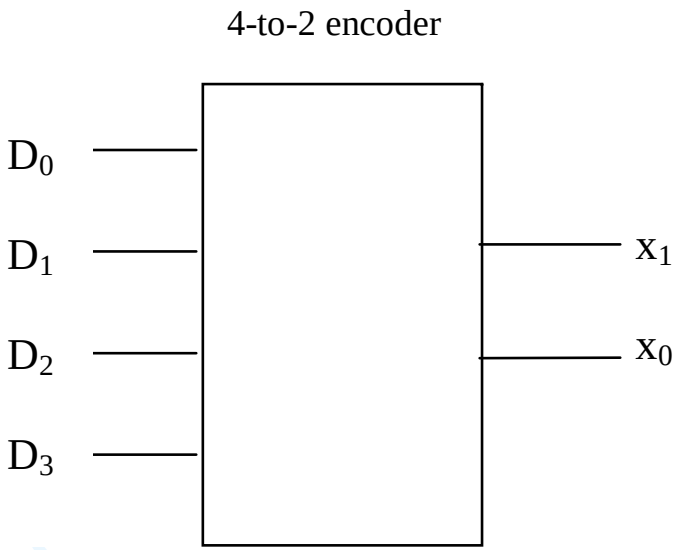


Figure 7.10 4-to-2 encoder.

Table 7.4 Truth table for a 4-to-2 encoder.

D_3	D_2	D_1	D_0	x_1	x_0
1	0	0	0	1	1
0	1	0	0	1	0
0	0	1	0	0	1
0	0	0	1	0	0

$$x_1 = \Sigma\, m(4, 8) + d(0, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15) = D_3 + D_2$$

$$x_0 = \Sigma\, m(2, 8) + d(0, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15) = D_3 + D_1$$

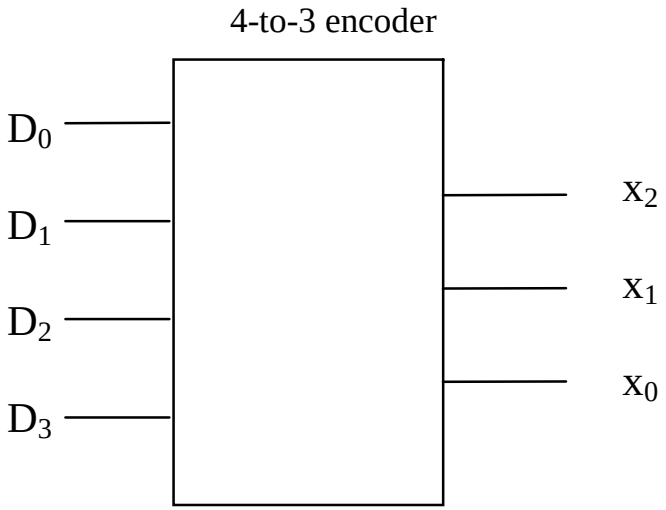


Figure 7.11 4-to-3 encoder.

Table 7.5 Truth table for a 4-to-3 encoder.

D_3 D_2 D_1 D_0	x_2 x_1 x_0
1 0 0 0	1 1 1
0 1 0 0	1 1 0
0 0 1 0	1 0 1
0 0 0 1	1 0 0
All other input states	0 0 0

$$x_2 = \Sigma\, m(1, 2, 4, 8)$$
$$= D_3'D_2'D_1'D_0 + D_3'D_2'D_1D_0' + D_3'D_2D_1'D_0' + D_3D_2'D_1'D_0'$$

$$x_1 = \Sigma\, m(4, 8) = D_3'D_2D_1'D_0' + D_3D_2'D_1'D_0'$$

$$x_0 = \Sigma\, m(2, 8) = D_3'D_2'D_1D_0' + D_3D_2'D_1'D_0'$$

7.2.2 Priority Encoders

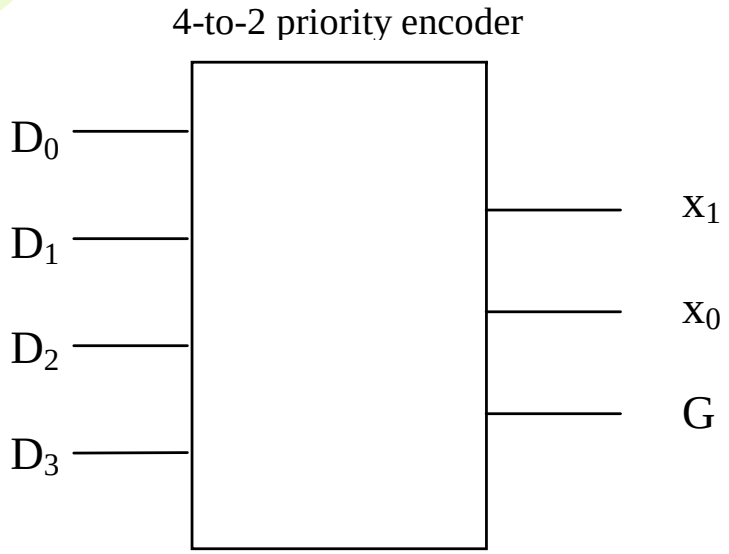


Figure 7.12 4-to-2 priority encoder.

Table 7.6 Truth table for a 4-to-2 priority encoder.

D_3	D_2	D_1	D_0	x_1	x_0	G
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	d	0	1	1
0	1	d	d	1	0	1
1	d	d	d	1	1	1

$$x_1 = \Sigma\, m(4 - 7, 8 - 15) = D_3 + D_2'$$

$$x_0 = \Sigma\, m(2, 3, 8 - 15) = D_3 + D_2'D_1$$

$$G = \Sigma\, m(1\text{-}15) = M_0 = D_3 + D_2 + D_1 + D_0$$

7.3 Multiplexers

7.3.1 Multiplexer Structure

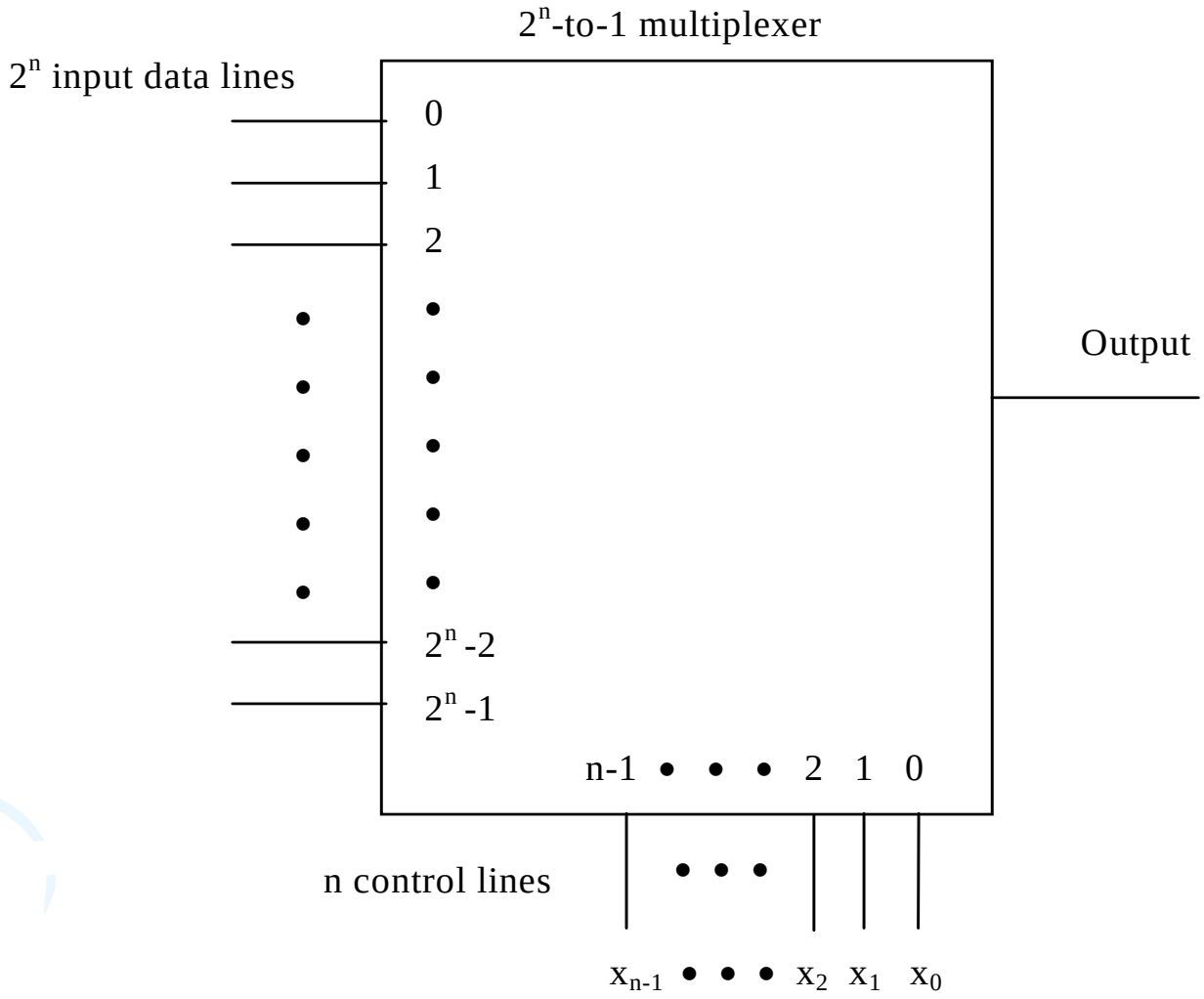


Figure 7.13 Logic diagram of a 2^n-to-1 multiplexer.

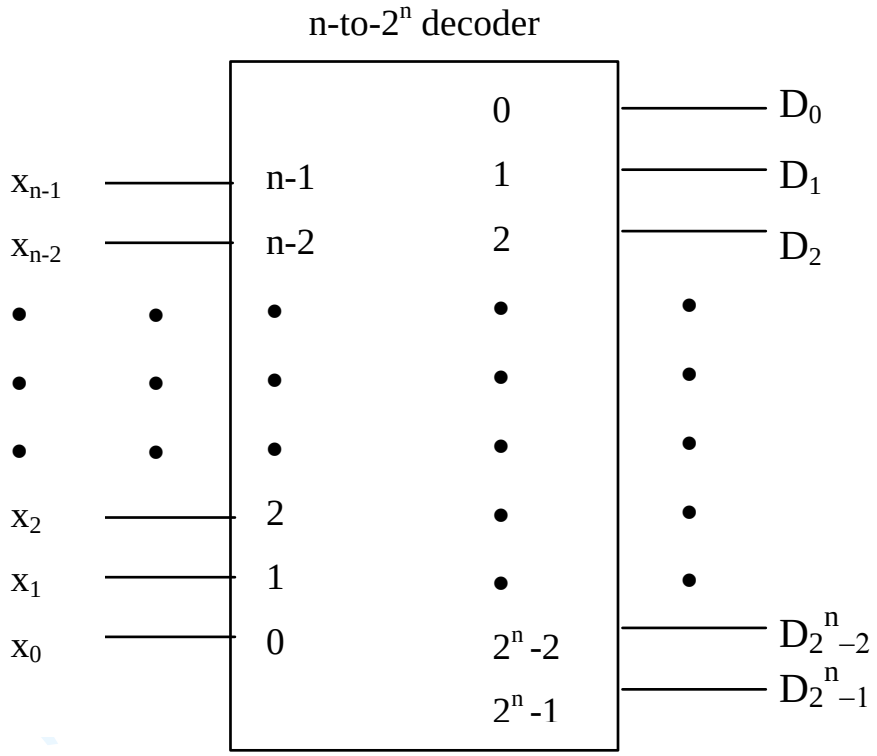
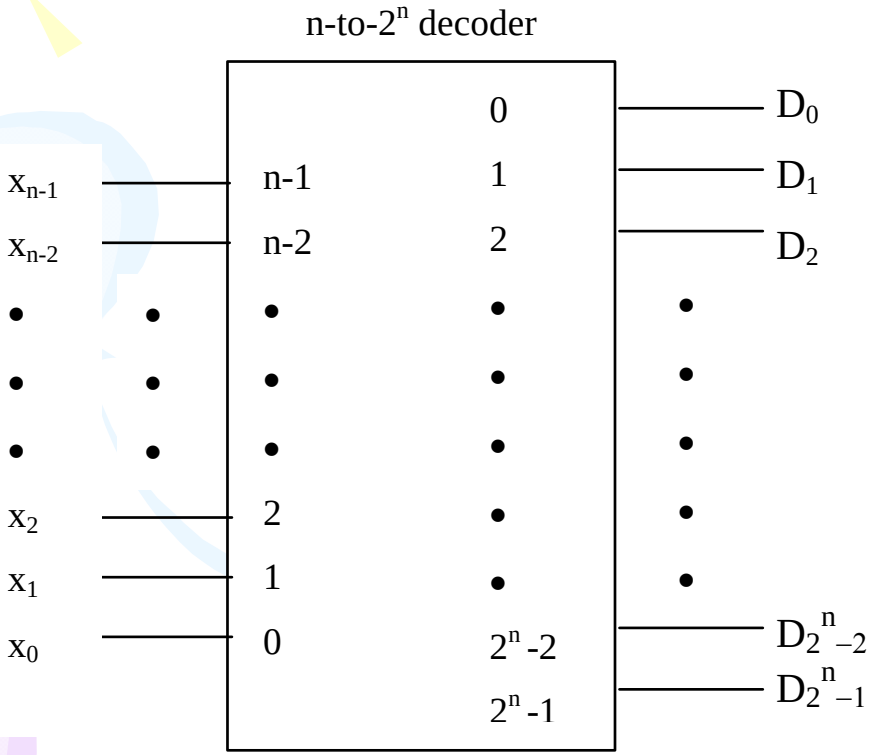


Figure 7.1 n-to-2^n decoder.



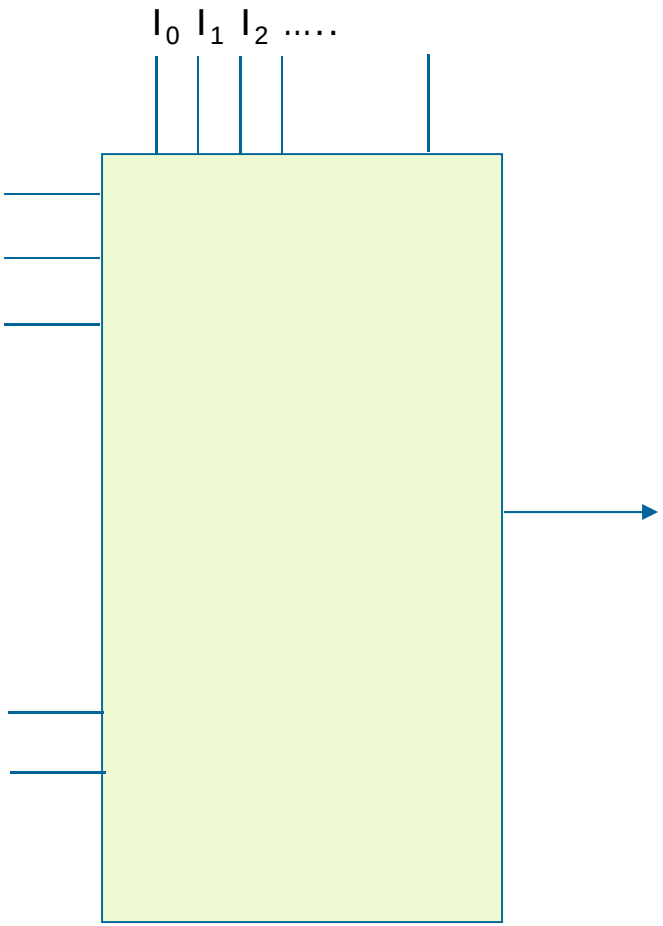
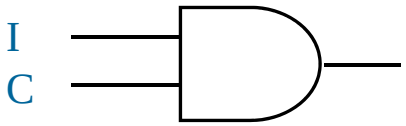
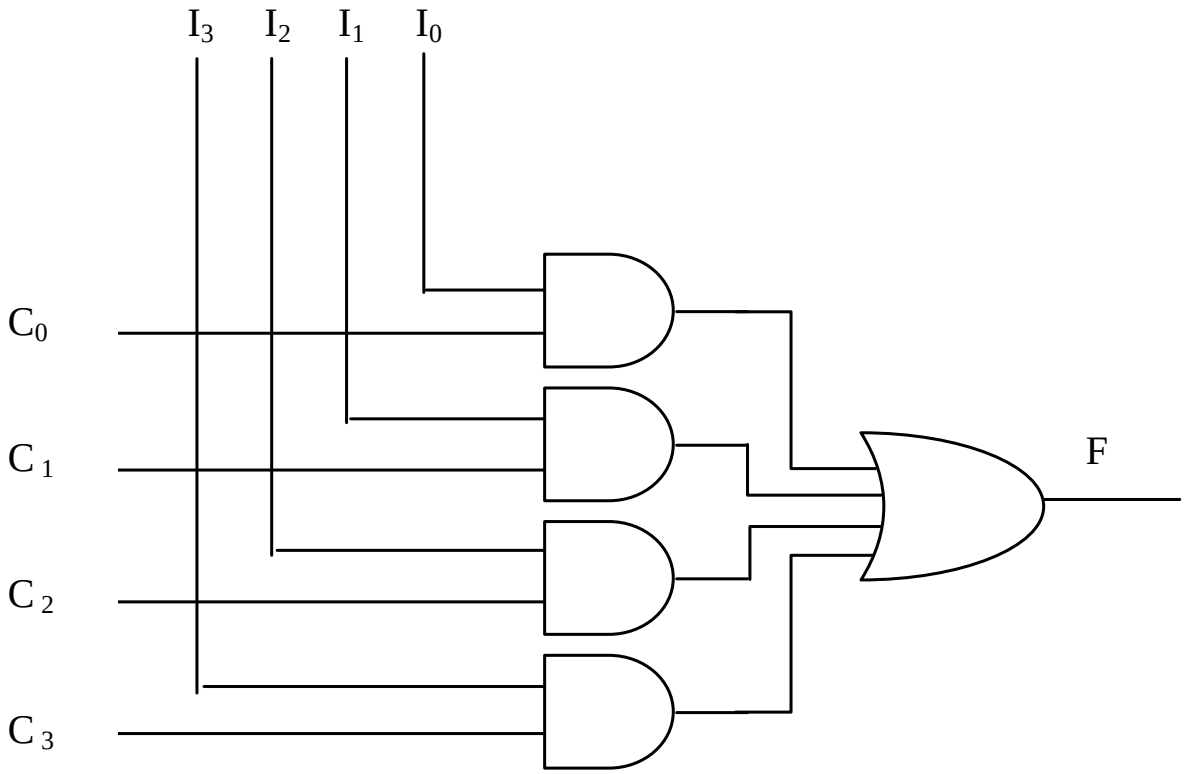


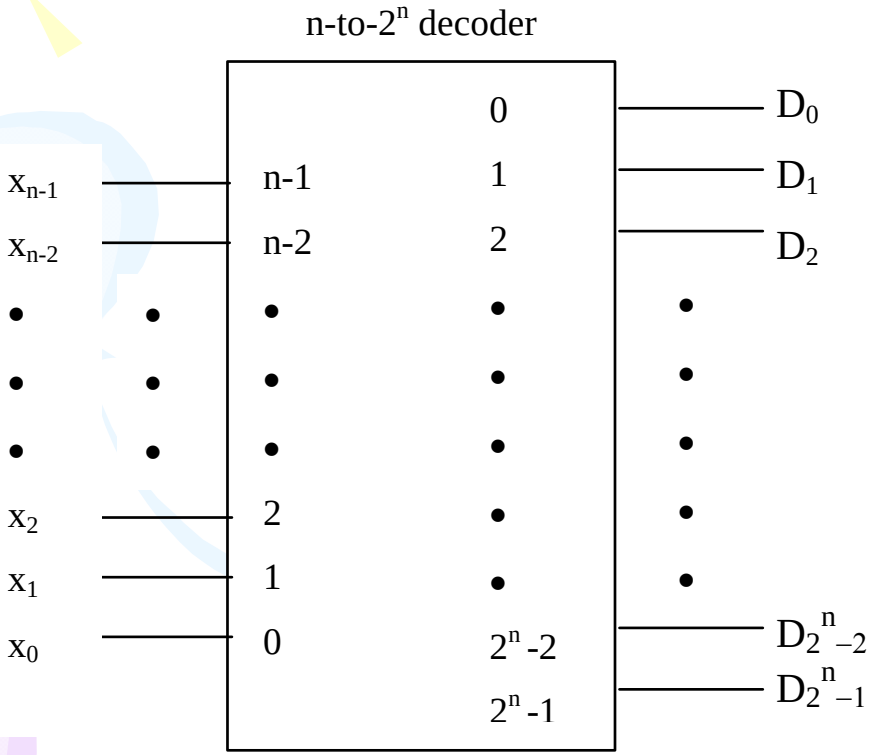
Figure 7.1 n-to-2^n decoder.



Y = 0 if C = 0

Y = I if C = 1





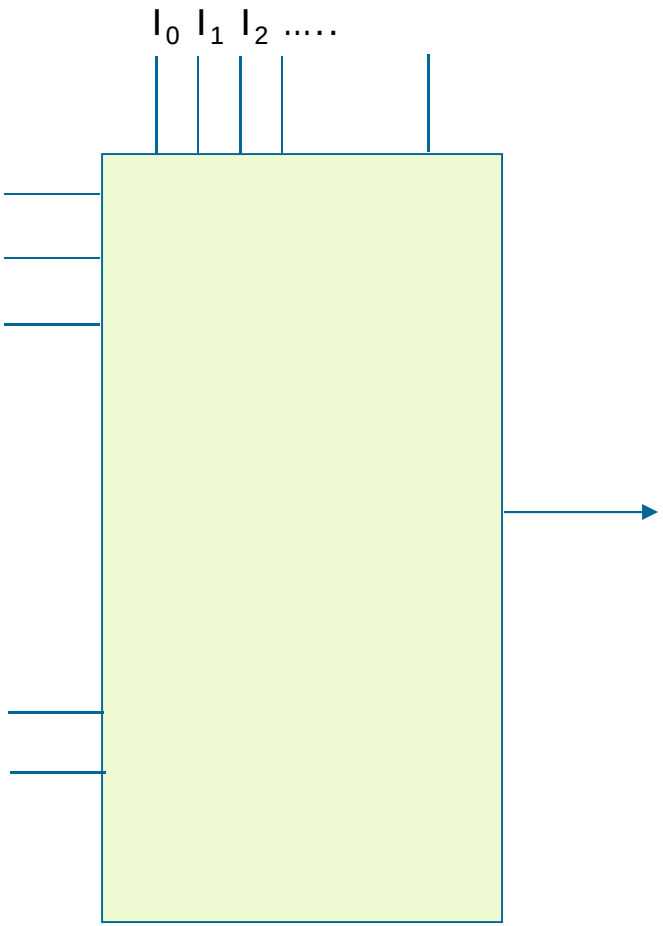


Figure 7.1 n-to-2^n decoder.

Table 7.7 Truth table for a 4-to-1 multiplexer.

A	B	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

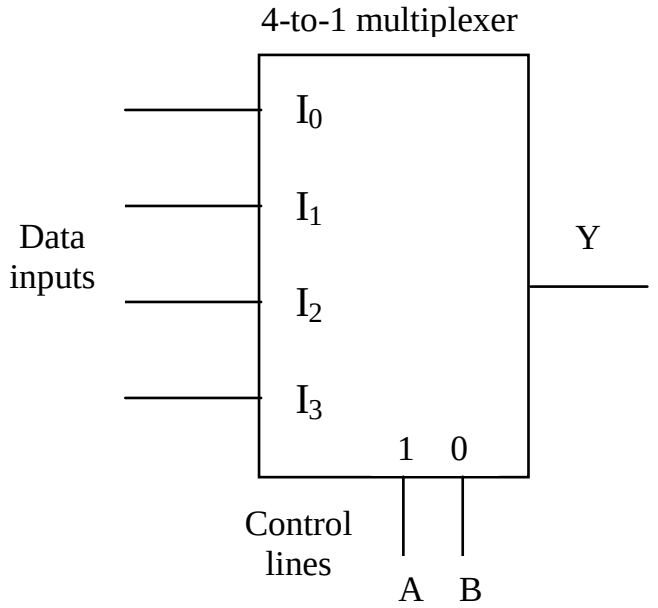


Figure 7.14 Logic diagram for a 4-to-1 multiplexer.

$$Y = A'B'I_0 + A'BI_1 + A'BI_2 + ABI_3$$

$$Y = m_0I_0 + m_1I_1 + m_2I_2 + m_3I_3 = \sum_{i=0}^{3} m_i I_i$$

The above equation can be generalized to a 2^n-to-1 multiplexer.

$$Y = \sum_{i=0}^{2^n - 1} m_i I_i$$

Table 7.7 Truth table for a 4-to-1 multiplexer.

A	B	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

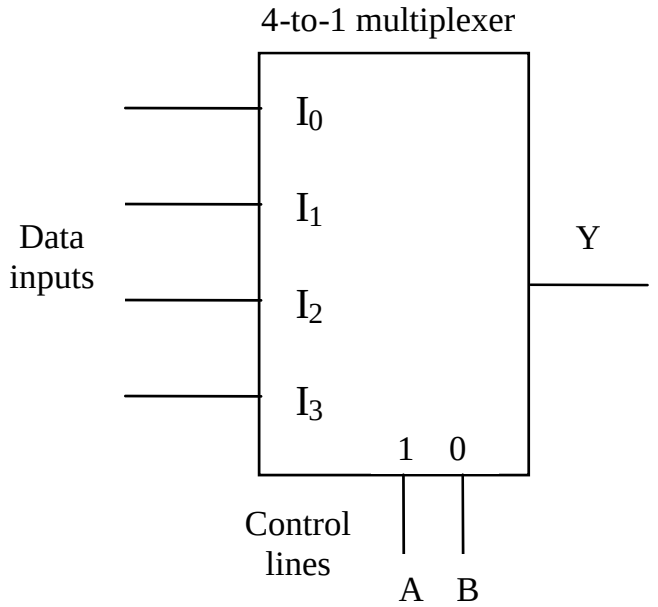


Figure 7.14 Logic diagram for a 4-to-1 multiplexer.

$$Y = A'B'I_0 + A'BI_1 + A'BI_2 + ABI_3$$

$$Y = m_0I_0 + m_1I_1 + m_2I_2 + m_3I_3 = \sum_{i=0}^{3} m_i I_i$$

The above equation can be generalized to a 2^n-to-1 multiplexer.

$$Y = \sum_{i=0}^{2^n - 1} m_i I_i$$

7.3.2 Design of Multiplexers

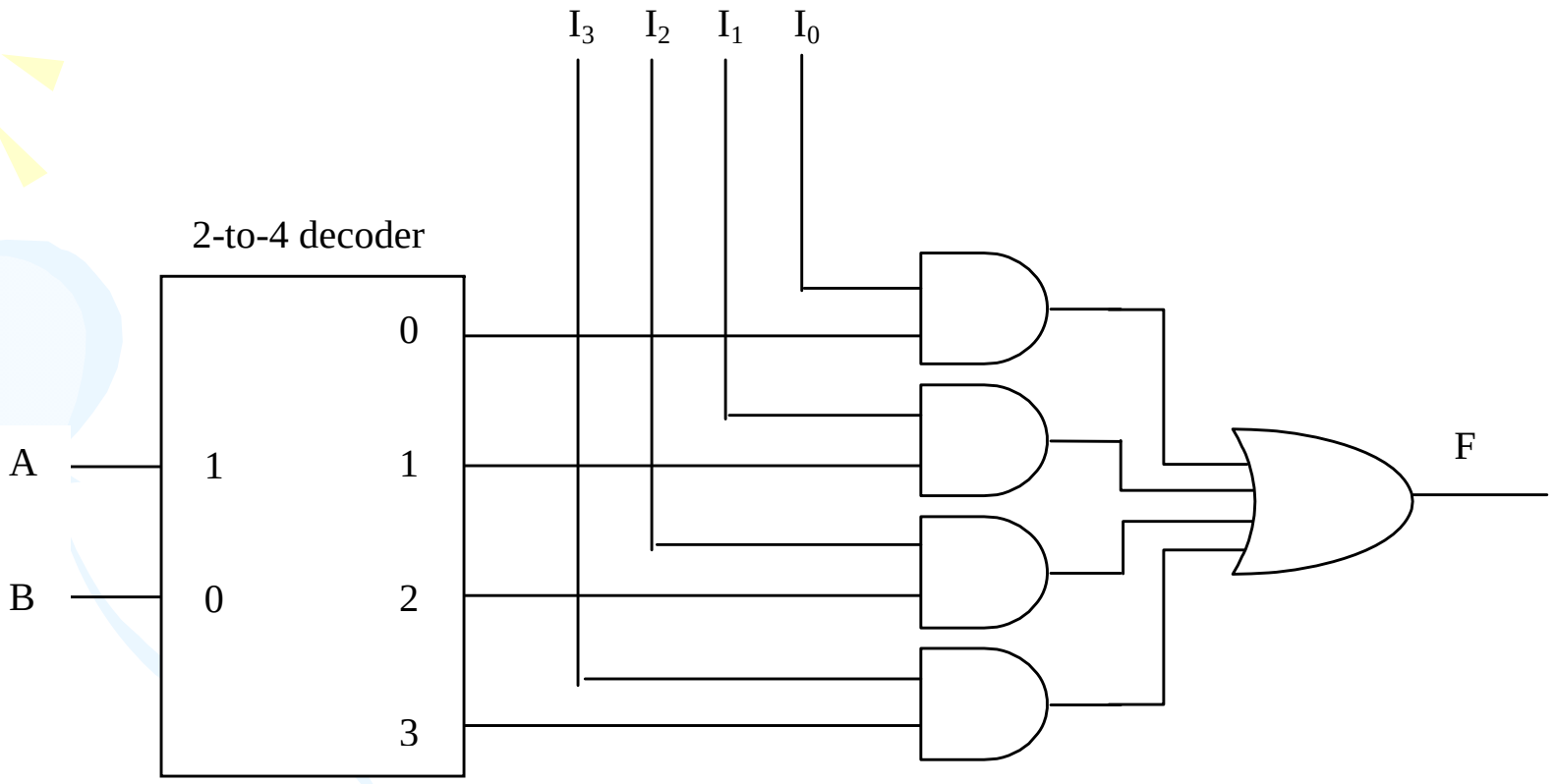
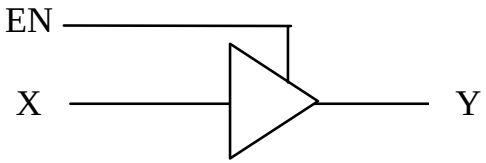


Figure 7.15 Design of a 4-to-1 multiplexer using a 2-to-4 decoder.

Figure 7.16 Logic diagram of a tri-state buffer.



EN = 1 X = Y
EN = 0 High Z

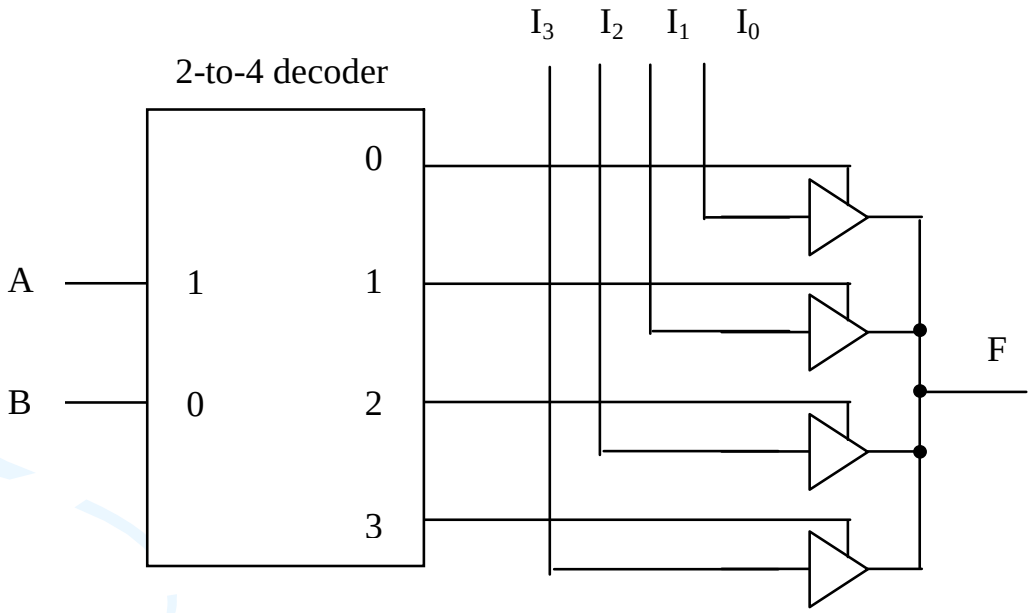


Figure 7.17 Design of a multiplxer using a decoder and four tri-state buffers.

7.3.3 Multiplexers with Enable Control

Similar to decoders, multiplexers may be enabled or disabled. When the enable signal is asserted, a multiplexer is activated. One of the data inputs is routed to the output. When the enable signal is de-asserted, a multiplexer is disabled. The output is de-asserted and has a value of 0 for active-high output, or a value of 1 for active-low output. The standard expression for a 2^n-to-1 multiplexers can be modified as follows. EN is the enable input.

$$Y = EN \left(\sum_{i=0}^{2^n - 1} m_i I_i \right)$$

For an active-low enable input /EN,

$$Y = (/EN)' \left(\sum_{i=0}^{2^n - 1} m_i I_i \right)$$

7.3.4 Expansion of Multiplexers

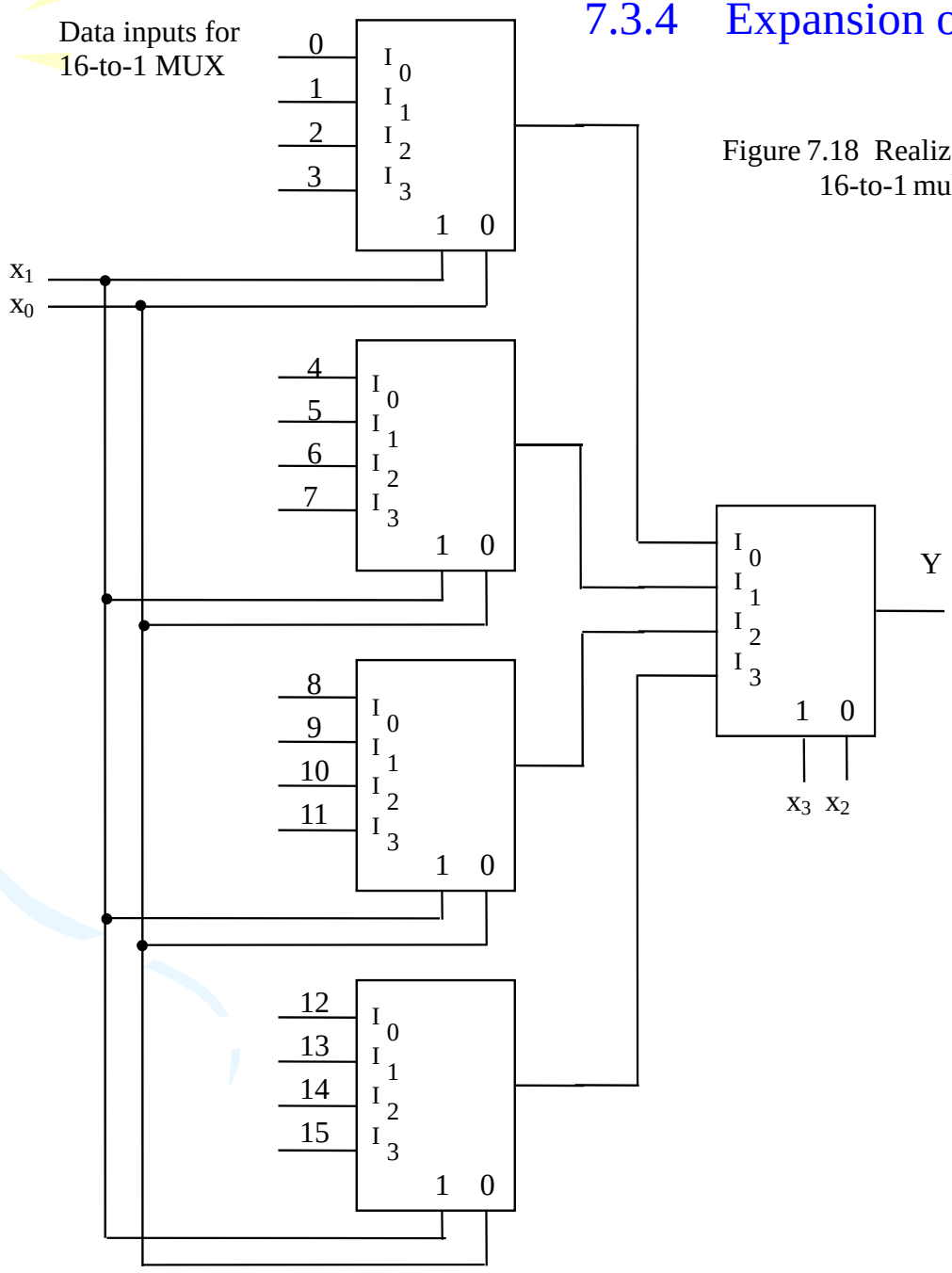


Figure 7.18 Realization of 16-to-1 multiplexer.

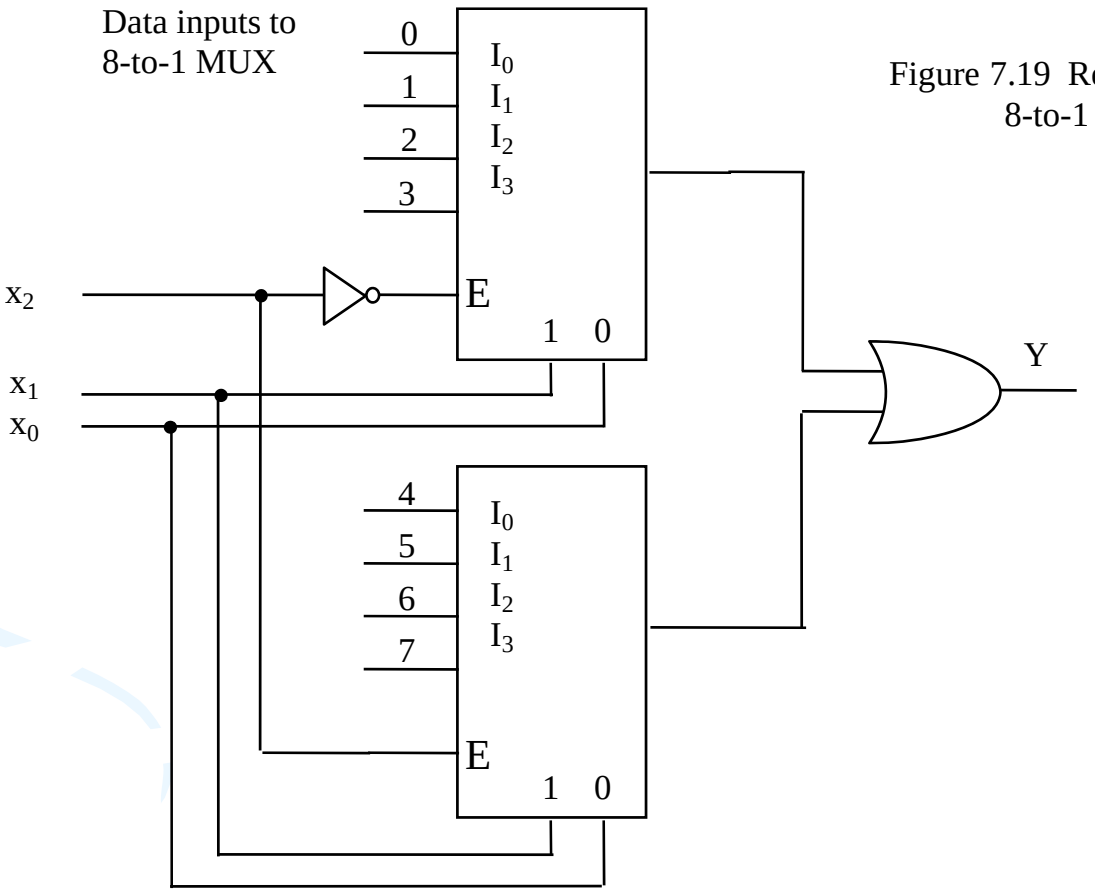


Figure 7.19 Realization of 8-to-1 multiplexer.

7.3.5 Implementation of Functions Using Multiplexers

Table 7.8 Combined table for F(A,B,C) and an 8-to-1 multiplexer.

A	B	C	Y	F(A,B,C)
0	0	0	I_0	0
0	0	1	I_1	0
0	1	0	I_2	1
0	1	1	I_3	1
1	0	0	I_4	1
1	0	1	I_5	0
1	1	0	I_6	0
1	1	1	I_7	1

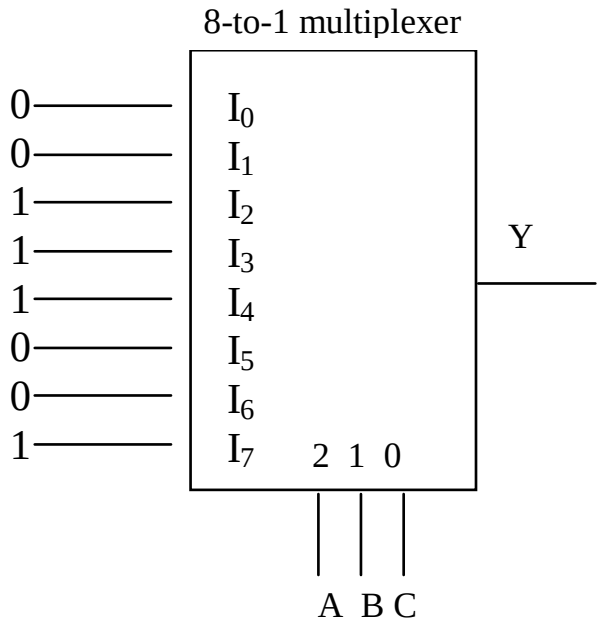
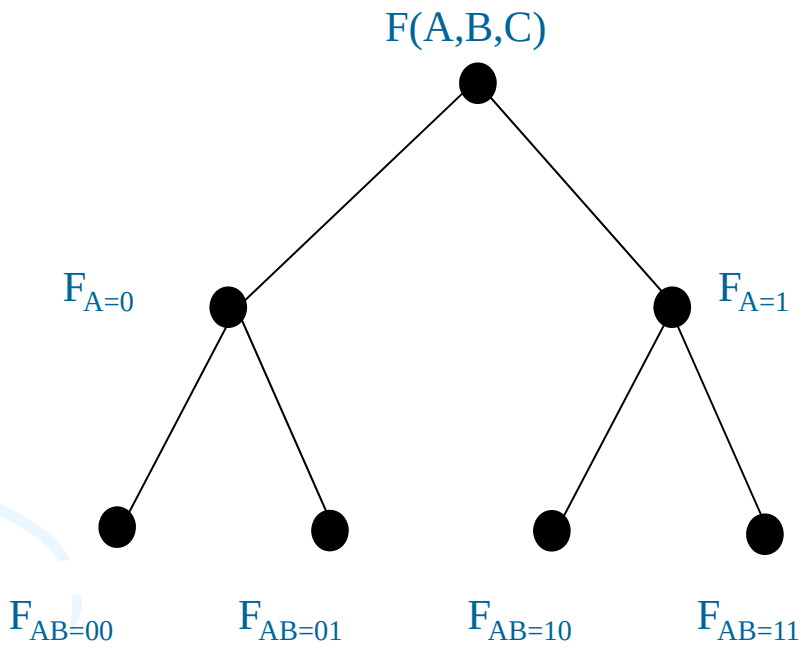


Figure 7.20 Implementation of a 3-variable function by an 8-to-1 multiplexer.

Implementation of F(A,B,C) by a 4-to-1 multiplexer

3-variable function F(A,B,C) is expanded with A and B

$$F = A'B'F_{AB=00} + A'B\,F_{AB=01} + AB'\,F_{AB=10} + AB\,F_{AB=11} \qquad (7.2)$$



Implementation of F(A,B,C) by a 4-to-1 multiplexer

4-to-1 multiplexer output $Y = A'B'(I_0) + A'B(I_1) + AB'(I_2) + AB(I_3)$ (7.1)

3-variable function F(A,B,C) is expanded with A and B

$$F = A'B'F_{AB=00} + A'B\,F_{AB=01} + AB'\,F_{AB=10} + AB\,F_{AB=11} \quad (7.2)$$

Compare Equations (7.1) and (7.2)

F = Y if $I_0 = F_{AB=00}, I_1 = F_{AB=01},$
$I_2 = F_{AB=10},$ $I_3 = F_{AB=11}$

$F(A,B,C) = \Sigma\, m(2, 3, 4, 7) = A'B + BC + AB'C'$

$I_0 = F_{AB=00} = 0$

$I_1 = F_{AB=01} = 1$

$I_2 = F_{AB=10} = C'$

$I_3 = F_{AB=11} = C$

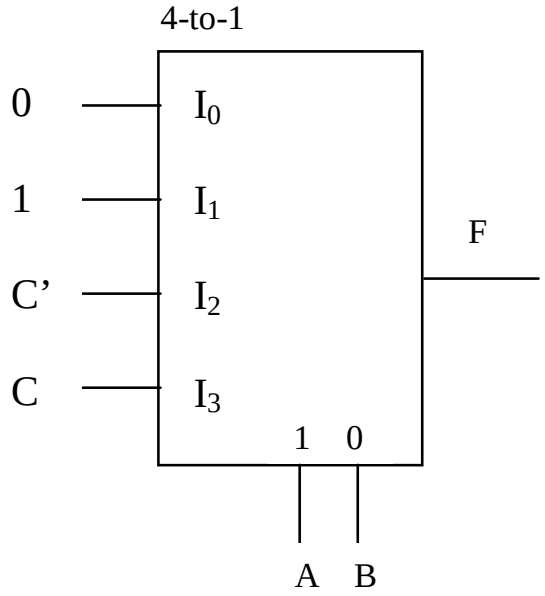


Figure 7.21 Realization of a 3-variable function by a 4-to-1 multiplexer.

❖ Example 7.1

A 4-variable function is implemented by an 8-to-1 multiplexer in this example.The minterm list form of the function is

$$F(A,B,C,D) = \Sigma\, m(0, 2, 3, 5, 7, 10, 14, 15)$$

$I_0 = B'$ $I_1 = B$ $I_2 = B'$ $I_3 = 1$

$I_4 = 0$ $I_5 = 0$ $I_6 = 1$ $I_7 = B$

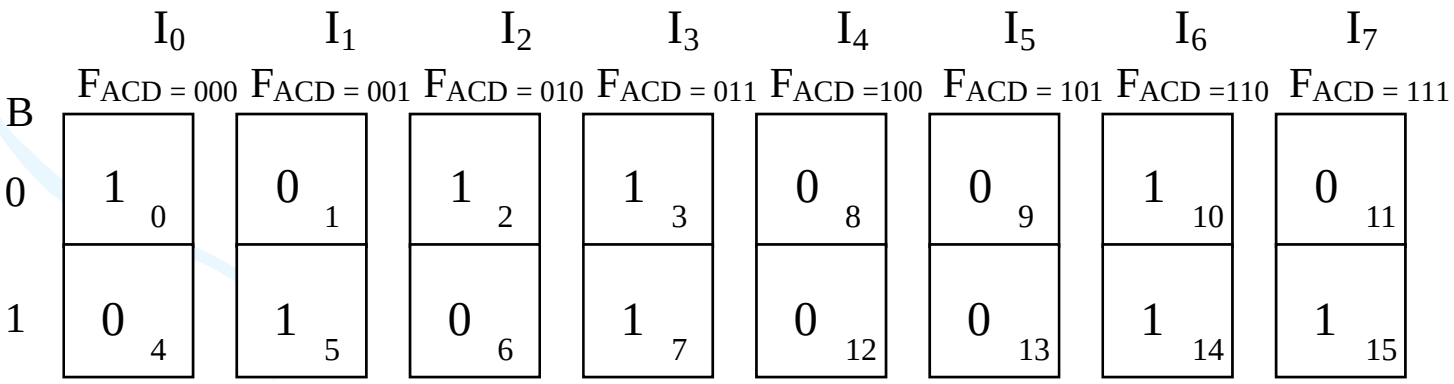


Figure 7.22 Sub-function K-maps as data inputs in the implementation of a 4-variable function by an 8-to-1 multiplexer.

Example 7.2

Implementation of a 4-variable function F using a 4-to-1 multiplexer.

$F(A, B, C, D) = \Sigma\, m(0, 1, 3, 5, 8, 11, 14, 15) + d(9, 10, 13)$

Control inputs A, B

$I_0 = C' + D$ $I_1 = C'D$

$I_2 = 1$ $I_3 = C$

Control inputs C, D

$I_0 = B'$ $I_1 = 1$

$I_2 = A$ $I_3 = A + B'$

CD	I_0 $F_{AB=00}$	I_1 $F_{AB=01}$	I_3 $F_{AB=11}$	I_2 $F_{AB=10}$
00	1 0	0 4	0 12	1 8
01	1 1	1 5	d 13	d 9
11	1 3	0 7	1 15	1 11
10	0 2	0 6	1 14	d 10

		AB 00	01	11	10
I_0	$F_{CD=00}$	1 0	0 4	0 12	1 8
I_1	$F_{CD=01}$	1 1	1 5	d 13	d 9
I_3	$F_{CD=11}$	1 3	0 7	1 15	1 11
I_2	$F_{CD=10}$	0 2	0 6	1 14	d 10

Figure 7.23 Sub-function K-maps as data inputs in the implementation of a 4-variable function by a 4-to-1 multiplexer.

Control inputs B, C

$I_0 = 1$ $I_1 = D$

$I_2 = D$ $I_3 = A$

Control inputs A, D

$I_0 = B'C'$ $I_1 = B' + C'$

$I_2 = B' + C$ $I_3 = 1$

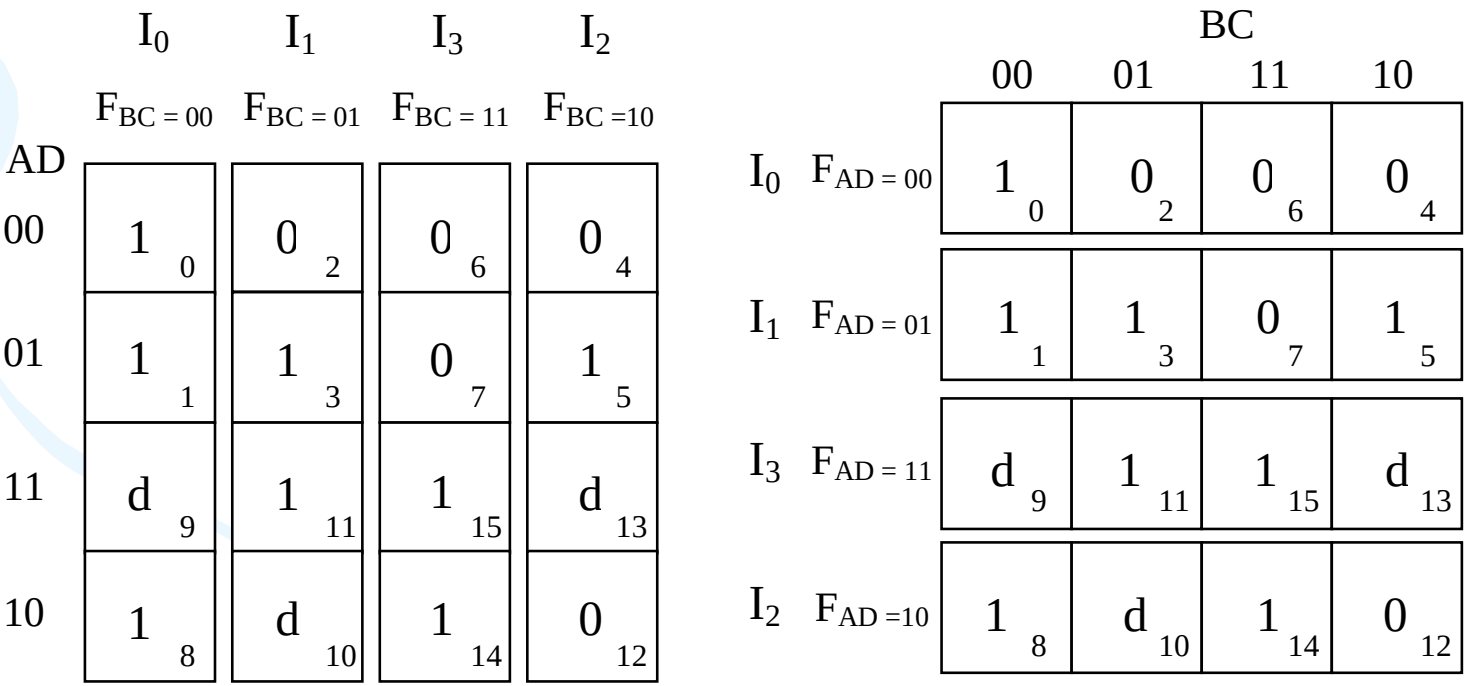


Figure 7.23 Sub-function K-maps as data inputs in the implementation of a 4-variable function by a 4-to-1 multiplexer.

Control inputs A, C

$I_0 = B' + D$ $I_1 = B'D$

$I_2 = B'$ $I_3 = 1$

Control inputs B, D

$I_0 = C'$ $I_1 = 1$

$I_2 = AC$ $I_3 = A + C'$

BD	I_0 $F_{AC=00}$	I_1 $F_{AC=01}$	I_3 $F_{AC=11}$	I_2 $F_{AC=10}$
00	1 0	0 2	d 10	1 8
01	1 1	1 3	1 11	d 9
11	1 5	0 7	1 15	d 13
10	0 4	0 6	1 14	0 12

		AC 00	01	11	10
I_0	$F_{BD=00}$	1 0	0 2	d 10	1 8
I_1	$F_{BD=01}$	1 1	1 3	1 11	d 9
I_3	$F_{BD=11}$	1 5	0 7	1 15	d 13
I_2	$F_{BD=10}$	0 4	0 6	1 14	0 12

Figure 7.23 Sub-function K-maps as data inputs in the implementation of a 4-variable function by a 4-to-1 multiplexer.

Control inputs A, B	$I_0 = C' + D$	$I_1 = C'D$
	$I_2 = 1$	$I_3 = C$
Control inputs C, D	$I_0 = B'$	$I_1 = 1$
	$I_2 = A$	$I_3 = A + B'$
Control inputs B, C	$I_0 = 1$	$I_1 = D$
	$I_2 = D$	$I_3 = A$
Control inputs A, D	$I_0 = B'C'$	$I_1 = B' + C'$
	$I_2 = B' + C$	$I_3 = 1$
Control inputs A, C	$I_0 = B' + D$	$I_1 = B'D$
	$I_2 = B'$	$I_3 = 1$
Control inputs B, D	$I_0 = C'$	$I_1 = 1$
	$I_2 = AC$	$I_3 = A + C'$

7.4 Demultiplexer

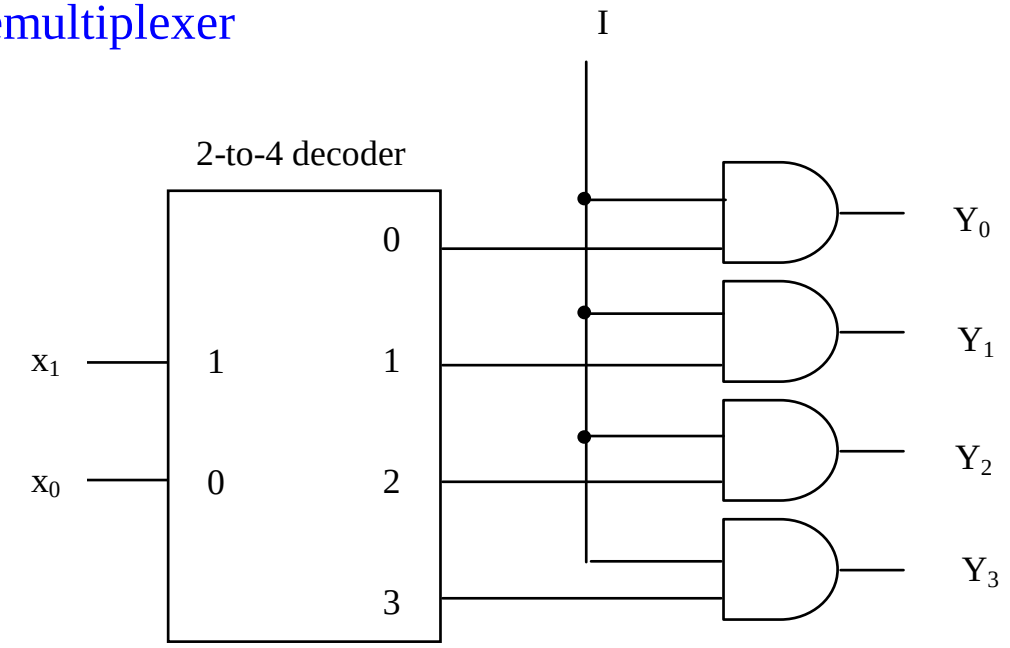


Figure 7.24 Example of a de-multiplexer.

2-to-4 decoder with enable EN (Section 7.1.4)	Demultiplexer
$D_0 = EN\ (x_1' x_0')$	$Y_0 = I\ (x_1' x_0')$
$D_1 = EN\ (x_1' x_0)$	$Y_1 = I\ (x_1' x_0)$
$D_2 = EN\ (x_1 x_0')$	$Y_2 = I\ (x_1 x_0')$
$D_3 = EN\ (x_1 x_0)$	$Y_3 = I\ (x_1 x_0)$

EN input of decoder as data input for demultiplexer

Demultiplexer with Enable

$Y_0 = I \bullet EN \bullet (x_1' x_0')$

$Y_1 = I \bullet EN \bullet (x_1' x_0)$

$Y_2 = I \bullet EN \bullet (x_1 x_0')$

$Y_3 = I \bullet EN \bullet (x_1 x_0)$

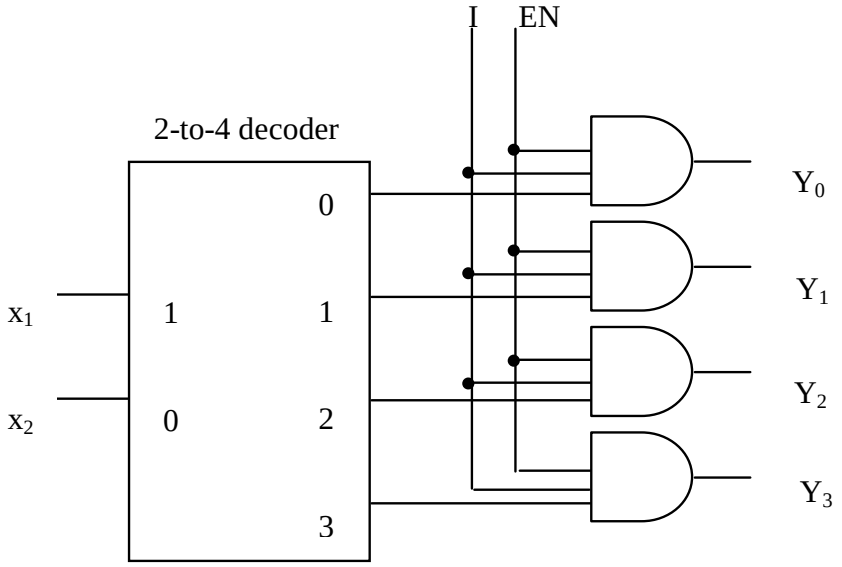


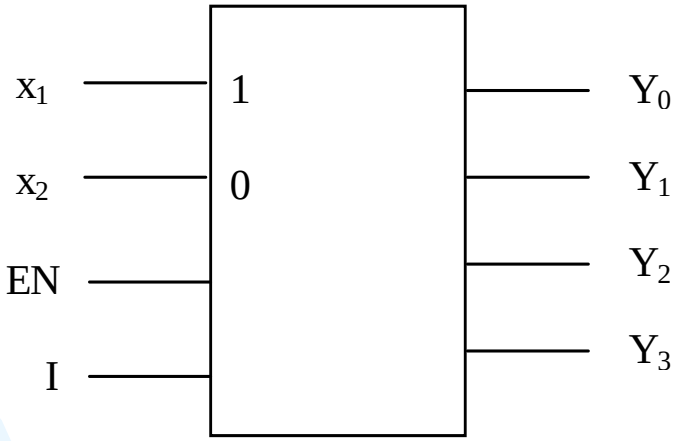
Figure 7.25 A de-multiplexer with enable input.

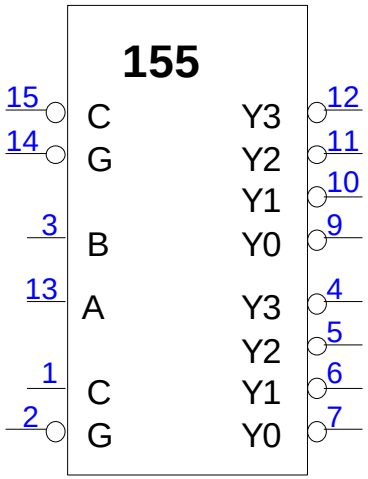
Demultiplexer with Enable

Data input: I
Control signals: x_1, x_2
Enable (Strobe): EN
Outputs: Y_0, Y_1, Y_2, Y_3

Decoder with Enable

Inputs: x_1, x_2
Enable (strobe): EN, I
Outputs: Y_0, Y_1, Y_2, Y_3





74155 Dual 2-to-4 Decoders/Demultiplexers

EN (active-high) → G (active-low)

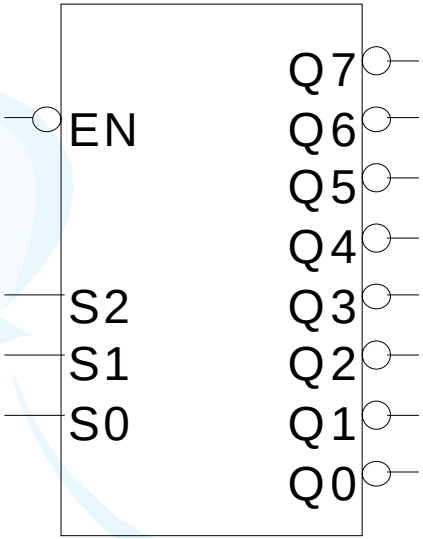
I (active-high) → C (active-low in 1), C (active-high in 2)

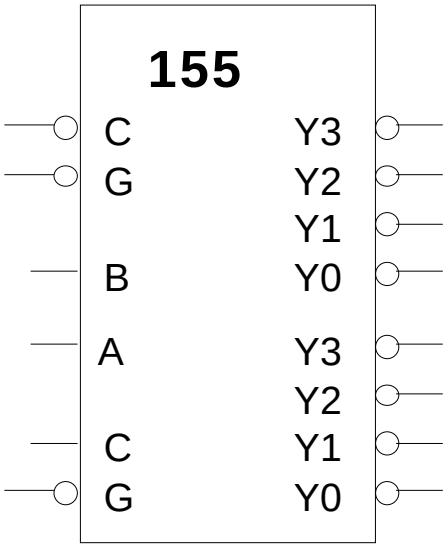
x_1, x_2 → B, A respectively

Active-high outputs → Active-low outputs

Conversion of 74155 to 3-to-8 Decoder

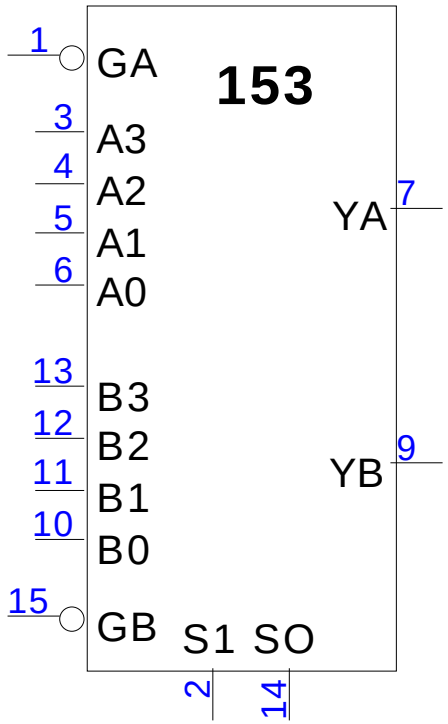
3-to-8 decoder





74153 Dual 4-to-1 Multiplexer

Active-low strobe G. Active-high output.



Conversion of 74153 to 8-to-1 Multiplexer