Cache: located between CPU registers and main memory

Base register: A register that holds the beginning physical address of the current partition

Limit register: specifies the size of the range

Base AND limit registers: Define logical address space usable by a process

Compiled code addresses: Bind to relocatable addresses. Binding combines physical and logical addresses

The binding can happen at 3 stages: 1. Compile time 2. Load time 3. Execution time

Compile time: If memory location known prior, absolute code can be generated; must recompile code if starting location changes

Load time: Must generate relocatable code if memory location is not known at compile time

Execution time: Binding delayed until run time if the process can be moved during its execution from one memory segment to another

Memory Management Unit: Device that maps virtual to physical addresses

Logical address: Generated by CPU, also referred to as virtual address

Physical address: address seen by memory unit

Simple scheme: Uses a relocation register which just adds a base value to addresses

Swapping: Allows total physical memory space of processes to exceed physical memory

Swapping: The process of moving data from one running application out of RAM and into virtual memory

Def^n: Process swapped out temporarily to backing store then brought back in for continued execution

Backing store: Fast disk large enough to accommodate copes of all memory images

Roll out, roll in: swapping variant for priority-based scheduling. Lower priority process swapped out so that higher priority process can be loaded

Memory allocation: Limited resource, must allocate efficiently

Contiguous allocation: Fixed partition and Variable partition

Fixed Partition: Memory is pre-partitioned; the OS must assign each process to the best free partition

Variable partition: -Degree of multiprogramming limited by number of partitions -Variable-partition sizes for efficiency (sized to a given process' needs)

Hole: Block of available memory; holes of various sizes are scattered throughout memory

Solutions to dynamic storage a: First fit, best fit, worst fit

First fit: Allocate the first hole that is big enough

Best fit: Allocate the smallest hole that is big enough (must search entire list) -> smallest leftover hole

Worst fit: Allocate the largest hole (search list) -> largest leftover hole

Segmentation: Noncontiguous allocation. Memory management scheme that supports user view of memory, where the memory is divided into variable sized chunks which can be allocated to processes

Logical address consists: two tuples <segment number, offset>

Segment table: maps 2D physical addresses. Each table entry has base and limit

Segment table base register: points to the segment table's location in memory

Stall: CPU does not have the data required to complete the instruction that it is executing

Input Queue: The processes on the disk that are waiting to be brought into memory for execution

Absolute Code: Code which runs at a specific place in memory. Generated by compile time address binding

Relocatable Code: Is code which can be moved (by the OS) from one area of memory to another

Memory Address Register (MAR): Holds the address in memory of the instruction at present being executed

Virtual Address: An address that corresponds to a location in virtual space and is translated by address mapping to a physical address when memory is accessed

Logical Address Space: Set of all logical addresses generated by a program

Physical Address Space: Set of all physical addresses generated by a program

Relocation Register: A register that contains the value that must be added to each address referenced in the program so that the Memory Manager will be able to access the correct memory addresses

Dynamic Loading: Routine is not loaded until it is called

Dynamically Linked Libraries: Library routines that are linked to a program during execution

Static Linking: A linking process in which library calls and other functions can't be changed after they're inserted into executable code

Shared Libraries: Other programs linked before the new library was installed will continue using the older library

Backing Store: Secondary storage device that is used as a swapping device to hold processes to be swapped into and out of memory

Ready Queue: Set of all processes residing in main memory, ready and waiting to execute

Double Buffering: Two areas of memory set aside for data transfer between the processor and peripherals. As one is emptied the other is filled up in order to speed up transfer

Application State: Is used to store data that is used throughout an application.

Contiguous Memory Allocation: Each process is contained in a single section of memory that is contiguous to the section containing the next process

Multiple-Partition Method: When a partition is free, a process is selected from the input queue and is loaded into the free partition

Variable-Partition Scheme: The operating system keeps a table indicating which parts of memory are available and which are occupied

Dynamic Storage-Allocation Problem: Concerns how to satisfy a request of size n from a list of free holes

External Fragmentation: Total memory space exists to satisfy a request, but it is not contiguous

50-percent Rule: You cannot recover if you are 50 percent or more at fault

Internal Fragmentation: Allocated memory may be slightly larger than requested memory; this size difference is memory internal to a partition, but not being used

Compaction: The goal is to shuffle the memory contents so as to place all free memory together in one large block

Segment Base: Contains starting physical address where the segment resides in memory

Segment Limit: Specifies the length of the segment

Paging: The process of swapping data or instructions that have been placed in the swap file for later use back into active random access memory (RAM). The contents of the hard drive's swap file then become less active data or instructions

Page Number (p): Used as an index into a page table which contains base address of each page in physical memory

Page Offset (d): Offset to a page base address used to determine a physical memory address

Page Table: Contains the base address of each page in physical memory

Registers: Small, high-speed storage locations that temporarily hold data and instructions

Page-Table Base Register (PTBR): Pointer to page tables stored in main memory

Translation Look-Aside Buffer: A small but fast-lookup hardware cache which stores page and frame numbers for memory access

Wired Down: Cannot be removed from TLB

Address-Space Identifiers (ASIDs): Uniquely identifies each process to provide address-space protection for that process

Hit Ratio: The percentage of times that the page number of interest is found in the TLB

Effective Memory-Access Time: Average time required to access memory based on the TLB Hit Ratio

Valid-Invalid Bit: This bit is inside the page table to notify if it is in memory or not. V == in memory i == not in memory

Page-Table Length Register (PTLR): Register indicating the size of the page table

Reentrant Code: Code that can be used by two or more processes at the same time; each shares the same copy of the executable code but has separate data areas; pure code

Hierarchical Paging: Paging system where the page table is itself paged to prevent the need to allocate a contiguous block to a large table

Forward-Mapped Paging: Hierarchical paging, starting from the outer page table inward

Hashed-Page Table: Hash value is virtual page number, linked list of elements

Clustered Page Tables: Similar to hashed page tables except that each entry in the hash table refers to several pages (such as 16) rather than a single page

Sparse (address space): A virtual address space which includes holes

Inverted Page Table: Page table that is indexed by frame rather than by page

Local Descriptor Table (LDT): Information about the first partition is kept here

Global Descriptor Table (GDT): Information about the second partition is kept here

Page Address Extension (PAE): Allows 32-bit processors to access a physical address space larger than 4 GB