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**Vérification d'une méthodologie pour la conception de systèmes
numériques critiques**

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Le Date de la soutenance

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The acknowledgments and the people to thank go here, don't forget to include your project advisor...

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List of Abbreviations

SITPN	Synchronously executed Interpreted Time Petri Net with priorities
VHDL	Very high speed integrated circuit Hardware Description Language
PCI	Place Component Instance
TCI	Transition Component Instance
GPL	Generic Programming Language
HDL	Hardware Description Language
LRM	Language Reference Manual

For/Dedicated to/To my...

Chapter 1

\mathcal{H} -VHDL: a target hardware description language

- Make a remark on the notation of design states, e.g. \mathcal{E}'' refers to the set of events of design state σ'' when there is no ambiguity.
- Two points of view to consider the semantics of VHDL: simulation or synthesis. Simulation described in the LRM; synthesis, problem is that there are no standard, unlike Verilog (cite Verilog standard synthesis semantics).
- There are different kinds of component instantiation statement but we only refer to design instantiation statement.
- Talk about error cases in the implementation part (?)

1.1 Presentation of the VHDL language

The intent here is to give an overview of the VHDL language, its purpose, its main syntactical constructs, and an informal description of its semantics as presented in the Language Reference Manual (LRM) [13]. The VHDL language offers a lot of possibility in terms of hardware (and even software) description. Here, we are not trying to be exhaustive in our presentation of the language. We will only maintain our description of the VHDL concepts in the scope that is of interest to us. The readers that are interested in learning more about the VHDL language can refer to [13], [1] and [21].

1.1.1 Main concepts

The VHDL acronym stands for Very high speed integrated circuit Hardware Description Language. As its name indicates, the main purpose of the VHDL language is to describe hardware circuits. There are two approaches to the description of circuits. The first aims at the simulation of the described circuits, and the second aims at the synthesis of described circuits on physical supports. Thus, the constructs of the VHDL language must be interpreted depending on the

purpose of the designer. For instance, the language gives the possibility to describe the connection of wires inside a circuit. A wire is represented by the concept of *signal*. In the context of circuit simulation, a *signal* can be compared to a variable; it has a given type and holds a value that fluctuates in the course of the simulation. In the context of synthesis, a signal really describes a physical wire and must be considered as so. From these two approaches to circuit description arise two ways of considering the semantics of the language (see Section 1.2).

In VHDL, a top-level program is called a *design*. A design describes a hardware circuit. As explained in Chapter ??, the hilecop transformation generates a VHDL design implementing the input SITPN model. To do so, the transformation generates and connects the component instances of two previously defined VHDL designs: the *place* design that implements the concept of a SITPN place, and the *transition* design that implements a SITPN transition. These designs were defined by the INRIA CAMIN team at the creation of the HILECOP methodology. In the following sections, we will be using excerpts of the definition of the place and transition designs to illustrate the content of VHDL programs and the rules of the VHDL language semantics. The reader will find the source code of the place and transition designs in concrete and abstract syntax in Appendices A and B.

A VHDL design is composed of two descriptive parts. The first part is called the entity and describes the interfaces of a circuit, namely: the input and output ports, and the generic constants. Listing 1.1 is an excerpt of the transition design's entity that defines the generic constants, the input and output port interfaces of the design. Figure 1.1 is a visual representation of the interfaces of the transition design.

```

1  entity transition is
2    generic(
3      transition_type : transition_t := NOT_TEMPORAL;
4      input_arcs_number : natural := 1;
5      conditions_number : natural := 1;
6      maximal_time_counter : natural := 1
7    );
8    port(
9      clock : in std_logic;
10     reset_n : in std_logic;
11     input_conditions : in std_logic_vector(conditions_number-1 downto 0);
12     time_A_value : in natural range 0 to maximal_time_counter;
13     time_B_value : in natural range 0 to maximal_time_counter;
14     input_arcs_valid : in std_logic_vector(input_arcs_number-1 downto 0);
15     reinit_time : in std_logic_vector(input_arcs_number-1 downto 0);
16     priority_authorizations : in std_logic_vector(input_arcs_number-1 downto 0);
17     fired : out std_logic
18   );
19 end transition;
```

LISTING 1.1: The entity part of the transition design in concrete VHDL syntax.

The generic clause of the entity holds the declaration of the generic constants. The purpose of generic constants is either to represent some dimensions of the design (e.g. the size of ports, internal signals...) or to represent constant values used throughout the design. In Listing 1.1,

one can see that the `conditions_number` generic constant gives a dimension to the type of the `input_conditions` input port, which is an array of Boolean values with indexes ranging from 0 to `conditions_number-1` (that is the meaning of `std_logic_vector (conditions_number-1 downto 0)`). The port clause holds the declaration of input and output ports of the design. The `in` keyword indicates the declaration of an input port and the `out` indicates the declaration of an output port.

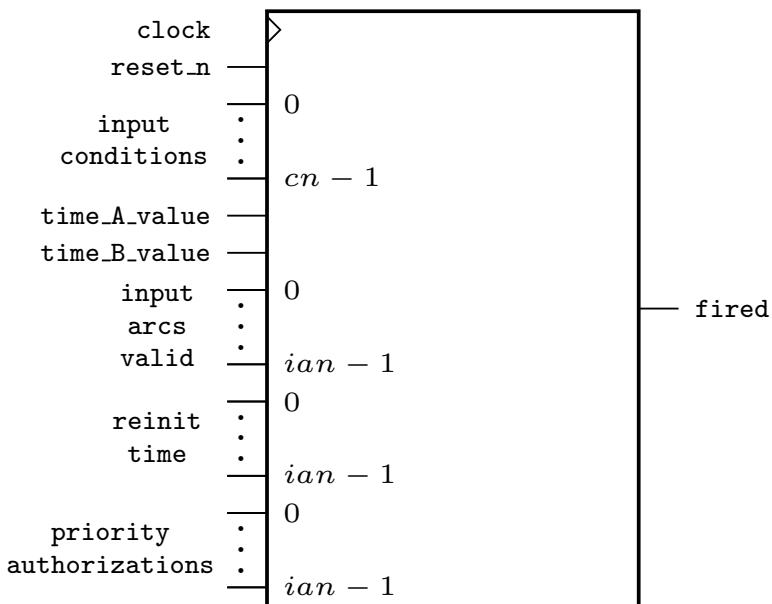


FIGURE 1.1: A representation of the transition design entity. On the left side, the input port interface of the transition design; cn stands for `conditions_number` and ian stands for `input_arcs_number`, i.e. two of the generic constants declared in the generic clause of the transition design entity; the numbers at the right of the input pins represent the pin indexes. On the right side, the output port interface of the transition design.

The second part of a VHDL design is called the architecture. The architecture describes the internal behavior of the design. It declares all the internal signals involved in the description of the design behavior. Then, there are three ways to describe the behavior itself: by using processes, by instantiating other designs (also called, component instantiations), or by combining both technics (the latter option is chosen in the VHDL designs generated by the HILECOP transformation).

Behavior specification with processes

The first way is to specify one or multiple processes. Processes are concurrent statements that describes the wiring or the operations performed on the signals of a given design. A process declares a sensitivity list that corresponds to the signals read in the process statement body; also, it possibly declares internal variables. The sensitivity list is only useful for the purpose of simulation. It permits to resume the execution of a process when the value of one of the signals

of its sensitivity list changes. Listing 1.2 gives an excerpt of the transition design architecture containing the declarative part of the architecture (i.e. internal signals) and three of the processes describing the transition design behavior, namely: the condition_evaluation process, the firable process and the fired_evaluation process.

```

1  architecture transition_architecture of transition is
2    signal s_condition_combination: std_logic;
3    signal s_enabled: std_logic;
4    signal s_firable: std_logic;
5    signal s_firing_condition: std_logic;
6    signal s_priority_combination: std_logic;
7    signal s_reinit_time_counter: std_logic;
8    signal s_time_counter: natural range 0 to maximal_time_counter;
9  begin
10
11    condition_evaluation: process(input_conditions)
12      variable v_internal_condition: std_logic;
13    begin
14      v_internal_condition := '1';
15
16      for i in 0 to conditions_number - 1 loop
17        v_internal_condition := v_internal_condition and input_conditions(i);
18      end loop;
19
20      s_condition_combination <= v_internal_condition;
21    end process condition_evaluation;
22
23    ...
24
25    firable: process(reset_n, clock)
26    begin
27      if (reset_n = '0') then
28        s_firable <= '0';
29      elsif falling_edge(clock) then
30        s_firable <= s_firing_condition;
31      end if;
32    end process firable;
33
34    fired_evaluation: process (s_firable, s_priority_combination)
35    begin
36      fired <= s_firable and s_priority_combination;
37    end process fired_evaluation;
38
39  end transition_architecture;
```

LISTING 1.2: An excerpt of the architecture part of the transition design in concrete VHDL syntax.

In Listing 1.2, from Line 2 to Line 8, the architecture declares the internal signals of the transition design. Then, Line 11 begins the declaration of the condition_evaluation process. The sensitivity list of the condition_evaluation process holds one signal, the input_conditions input port, and declares a local variable v_internal_condition.

In the statement body of a process, the designer can use control flow statements common to most of the generic programming languages (if statement, for loops...), and also statements that are specific to the VHDL language. The most representative statement, and the one of interest to us, is the *signal assignment* statement. The signal assignment statement relate a given signal identifier to a source expression. For instance, at Line 20 of Listing 1.2, the signal assignment statement, represented with the \leftarrow operator, assigns the value of the internal variable v_internal_condition to signal s_condition_evaluation; the v_internal_variable that itself holds the Boolean product between the members of the input_conditions input port performed in the for loop of Lines 16 to 18.

When considering a VHDL design in the point of view of hardware synthesis, a signal assignment statement specifies a wiring between a target signal identifier and other source signals. Figure 1.2 gives a synthesis-oriented view of the processes described in Listing 1.2.

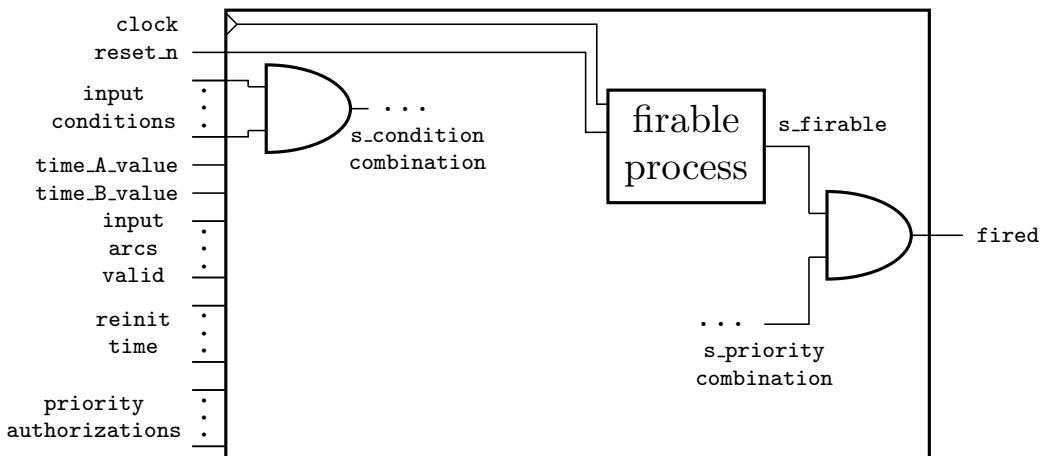


FIGURE 1.2: A representation of a part of the transition design architecture comprising three processes. On the left side, the condition_evaluation process connecting the input_conditions input port to the s_condition_combination internal signal; the firable process in the middle; on the right side, the fired_evaluation process connecting the s_firable and the s_priority_combination signals to the fired output port.

In Figure 1.2, the condition_evaluation process is represented as an and port performing the product over the elements of the input_conditions input port. The fired_evaluation process is a simple and gate connecting the fired output port to the s_firable and s_priority_combination internal signals. The firable process is a *synchronous* process. It responds to the event of the clock signal. In its statement body, the firable process assigns the value of the internal signal s_firing_condition to the signal s_firable only at the occurrence of the falling edge of the clock signal (captured by the expression falling_edge(clock) where falling_edge is a primitive function of the VHDL language). In the point of view of simulation, there

are no distinction between synchronous processes and *combinational* processes, i.e. processes that are executed independently of the occurrence of a clock signal. However, in the point of view of synthesis, processes responding to a clock signal follow the rules of the synchronous logic, whereas, combinational processes follow the rules of combinational logic.

To complete the presentation of the statements to be found in the body of processes, the VHDL language is also equipped with timing constructs, i.e. statements that explicitly specify an amount of time in a given time unit. The signal assignment statement possibly specifies a time clause indicating when the assignment must be performed. For instance, the signal assignment statement specifying that the value of signal *b* must be assigned to signal *a* in 3 milliseconds takes the form: *a* \leftarrow *b* in 3 ms. When no time clause is specified for a signal assignment statement, we talk about a δ -delay signal assignment, i.e. the application of the signal assignment is related to some δ interval corresponding the propagation time through a wire. When a time clause is specified, we talk about an unit-delay signal assignment. δ -delay signal assignments are synthetizable, meaning they have an equivalent implementation on a physical device, whereas, unit-delay signal assignments can not be synthetized. Unit-delay signal assignments do not appear neither in the VHDL designs generated by HILECOP transformation nor in the declaration of the place and transition designs. We are only mentioning their existence here because they are the witnesses of the two time paradigms that inhabit the simulation algorithm describe the semantics of the VHDL language: δ time and real time.

Behavior specification with design instances

The second way to specify the behavior of a design is to use other designs, or rather instances of other designs, as components of the circuits. In that case, the design is said to be composite as it embeds instances of other designs in its own behavior. Also, a design at the highest level of embedding, i.e. that is not instantiated as a part of another design's behavior, is called a *top-level* design. The design instantiation, or component instantiation, statement permits to instantiate a design in an embedding architecture. When instantiating a design with a design instantiation statement, the designer provides the component instance with an identifier. Then, the design instance must be dimensioned; this is performed through a generic map that associates the generic constants of the design being instantiated to a static value. Finally, the designer specifies how the component instance is connected to the other elements of the architecture. A port map associates the input ports and output ports of the component instance to expressions or to the signals of the embedding architecture. Listing 1.3 shows an example of instantiation of the HILECOP's transition design. This instance is involved in the definition of the behavior of an embedding design called toplevel.

```

1  architecture toplevel_architecture of toplevel is
2  begin
3
4  ...
5  idt : entity transition
6  generic map (
7    transition_type => NOT_TEMPORAL,
8    input_arcs_number => 1,
9    conditions_number => 1,
```

```

9      maximal_time_counter => 1
10   )
11   port map (
12     clock => clock,
13     reset_n => reset_n,
14     time_A_value => 0,
15     time_B_value => 0,
16     input_conditions(0) => id0,
17     input_arcs_valid(0) => id1,
18     priority_authorizations(0) => '1',
19     reinit_time(0) => id2,
20     fired => id3
21   );
22   ...
23 end toplevel_architecture;

```

LISTING 1.3: An example of design instantiation statement in the architecture of the toplevel design. Here, the design being instantiated is the transition design.

In Listing 1.3, the transition component instance has the identifier id_t . Following the entity keyword is the name of the design being instantiated; here, the transition design. Then, the generic map associates the generic constants of the transition design (i.e. the left side of the arrow, also called the *formal* part) to static values (i.e. the right side of the arrow called the *actual* part). This permits the dimensioning the component instance. For example, remember that the `input_arcs_number` generic constant value determines the number of elements in the composite input ports `input_arcs_valid`, `priority_authorizations` and `reinit_time`. The port map associates the input ports of the transition design to expressions. For instance, the `time_A_value` input port is connected to the constant value 0, and the `input_conditions` input port is connected to the internal signal id_0 at index 0. The port map also associates the output ports with signal identifiers. Contrary to the association of input ports, output ports can not be associated to expressions as output port association describes a direct wiring. In the port map described in Listing 1.3, the association `fired` \Rightarrow id_3 expresses that the `fired` output port is connected to the signal id_3 , where signal id_3 is defined in the embedding design. Figure 1.3 illustrates the transition design instance id_t and the wiring of its input and output port interfaces inside the toplevel design.

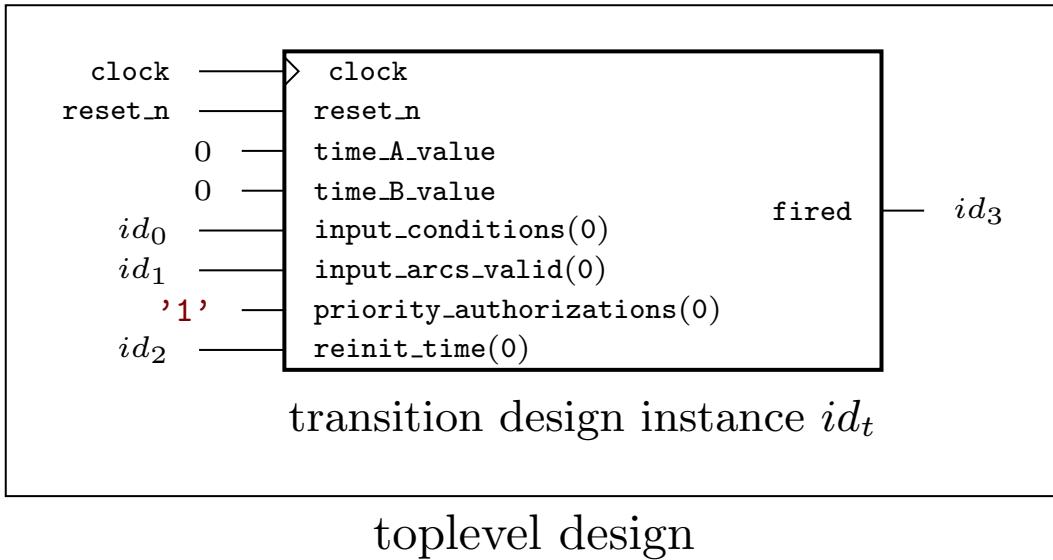


FIGURE 1.3: Visual representation of a design instantiation statement. Here, the figure represents the transition design instance described in Listing 1.3.

1.1.2 Informal semantics of the VHDL language

Even though, in practice, there are two ways to consider a VHDL design, i.e. a synthesis-oriented way and a simulation-oriented way, the LRM does not define a synthesis-oriented semantics for the VHDL language. A synthesis-oriented semantics gives an interpretation to a design by describing an equivalent in a lower level formalism, closer to the physical circuit. For instance, the Verilog language gives a synthesis-oriented semantics to its programs by defining an equivalent RTL level description [15]. The LRM gives an informal semantics to VHDL designs through the definition of a simulation algorithm. The purpose of simulation is to compute the evolution of the values of signals during a certain time interval. Through the simulation process, the designer is able to control the behavior of the modeled circuits and to detect flaws in the evolution of the signal values.

Former to the simulation, the LRM defines an elaboration phase that permits to transform a design into a simulation-ready execution model. The elaboration phase has several goals. First, it builds the simulation environment and a starting design simulation state. The simulation environment is built based on the declarative parts of the top-level design; it maps the signals to their types. In the design simulation state, each signal is associated with a current value and with a driver. A driver maps time points to values and the association between a given time point and a signal value is called a transaction. The necessity of drivers is explained by the presence of unit-delay signal assignments. A unit-delay signal assignment specify a time clause indicating when a giving assignment must be performed, e.g. $a \Leftarrow b$ in 3ms (signal a takes the value of signal b in 3 milliseconds). Thus, when a unit-delay signal assignment is executed in the course of a simulation, its effect is to change the driver of the target signal by posting a new transaction. For instance, let T_c by the current simulation time, the execution of statement $a \Leftarrow \text{true}$ in 2ns sets a new transaction in the driver of signal a . The new

transaction associates the value true to the time point $T_c + 2\text{ns}$. Note that without unit-delay signal assignments, drivers are not needed as all assignments take their effects at the current simulation time. Second, the elaboration checks the well-formedness of the design by performing static type-checking on the behavioral part of the design. It also checks that the connection between signals respect certain rules, for instance, that there are no multiply-driven signals, i.e. signals that are written to by multiple processes. Finally, the elaboration operates some transformations over the VHDL code, and thus builds the *execution model*. To summarize, all concurrent statements of the behavioral part are transformed until the top-level design behavior is only composed of processes.

After the elaboration, the top-level design, or rather its corresponding execution model, is ready to be simulated. Two entities are involved in the simulation: the *sea* of processes obtained after the elaboration of the top-level design, and a *kernel* process. The kernel process orchestrates the simulation; it handles the time of the simulation, i.e. it holds a variable describing the current time of the simulation, and resumes the execution of processes. Figure 1.4, which is an excerpt from [5], describes the structure of the VHDL simulation algorithm.

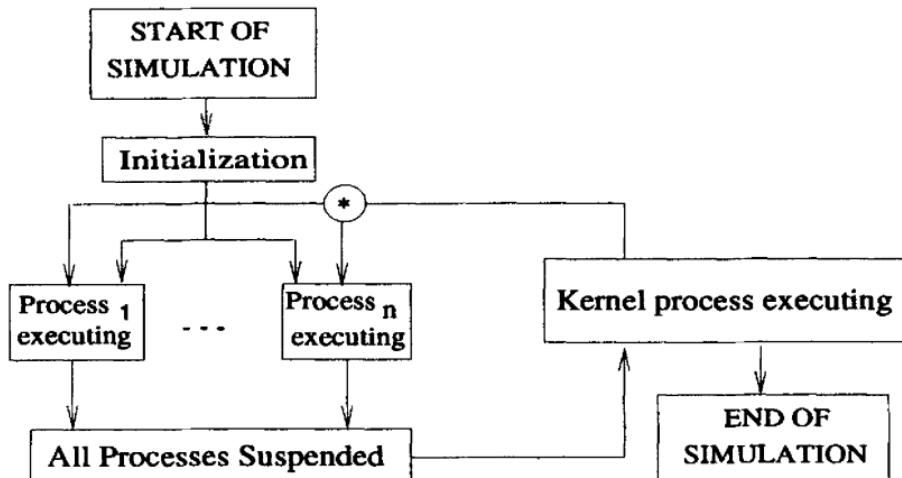


FIGURE 1.4: The VHDL simulation loop. Excerpt from [5].

The simulation starts with the initialization phase. During the initialization phase all processes are run exactly once. Then, the simulation cycles are structured as follows. All processes execute their statement body concurrently. New transactions are posted in the drivers of signals for every interpreted signal assignment statement. The execution goes on until all processes have executed their statement body and then have reached a suspension state. When, all processes are suspended, the kernel process takes over. Figure 1.5 shows the activity diagram associated with the kernel process.

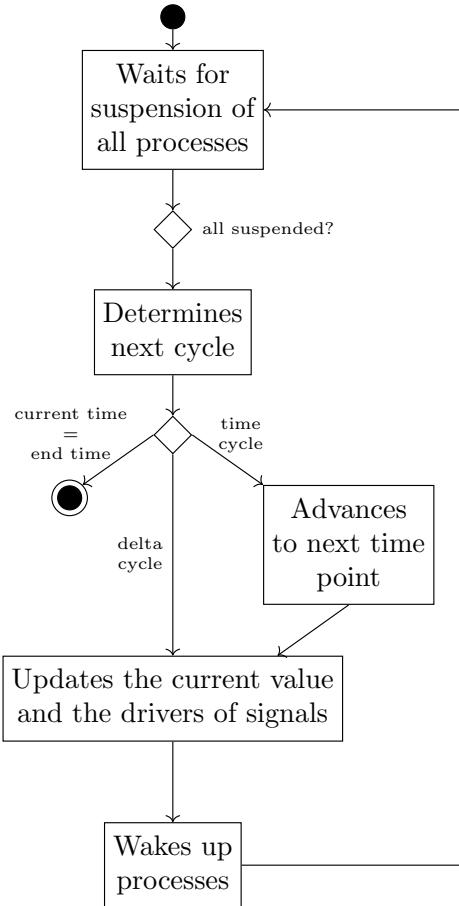


FIGURE 1.5: The activity diagram of the kernel process. Square boxes represent activities, diamond nodes are decision nodes. The black circle at the top represents the starting point of the activities; the other black circle in the middle of the diagram represents the end of all activities.

As shown in Figure 1.5, the kernel process will then determine the kind of simulation cycle that will be performed next. There are two kinds of cycles: delta cycle or time cycle. If the value of a signal changes at the current time point, i.e. its driver holds a transaction at the current time point with a new value, then a delta cycle must be performed. Then, the simulation time does not change. The kernel process updates the current value of signals and their drivers, and wakes up the processes sensitive to the signals that obtained new values. The repetition of multiple delta cycles corresponds to the stabilization of signal values, i.e. the propagation of values through the wires, that takes effect in a negligible δ time. If all signal values are stable at the current time point, then a time cycle must be performed. The kernel process looks up the drivers for the next time point where the value of a given signal will change. Then, the kernel process advances the simulation time to this next time point before updating the signal values and resuming the execution of processes. The simulation goes on like this, alternating between delta and time cycles, until the current time value reaches the time specified for the end of the simulation.

1.2 Choosing a formal semantics for VHDL

In the previous section, we presented the main concepts underlying the VHDL language and its informal semantics. We want to prove that the HILECOP transformation that generates VHDL code from SITPNs preserves the behavior of the initial model (i.e, the SITPN model) into the generated VHDL program. A formal semantics for the VHDL language is therefore a necessary element to be able to reason about the generated VHDL programs, and moreover to be able to compare their behaviors with the behaviors of the source SITPN models. Keeping that in mind, which formal semantics should we consider for VHDL?

The same holds for any research task: there is a tradeoff between finding a tool designed by others that will fit our needs, and creating our own tool that will mitigate the gaps between our needs and what is available in the literature. In the present case, the tool is a formal semantics for VHDL. Adopting a fully-set semantics found in the literature as a baseground for the implementation of a formal semantics for VHDL has multiple perks. First, it reduces the formalization effort, which is not a lesser point considering that the proof ahead might be long and must still be completed within the time span of the thesis. Still, the semantics would need to be implemented in Coq, if no implementation exists (or not written in Coq). Second, the formal semantics of programming languages found in the literature are often general in their approach, this to provide a generic framework to reason about programs. However, we must not loose sight of our goal which is to prove behavior preservation; a generic formal semantics could turn out to be too complex, or necessitate too much tweaking and thus hinder the fullfillment of our task. On the other side, creating our own formal semantics for VHDL, based on the work of others, is the best way to fit our needs in compliance with our final aim. However, the pitfalls are that the resulting semantics might prove to be very specific, therefore preventing others from using it. Also, a work of formalization would be necessary which, as we already stated, would be time consuming. In order to determine whether we ought to use an existing semantics or design a new one, we must first clearly specify our needs pertaining to the VHDL language.

1.2.1 Specifying our needs: HILECOP and VHDL

Two elements are of major influence to the specification of our needs for a formal semantics: first, the context of HILECOP and the specificities of the VHDL programs that are generated; second, the context of theorem proving. These two aspects entail the following considerations.

The need for coverage

The HILECOP methodology generates particular VHDL programs. Even if some transformations can be operated on the generated programs to simplify them, the looked-for formal semantics must be able to deal with a certain subset of the VHDL language. Especially, this subset must include:

- 0-delay (or δ -delay) signal assignments (equivalent to transport-delay signal assignment with a “0 ns” after clause).

- component instantiation statements with generic constant and port mapping.
- entity's generic constant clauses (declaration of generic constants in a design entity).

HILECOP's VHDL programs only deal with 0-delay signal assignments because they are the only kind of signal assignments that can be synthesized. As a matter of fact, the industrial compiler/synthesizer used in the HILECOP methodology only accepts VHDL programs with no timing constructs (i.e, no wait statements or delayed signal assignments) as input.

Concerning component instantiation statement, the VHDL LRM describes a way to transform these statements into equivalent process statements and block constructs [13, p. 141] which are a part of the elaboration of the design. However, we want to preserve the hierarchical structure provided by the component instance statements arguing that it will be easier to compare the state of a given SITPN model with a VHDL design state with an explicit hierarchical structure. Indeed, there exists a mapping between places and transitions of an SITPN and their mirror (generated by the transformation) place and transition component instances. This one-to-one correspondence might turn out to be handy to perform the proof of behavior preservation. Obviously, the semantics must cover the evaluation of process statements which are the core concurrent statements of VHDL programs.

The types of signals and variables used in HILECOP VHDL designs must have finite ranges of values. For instance, a VHDL signal that ranges over \mathbb{N} cannot be synthesized on a physical circuit. Indeed, \mathbb{N} has an infinite number of values, and would therefore require an infinite number of latches to be physically implemented. Moreover, as the number of latches used to implement a digital circuit greatly impacts the power consumption of the circuit, the types of signals and variables must be as constrained as possible to optimize the dimensioning of the circuit. The generic constant clauses of the HILECOP place and transition designs (see Section Presentation of the VHDL language) help limiting the type ranges. The generic constants define the bound of the array and natural range types for the different signals and variables declared in the place and transition designs' architecture. When a place or a transition component is instantiated, that is during the transformation of the SITPN model into VHDL code, its generic constants receive values via a generic map; we call it the dimensioning of the component instance. Therefore, generic constant clauses must belong to the subset of the VHDL language covered by the semantics (even though it seems a trivial formalization task compared to the core of the VHDL semantics).

The need for synchronous execution

The second property of HILECOP's generated VHDL programs is their synchronous execution. Indeed, the digital circuits designed with the HILECOP methodology are all synchronously executed on physical target. The generated VHDL designs declare a clock signal as an input port of their entity port interface. Thus, the behavioral part of the designs contains two kinds of processes: *synchronous* processes, i.e processes that are sensitive to the clock signal, and *combinational* processes, i.e processes that are not sensitive to the clock signal, and that are permanently running until the stabilization of the signal values. Synchronous processes react to

the events of the clock signal, i.e the rising and the falling edge, and possess blocks of sequential statements that are only executed at the precise moment of the clock event¹. Therefore, we are in a strong need of a semantics that deal with synchronism, and that explicitly integrates the synchronization with a clock signal into the expression of the simulation cycle. Thus, the two dimensions of time, respectively delta time and “real” time [22], that are part of the VHDL language, must be handled by our semantics. Delta time pertains to delta-cycles, which are triggered by the execution of delta-delay signal assignments, that is, the only kind of signal assignments found in HILECOP VHDL programs. Real time pertains to time-steps. When all signal values are stable (when there are no more delta-cycles), the simulation advances the current time value to the next time point where a relevant event happens. A relevant event could be the execution of the next pending signal assignment that was associated with a delay, or the end of a `wait for x` statement (where `x` specifies a time delay). In our case, neither delayed signal assignments nor wait statements are part the covered VHDL language subset. The only two relevant events to which the simulation advances during a time-step are the rising edge and the falling edge of the clock signal.

Other considerations

Considering the kind of proof that needs to be established, we would rather consider an operational semantics for VHDL than a denotational one. The reason is that, in the CompCert project [17], which is one of our major inpsiration source, the whole C compiler toolchain is verified by reasoning over the operational semantics of the source and target languages. A last consideration pertains to whether or not the VHDL semantics must explicitly handle errors. As the SITPN semantics does not include the production of error values, the handling of errors by the VHDL semantics is not a mandatory aspect.

Qualifying criterions

We here give the list of the qualifying criterions that will help to analyze the different VHDL semantics encountered in the literature and presented in the next section. The three most relevant criterions are:

- *Synchronism.* We distinguish three levels for this criterion:
 - Synchronism is not expressible in the considered VHDL semantics.
 - Synchronism is expressible in the considered VHDL semantics. Synchronism is expressible if time-steps are handle in the semantics, at least to be able to represent clock events.
 - Synchronism is explicit, i.e. the simulation loop is built around the occurrences of clock events.

We will promote the semantics that explicitly formalize a synchronized execution of a VHDL design.

¹These blocks are guarded by the expressions `rising_edge(clk)` and `falling_edge(clk)`.

- *Component instantiation.* Either the semantics handle the component instantiation statement in its simulation rules, or component instantiation statements must be transformed in order to be executed. We will promote the semantics that handle component instantiation statements without transformation.
- *Elaboration.* This criterion expresses the ability of the semantics to handle constrained types, i.e. arrays and natural ranges, and generic constant clauses that are both dealt with during *elaboration* phase. Either the semantics handle these constructs or it does not. Of course, we will promote the first kind of semantics.

1.2.2 Looking for an existing formal semantics

Here, we give a summary of the work found in the literature pertaining to the formalization of the VHDL language semantics. Articles are gathered and presented depending on the type of semantics that is used in the formalization (operational, denotational, axiomatic...). Each semantics is analyzed regarding the needs that were previously expressed.

Denotational semantics

Some authors have been interested in giving a formal denotational semantics to VHDL. In a general manner, these authors want to reason about VHDL programs: prove properties over a VHDL program, prove that two programs are equivalent... Such tasks that are more fit for a denotational semantics.

In [10], the authors give a denotational semantics to the VHDL language, this leveraging the Focus [7] method for the development of distributed systems. Signal values and their evolution through time are represented as streams of values. Statements are denoted as stream-processing functions. Processes are stream-processing functions that takes input signal streams (signals of the sensitivity list) and yields transaction traces (i.e, waveforms) over output signals (i.e, signal that are written by the process). Transaction traces are merged together as the result of the concurrent execution of processes. Resolution functions are used in case of multiply-driven signals (i.e, signals that receive a value from multiple processes). The authors only consider 0-delay signal assignment in their semantics, stating that it is sufficient to “consider time at a logical level to model both synchronous and asynchronous designs”. However, it necessitates some transformations on a design that has a synchronous execution to express it only with 0-delay signal assignments. Therefore, this semantics does not express synchronism of execution in an explicit manner. Moreover, the component instantiation statement is not treated by the semantics.

In [4], the authors give a denotational, yet relational, semantics for VHDL. A state of a VHDL design is represented by a function binding signals to values; a worldline is a time-ordered list of states. Statements (including processes) are denoted in the semantics by a relation that binds an input couple, composed of a time point and a worldline, to an output couple of the same type. Multiple input and output couples possibly satisfy the relation denoting a particular statement; thus, the semantics is undeterministic. The semantics tries to abstract from the formalization of the simulation cycle as it is done in the LRM. The authors want to

establish a semantics that is abstract enough to be able to compare all other works of formalization with the authors semantics. The authors also give an axiomatic semantics (i.e, in the Hoare logic style) which is proved to be sound and complete with the first denotational semantics. A Prolog [6] implementation of the axiomatic semantics is given. Regarding our needs, the semantics only deals with unit-delay signal assignments (no 0-delay), and therefore does not cover the VHDL subset that we are interested in. The hierarchical structure of designs is also not preserved, and, although expressible, the semantics does explicitly express a synchronous simulation cycle.

The denotational semantics expressed in [20] uses interval temporal logic as an underlying model. Leveraging this underlying model, the authors are interested in proving some properties over VHDL designs to help compilers to optimize the code, for instance, by using rewrite rules proved to be valid against the model. Some of the proofs laid out by the authors are embedded in PVS [19]. The expression of the dynamic model uses many concepts described in the LRM, like drivers, port association, driving and effective values for signals. The semantics deals with both unit-delay and δ -delay. The semantics works on fully-elaborated designs, therefore, it does not deal with component instance statements. Moreover, interval temporal logic is useful to reason on the VHDL designs in the presence of delays, however, it loses its interest for designs presenting only 0-delay assignments.

Joining the common opinion, in [2], the author states that “denotational semantics is more adequate for mathematical reasoning”. The author formalizes the VHDL semantics to prove the equivalence between VHDL programs (for instance, a specification and an implementation). What is of major interest regarding our needs is that the author is interested in expressing a simulation cycle for synchronous designs. Therefore, a distinction is made between combinational and synchronous processes in the abstract syntax. Moreover, this work formalizes the elaboration part of a VHDL design former to the simulation; also, the elaboration keeps the hierarchical setting of the VHDL design, that is component instantiation statements are not replaced by processes. Due to the time abstraction, the semantics only deals with 0-delay. It is explained by the fact that the reference time-unit is the clock period (i.e, the only known time-step), and the advancing of time, happening during the simulation cycle as described in the LRM, is captured within the setting of the simulation cycle. Also, the semantics takes primary inputs into account (i.e, input ports of the top-level design); to preserve a synchronous behavior for the simulated design, the hypothesis is made that the values of the primary inputs are stable between two clock events. The only critic that can be made to this semantics regarding our needs is that it is expressed in denotational style.

Operational semantics

Multiple works formalize an operational semantics for VHDL. Naturally, these works are interested in the formal description of the VHDL simulator, more or less closely to the description of the LRM.

In [3], a formal description of a *functional* semantics for VHDL is laid out based on stream-processing functions. The semantics is expressed with the functional programming language Gofer [16], thus enabling the computation of execution traces, that is, the computation of the streams representing the values taken by signals over time. As in the former work of the same

author [4], only unit-delay signal assignments are dealt with, however, this time the author describes a deterministic operational semantics. Regarding our needs, this work is neither interested in preserving the hierarchical structure of VHDL designs, and no mention is made regarding how a design is elaborated, nor in expressing an explicit synchronous simulation cycle.

In [5], the authors formalize the simulation loop of the LRM using Evolving Algebra machines (EA-machines). All important constructs of the VHDL language are represented as records; processes are represented as concurrent agents running pseudo-codes, and the simulation control flow is passed to and fro between the kernel process (i.e, the simulation orchestrator) and the rest of the processes that execute the design behavior. This semantics implements closely the simulation loop as described in the LRM. Therefore, it is very rich and deals with most of the VHDL constructs, including the two time paradigms of the language. Moreover, the semantics works on fully-elaborated designs, therefore, component instantiation statements are omitted. However, a synchronous execution is fully expressible even if not explicitly embedded in the expression of the simulation loop.

In [24], the author presents a natural semantics for VHDL. The simulation loop is expressed by inference rules, and the execution of processes is based on the events over signals of their corresponding sensitivity lists. The execution of statements computes transaction traces, that is, the projected waveforms for signals over the future of the simulation. The semantics deals both with unit and delta delays. Regarding our needs, this semantics covers the subset of the VHDL language that we are interested in, even if, it also covers some constructs pertaining to unit delays that are irrelevant to us (like wait and unit-delay signal assignment statements). A synchronous execution is expressible within the semantics, although it would be hidden in the inference rule formalizing the generic simulation loop. Also, the semantics does not provide its simulation loop with a simulation horizon (a maximum number of simulation cycle to be computed). The simulation ends when signal values evolve no more. The question of the influence of the environment, measured through the values of the primary inputs of a design, is not discussed.

In [11], the author presents an operational semantics for VHDL in the small-step style. The semantics follows closely the simulation cycle described in the LRM; however it is very concise and clear. The covered VHDL subset comprises arbitrary wait statements, and both unit and delta-delay signal assignments. There is an interested discussion about the non-determinism of VHDL, since it is a concurrent programming language: it entails that non-determinism is only existent at the processes level, that is, internal sequential statement of processes can be executed in an undeterministic manner (referred to by the author as A actions, that is, *internal* actions). But at every delta or time step (referred to as δ and T actions) of the execution, the design state can be computed in a deterministic manner, since all process have reached a wait statement that stalled the execution of their inner body. The author is interested in the comparison of the behavior, and therefore, the equivalence between VHDL programs. He describes two strategies to compare VHDL programs. The first one is bisimulation; it is based on the comparison of the sequence of actions (either A, δ or T actions) performed by the two programs. The second one is observational equivalence; it is based on the observation of the value of the output signals of two VHDL programs (the observees), that receive values in their input signals from another VHDL program (the observer). The observer stimulates the

entries of the observees and reaches a success state based on its observations of the value of the outputs. Regarding our needs, this semantics permits the description of our synchronous simulation cycle. However, like most of the semantics presented here, the component instantiation statement is not supported as it stands, but it is rather transformed into the equivalent processes statements. Small-step semantics is not needed in our case because we are only interested in the values of signals at the delta and time steps (for us, time steps correspond to clock events). We are not interested to capture the design states in the middle of the execution of a process body. We are more interested in "weak bisimulation", therefore forsaking the internal actions (i.e, A actions, execution of a process body that does not end in a wait statement) performed by a VHDL program. Indeed, a natural operational semantics in the style of Van Tassel's [24] is sufficient in our case. In [23], the authors extend the work of [11], especially by handling shared variables, in the presence of which a VHDL program can have a concrete underterministic behavior. The authors are also interested in the equivalence between two VHDL programs, and they are interested in determining a unique meaning property for VHDL programs. The unique meaning property states that the execution of a VHDL design in the presence of shared variables is unique. This work is interesting as it points out the fact that VHDL is not only subject to benign undeterminism. However, we are not interested in dealing with constructs so advanced as shared variables or postponed processes, therefore, this work is not really relevant to us.

Translational semantics

Another kind of semantics, called "translational", is interested in establishing a formal semantics for VHDL by translating a VHDL design into another formal model. Thus, the semantics of VHDL is modeled by the translation and the formal semantics of the target model. The target model has the ability to model concurrency, which is one of the specificity of VHDL. Moreover, target models are chosen because of the tools that they provide for analysis, and thus, a translational semantics for VHDL is often related to model checking considerations.

In [22], the author expresses the formal semantics of VHDL by translating a VHDL design into a corresponding flowgraph. All VHDL constructs, ranging from sequential statements to concurrent processes, are expressed with individual flowgraphs that are then composed together through their interfaces. The simulation cycle of VHDL is also encoded by means of connected flow graphs: one for the "execution part" of the semantics, that is, all processes run until blocked in a wait configuration, and one for the update part (i.e, the kernel process in the semantics of [5]). Flowgraphs come with a large amount of tools for analysis, and this translational semantics is involved in the setting of a framework to reason about VHDL programs using multiple techniques (automatic theorem proving, model checking...). All these techniques lean on the flowgraph formalism.

In [9], the author introduces a translational semantics for VHDL based on deterministic finite-state automata. Again, the reason for using such automata lies in the existence of many analysis tools. Moreover, forcing the generation of deterministic automata improves the time execution of model-checking techniques. The translation is performed on an elaborated VHDL design; a data space stores the values of signals and variables, and automata represent the control-flow of VHDL statements. Each VHDL statement is associated to a specific

automaton; sequence of statements are achieved by automaton composition. The simulation kernel is also represented by a specific automaton. Processes are composed together with respect to synchronization states, i.e. states that permit to pass the control from one process to another (for instance, after a wait statement), therefore achieving determinism in the control flow of the overall automaton.

In [18], the author presents a translation from VHDL to Coloured Petri Nets (CPNs) thus giving a formal semantics to VHDL constructs. The author approach to VHDL semantics is a strict translation of the “event-based” VHDL simulator by means of Petri nets. The author translates VHDL execution models (sea of processes) into CPNs, and also translates the kernel process into a CPN. The kernel process has previously been expressed as a VHDL process so that the translation into CPN is similar to the translation of other processes. Signals are not represented in the subnets, instead, three shared variables depict the signal states: one variable for the driving, one for the effective and one for the current value of a given signal. Colour domains of places in the subnets represent the different types of VHDL domains. Variables are represented by tokens. Values in drivers are represented by sequences of transactions (equivalent to waveforms); the author defines a set of functions that are convenient to handle sequences of transactions. Sequential statements are partitioned into two kinds: control flow (if, loop, case...) and notation (operations on signals and variables) nets. Processes subnets are made by the fusing of each sequential statements in the process body. There is a special *Resume* place that can be set by the kernel process to resume the activity of a process. Concurrency is not discussed here, as the Petri net models are inherently concurrent models. The kernel process is a broad CPN having some of its places interfaced with the process subnets. The decoloration of the Petri net enables the analysis of the model and the detection of dead-locks.

In [8], the author gives a formal semantics to VHDL by transforming a VHDL design into an abstract machine, i.e defined by a set of inputs, outputs, states and transition function over states and outputs. The author is interested in the verification of properties over VHDL designs (temporal properties) or to prove equivalence between designs (bisimulation). To operate this transformation, only a subset of VHDL is considered, otherwise a finite-state representation is not reachable. The covered VHDL subset consists of objects with finite types, and no quantitative timing constructs (no after clause in signal assignments or for clause in wait statements). The author claims that a VHDL design is implemented by an abstract machine if they have the same observational behavior, i.e, for the same value in their inputs they yield the same values in their outputs. Each process statement part is transformed into a decision diagram (control flow graph); then, the decision diagram encodes the transition functions over states and outputs in the abstract machine implementing the corresponding process. Process statements are composed in relation to some composition operator. Moreover, the article lays out a method to transform a block statement into an abstract machine. The initiative is to be noticed as there are few papers of the VHDL semantics that are interested in such hierarchical constructs as block or component instantiation statements. The article concludes with an expression of the space of complexity entailed by the transformation of a VHDL design into an abstract machine.

Although the translational semantics described above meet most of the qualifying criterions in relation to our needs, we are not especially interested in implementing one of these. The main reason being that it would necessitate the implementation of the transformation from the abstract VHDL syntax to the target model in addition to the implementation of the semantics

of the target model.

Table 1.1 summarizes the analysis of the VHDL semantics encountered during our literature review. Table 1.1 compares the different VHDL semantics in relation to the qualifying criterions (see Section 1.2.1).

		Fuchs and Mandler [10]	Breuer et al. [4]	Pandey et al. [20]	Borrione and Salem [2]	Breuer et al. [3]	Böger et al. [5]	Van Tassel [24]	Goossens [11]	Reetz and Kropf [22]	Döhmen and Hermann [9]	Olcov [18]	Déharbe and Borrione [8]
Semantics Description	Kind	D	D, A	D	D	O	O	O	O	T	T	T	T
Purpose	AR, ATP	AR	AR	AR	SS	SS	SS, ITP	SS, MC	ATP, MC, ITP	MC, ITP	MC	MC	MC
Qualifying Criterions	Component Instantiation	T	T	T	N	T	T	T	T	T	T	T	N
	Synchronism	NE	NE	NE	Ex	E	E	E	E	E	E	E	NE
	Elaboration	✗	✗	✗	✓	✗	✗	✓	✗	✗	✗	✗	✓
Extra. Informations.	Impl. Technology	Focus [7]	Prolog [6]	PVS [19]	?	Gofer [16]	?	HOL [12]	?	HOL [12]	?	?	?
	Particular Model or Data Types	Stream Processing	No	Interval Temporal Logic	No	Stream Processing	Evolving Algebra Machines	Natural Semantics (big-step)	Structural Semantics (small-step)	Flow Graphs	Finite-State Automatons	Colored Petri Nets	Abstract Machines and Decision Diagrams

TABLE 1.1: A comparative summary on VHDL formal semantics.

- Kind : D (Denotational) - A (Axiomatic) - O (Operational) - T (Translational).
- Purpose : AR (Abstract Reasoning) - ATP (Automatic Theorem Proving) - SS (Simulator Specification) - ITP (Interactive Theorem Proving) - MC (Model Checking).
- Component Instantiation : T (statement is *Transformed* into equivalent processes) - N (statement is *Natively* taken into account in the semantics).
- Synchronism : E (Expressible within the semantics) - NE (Not Expressible within the semantics) - Ex (Explicitly built in the semantics).

To summarize, we are interesting in a semantics with an operational setting, built for the purpose of interactive theorem proving (ideally, with an existing implementation in the Coq proof assistant). Most important, the formal semantics must be able to deal with the expression of synchronous designs, that is, designs synchronized with a clock signal. Therefore, a synchronous simulation cycle must be at least expressible within the semantics. Moreover, the semantics must handle component instantiation statements as they are, that is, without transforming them into equivalent processes. As a bonus, the semantics should formalize the elaboration part of VHDL semantics.

In Table 1.1, cells are colored in green when the cell's content foster the adoption of the semantics, in yellow when the content does not go towards the adoption of the semantics but is not disqualifying, and red when the content is a disqualifying criterion. Cell are labelled in light grey when their content is neutral in relation to the semantics adoption. Now comparing

the entries of Table 1.1 with the expression of our needs, we can discard the semantics with a cell labelled in red, that is most of the denotational semantics; moreover, all translational semantics are let aside for the reasons cited before. The candidate semantics are the operational semantics, plus the denotational semantics by Borrione and Salem [2], the only semantics that formalizes an explicitly synchronous simulation cycle. The semantics that is the most likely to be adopted is the Borrione and Salem's semantics. However, we prefer an operational setting for our semantics because it is more fit to our task. To lower down the complexity of proofs, we really need a semantics that builds the synchronism into its simulation cycle, therefore putting aside all the intricacies of the full-blown VHDL simulation cycle. Moreover, the big-step style for an operational semantics is more relevant to us; as stated before, we are not interested in the intermediary states of computation that a small-step style semantics considers. Based on the observations, we have decided to formalize our own VHDL semantics inspired from the semantics of Borrione and Salem's [2] and Van Tassel's [24]. The following sections are dedicated to the presentation of the syntax and semantics of a subset of VHDL called \mathcal{H} -VHDL. \mathcal{H} -VHDL embeds the subset of VHDL that we are interested in when considering the VHDL designs generated by the HILECOP transformation.

1.3 Abstract syntax for \mathcal{H} -VHDL

In this section, we describe the abstract syntax of \mathcal{H} -VHDL, the subset of VHDL covering all the constructs present in the generated \mathcal{H} -VHDL programs. Terminals of the language will be written in typewriter font, or will be enclosed in simple quotes for symbols with no typewriter representation. The a^* denotes a possibly empty repetition of the element a ; the a^+ denotes a non-empty repetition of a .

1.3.1 Design declaration

As in [24], we define the *design* construct in the \mathcal{H} -VHDL's abstract syntax which has no equivalent in the concrete syntax of VHDL.

```

design ::= design ide ida gens ports sigs cs
gens  ::= gdecl*
ports ::= pdecl*
sigs  ::= sdecl*
```

```

gdecl ::= (id,  $\tau$ , e)
pdecl ::= ((in | out), id,  $\tau$ )
sdecl ::= (id,  $\tau$ )
```

In the above entry, id_e indicates the entity identifier and id_a the architecture identifier of the declared design. The *gens* entry corresponds to the generic clause, i.e. the declaration list for the generic constants of the design. A generic constant is declared via the *gdecl* entry; it generic constant declaration is a triplet composed of a generic constant identifier, a type indication and

an expression denoting its default value. The ports entry holds the declaration of the input and output ports of the design. A port declaration (i.e. the pdecl entry) is a triplet composed of a port type, i.e. in or out, a port identifier, and a type indication. The sigs entry is the list declaring the internal signals of the design. An internal signal declaration entry (i.e. sdecl) is a couple composed of a signal identifier and a type indication. The cs entry represents the concurrent statements composing the behavior of the design.

1.3.2 Concurrent statements

`cs ::= psstmt | cistmt | cs || cs | null`

In \mathcal{H} -VHDL, two kinds of concurrent statements are available to describe the behavior of a design: process statements, represented by the psstmt entry, and component instantiation statements, represented by the cistmt entry. Concurrent statements are composable through the `||` operator. We add the `null` statement to help represent empty behaviors.

Process statement

```
psstmt ::= process (idp, sl, vars, ss)
sl      ::= id*
vars    ::= vdecl*
vdecl   ::= (id, τ)
```

A process statement declares a sensitivity, i.e. the `sl` entry, which is a list of signal identifiers. In order to be well-formed, the signals of a sensitivity list must be either internal signals or input ports of the design. The process possibly declares a set internal variables, i.e. the `vars` entry. A variable declaration entry is a couple composed of a variable identifier and a type indication. The `ss` entry represents the sequence of statements composing the body of the process, i.e. the part that will be executed during the simulation.

Component instantiation statement

```
cistmt ::= comp (idc, ide, gmap, ipmap, opmap)
gmap   ::= assocg*
ipmap  ::= associp*
opmap  ::= assocop*
assocg ::= (id, e)
associp ::= (name, e)
assocop ::= (id, (name | open)) | (id(e), name)
```

The identifier `idc` represents the name of component instance. Identifier `ide` points out the name of the design, i.e. the entity identifier, being instantiated here. The `gmap` entry describes

the list of associations between generic constant identifiers and expressions. The ipmap entry is the list of associations between input port identifiers (or indexed identifiers) and expressions. The opmap entry is the list of associations between output port identifiers (or indexed identifiers) and signal names, or the open keyword. Associating the open keyword with an output port identifier in an output port pmap indicates that the port is not connected.

1.3.3 Sequential statements

```
ss ::= name ⇐ e | name := e | if (e) ss [ss] | for (id, e, e) ss
      | falling ss | rising ss | rst ss ss' | ss; ss | null
```

The ss entry defines the sequential statements that compose the body of processes. The signal assignment statement is represented with the \Leftarrow operator; the variable assignment statement with the $:=$ operator. Among the control flow statements, the falling statement (resp. rising ss) declares a block of sequential statements to be executed only at the falling edge (resp. rising edge) of the clock signal (see Section 1.6.5). Also, the rst statement declares two blocks, the first one must be executed during the initialization phase of the simulation; otherwise, the second one is executed (see Section 1.6.4).

1.3.4 Expressions, names and types.

```
e ::= e and e | e or e | not e | e = e | e ≠ e
     | e < e | e <= e | e > e | e >= e | e + e | e - e
     | name | natural | boolean | (e+)
name ::= id | id( e )
boolean ::= true | false
τ ::= boolean | natural (e, e) | array (τ, e, e)
```

The expression entry declares a set of operators over Boolean expressions, and natural numbers expressions. The natural non-terminal represents the set of natural numbers (\mathbb{N}). The id non-terminal represents the set of identifiers, comparable to the set of strings, or any infinitely enumerable set. In what follows, identifiers will be enclosed in double quotes at the time of their declaration, and they will appear without double quotes when used in expressions.

1.3.5 Examples of \mathcal{H} -VHDL abstract syntax

Listing 1.4 gives the translation in abstract \mathcal{H} -VHDL syntax of the declarative part of the transition design presented in Listings 1.1 and 1.2 in concrete VHDL syntax.

```
1 design "transition" "transition_architecture"
2   -- Generic clause
3   (("transition_type", natural(0, 2), 0),
```

```

4   ("input_arcs_number", natural(0, NATMAX), 1),
5   ("conditions_number", natural(0, NATMAX), 1),
6   ("maximal_time_counter", natural(0, NATMAX), 1))

7
8   -- Port clause
9   ((in, "input_conditions", array(boolean, 0, conditions_number-1)),
10    (in, "time_A_value", natural(0, maximal_time_counter)),
11    (in, "time_B_value", natural(0, maximal_time_counter)),
12    (in, "input_arcs_valid", array(boolean, 0, input_arcs_number-1)),
13    (in, "reinit_time", array(boolean, 0, input_arcs_number-1)),
14    (in, "priority_authorizations", array(boolean, 0, input_arcs_number-1)),
15    (out, "fired", boolean))

16
17   -- Internal signals
18   (("s_condition_combination", boolean),
19    ("s_enabled", boolean),
20    ...
21    ("s_time_counter", natural(0, maximal_time_counter)))

22
23   -- Concurrent statements
24   CS

```

LISTING 1.4: The transition design's declarative parts in abstract \mathcal{H} -VHDL syntax.

In Listing 1.4, the type indication of the “transition_type” generic constant has been transformed from the temporal_t enumeration type to the natural(0,2) type. The temporal_t enumeration type, defined through the three values {NOT_TEMPORAL, TEMPORAL_A_A, TEMPORAL_A_B}, is naturally transformed into a natural range. This transformation is only valid because the temporal_t type is only defined and used in the transition design which has a static behavior. Also, the std_logic type defined in the VHDL Std Logic 1164 library [14] is transformed into the Boolean type, and the std_logic_vector is transformed into the array of Booleans type. This transformation is valid because, in the transition and place designs and also in the generated designs, we are only referring to the values '0' and '1' among all the values enumerated by the std_logic type (see [14, p. 2]). Also, note that the clock and reset_n input ports declared in the port clause of the transition design are removed in the hvhdl version. In the \mathcal{H} -VHDL abstract syntax, the if statements that were testing the value of the clock and the reset_n signals have been turned into specific sequential statements (i.e rst, falling and rising blocks). Thus, we don't need the clock and reset_n signals in the port declaration list anymore.

Listing 1.5 presents the translation in \mathcal{H} -VHDL abstract syntax of the two of the processes presented in Listing 1.2.

```

1   process ("condition_evaluation", ("input_conditions"),
2           ("v_internal_condition", boolean)),
3   v_internal_condition := ⊤;
4   (for ("i", 0, conditions_number - 1)
5       (v_internal_condition := v_internal_conditions and input_conditions(i)));

```

```

6      s_condition_combination <= v_internal_condition
7  ) ||
8  process ("firable",("clk"),∅,
9    rst (s_firable <= ⊥)
10   (falling (s_firable <= s_firing_condition))
11 )

```

LISTING 1.5: The condition_evaluation and firable processes in \mathcal{H} -VHDL abstract syntax. The two processes are defined in the behavior of the transition design.

In Listing 1.5, inner blocks of sequential statements are enclosed between parentheses to ease the reading, albeit parentheses are not part of the \mathcal{H} -VHDL syntax. The body of the firable process gives an example of the use of a `rst` block and a falling block. One can see, from the comparison of Listing 1.2 and 1.5, that a `rst ss ss'` statement is the translation of the concrete VHDL statement `if reset_n = '0' then ss else ss' endif;`. Comparing the same listings, a `falling ss` statement is the translation of the concrete VHDL statement `if falling_edge(clock) then ss end if;`.

Listing 1.6 shows the translation in \mathcal{H} -VHDL abstract syntax of the component instantiation statement laid out in Listing 1.3.

```

1  comp (idt, "transition",
2    -- Generic map
3    (transition_type => 0,
4      input_arcs_number => 1,
5      conditions_number => 1,
6      maximal_time_counter => 1),
7    -- Input port map
8    (time_A_value => 0,
9      time_B_value => 0,
10     input_conditions(0) => id0,
11     input_arcs_valid(0) => id1,
12     priority_authorizations(0) => ⊤,
13     reinit_time(0) => id2),
14    -- Output port map
15    (fired => id3)

```

LISTING 1.6: An example of instantiation of the transition design in \mathcal{H} -VHDL abstract syntax. The transition component instance is named id_t .

The statement of Listing 1.6 is almost similar to the one of Listing 1.3. The NOT_TEMPORAL value associated to the `transition_type` constant is turned into 0 (remember the `temporal_t` enumeration type is transformed into a natural range).

1.4 Preliminary definitions

1.4.1 Semantic domains

Let id denote the set of identifiers in the semantic domain. We write $prefix\text{-}id$ to denote arbitrary subsets of the id set. The $type$ and $value$ semantical types are defined as follows:

$type ::= \text{bool} \mid \text{nat}(\text{nat},\text{nat}) \mid \text{array } (type,\text{nat},\text{nat})$

$value ::= \text{bool} \mid \text{nat} \mid \text{array}$

$\text{bool} ::= \text{'T'} \mid \text{'_}'$

$\text{nat} ::= 0 \mid 1 \mid \dots \mid \text{NATMAX}$

$\text{array} ::= (\text{value}^+)$

TABLE 1.2: The $type$ and $value$ semantical types.

In Table 1.2, the $type$ type is in any way similar to the τ entry of the abstract syntax, however, all constraint bounds in the nat and array types have been evaluated to natural numbers. NATMAX denotes the maximum value for a natural number. The NATMAX value depends on the implementation of the VHDL language; NATMAX must at least be equal to $2^{31} - 1$. Note that the array value contains at least one value as an array's index range contains at least one index (that is index 0).

Notation 1 (Partial functions). *Here, we present our notations pertaining to partial functions:*

- The \nrightarrow arrow denotes a partial function.
- The \rightarrow denotes an application (i.e, a total function).
- For all $f \in A \nrightarrow B$, $x \in f$ states that x is in the domain of function f .
- For all $f \in A \nrightarrow B$ and $g \in A \nrightarrow C$, $f \subseteq g$ states that the domain of f is a subset of the domain of g .
- For all $X \subset A$ and $f \in A \nrightarrow B$, $X \subseteq f$ states that X is a subset of the domain of f .

1.4.2 Elaborated design and design state

Now, let us define the structure of an elaborated design which is a structure bound to a given \mathcal{H} -VHDL design and to a design store, i.e a global environment mapping identifiers to \mathcal{H} -VHDL designs. Only the designs referenced into the global design store can be instantiated as component instances in the behavior of a given design. The elaborated design structure is built during the elaboration phase (see Section 1.5). Then, the elaborated design will act as a run-time environment in the expression of the simulation rules. Let $ElDesign(d, \mathcal{D})$ be the set of the elaborated designs for a given \mathcal{H} -VHDL design d and a design store \mathcal{D} . An elaborated design is a composite environment built out of multiple sub-environments. Each sub-environment is a table, represented as a function, mapping identifiers of a certain category of constructs (e.g,

input port identifiers) to their declaration information (e.g, type indication for input ports). We represent an elaborated design as a record where the fields are the sub-environments. An elaborated design is defined as follows:

Definition 1 (Elaborated Design). *For a given \mathcal{H} -VHDL design $d \in \text{design}$ s.t. $d = \text{design } id_e$, id_a gens ports $sigs$ behavior and a given design store $\mathcal{D} \in \text{entity-id} \rightarrow \text{design}$, an elaborated design $\Delta \in ElDesign(d, \mathcal{D})$ is a record $\langle Gens, Ins, Outs, Sigs, Ps, Comps \rangle$ where:*

- $Gens \in \text{generic-id} \rightarrow (\text{type} \times \text{value})$ where $\text{generic-id} = \{id \mid (id, \tau, e) \in \text{gens}\}$, is the partial function yielding the type and the value of generic constants.
- $Ins \in \text{input-id} \rightarrow \text{type}$ where $\text{input-id} = \{id \mid (\text{in}, id, \tau) \in \text{ports}\}$, is the partial function yielding the type of input ports.
- $Outs \in \text{output-id} \rightarrow \text{type}$ where $\text{output-id} = \{id \mid (\text{out}, id, \tau) \in \text{ports}\}$, the partial function yielding the type of output ports.
- $Sigs \in \text{declared-signal-id} \rightarrow \text{type}$ where $\text{declared-signal-id} = \{id \mid (id, \tau) \in \text{sigs}\}$, the partial function yielding the type of declared signals.
- $Ps \in \text{process-id} \rightarrow (\text{variable-id}(id_p) \rightarrow (\text{type} \times \text{value}))$ where $\text{process-id} = \{id_p \mid \text{process}(id_p, sl, vars, ss) \in \text{behavior}\}$, the partial function associating processes to their local environment. Local environments are functions mapping local variable identifiers to their corresponding type and value. Therefore, each set of local variable identifiers $\text{variable-id}(id_p)$ depends on the process identifier (represented by id_p) passed as the first argument of the Ps function.
- $Comps \in \text{component-id} \rightarrow ElDesign(d_e, \mathcal{D})$, where $\text{component-id} = \{id_c \mid \text{comp}(id_c, id_e, gm, ipm, opm) \in \text{behavior}\}$, the partial function mapping component instance ids to their elaborated design version. The set $ElDesign(d_e, \mathcal{D})$ depends on the design d_e from which the component identifier id_c , passed as the first argument of the $Comps$ function, is an instance. Design d_e is retrieved from the design store \mathcal{D} s.t. $d_e = \mathcal{D}(id_e)$.

We assume that there are no overlapping between the identifiers of the sub-environments (i.e, an identifier belongs to at most one sub-environment). When there is no ambiguity, we write $\Delta(x)$ to denote the value returned for identifier x , where x is looked up in the appropriate field of Δ . We write $x \in \Delta$ to state that identifier x is defined in one of Δ 's fields. We note $\Delta(x) \leftarrow v$ the overriding of the value associated to identifier x with value v in the appropriate field of Δ , $\Delta \cup (x, v)$ to note the addition the mapping from identifier x to value v in the appropriate field of Δ , that assuming $x \notin \Delta$. We write $x \in \mathcal{F}(\Delta)$, where \mathcal{F} is a field of Δ , when more precision is needed regarding the lookup of identifier x in the record Δ .

Let $\Sigma(\Delta)$ be the set of design states for a given elaborated design Δ . A design state of Δ is defined as follows:

Definition 2 (Design state). *A design state $\sigma \in \Sigma(\Delta)$, for a given design $d \in \text{design}$, a given design store \mathcal{D} and an elaborated design $\Delta \in ElDesign(d, \mathcal{D})$, is a record $\langle \mathcal{S}, \mathcal{C}, \mathcal{E} \rangle$ where:*

- $\mathcal{S} \in \text{signal-id} \rightarrow \text{value}$, the partial function yielding the current values of the design's signals (ports and declared signals).

- $\mathcal{C} \in \text{component-id} \rightarrow \Sigma(\Delta_c)$, the partial function yielding the current state of design's component instances, where $\Delta_c = \Delta(id_c)$ and $id_c \in \text{component-id}$ is the component identifier passed to function \mathcal{C} .
- $\mathcal{E} \subseteq \text{signal-id} \sqcup \text{component-id}$, the set of signal and component instance identifiers that generated an event at the considered design state.

The *signal-id* subset is the disjoint union of *input-id*, *output-id* and *declared-signal-id*. We use $\sigma(id)$ to denote the value associated to an identifier in the signal store \mathcal{S} or in the component store \mathcal{C} fields. When there is no ambiguity, we write $id \in \sigma$ to state that an identifier is defined in either the signal store \mathcal{S} or the component store \mathcal{C} fields. Also, when there is no ambiguity, we rely on indices or exponents to qualify the signal store, the component instance store and the set of events of a given design state. For instance, \mathcal{C}_0 denotes the component instance store of design state σ_0 , and \mathcal{E}' denotes the set of events of design state σ' , etc.

Notation 2 (No events design state). *For a given \mathcal{H} -VHDL design d , a design store \mathcal{D} , and an elaborated design $\Delta \in \text{ElDesign}(d, \mathcal{D})$, the function $\text{NoEv} \in \Sigma(\Delta) \rightarrow \Sigma(\Delta)$ returns a design state similar to the one passed in parameter only with an empty set of events. I.e, for all design state $\sigma \in \Sigma(\Delta)$ s.t. $\sigma = \langle \mathcal{S}, \mathcal{C}, \mathcal{E} \rangle$, $\text{NoEv}(\sigma) = \langle \mathcal{S}, \mathcal{C}, \emptyset \rangle$.*

1.5 Elaboration rules

The goal of the elaboration phase is to build an elaborated design Δ along with a *default* state σ_e , out of a \mathcal{H} -VHDL design d . The elaboration relation also covers type-checking operations for the declarative and behavioral parts of design d . Even though the elaboration of a design is described in the LRM, the formalization of this phase has been performed in few works only [2, 8, 24], and never in a setting that covers both syntactical well-formedness and type-checking of the designs. We are interested in the formalization of the elaboration phase because we are interested in the *well-formedness* of the programs generated by the HILECOP transformation. Here, the term *well-formedness* refers to a syntactically valid design, w.r.t. the syntactic rules of the VHDL language, and to a well-typed design, w.r.t. the typing rules defined in the LRM. Formalizing the elaboration phase is also a way to define how the runtime environment and the runtime state of the simulation are built. For now, we haven't tackle down the proof that the \mathcal{H} -VHDL designs generated by HILECOP are elaborable, i.e. syntactically well-formed and well-typed. As explained in Chapter ??, this task is foreseen in our work perspectives. Contrary to what is prescribed in the LRM [13, p. 166], we are not dealing with the transformation of the component instantiation statements into block statements in our formalization of the elaboration phase. We prefer to preserve the hierarchical structure of the design (i.e. its composite structure) during its elaboration. We argue that dealing with component instantiation statements instead of block statements does not complexify the semantics of the \mathcal{H} -VHDL simulation rules.

In the following sections describing the elaboration and the simulation rules of the \mathcal{H} -VHDL semantics, the green frames adds explanations about the premises of the rules and the ref frames brings explanations about the side conditions of the rules.

1.5.1 Design elaboration

Component instances possibly define the behavior of a design. Each component instance declares the entity identifier that points out to the specific design being instantiated. Therefore, for each instantiation, the associated design must be known through the definition of a global design declaration environment called a *design store*. A design store is defined as follows:

Definition 3 (Design store). *A design store $\mathcal{D} \in \text{entity-id} \rightarrow \text{design}$ is the partial function mapping design identifiers (i.e. the entity identifier of designs) to their corresponding representation in abstract syntax. As a prerequisite to the elaboration of HILECOP-generated designs (i.e., resulting from the transformation of a SITPN into an \mathcal{H} -VHDL design), a particular design store $\mathcal{D}_{\mathcal{H}}$ is defined. Design store $\mathcal{D}_{\mathcal{H}}$ holds the bindinds between the transition and place entity identifiers (i.e. "transition" and "place") and the description of the place and transition designs:*

$$\mathcal{D}_{\mathcal{H}} := \{ ("transition", \text{design } "transition" \text{ "transition_architecture" } \text{gens}_t \text{ ports}_t \text{ sigs}_t \text{ cs}_t), \\ ("place", \text{design } "place" \text{ "place_architecture" } \text{gens}_p \text{ ports}_p \text{ sigs}_p \text{ cs}_p) \}$$

The full definition of the place and transition designs in abstract syntax are given in Appendices A and B.

At the beginning of the elaboration phase, a function $\mathcal{M}_g \in \text{generic-id} \rightarrow \text{value}$ mapping the top-level design's generic constants to values is passed as an element of the environment. The \mathcal{M}_g function is referred to as the *dimensioning* function.

$$\begin{array}{c} \text{DESIGNELAB} \\ \Delta_{\emptyset}, \mathcal{M}_g \vdash \text{gens} \xrightarrow{\text{egens}} \Delta \\ \Delta, \sigma_{\emptyset} \vdash \text{ports} \xrightarrow{\text{eports}} \Delta', \sigma \\ \Delta', \sigma \vdash \text{sigs} \xrightarrow{\text{esigs}} \Delta'', \sigma' \\ \Delta'', \sigma' \vdash \text{cs} \xrightarrow{\text{ebeh}} \Delta''', \sigma'' \\ \hline \mathcal{D}, \Delta''' \vdash \text{design id}_e \text{ id}_a \text{ gens ports sigs cs} \xrightarrow{\text{elab}} \Delta''', \sigma'' \end{array}$$

where Δ_{\emptyset} denotes an empty elaborated design, that is an elaborated design initialized with empty fields (empty tables). In the same manner, σ_{\emptyset} denotes an empty design state. The effect of the *egens*, *eports*, *esigs* and *ebeh* that respectively deal with the elaboration of the generic constants, the ports, the architecture declarative part and the behavioral part of the design, are explicated in the following sections.

Example of a design elaboration

The elaborated design and the default design state resulting of the elaboration of the transition design for a given dimensioning function \mathcal{M} are the presented through the Δ and σ_e structures in Figures 1.6 and 1.7. The value of the dimensioning function \mathcal{M} is the set of couples $\{("transition_type", 2), ("conditions_number", 2), ("input_arcs_number", 4)\}$.

```


$$\Delta := \{$$

  
$$Gens := \{("transition\_type", (nat(0,2),2)),$$

    
$$("conditions\_numbers", (nat(0,NATMAX),2))$$

    
$$("input\_arcs\_number", (nat(0,NATMAX),4))$$

    
$$("maximal\_time\_counter", (nat(0,NATMAX),1)))\},$$

  
$$Ins := \{("input\_conditions", array(bool,0,1)),$$

    
$$("time\_A\_value", nat(0,1)),$$

    
$$("time\_B\_value", nat(0,1)),$$

    
$$("input\_arcs\_valid", array(bool,0,3)),$$

    
$$("reinit\_time", array(bool,0,3)),$$

    
$$("priority\_authorizations", array(bool,0,3)))\},$$

  
$$Outs := \{("fired", bool)\}$$

  
$$Sigs := \{("s\_condition\_combination", bool),$$

    
$$("s\_enabled", bool),$$

    
$$("s\_time\_counter", nat(0,1)))\},$$

  
$$Ps := \{("condition\_evaluation", \{("v\_internal\_condition", (bool, \perp))\}),$$

    
$$("firable", \emptyset)\}$$

  
$$Comps := \emptyset$$


$$\}$$


```

FIGURE 1.6: An elaborated version of the transition design; the sub-environments of the elaborated design structure (i.e. functions) are represented by sets of couples.

For the sake of conciseness, Figure 1.6 gives only a part of the *Sigs* and *Ps* sub-environments resulting from the elaboration of the transition design. In Figure 1.6, the generic constants of the transition design received their values from the dimensioning function \mathcal{M} . As it is not defined in the domain of \mathcal{M} , the *maximal_time_counter* generic constant is associated with its default value. Also, all the types associated with ports and internal signals have been *resolved*; i.e. the expressions qualifying the upper and lower bound of ranges, in the definition of natural range types or array types, have been evaluated. Due to the presence of generic constant identifiers in the expression of type ranges, we had to wait for the generic constants to receive a value. For example, *array(boolean, 0, conditions_number-1)* is the type indication associated with the *input_conditions* input port. The dimensioning function sets the value of the *conditions_number* generic constant to 2. After elaboration, the type indication *array(boolean, 0, conditions_number-1)* is transformed into the type *array(bool,0,1)*. The *Ps* sub-environment associates each process identifier to a local environment, i.e. a mapping between local variables declared in the process and a couple (*type, value*). In a local environment, each local variable has an initial value corresponding to the implicit default value of its type (see Section 1.5.7). The behavior of the transition design is set with processes only. Thus, the *Comps* sub-environment, that maps each component instance identifier to an elaborated

design structure, is empty.

Figure 1.7 shows the default design state σ_e of Δ . In the default design state of an elaborated design, the value of all signals corresponds to the implicit default value of signals (i.e. deduced from the type of signals, see Section 1.5.7).

$$\begin{aligned} \sigma_e := & \{ \\ & \mathcal{S} := \{ ("input_conditions", (\perp, \perp)), \\ & ("time_A_value", 0), \\ & ("time_B_value", 0), \\ & ("input_arcs_valid", (\perp, \perp, \perp)), \\ & ("reinit_time", (\perp, \perp, \perp)), \\ & ("priority_authorizations", (\perp, \perp, \perp)), \\ & ("fired", \perp), \\ & ("s_condition_combination", \perp), \\ & ("s_enabled", \perp), \\ & ("s_time_counter", 0) \}, \\ & \mathcal{C} := \emptyset \\ & \mathcal{E} := \emptyset \\ & \} \end{aligned}$$

FIGURE 1.7: The default design state associated built during the elaboration phase along the elaborated design of Figure 1.6. We use values enclosed between parentheses to represent array values.

The component store of design state σ_e is empty as there are no component instances defining the behavior of the transition design. Also, the set of events of a default design state is always empty.

1.5.2 Generic clause elaboration

The *e*gens relation elaborates a list of generic constant declarations.

Premises

- $e\text{type}_g$ transforms a type indication, specifically attached to a generic constant declaration, into a *type* instance and checks its well-formedness (see Section 1.5.5).
- The *e* relation links an expression *e* to its value *v* in a given context (see Section 1.6.9). The context of evaluation for an expression is composed of a given elaborated design, a given design state, and given local environment. We omit symbols at the left of the thesis when they refer to empty structures. For instance, $\vdash e \xrightarrow{e} v$ is a notation for $\Delta_\emptyset, \sigma_\emptyset, \Lambda_\emptyset \vdash e \xrightarrow{e} v$.
- SE_l states that an expression is *locally static* (see Section 1.5.9).

- $v \in_c T$ and $\mathcal{M}(\text{id}_g) \in_c T$ checks that the default value and the value of yielded by the dimensioning function belongs to the type of the declared generic constant (see Section 1.5.8).

Side conditions

The expression $\text{id}_g \in \Delta$ checks that the generic constant identifier id_g is not already defined in the *Gens* sub-environment of the elaborated design Δ .

GENELABDIMEN

$$\frac{\vdash \tau \xrightarrow{e\text{type}_g} T \quad \vdash e \xrightarrow{e} v \quad SE_l(e) \quad \mathcal{M}(\text{id}_g) \in_c T \quad \begin{array}{l} v \in_c T \\ \text{id}_g \notin \Delta \end{array}}{\Delta, \mathcal{M} \vdash (\text{id}_g, \tau, e) \xrightarrow{egens} \Delta \cup (\text{id}_g, (T, \mathcal{M}(\text{id}_g))) \quad \text{id}_g \in \mathcal{M}}$$

The GENELABDEFAULT states that the value of declared generic constant is defined by its default value when no value is specified by the dimensioning function \mathcal{M} .

GENELABDEFAULT

$$\frac{\vdash \tau \xrightarrow{e\text{type}_g} T \quad \vdash e \xrightarrow{e} v \quad SE_l(e) \quad v \in_c T \quad \text{id}_g \notin \Delta}{\Delta, \mathcal{M} \vdash (\text{id}_g, \tau, e) \xrightarrow{egens} \Delta \cup (\text{id}_g, (T, v)) \quad \text{id}_g \notin \mathcal{M}}$$

GENELABCOMP

$$\frac{\Delta, \mathcal{M} \vdash \text{gdecl} \xrightarrow{egens} \Delta' \quad \Delta', \mathcal{M} \vdash \text{gens} \xrightarrow{egens} \Delta''}{\Delta, \mathcal{M} \vdash \text{gdecl, gens} \xrightarrow{egens} \Delta''}$$

1.5.3 Port clause elaboration

The *eports* relation elaborates each port declaration defined in a design's port clause. For each port declaration, the *eports* relation transforms the port's type indication into a semantic type and retrieves the implicit default value of this type. Then, the *eports* relation adds the binding between the input (resp. output) port identifier and its type to the *Ins* (resp. *Outs*) sub-environment of the elaborated design structure Δ . It also adds the binding between the input (resp. output) port identifier and its implicit default value to the default design state σ .

Premises

- The *eotype* relation associates a type indication to its corresponding semantic type and checks its well-formedness (see Section 1.5.5).
- The *defaultv* relation associates a given semantic type to its implicit *default* value.

$$\text{INPORTELAB} \quad \frac{\Delta \vdash \tau \xrightarrow{\text{etype}} T \quad \Delta \vdash T \xrightarrow{\text{defaultv}} v}{\Delta, \sigma \vdash (\text{in}, \text{id}, \tau) \xrightarrow{\text{eports}} \Delta \cup (id, T), \sigma \cup (id, v)} \quad \begin{array}{l} \text{id} \notin \Delta \\ \text{id} \notin \sigma \end{array}$$

$$\text{OUTPORTELAB} \quad \frac{\Delta \vdash \tau \xrightarrow{\text{etype}} T \quad \Delta \vdash T \xrightarrow{\text{defaultv}} v}{\Delta, \sigma \vdash (\text{out}, \text{id}, \tau) \xrightarrow{\text{eports}} \Delta \cup (id, T), \sigma \cup (id, v)} \quad \begin{array}{l} \text{id} \notin \Delta \\ \text{id} \notin \sigma \end{array}$$

$$\text{PORTELABCOMP} \quad \frac{\Delta, \sigma \vdash \text{pdecl} \xrightarrow{\text{eports}} \Delta', \sigma' \quad \Delta', \sigma' \vdash \text{ports} \xrightarrow{\text{eports}} \Delta'', \sigma''}{\Delta, \sigma \vdash \text{pdecl, ports} \xrightarrow{\text{eports}} \Delta'', \sigma''}$$

1.5.4 Architecture declarative part elaboration

The *esigs* relation elaborates each internal signal declaration defined in the declarative part of a design's architecture. For each signal declaration, the *esigs* relation transforms the signal's type indication into a semantic type and retrieves the implicit default value of this type. Then, the *esigs* relation adds the binding between the signal identifier and its type to the *Sigs* sub-environment of the elaborated design structure Δ . It also adds the binding between the signal identifier and its implicit default value to the default design state σ .

$$\text{SIGELAB} \quad \frac{\Delta \vdash \tau \xrightarrow{\text{etype}} T \quad \Delta \vdash T \xrightarrow{\text{defaultv}} v}{\Delta, \sigma \vdash (\text{id}, \tau) \xrightarrow{\text{esigs}} \Delta \cup (id, T), \sigma \cup (id, v)} \quad \begin{array}{l} \text{id} \notin \Delta \\ \text{id} \notin \sigma \end{array}$$

$$\text{SIGELABCOMP} \quad \frac{\Delta, \sigma \vdash \text{sdecl} \xrightarrow{\text{esigs}} \Delta', \sigma' \quad \Delta', \sigma' \vdash \text{sigs} \xrightarrow{\text{esigs}} \Delta'', \sigma''}{\Delta, \sigma \vdash \text{sdecl, sigs} \xrightarrow{\text{esigs}} \Delta'', \sigma''}$$

1.5.5 Type indication elaboration

The *etype* relation checks the well-formedness of a type indication τ , and transforms it into a semantic type (as defined in Table 1.2). A type indication τ is well-formed in the context Δ if τ denotes the boolean keyword or the nat or array keywords with a *well-formed* constraint, and a well-formed element type in the array case.

$$\text{ETYPEBOOL} \quad \frac{}{\Delta \vdash \text{boolean} \xrightarrow{\text{etype}} \text{bool}}$$

$$\text{ETYPENAT} \quad \frac{\Delta \vdash (\text{e}, \text{e}') \xrightarrow{\text{econstr}} (\text{v}, \text{v}')}{\Delta \vdash \text{natural}(\text{e}, \text{e}') \xrightarrow{\text{etype}} \text{nat}(\text{v}, \text{v}')}$$

$$\text{ETYPEARRAY} \quad \frac{\Delta \vdash \tau \xrightarrow{\text{etype}} T \quad \Delta \vdash (e, e') \xrightarrow{\text{econstr}} (v, v')}{\Delta \vdash \text{array}(\tau, e, e') \xrightarrow{\text{etype}} \text{array}(T, v, v')}$$

The *econstr* relation checks that a constraint is well-formed and evaluates the constraint bounds. A constraint is well-formed in the context Δ if:

- its bounds are globally static expressions [13, p.36] of the nat type.
- its lower bound value is inferior or equal to its upper bound value.

Remark 1 (Type of constraints). As the VHDL language reference stays unclear about the type of range and index constraints [13, p.33], we add the restriction that range and index constraints must have bounds of the nat type (i.e. value of type nat).

Premises

- The \in_c relation states that a given value conforms to a given type (see Section 1.5.5).
- The SE_g relation states that an expression is *globally* static (see Section 1.5.9).

$$\text{ECONSTR} \quad \frac{\Delta \vdash SE_g(e) \quad \Delta \vdash e \xrightarrow{e} v \quad v \in_c \text{nat}(0, \text{NATMAX}) \quad \Delta \vdash SE_g(e') \quad \Delta \vdash e' \xrightarrow{e'} v' \quad v' \in_c \text{nat}(0, \text{NATMAX})}{\Delta \vdash (e, e') \xrightarrow{\text{econstr}} (v, v')} \quad v \leq v'$$

When considering a type indication in a generic constant declaration, the definition of well-formedness differs slightly from the general definition. A type indication τ associated to a generic constant declaration is well-formed if τ denotes the boolean keyword, or the nat keyword with a *well-formed* constraint. A generic constant can not be associated with a composite type indication (i.e. an array type). The etype_g relation is specially defined to check the well-formedness of a type indication associated with a generic constant declaration.

$$\text{ETYPEGBOOL} \quad \frac{}{\vdash \text{boolean} \xrightarrow{\text{etype}} \text{bool}} \quad \text{ETYPEGNAT} \quad \frac{\Delta \vdash (e, e') \xrightarrow{\text{econstr}_g} (v, v')}{\vdash \text{natural}(e, e') \xrightarrow{\text{etype}} \text{nat}(v, v')}$$

The econstr_g relation checks that a *generic* constraint (i.e. a constraint appearing in a type indication associated with a generic constant declaration) is well-formed and evaluates the constraint bounds. A *generic* constraint is well-formed if:

- its bounds are locally static expressions [13, p.36] of the nat type.
- its lower bound value is inferior or equal to its upper bound value.

$$\text{ECONSTRG} \quad \frac{\begin{array}{c} SE_l(e) \vdash e \xrightarrow{e} v \quad v \in_c \text{nat}(0, \text{NATMAX}) \\ SE_l(e') \vdash e' \xrightarrow{e} v' \quad v' \in_c \text{nat}(0, \text{NATMAX}) \end{array}}{\vdash (e, e') \xrightarrow{econstr_g} (v, v')} \quad v \leq v'$$

1.5.6 Behavior elaboration

The *ebeh* relation elaborates each concurrent statement composing the behavioral part of a design's architecture.

Elaboration of concurrent statements

The elaboration of the composition of concurrent statements is performed in a sequential manner.

$$\text{CSPARELAB} \quad \frac{\mathcal{D}, \Delta, \sigma \vdash \text{cs} \xrightarrow{ebeh} \Delta', \sigma' \quad \mathcal{D}, \Delta', \sigma' \vdash \text{cs}' \xrightarrow{ebeh} \Delta'', \sigma''}{\mathcal{D}, \Delta, \sigma \vdash \text{cs} || \text{cs}' \xrightarrow{ebeh} \Delta'', \sigma''} \quad \text{CSNULLELAB} \quad \frac{}{\mathcal{D}, \Delta, \sigma \vdash \text{null} \xrightarrow{ebeh} \Delta, \sigma}$$

Process statement elaboration

To elaborate a process statement, the *ebeh* relation associates the process identifier to a local environment. The *ebeh* builds the local environment from the process's local variable declaration list (see the *evars* relation). The *ebeh* relation also checks that the sequential statements composing the body of the process are well-typed (see the *valid_{ss}* relation in Section 1.5.11).

Premises

The *valid_{ss}* relation states that a sequential statement is well-typed in the context Δ, σ, Λ . During the elaboration of a process contained in the behavioral part of a design, Δ represents the elaborated design structure being built, σ is the default design state being built, and Λ is the local variable environment deduced from the elaboration of the process declarative part.

Side conditions

$sl \subseteq Ins(\Delta) \cup Sigs(\Delta)$ indicates that the sensitivity list sl must only contain signal identifiers that are readable, that is, *input* ports and declared signals.

PSELAB

$$\frac{\Delta, \Lambda_\emptyset \vdash \text{vars} \xrightarrow{evars} \Lambda \quad \Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(\text{ss}) \quad id_p \notin \Delta}{\mathcal{D}, \Delta, \sigma \vdash \text{process } (id_p, sl, \text{vars}, \text{ss}) \xrightarrow{ebeh} \Delta \cup (id_p, \Lambda), \sigma \quad sl \subseteq Ins(\Delta) \cup Sigs(\Delta)}$$

Process declarative part elaboration

The $evars$ relation builds a local environment out of a process declarative part.

$$\text{VARELAB} \quad \frac{\Delta \vdash \tau \xrightarrow{etyp} T \quad \vdash T \xrightarrow{defaultv} v \quad id \notin \Lambda}{\Delta, \Lambda \vdash (id, \tau) \xrightarrow{evars} \Lambda \cup (id, (T, v)) \quad id \notin \Delta}$$

$$\text{VARELABCOMP} \quad \frac{\Delta, \Lambda \vdash \text{vdecl} \xrightarrow{evars} \Lambda' \quad \Delta, \Lambda' \vdash \text{vars} \xrightarrow{evars} \Lambda''}{\Delta, \Lambda \vdash \text{vdecl, vars} \xrightarrow{evars} \Lambda''}$$

Component instantiation statement elaboration

To elaborate a component instantiation statement, the $ebeh$ relation first builds a dimensioning function \mathcal{M} out of the component instance generic map. Then, the design associated with the entity identifier declared by the component instance (i.e. id_e) is looked up and retrieved from the design store \mathcal{D} . Then, the $ebeh$ relation appeals to the $elab$ relation to build an elaborated version Δ_c and a default design state δ_c for the retrieved design given the specific dimensioning function \mathcal{M} . Consequently, the definition of the $elab$ and $ebeh$ relations is mutually recursive.

Premises

- The $emapg$ relation builds a function $\mathcal{M} : \text{generic-id} \nrightarrow \text{value}$ out of a generic map (see definition below).
- valid_{ipm} (resp. valid_{opm}) states that an input port map (resp. output port map) is valid, i.e well-formed and well-typed (see Section 1.5.10).

Side conditions

$\mathcal{M} \subseteq Gens(\Delta_c)$ checks that the generic map $gmap$ contains references to known generic constant identifiers only.

COMPELAB

$$\frac{\begin{array}{c} \mathcal{M}_\emptyset \vdash \text{gmap} \xrightarrow{\text{emapg}} \mathcal{M} \\ \mathcal{D}, \mathcal{M} \vdash \mathcal{D}(\text{id}_e) \xrightarrow{\text{elab}} \Delta_c, \sigma_c \quad \Delta, \Delta_c, \sigma \vdash \text{valid}_{ipm}(\text{i}) \\ \Delta, \Delta_c \vdash \text{valid}_{opm}(\text{o}) \end{array}}{\mathcal{D}, \Delta, \sigma \vdash \text{comp} (\text{id}_c, \text{id}_e, \text{g}, \text{i}, \text{o}) \xrightarrow{\text{ebeh}} \Delta \cup (\text{id}_c, \Delta_c), \sigma \cup (\text{id}_c, \sigma_c)} \quad \begin{array}{l} \text{id}_c \notin \Delta, \text{id}_c \notin \sigma \\ \text{id}_e \in \mathcal{D} \\ \mathcal{M} \subseteq \text{Gens}(\Delta_c) \end{array}$$

A port map is a mapping between expressions and signals coming from an embedding design (Δ) and ports of an internal component instance (Δ_c). The formal part of an port map entry (i.e, left of the arrow) belongs to the internal component, whereas the actual part (i.e, right of the arrow) refers to the embedding design. Therefore, we need both Δ and Δ_c to verify if a port map is well-typed leveraging the valid_{pm} predicate.

Remark 2 (Valid generic map). Note that we are not checking the validity of the generic map. In case of an ill-formed generic map, a inconsistent mapping \mathcal{M} is generated by the emapg that will make the elab relation, taking \mathcal{M} as a parameter, never derivable. Therefore, the elab relation does an implicit validity check on the generic map.

The emap_g relation builds a dimensioning function out of generic map.

$$\frac{\begin{array}{c} \text{ASSOCGELAB} \\ SE_l(e) \vdash e \xrightarrow{e} v \end{array}}{\mathcal{M} \vdash \text{id}_g \Rightarrow e \xrightarrow{\text{emapg}} \mathcal{M} \cup (\text{id}_g, v)} \quad \text{id}_g \notin \mathcal{M} \quad \frac{\begin{array}{c} \text{GMAPELABCOMP} \\ \mathcal{M} \vdash \text{assoc}_g \xrightarrow{\text{emapg}} \mathcal{M}' \quad \mathcal{M}' \vdash \text{gmap} \xrightarrow{\text{emapg}} \mathcal{M}'' \end{array}}{\mathcal{M} \vdash \text{assoc}_g, \text{gmap} \xrightarrow{\text{emapg}} \mathcal{M}''}$$

An assoc_g entry doesn't allow indexed identifiers in its formal part, due to the restriction of generic constants to scalar types. Note that this restriction is not imposed by the LRM. We choose to adopt this simplification of the VHDL syntax since the case of generic constants with composite types is never encountered in the HILECOP VHDL programs.

Example of component instantiation statement elaboration

The following rule describes the elaboration of the transition component instance presented Listing 1.6. Here, Δ represents the (partially-built) elaborated version of the design that contains the transition component instance id_t in its behavior. σ represents the (partially-built) default state of the same embedding design. Due to the size of definitions, the generic map (resp. the input port and output port map) of the transition component instance id_t is aliased by g_t (resp. i_t and o_t) (see Listing 1.6 for the full definitions).

$$\frac{\begin{array}{c} \mathcal{M}_\emptyset \vdash \text{g}_t \xrightarrow{\text{emapg}} \mathcal{M} \\ \mathcal{D}, \mathcal{M} \vdash \mathcal{D}_{\mathcal{H}}("transition") \xrightarrow{\text{elab}} \Delta_t, \sigma_t \quad \Delta, \Delta_t, \sigma \vdash \text{valid}_{ipm}(\text{i}_t) \\ \Delta, \Delta_t \vdash \text{valid}_{opm}(\text{o}_t) \end{array}}{\mathcal{D}_{\mathcal{H}}, \Delta, \sigma \vdash \text{comp} (\text{id}_t, "transition", \text{g}_t, \text{i}_t, \text{o}_t) \xrightarrow{\text{ebeh}} \Delta \cup (\text{id}_t, \Delta_t), \sigma \cup (\text{id}_t, \sigma_t)} \quad \begin{array}{l} \text{id}_t \notin \Delta, \text{id}_t \notin \sigma \\ "transition" \in \mathcal{D}_{\mathcal{H}} \\ \mathcal{M} \subseteq \text{Gens}(\Delta_t) \end{array}$$

where:

- $\mathcal{M} := \{("transition_type", 0), ("input_arcs_number", 1), ("conditions_number", 1), ("maximal_time_counter", 1)\}$
- $\mathcal{D}_{\mathcal{H}}("transition") := \text{design } "transition" \text{ "transition_architecture" } g_{st} \text{ } p_{st} \text{ } s_{st} \text{ } c_{st}$
- $G_{st}(\Delta_t) := \{("transition_type", nat(0, 2)), ("input_arcs_number", nat(0, NATMAX)), ("conditions_number", nat(0, NATMAX)), ("maximal_time_counter", nat(0, NATMAX))\}$

Then, the transition design declaration is retrieved from the design store $\mathcal{D}_{\mathcal{H}}$, which is the specific HILECOP design store. By definition, the HILECOP design store maps the transition and the place identifiers to their corresponding design declaration (the side condition " $transition \in \mathcal{D}_{\mathcal{H}}$ " is true). Then, the *elab* relation builds the elaborated design Δ_t and the default design state σ_t from the transition design declaration given the dimensioning function \mathcal{M} . We do not detail the content of Δ_t and σ_t as it is really close to the content of Figures 1.6 and 1.7. Finally, a mapping between the identifier id_t and Δ_t is added to the *Comps* sub-environment of Δ , i.e. $\Delta \cup (id_t, \Delta_t)$. Also, a mapping between the identifier id_t and the default state σ_t is added to the component store \mathcal{C} of σ , i.e. $\sigma \cup (id_t, \sigma_t)$.

1.5.7 Implicit default value

According to the VHDL reference, when declaring a port, a signal or a variable, these items must receive an implicit default value depending on their types [13, p.61, 64, 173]. The *defaultv* relation determines the default value for a given type.

$$\frac{\text{DEFAULTVBOOL}}{\text{bool} \xrightarrow{\text{defaultv}} \perp} \quad \frac{\text{DEFAULTVCNAT} \quad n \leq m}{nat(n, m) \xrightarrow{\text{defaultv}} n}$$

$$\frac{\text{DEFAULTVCARR}}{T \xrightarrow{\text{defaultv}} v} \frac{}{array(T, n, m) \xrightarrow{\text{defaultv}} \text{create_array}(size, T, v)} \quad \begin{matrix} n \leq m \\ size = (m - n) + 1 \end{matrix}$$

`create_array(size, T, v)` creates an array of size *size*, containing elements of type *T*, where each element is initialized with the value *v*.

1.5.8 Typing relation

The typing relation \in_c checks that a given value conforms to a given type.

$$\frac{\text{IsBOOL}}{b \in \mathbb{B}} \quad b \in \mathbb{B} \quad \frac{\text{IsCNAT}}{n \in_c nat(l, u)} \quad n \in [l, u] \quad \frac{\text{ARRAY}}{v_i \in_c T} \quad i = 1, \dots, n$$

$$\Delta \vdash (v_1, \dots, v_n) \in_c array(T, l, u) \quad n = (u - l) + 1$$

1.5.9 Static expressions

Static expressions are either locally static or globally static; the LRM defines locally static and globally static expressions as follows.

Locally static expressions

An expression is *locally* static if:

- It is composed of operators and operands of a *scalar* type (i.e, natural or boolean).
- It is a *literal* of a scalar type.

The SE_l relation, defined by the following rules, states that an expression is locally static.

$$\frac{\text{LSENAT}}{SE_l(n)} \quad n \in \mathbb{N} \quad \frac{\text{LSEBOOL}}{SE_l(b)} \quad b \in \mathbb{B} \quad \frac{\text{LSENAT}}{SE_l(\text{not } e)} \quad \frac{\text{LSEBINOP}}{SE_l(e) \quad SE_l(e')} \quad op \in \{ +, -, =, \neq, <, \leq, >, \geq, \text{and}, \text{or} \}$$

Globally static expressions

An expression is *globally* static in the context Δ if:

- It is a generic constant.
- It is an array aggregate composed of globally static expressions.
- It is a locally static expression.

The SE_g relation, defined by the following rules, checks that an expression is globally static in a given context Δ .

$$\frac{\text{GSELOCAL}}{SE_l(e)} \quad \frac{\text{GSEGEN}}{\Delta \vdash SE_g(id_g)} \quad id_g \in Gens(\Delta) \quad \frac{\text{GSEAGGREGATE}}{\Delta \vdash SE_g((e_1, \dots, e_n))} \quad i = 1, \dots, n$$

1.5.10 Valid port map

Valid input port map

The valid_{ipm} predicate states that an *input* port map is valid in the context Δ, Δ_c , where Δ is the embedding design structure and Δ_c denotes the component instance owner of the input port map, if:

- All ports defined in Δ_c are exactly mapped once in the input port map.
- For each input port map entry, the formal and actual part are of the same type.

Premises

- $list_{ipm}$ builds a set $\mathcal{L} \subset id \sqcup (id \times \mathbb{N})$ out of the input port map.
- check_{pm} checks the validity of a port map based on the corresponding port list (here, the input ports of Δ_c) and the set built by the $list_{ipm}$ relation.

$$\begin{array}{c} \text{VALIDIPM} \\ \Delta, \Delta_c, \sigma, \mathcal{L}_\emptyset \vdash \text{ipmap} \xrightarrow{list_{ipm}} \mathcal{L} \quad \text{check}_{pm}(\text{Ins}(\Delta_c), \mathcal{L}) \\ \hline \Delta, \Delta_c, \sigma \vdash \text{valid}_{ipm}(\text{ipmap}) \end{array}$$

The $list_{ipm}$ relation builds a set of identifiers and couples (identifier, natural number) collected from the identifiers and indexed identifiers in the formal part (i.e. at the left of the association arrow) of an input port map. It also checks, for each association of the input port map, that the expression of the actual part are of the same type than the identifier or indexed identifier of the formal part.

Side conditions

- $\text{id}_f \in \text{Ins}(\Delta_c)$ checks that the identifier id_f is an input port identifier of Δ_c .
- $\text{id}_f \notin \mathcal{L}$ checks that the port identifier id_f is not already mapped, i.e. it is not already referenced in the \mathcal{L} set.

LISTIPMSIMPLE

$$\frac{\Delta, \sigma \vdash e \xrightarrow{e} v \quad v \in_c T \quad \text{id}_f \notin \mathcal{L}, \text{id}_f \in \text{Ins}(\Delta_c) \quad \Delta_c(\text{id}_f) = T}{\Delta, \Delta_c, \sigma, \mathcal{L} \vdash \text{id}_f \Rightarrow e \xrightarrow{list_{ipm}} \mathcal{L} \cup \{\text{id}_f\}}$$

Premises

$v_i \in_c nat(n, m)$ checks that the index value stays in the array bounds.

Side conditions

$id_f \notin \mathcal{L}$ and $(id_f, v_i) \notin \mathcal{L}$ checks that neither the port identifier id_f nor the couple port identifier id_f and index v_i are already mapped.

LISTIPMPARTIAL

$$\frac{SE_l(e_i) \quad \begin{array}{c} \vdash e_i \xrightarrow{e} v_i \\ \Delta, \sigma \vdash e \xrightarrow{e} v \\ v \in_c T \end{array} \quad \begin{array}{c} v_i \in_c nat(n, m) \\ id_f \notin \mathcal{L}, (id_f, v_i) \notin \mathcal{L} \\ id_f \in Ins(\Delta_c) \\ \Delta_c(id_f) = array(T, n, m) \end{array}}{\Delta, \Delta_c, \sigma, \mathcal{L} \vdash id_f(e_i) \Rightarrow e \xrightarrow{list_{ipm}} \mathcal{L} \cup \{ (id_f, v_i) \}}$$

LISTIPMCONS

$$\frac{\Delta, \Delta_c, \sigma, \mathcal{L} \vdash assoc_{ip} \xrightarrow{list_{ipm}} \mathcal{L}' \quad \Delta, \Delta_c, \sigma, \mathcal{L}' \vdash ipmap \xrightarrow{list_{ipm}} \mathcal{L}''}{\Delta, \Delta_c, \sigma, \mathcal{L} \vdash assoc_{ip}, ipmap \xrightarrow{list_{ipm}} \mathcal{L}''}$$

The $check_{pm}(Ports, \mathcal{L})$ predicate states that all port identifiers referenced in the domain of $Ports \in id \rightsquigarrow type$ appear in \mathcal{L} as a simple identifier, or if the port identifier is of type array, then all couples (id, i) must belong to \mathcal{L} , where i denotes all indexes of the array range and id , the port id.

$$\begin{aligned} check_{pm}(Ports, \mathcal{L}) \equiv & \forall id_f \in \text{dom}(Ports), id_f \in \mathcal{L} \vee (Ports(id_f) = array(T, n, m) \wedge \\ & \forall i \in [n, m], (id_f, i) \in \mathcal{L}) \end{aligned}$$

Example of input port map validity checking

We use the component instantiation statement of Listing 1.6 to illustrate the use of the $valid_{ipm}$ predicate. The following rule demonstrates the validity checking on the input port map of component instance id_t .

$$\begin{array}{c}
 \Delta, \Delta_c, \sigma, \mathcal{L}_\emptyset \vdash \begin{array}{l} (\text{time_A_value} \Rightarrow 0, \\ \text{time_B_value} \Rightarrow 0, \\ \text{input_conditions}(0) \Rightarrow id_0, \\ \text{input_arcs_valid}(0) \Rightarrow id_1, \\ \text{priority_authorizations}(0) \Rightarrow \top, \\ \text{reinit_time}(0) \Rightarrow id_2 \end{array} \xrightarrow{\text{list}_{ipm}} \mathcal{L} \quad \text{check}_{pm}(\text{Ins}(\Delta_c), \mathcal{L}) \\
 \hline
 \Delta, \Delta_c, \sigma \vdash \text{valid}_{ipm} \left(\begin{array}{l} (\text{time_A_value} \Rightarrow 0, \\ \text{time_B_value} \Rightarrow 0, \\ \text{input_conditions}(0) \Rightarrow id_0, \\ \text{input_arcs_valid}(0) \Rightarrow id_1, \\ \text{priority_authorizations}(0) \Rightarrow \top, \\ \text{reinit_time}(0) \Rightarrow id_2 \end{array} \right)
 \end{array}$$

where:

- $\text{Ins}(\Delta_c) := \{("time_A_value", nat(0,1)), ("time_B_value", nat(0,1)), ("input_conditions", array(bool, 0, 0)), ("input_arcs_valid", array(bool, 0, 0)), ("priority_authorizations", array(bool, 0, 0)), ("reinit_time", array(bool, 0, 0))\}$

In $\text{Ins}(\Delta_c)$, the types of input ports are deduced from the generic map of the transition component instance id_t .

- $\mathcal{L} := \{("time_A_value", "time_B_value", \\ ("input_conditions", 0), ("input_arcs_valid", 0), ("priority_authorizations", 0), ("reinit_time", 0)\}$

We add that the identifiers id_0 , id_1 and id_2 are referenced as internal signals of the Boolean type in the embedding elaborated design Δ , i.e:

- $Sigs(\Delta) := \{(id_0, \text{bool}), (id_1, \text{bool}), (id_2, \text{bool})\}$

Valid output port map

The valid_{opm} predicate states that an *output* port map is valid in the context Δ, Δ_c , where Δ is the embedding design structure and Δ_c denotes the component instance owner of the port map, if:

- An output port identifier appears at most once in the output port map.
- Two different output port identifiers cannot be connected to the same signal.
- For each output port map entry, the formal and the actual part are of the exact same type (i.e, in the sense of the Leibniz equality).

We allow partially connected output port map; i.e, an output port map where all output ports might not be present in the mapping. Such output ports are open by default.

Premises

$list_{opm}$ builds two sets $\mathcal{L}, \mathcal{L}_{ids} \subseteq id \sqcup (id \times \mathbb{N})$ out of the port map opmap. \mathcal{L}_{ids} is built incrementally to check that there are no multiply-driven signals resulting of the port map connection.

$$\text{VALIDOPM} \quad \frac{\Delta, \Delta_c, \mathcal{L}_\emptyset, \mathcal{L}_{ids_\emptyset} \vdash \text{opmap} \xrightarrow{list_{opm}} \mathcal{L}, \mathcal{L}_{ids}}{\Delta, \Delta_c \vdash \text{valid}_{opm}(\text{opmap})}$$

Side conditions

- $id_f \notin \mathcal{L}$ checks that the port identifier id_f is not already mapped (i.e, is not already used in the formal part of a port map entry).
- $id_a \notin \mathcal{L}_{ids}$ checks that the signal identifier id_a is not already mapped (i.e, is not already used in the actual part of a port map entry).
- $id_f \in Outs(\Delta_c)$ checks that id_f is an output port identifier of Δ_c .
- $id_a \in Sigs(\Delta) \cup Outs(\Delta)$ checks that id_a is either an output port or an internal signal identifier of Δ .
- $\Delta_c(id_f) = \Delta(id_a) = T$ checks that id_f and id_a are exactly of the same type.

LISTOPMSIMPLETOSIMPLE

$$\Delta, \Delta_c, \mathcal{L}, \mathcal{L}_{ids} \vdash id_f \Rightarrow id_a \xrightarrow{list_{opm}} \mathcal{L} \cup \{id_f\}, \mathcal{L}_{ids} \cup \{id_a\}$$

$id_f \notin \mathcal{L}, id_a \notin \mathcal{L}_{ids}$
 $id_f \in Outs(\Delta_c)$
 $id_a \in Sigs(\Delta) \cup Outs(\Delta)$
 $\Delta_c(id_f) = \Delta(id_a) = T$

Side conditions

$Outs_c(id_f) = T$ and $Sigs(id_a) = \text{array}(T, n, m)$ checks that the type of id_f and the type of the elements of id_a are the same. Note that id_a must denote an array as id_f is mapped to one subelement of id_a .

LISTOPMSIMPLETOPARTIAL

$$\frac{SE_l(e_i) \vdash e_i \xrightarrow{e} v_i \quad v_i \in_c nat(n, m)}{\Delta, \Delta_c, \mathcal{L}, \mathcal{L}_{ids} \vdash id_f \Rightarrow id_a(e_i) \xrightarrow{list_{opm}} \mathcal{L} \cup \{id_f\}, \mathcal{L}_{ids} \cup \{(id_a, v_i)\}}$$

$id_f \notin \mathcal{L}, id_a, (id_a, v_i) \notin \mathcal{L}_{ids}$
 $id_f \in Outs(\Delta_c)$
 $id_a \in Sigs(\Delta) \cup Outs(\Delta)$
 $\Delta_c(id_f) = T$
 $\Delta(id_a) = \text{array}(T, n, m)$

LISTOPMSIMPLETOOPEN

$$\Delta, \Delta_c, \mathcal{L}, \mathcal{L}_{ids} \vdash id_f \Rightarrow open \xrightarrow{list_{opm}} \mathcal{L} \cup \{id_f\}, \mathcal{L}_{ids}$$

$id_f \notin \mathcal{L}$
 $id_f \in Outs(\Delta_c)$

Remark 3 (Unconnected output port.). We forbid the case where an indexed formal part corresponding to the subelement of a composite output port is unconnected, i.e $\text{id}_f(e_i) \Rightarrow \text{open}$, as it could lead to the case where some subelements of a composite output port are connected while others are not (error case in [13, p.7]).

$\text{LISTOPMPARTIALTOSIMPLE}$ $\frac{SE_l(e_i) \vdash e_i \xrightarrow{e} v_i \quad v_i \in_c \text{nat}(n, m)}{\Delta, \Delta_c, \mathcal{L} \vdash \text{id}_f(e_i) \Rightarrow \text{id}_a \xrightarrow{\text{list}_{\text{opm}}} \mathcal{L} \cup \{(id_f, v_i)\}, \mathcal{L}_{ids} \cup \{id_a\}}$	$\text{id}_f, (\text{id}_f, v_i) \notin \mathcal{L}, \text{id}_a \notin \mathcal{L}_{ids}$ $\text{id}_f \in \text{Outs}(\Delta_c)$ $\text{id}_a \in \text{Sigs}(\Delta) \cup \text{Outs}(\Delta)$ $\Delta_c(\text{id}_f) = \text{array}(T, n, m)$ $\Delta(\text{id}_a) = T$
--	---

$\text{LISTOPMPARTIALTOPARTIAL}$ $\frac{\begin{array}{c} SE_l(e'_i) \vdash e'_i \xrightarrow{e} v'_i \quad v'_i \in_c \text{nat}(n', m') \\ SE_l(e_i) \vdash e_i \xrightarrow{e} v_i \quad v_i \in_c \text{nat}(n, m) \end{array}}{\Delta, \Delta_c, \mathcal{L} \vdash \text{id}_f(e_i) \Rightarrow \text{id}_a(e'_i) \xrightarrow{\text{list}_{\text{opm}}} \mathcal{L} \cup \{(id_f, v_i)\}, \mathcal{L}_{ids} \cup \{(id_a, v'_i)\}}$	$\text{id}_f, (\text{id}_f, v_i) \notin \mathcal{L}, \text{id}_a, (\text{id}_a, v'_i) \notin \mathcal{L}_{ids}$ $\text{id}_f \in \text{Outs}(\Delta_c)$ $\text{id}_a \in \text{Sigs}(\Delta) \cup \text{Outs}(\Delta)$ $\Delta_c(\text{id}_f) = \text{array}(T, n, m)$ $\Delta(\text{id}_a) = \text{array}(T, n', m')$
---	--

LISTOPMCONS

$\Delta, \Delta_c, \mathcal{L}, \mathcal{L}_{ids} \vdash \text{assoc}_{po} \xrightarrow{\text{list}_{\text{opm}}} \mathcal{L}', \mathcal{L}'_{ids} \quad \Delta, \Delta_c, \mathcal{L}', \mathcal{L}'_{ids} \vdash \text{opmap} \xrightarrow{\text{list}_{\text{opm}}} \mathcal{L}'', \mathcal{L}''_{ids}$	
$\Delta, \Delta_c, \mathcal{L}, \mathcal{L}_{ids} \vdash \text{assoc}_{po}, \text{opmap} \xrightarrow{\text{list}_{\text{opm}}} \mathcal{L}'', \mathcal{L}''_{ids}$	

Example of output port map validity checking

To illustrate the validity checking of an output port map as performed by the $\text{valid}_{\text{opm}}$ predicate, we introduce in Listing 1.7 the instantiation in \mathcal{H} -VHDL abstract syntax of a place component id_p in the behavior of an embedding design.

```

1  comp (id_p, "place",
2    -- Generic map
3    (input_arcs_number => 1,
4      output_arcs_number => 1,
5      maximal_marking => 1),
6    -- Input port map
7    (initial_marking => 1,
8      input_arcs_weights(0) => 1,
9      output_arcs_types(0) => 0,
10     output_arcs_weights(1) => 1,
11     input_transitions_fired(0) => id_0,
12     output_transitions_fired(0) => id_1),
13   -- Output port map
14   (output_arcs_valid(0) => id_2,
```

```

15 priority_authorizations(0) => id3,
16 reinit_transitions_time(0) => id4,
17 marked => id5);

```

LISTING 1.7: An example of instantiation of the place design in \mathcal{H} -VHDL abstract syntax. The place component instance is named id_p .

The following rule describes the validity checking of the output port map of component id_p .

$$\begin{array}{c}
 \Delta, \Delta_c, \emptyset, \emptyset \vdash \text{priority_authorizations}(0) \Rightarrow id_3, \\
 \text{reinit_transitions_time}(0) \Rightarrow id_4, \\
 \text{marked} \Rightarrow id_5
 \end{array} \xrightarrow{\text{list}_{opm}} \left\{ \begin{array}{l} ("output_arcs_valid", 0), \\ ("priority_authorizations", 0) \\ ("reinit_transitions_time", 0), \\ "marked" \end{array} \right\}, \{id_2, id_3, id_4, id_5\}$$

$$\Delta, \Delta_c \vdash \text{valid}_{opm} \left(\begin{array}{l} \text{output_arcs_valid}(0) \Rightarrow id_2, \\ \text{priority_authorizations}(0) \Rightarrow id_3, \\ \text{reinit_transitions_time}(0) \Rightarrow id_4, \\ \text{marked} \Rightarrow id_5 \end{array} \right)$$

1.5.11 Valid sequential statements.

The valid_{ss} predicate states that a sequential statement is well-typed in the context Δ, σ, Λ .

Well-typed signal assignment.

Premises

- $\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v$ evaluates the expression assigned to signal id_s in the context Δ, σ, Λ . During the elaboration, σ corresponds to the default design state, i.e. where each signal is associated to its type default value.
- $v \in_c T$ checks that the value of expression e conforms to the type of signal id_s .

WELLYPESIGASSIGN

$$\frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v \in_c T \quad id_s \in Sigs(\Delta) \cup Outs(\Delta)}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(id_s \Leftarrow e)} \quad \Delta(id_s) = T$$

WELLYPEDIDXSIGASSIGN

$$\frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v \in_c T \quad \Delta, \sigma, \Lambda \vdash e_i \xrightarrow{e} v_i \quad v_i \in_c nat(n, m) \quad id_s \in Sigs(\Delta) \cup Outs(\Delta)}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(id_s(e_i) \Leftarrow e)} \quad \Delta(id_s) = array(T, n, m)$$

Well-typed variable assignment.

WELLTYPEDVARASSIGN

$$\frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v \in_c T \quad \text{id}_v \in \Lambda}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(\text{id}_v := e) \quad \Lambda(\text{id}_v) = (T, val)}$$

WELLTYPEDIDXVARASSIGN

$$\frac{\begin{array}{c} \Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v \in_c T \\ \Delta, \sigma, \Lambda \vdash e_i \xrightarrow{e} v_i \quad v_i \in_c \text{nat}(n, m) \quad \text{id}_v \in \Lambda \end{array}}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(\text{id}_v(e_i) := e) \quad \Lambda(\text{id}_v) = (\text{array}(T, n, m), val)}$$

Well-typed if statements.

WELLTYPEDIF

$$\frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v \in_c \text{bool} \quad \Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(ss)}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(\text{if } (e) ss)}$$

WELLTYPEDIFELSE

$$\frac{\begin{array}{c} \Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v \in_c \text{bool} \quad \Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(ss) \\ \Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v' \quad v' \in_c \text{bool} \quad \Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(ss') \end{array}}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(\text{if } (e) ss ss')}$$

Well-typed loop statement.

WELLTYPEDLOOP

$$\frac{\begin{array}{c} \Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v \in_c \text{nat}(0, \text{NATMAX}) \\ \Delta, \sigma, \Lambda \vdash e' \xrightarrow{e'} v' \quad v' \in_c \text{nat}(0, \text{NATMAX}) \quad \Delta, \sigma, \Lambda' \vdash \text{valid}_{ss}(ss) \end{array}}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(\text{for } (\text{id}_v, e, e') ss)} \quad \Lambda' = \Lambda \cup (\text{id}_v, (\text{nat}(v, v'), v))$$

Well-typed rising and falling edge blocks

WELLTYPEDRISING

$$\frac{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(ss)}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(\text{rising ss})}$$

WELLTYPEDFALLING

$$\frac{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(ss)}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(\text{falling ss})}$$

Well-typed rst blocks

$$\frac{\text{WELLTYPEDRST} \quad \Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(ss) \quad \Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(ss')}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(\text{rst } ss \ ss')}$$

Well-typed null statement

$$\frac{\text{WELLTYPEDNULL}}{\Delta, \sigma, \Lambda \vdash \text{valid}_{ss}(\text{null})}$$

1.6 Simulation rules

In this section, we formalize a specific simulation algorithm for the \mathcal{H} -VHDL designs. This algorithm is much simpler than the one presented in the LRM. This is mostly due to the fact that \mathcal{H} -VHDL is a subset of VHDL that aims at the description of synthesizable and synchronous designs. Synthesizable designs mean that the only kind of signal assignment used to describe the design behaviors are δ -delay signal assignments. Leaving apart the synchronous side, we only need a simulation algorithm that performs *delta cycles* (see Section 1.1.2) to simulate such synthesizable designs. However, \mathcal{H} -VHDL designs are also synchronous designs. As such, an \mathcal{H} -VHDL design is equipped with a clock input port. The value of the clock input port changes from 0 to 1 and inversely at constant rate, i.e. the clock rate. One can see the changing of the value of the clock input port as the result of the execution of a unit-delay signal assignment where the time clause is equal to half the clock period. Listing 1.6 illustrates how a \mathcal{H} -VHDL design $t1$ can be embedded in another top-level design with a process regulating the value of a clock signal by using a unit-delay signal assignment. Listing 1.6 presents the behavioral part of the architecture of the embedding top-level design.

```

1  architecture toplevel_arch of toplevel is
2  begin
3
4      clkp : process (clock)
5      begin
6          clock <= not clock after  $\tau$  -- where  $\tau$  is half a clock period
7      end process clkp;
8
9      idt1 : entity t1
10     generic map (... )
11     port map (clock => clock, ... );
12
13  end toplevel_arch;
```

In Listing 1.6, the `c1kp` process assigns the clock signal with its inverse value after τ unit of time where τ corresponds to half the clock period. Of course, the clock period is specified by the designer of the circuit. The component instance id_{tl} corresponds to the instantiation of the \mathcal{H} -VHDL design `t1`, i.e. the one we want to simulate. The `clock` input port of id_{tl} is connected to the `clock` signal of the embedding design. Thus, when the value of the clock signal changes every half clock period, the processes that react to the changes of the clock signal, i.e. the so-called *synchronous* processes, are executed in the body of component instance id_{tl} . Then, it is the turn of *combinational* processes, i.e. processes that follow the combinational logic and thus do not react to the changes of the clock signal, to be executed until stabilization of all signal values. Using the terms of the LRM simulation algorithm, what will happen when trying to simulate the design of Listing 1.6 will be an alternation between one time cycle to move to the next clock event and execute synchronous processes, followed by many delta cycles corresponding to the execution of combinational processes until stabilization. Thus, we choose to embed this alternation within the definition of our simulation algorithm.

We must add a last element to the definition of our simulation algorithm. The top-level designs generated by the HILECOP transformation interact with their environment through their input ports. The input ports of a top-level design are called *primary* input ports. In our simulation algorithm, we need to represent the capture and the injection of the values of primary input ports and how this affect the values of the internal signals of the simulated design.

Finally, Algorithm 1 gives an overview in a pseudo-code language of our simulation algorithm. This simulation algorithm is formalized in a small-step semantics style in the following sections.

Algorithm 1: `Simulation($\Delta, \sigma_e, cs, E_p, nbOfCycles$)`

```

// Initialization phase.
1  $\sigma'_e \leftarrow \text{RunAllOnce}(\Delta, \sigma_e, cs)$ 
2  $\sigma \leftarrow \text{Stabilize}(\Delta, \sigma'_e, cs)$ 

// Main loop.
3  $T_c \leftarrow 0$ 
4  $\theta \leftarrow [\sigma]$ 

5 while  $T_c \leq nbOfCycles$  do
6    $\sigma_i \leftarrow \text{Inject}_{\uparrow}(\Delta, \sigma, E_p, T_c)$ 
7    $\sigma_{\uparrow} \leftarrow \text{RisingEdge}(\Delta, \sigma_i, cs)$ 
8    $\sigma' \leftarrow \text{Stabilize}(\Delta, \sigma_{\uparrow}, cs)$ 
9    $\sigma'_i \leftarrow \text{Inject}_{\downarrow}(\Delta, \sigma', E_p, T_c)$ 
10   $\sigma_{\downarrow} \leftarrow \text{FallingEdge}(\Delta, \sigma'_i, cs)$ 
11   $\sigma \leftarrow \text{Stabilize}(\Delta, \sigma_{\downarrow}, cs)$ 
12   $\theta \leftarrow \theta \uplus [\sigma', \sigma]$ 
13   $T_c \leftarrow T_c + 1$ 

14 return  $\theta$ 
```

Algorithm 1 defines an elaborated design Δ and a default design state σ_e as parameters. We assume that they are the result of the elaboration of the design being simulated. cs corresponds to the behavior of the design, i.e. the one that will be executed during the simulation. E_p is the environment that will provide values to the primary input ports. $nbOfCycles$ corresponds

to the number of simulation cycles to be performed. Algorithm 1 begins with an initialization phase (following the LRM simulation algorithm); all processes are run exactly once followed by a stabilization phase (multiple delta cycles). Line 3 initializes the variable T_c to zero. T_c represents the current count of simulation cycles. Line 4 initializes the variable θ with a singleton list holding state σ , i.e. the initial simulation state. Then, the same loop is performed until T_c reaches the prescribed number of simulation cycles. First, the values of primary input ports are retrieved from the environment E_p for the current count T_c and the current clock event (i.e. either \uparrow or \downarrow); this is performed by the Inject_\uparrow (resp. Inject_\downarrow) at the rising edge of the clock; then, all parts of cs that react to the rising edge (resp. falling edge) of the clock signal are executed; finally, the combinational parts of cs are executed until stabilization of all signals. At Line 12, the states obtained at the middle and at the end of the clock cycle are appended to the simulation trace θ . Note that we only register stable states in the simulation trace. To conclude the simulation cycle, the current count is incremented. After the execution of all simulation cycles, Algorithm 1 returns the simulation trace.

1.6.1 Full simulation

The full simulation process is decomposed in two steps. The first step is the elaboration phase that builds an elaborated version of a \mathcal{H} -VHDL design along with its default state, and type-checks the design. Previous to the elaboration phase, the top-level design receives a value for each of its generic constant; we refer to it as the *dimensioning* of the top-level design. The second step is the simulation phase that executes the behavioral part of the top-level design starting from an initial state. The simulation is decomposed into simulation cycles. Each simulation cycle is divided in four parts entailed by the *synchronous* execution of \mathcal{H} -VHDL top-level designs, i.e designs whose behavior depend on a clock signal. The four parts are, first, the execution of concurrent statements responding to the rising edge of the clock signal, then, a phase of signal stabilization followed by the execution of concurrent statements responding to the falling edge of the clock signal, and finally another phase of signal stabilization. At each clock event, the value of the primary inputs of the design being currently simulated are captured and injected in the simulation; primary inputs receive values from the design environment. Here, the environment is represented by a function mapping input port identifiers to values depending on the current count of simulation cycles and the considered clock event. This leads to the following hypothesis:

Hypothesis 1 (Stable primary inputs). *The values of primary inputs (i.e, input ports of the top-level design) are captured at each clock event, and therefore are stable (i.e, their values do not change) between two contiguous clock events.*

Hypothesis 1 arises from the fact that the clock signal sample rate respects the Nyquist-Shannon sampling theorem. Therefore, the sample rate of the design's clock is sufficient to capture all events possibly arising in the environment. We only need to settle the values of the primary inputs at the clock edges.

Also, after each clock event phase follows a signal stabilization phase in the proceedings of a simulation cycle. One more hypothesis is needed here:

Hypothesis 2 (Stabilization). *All signals have enough time to stabilize during the signal stabilization phase that happens between two clock events.*

As a \mathcal{H} -VHDL design represents a physical circuit, one can assume that the represented circuit is analyzed former to the simulation. Therefore, one knows exactly how much time is needed to propagate signal values through the longest physical path; as a consequence, a proper clock frequency is set ensuring signal stabilization between two clock events. Thus, Hypothesis 2 arises from the latter facts.

The *full* simulation relation takes in parameter a top-level design d , a design store $\mathcal{D} \in id \rightsquigarrow \text{design}$, an elaborated design $\Delta \in ElDesign(d)$, a dimensioning function $\mathcal{M}_g \in Gens(\Delta) \rightsquigarrow \text{value}$, a primary input environment $E_p \in (\mathbb{N} \times Clk) \rightarrow (Ins(\Delta) \rightarrow \text{value})$, a simulation cycle count $\tau \in \mathbb{N}$, and a simulation trace $\theta \in \text{list}(\Sigma(\Delta))$, corresponding to the list of states yielded by design d after τ simulation cycles. Note that we use the pointed notation to access the behavioral part of design d , written $d.cs$. It is this part of the design that is executed during the simulation, and therefore is passed as a parameter of the initialization and simulation relations.

$$\begin{array}{c} \text{FULLSIM} \\ \hline \mathcal{D}, \mathcal{M}_g \vdash d \xrightarrow{\text{elab}} \Delta, \sigma \quad \mathcal{D}, \Delta, \sigma \vdash d.cs \xrightarrow{\text{init}} \sigma_0 \quad \mathcal{D}, E_p, \Delta, \tau, \sigma_0 \vdash d.cs \rightarrow \theta \\ \hline \mathcal{D}, \Delta, \mathcal{M}_g, E_p, \tau \vdash d \xrightarrow{\text{full}} (\sigma_0 :: \theta) \end{array}$$

where:

- $\mathcal{M}_g \in Gens(\Delta) \rightsquigarrow \text{value}$, the function yielding the values of generic constants for a given top-level design, referred to as the *dimensioning* function.
- $E_p \in (\mathbb{N} \times Clk) \rightarrow (\text{ident} \rightsquigarrow \text{value})$, the function yielding a mapping from primary inputs (i.e, input ports of the top-level design) to values at a given simulation cycle count (i.e, the \mathbb{N} argument), and a given clock event (i.e, the Clk argument, where $Clk = \{\uparrow, \downarrow\}$).
- τ , the number of simulation cycles to execute. The value of τ is decremented at each clock cycle until it reaches zero (see Section 1.6.2).

1.6.2 Simulation loop

$$\frac{\text{SIMEND}}{\mathcal{D}, E_p, \Delta, 0, \sigma \vdash cs \rightarrow []} \qquad \frac{\text{SIMLOOP}}{\mathcal{D}, E_p, \Delta, \tau, \sigma \vdash cs \xrightarrow{\uparrow\downarrow} \sigma', \sigma'' \quad \mathcal{D}, E_p, \Delta, \tau - 1, \sigma'' \vdash cs \rightarrow \theta \quad \tau > 0} \quad \mathcal{D}, E_p, \Delta, \tau, \sigma \vdash cs \rightarrow (\sigma' :: \sigma'' :: \theta)$$

1.6.3 Simulation cycle

To ease the reading of forward simulation rules, we need to introduce two notations.

Notation 3 (Overriding union). For all partial function $f, f' \in X \rightarrow Y$, $f \overset{\leftarrow}{\cup} f'$ denotes the overriding union of f and f' such that $f \overset{\leftarrow}{\cup} f'(x) = \begin{cases} f'(x) & \text{if } x \in \text{dom}(f') \\ f(x) & \text{otherwise} \end{cases}$

Notation 4 (Differentiated intersection domain). For all partial function $f, f' \in X \rightarrow Y$, $f \overset{\neq}{\cap} f'$ denotes the intersection of the domain of f and f' for which f and f' yields different values. That is, $f \overset{\neq}{\cap} f' = \{x \in \text{dom}(f) \cap \text{dom}(f') \mid f(x) \neq f'(x)\}$.

Definition 4 (Input port values update). Given an \mathcal{H} -VHDL design $d \in \text{design}$, a design store $\mathcal{D} \in id \rightarrow \text{design}$, an elaborated design $\Delta \in ElDesign(d, \mathcal{D})$, a simulation environment $E_p \in (\mathbb{N} \times \{\uparrow, \downarrow\}) \rightarrow (\text{Ins}(\Delta) \rightarrow \text{value})$, let us define the relation expressing the update of the values of the input ports of Δ at a given design state $\sigma \in \Sigma(\Delta)$, clock cycle count $\tau \in \mathbb{N}$, and clock event $clk \in \{\uparrow, \downarrow\}$, and thus resulting in a new state $\sigma_i \in \Sigma(\Delta)$. The relation is written $\text{Inject}_{clk}(\sigma, E_p, \tau, \sigma_i)$ and verifies that: $\sigma = \langle \mathcal{S}, \mathcal{C}, \mathcal{E} \rangle$ and $\sigma_i = \langle \mathcal{S} \overset{\leftarrow}{\cup} E_p(\tau, clk), \mathcal{C}, \mathcal{E} \rangle$.

The cycle relation states that the design state σ'' is the result of the execution of concurrent statement cs over one simulation cycle, this starting from state σ . As told in Hypothesis 1, we update the input port values at each clock event. New input port values are coming from the environment E_p . The updates are made in the definitions of σ_i and σ'_i . These definitions are expressed as side conditions.

$$\frac{\begin{array}{c} \text{SIMCYC} \\ \mathcal{D}, \Delta, \sigma_i \vdash cs \xrightarrow{\uparrow} \sigma_{\uparrow} \quad \mathcal{D}, \Delta, \sigma_{\uparrow} \vdash cs \rightsquigarrow \sigma' \\ \mathcal{D}, \Delta, \sigma'_i \vdash cs \xrightarrow{\downarrow} \sigma_{\downarrow} \quad \mathcal{D}, \Delta, \sigma_{\downarrow} \vdash cs \rightsquigarrow \sigma'' \\ \hline \mathcal{D}, E_p, \Delta, \tau, \sigma \vdash cs \xrightarrow{\uparrow, \downarrow} \sigma', \sigma'' \end{array}}{\text{Inject}_{\uparrow}(\sigma, E_p, \tau, \sigma_i) \quad \text{Inject}_{\downarrow}(\sigma', E_p, \tau, \sigma'_i)}$$

1.6.4 Initialization rules

$$\frac{\begin{array}{c} \text{INIT} \\ \mathcal{D}, \Delta, \sigma \vdash cs \xrightarrow{\text{runinit}} \sigma' \quad \mathcal{D}, \Delta, \sigma' \vdash cs \rightsquigarrow \sigma'' \\ \hline \mathcal{D}, \Delta, \sigma \vdash cs \xrightarrow{\text{init}} \sigma'' \end{array}}$$

At the initialization phase, the block of sequential instructions of all processes is executed exactly once ($\xrightarrow{\text{runinit}}$), then a stabilization phase follows (\rightsquigarrow). It is during the initialization phase that the first part of `rst ss ss'` is executed. A block (`rst ss ss'`) is equivalent to (`if rst = '0' then ss else ss'`) where `rst` is a reserved signal identifier. Therefore, when considering a `rst` block, the `runinit` relation executes the `ss` block; at every other moment of the simulation, the `ss'` block is executed. This mimicks the conventional proceeding of a simulation where the `rst` signal (for `reset` signal) is set to false during the initialization (only during the `runinit` phase, not during the stabilization phase), and then is set to true for the rest of the simulation.

Evaluation of a process statement

Premises

- The i flag of the ss_i relation indicates that all sequential instructions responding to the initialization phase (i.e, `rst` blocks) will be executed.
- The set of events of state σ is emptied ($NoEv(\sigma)$) before the evaluation of the process statement body, and the resulting state is the starting state that will be written through the execution of the process statement body.

$$\text{PSRUNINIT} \quad \frac{\Delta, \sigma, NoEv(\sigma), \Lambda \vdash ss \xrightarrow{ss_i} \sigma', \Lambda' \quad \Delta(id_p) = \Lambda}{\mathcal{D}, \Delta, \sigma \vdash \text{process } (id_p, sl, vars, ss) \xrightarrow{runinit} \sigma'}$$

Evaluation of a component instantiation statement

$$\text{COMP RUNINIT} \quad \frac{\begin{array}{c} \Delta, \Delta_c, \sigma, \sigma_c \vdash i \xrightarrow{mapip} \sigma'_c \\ \mathcal{D}, \Delta_c, \sigma'_c \vdash \mathcal{D}(id_e).cs \xrightarrow{runinit} \sigma''_c \\ \Delta, \Delta_c, NoEv(\sigma), \sigma''_c \vdash o \xrightarrow{mapop} \sigma' \end{array} \quad id_e \in \mathcal{D} \quad \Delta(id_c) = \Delta_c, \sigma(id_c) = \sigma_c}{\mathcal{D}, \Delta, \sigma \vdash \text{comp } (id_c, id_e, g, i, o) \xrightarrow{runinit} \sigma'' \quad \sigma'' = \langle \mathcal{S}', \mathcal{C}'(id_c) \leftarrow \sigma''_c, \mathcal{E}' \cup (\mathcal{C} \setminus \mathcal{C}') \rangle}$$

Evaluation of the composition of concurrent statements

$$\text{PARRUNINIT} \quad \frac{\mathcal{D}, \Delta, \sigma \vdash cs \xrightarrow{runinit} \sigma' \quad \mathcal{D}, \Delta, \sigma \vdash cs' \xrightarrow{runinit} \sigma'' \quad \mathcal{E}' \cap \mathcal{E}'' = \emptyset}{\mathcal{D}, \Delta, \sigma \vdash cs || cs' \xrightarrow{runinit} \text{merge}(\sigma, \sigma', \sigma'')} \quad \text{NULLRUNINIT} \quad \frac{}{\Delta, \sigma \vdash \text{null} \xrightarrow{runinit} NoEv(\sigma)}$$

The `merge` function computes a new state based on the original state o , and the states s and s' yielded by the computation of two concurrent statements. In the resulting state, the signal value store S_m is a function merging together the signal store functions at state o , s and s' . S_m yields values from the signal store \mathcal{S} (resp. \mathcal{S}') for all signal that belongs to the set of events at state s (resp. s'), and yields values from the original signal store \mathcal{S}_o for all unchanged signals. The same goes for the resulting component instance state store C_m . The new set of events \mathcal{E}_m is the union between set of events at state s and s' . The `merge` correctly merges the state o , s and s' only if the set of events of s and s' are disjoint. Fortunately, the PARRUNINIT rule that calls to the `merge` function defines the condition of disjoint set of events as a side condition.

```

1 Definition merge(o,s,s') :=
2   let o = ( $\mathcal{S}_o, \mathcal{C}_o, \mathcal{E}_o$ ) in
3   let s = ( $\mathcal{S}, \mathcal{C}, \mathcal{E}$ ) in
4   let s' = ( $\mathcal{S}', \mathcal{C}', \mathcal{E}'$ ) in
5   let  $\mathcal{S}_m = \lambda id. \text{if } id \in \mathcal{E} \text{ then } \mathcal{S}(id) \text{ else if } id \in \mathcal{E}' \text{ then } \mathcal{S}'(id) \text{ else } \mathcal{S}_o(id)$ 
6   let  $\mathcal{C}_m = \lambda id. \text{if } id \in \mathcal{E} \text{ then } \mathcal{C}(id) \text{ else if } id \in \mathcal{E}' \text{ then } \mathcal{C}'(id) \text{ else } \mathcal{C}_o(id)$ 
7   let  $\mathcal{E}_m = \mathcal{E} \cup \mathcal{E}'$  in  $(\mathcal{S}_m, \mathcal{C}_m, \mathcal{E}_m)$ .

```

Remark 4 (No multiply-driven signals). For all states $\sigma = (\mathcal{S}, \mathcal{C}, \mathcal{E})$ and $\sigma' = (\mathcal{S}', \mathcal{C}', \mathcal{E}')$ resulting from the execution of two concurrent statements cs and cs' , $\mathcal{E} \cap \mathcal{E}' = \emptyset$. Otherwise, there exists some multiply-driven signals, which are forbidden in our semantics.

1.6.5 Clock phases rules

The following rules express the evaluation of concurrent statements at clock phases, i.e, the \uparrow and \downarrow phases. The clock signal, triggering the evaluation of synchronous process statements, is represented by the reserved signal identifier `clk`. Thus, synchronous processes are processes containing the `clk` in their sensitivity list.

Evaluation of a process statement

$$\frac{\text{PsRENOCLK}}{\mathcal{D}, \Delta, \sigma \vdash \text{process } (\text{id}_p, \text{sl}, \text{vars}, \text{ss}) \xrightarrow{\uparrow} \sigma} \quad \text{clk} \notin \text{sl}$$

Premises

The \uparrow flag in the ss_{\uparrow} relation indicates that rising blocks will be executed.

$$\frac{\text{PsRECLK}}{\mathcal{D}, \Delta, \sigma \vdash \text{process } (\text{id}_p, \text{sl}, \text{vars}, \text{ss}) \xrightarrow{\uparrow} \sigma'} \quad \frac{\Delta, \sigma, \text{NoEv}(\sigma), \Lambda \vdash \text{ss} \xrightarrow{ss_{\uparrow}} \sigma', \Lambda' \quad \text{clk} \in \text{sl} \quad \Delta(\text{id}_p) = \Lambda}{\Delta, \sigma \vdash \text{process } (\text{id}_p, \text{sl}, \text{vars}, \text{ss}) \xrightarrow{\uparrow} \sigma'}$$

$$\frac{\text{PsFENOCLK}}{\mathcal{D}, \Delta, \sigma \vdash \text{process } (\text{id}_p, \text{sl}, \text{vars}, \text{ss}) \xrightarrow{\downarrow} \sigma} \quad \text{clk} \notin \text{sl}$$

Premises

The \downarrow flag in the ss_{\downarrow} relation indicates that falling blocks will be executed.

$$\text{PsFECLK} \quad \frac{\Delta, \sigma, NoEv(\sigma), \Lambda \vdash ss \xrightarrow{ss\downarrow} \sigma', \Lambda' \quad \text{clk} \in sl}{\mathcal{D}, \Delta, \sigma \vdash \text{process } (\text{id}_p, sl, \text{vars}, ss) \xrightarrow{\downarrow} \sigma'} \quad \Delta(\text{id}_p) = \Lambda$$

Evaluation of a component instantiation statement

$$\text{COMPRE} \quad \frac{\begin{array}{c} \Delta, \Delta_c, \sigma, \sigma_c \vdash i \xrightarrow{mapip} \sigma'_c \\ \mathcal{D}, \Delta_c, \sigma'_c \vdash \mathcal{D}(\text{id}_e).cs \xrightarrow{\uparrow} \sigma''_c \\ \Delta, \Delta_c, \sigma, \sigma''_c \vdash o \xrightarrow{mapop} \sigma' \end{array}}{\mathcal{D}, \Delta, \sigma \vdash \text{comp } (\text{id}_c, \text{id}_e, g, i, o) \xrightarrow{\uparrow} \sigma''} \quad \begin{array}{l} id_e \in \mathcal{D} \\ \Delta(\text{id}_c) = \Delta_c, \sigma(\text{id}_c) = \sigma_c \\ \sigma'' = <\mathcal{S}', \mathcal{C}'(\text{id}_c) \leftarrow \sigma''_c, \mathcal{E}' \cup (\mathcal{C} \cap \mathcal{C}')> \end{array}$$

$$\text{COMPFE} \quad \frac{\begin{array}{c} \Delta, \Delta_c, \sigma, \sigma_c \vdash i \xrightarrow{mapip} \sigma'_c \\ \mathcal{D}, \Delta_c, \sigma'_c \vdash \mathcal{D}(\text{id}_e).cs \xrightarrow{\downarrow} \sigma''_c \\ \Delta, \Delta_c, \sigma, \sigma''_c \vdash o \xrightarrow{mapop} \sigma' \end{array}}{\mathcal{D}, \Delta, \sigma \vdash \text{comp } (\text{id}_c, \text{id}_e, g, i, o) \xrightarrow{\downarrow} \sigma''} \quad \begin{array}{l} id_e \in \mathcal{D} \\ \Delta(\text{id}_c) = \Delta_c, \sigma(\text{id}_c) = \sigma_c \\ \sigma'' = <\mathcal{S}', \mathcal{C}'(\text{id}_c) \leftarrow \sigma''_c, \mathcal{E}' \cup (\mathcal{C} \cap \mathcal{C}')> \end{array}$$

Evaluation of the composition of concurrent statements

$$\text{PARFE} \quad \frac{\mathcal{D}, \Delta, \sigma \vdash cs \xrightarrow{\downarrow} \sigma' \quad \mathcal{D}, \Delta, \sigma \vdash cs' \xrightarrow{\downarrow} \sigma'' \quad \mathcal{E}' \cap \mathcal{E}'' = \emptyset}{\mathcal{D}, \Delta, \sigma \vdash cs || cs' \xrightarrow{\downarrow} \text{merge}(\sigma, \sigma', \sigma'')} \quad \text{NULLFE} \quad \frac{}{\Delta, \sigma \vdash \text{null} \xrightarrow{\downarrow} \sigma}$$

$$\text{PARRE} \quad \frac{\mathcal{D}, \Delta, \sigma \vdash cs \xrightarrow{\uparrow} \sigma' \quad \mathcal{D}, \Delta, \sigma \vdash cs' \xrightarrow{\uparrow} \sigma'' \quad \mathcal{E}' \cap \mathcal{E}'' = \emptyset}{\mathcal{D}, \Delta, \sigma \vdash cs || cs' \xrightarrow{\uparrow} \text{merge}(\sigma, \sigma', \sigma'')} \quad \text{NULLRE} \quad \frac{}{\Delta, \sigma \vdash \text{null} \xrightarrow{\uparrow} \sigma}$$

1.6.6 Stabilization rules

$$\text{STABILIZEEND} \quad \frac{\mathcal{D}, \Delta, \sigma \vdash cs \xrightarrow{comb} \sigma \quad \mathcal{E} = \emptyset}{\mathcal{D}, \Delta, \sigma \vdash cs \rightsquigarrow \sigma}$$

STABILIZELOOP

$$\frac{\mathcal{D}, \Delta, \sigma \vdash \text{cs} \xrightarrow{\text{comb}} \sigma' \quad \mathcal{D}, \Delta, \sigma' \vdash \text{cs} \xrightarrow{\text{ss}_c} \sigma'' \quad \mathcal{E} \neq \emptyset}{\mathcal{D}, \Delta, \sigma \vdash \text{cs} \xrightarrow{\text{ss}_c} \sigma''} \quad \mathcal{E}'' = \emptyset$$

Evaluation of a process statement

Premises

The *c* flag (for *combinational*) on the ss_c relation indicates that instructions responding to clock events (falling and rising blocks) and instructions executed during the initialization phase only (rst blocks) will not be considered.

PsCOMB

$$\frac{\Delta, \sigma, \text{NoEv}(\sigma), \Lambda \vdash \text{ss} \xrightarrow{\text{ss}_c} \sigma', \Lambda'}{\mathcal{D}, \Delta, \sigma \vdash \text{process } (\text{id}_p, \text{sl}, \text{vars}, \text{ss}) \xrightarrow{\text{comb}} \sigma'} \quad \Delta(\text{id}_p) = \Lambda$$

Evaluation of a component instantiation statement

COMP COMB

$$\frac{\begin{array}{c} \Delta, \Delta_c, \sigma, \sigma_c \vdash \text{i} \xrightarrow{\text{mapip}} \sigma'_c \\ \mathcal{D}, \Delta_c, \sigma'_c \vdash \mathcal{D}(\text{id}_e). \text{cs} \xrightarrow{\text{comb}} \sigma''_c \\ \Delta, \Delta_c, \text{NoEv}(\sigma), \sigma''_c \vdash \text{o} \xrightarrow{\text{mapop}} \sigma' \end{array}}{\mathcal{D}, \Delta, \sigma \vdash \text{comp } (\text{id}_c, \text{id}_e, \text{g}, \text{i}, \text{o}) \xrightarrow{\text{comb}} \sigma''} \quad \begin{array}{l} \text{id}_e \in \mathcal{D} \\ \Delta(\text{id}_c) = \Delta_c, \sigma(\text{id}_c) = \sigma_c \end{array} \quad \sigma'' = <\mathcal{S}', \mathcal{C}'(\text{id}_c) \leftarrow \sigma''_c, \mathcal{E}' \cup (\mathcal{C} \setminus \mathcal{C}')>$$

Evaluation of the composition of concurrent statements

PARCOMB

$$\frac{\mathcal{D}, \Delta, \sigma \vdash \text{cs} \xrightarrow{\text{comb}} \sigma' \quad \mathcal{D}, \Delta, \sigma \vdash \text{cs}' \xrightarrow{\text{comb}} \sigma''}{\mathcal{D}, \Delta, \sigma \vdash \text{cs} \parallel \text{cs}' \xrightarrow{\text{comb}} \text{merge}(\sigma, \sigma', \sigma'')} \quad \mathcal{E}' \cap \mathcal{E}'' = \emptyset$$

NULLCOMB

$$\frac{}{\Delta, \sigma \vdash \text{null} \xrightarrow{\downarrow} \text{NoEv}(\sigma)}$$

1.6.7 Evaluation of input and output port maps

MAPSIMPLE

$$\frac{\Delta, \sigma \vdash e \xrightarrow{e} v \quad v \in_c T}{\Delta, \Delta_c, \sigma, \sigma_c \vdash \text{id}_s \Rightarrow e \xrightarrow{\text{mapip}} <\mathcal{S}', \mathcal{C}, \mathcal{E}>} \quad \begin{array}{l} \Delta_c(\text{id}_s) = T \\ \sigma_c = <\mathcal{S}, \mathcal{C}, \mathcal{E}> \\ \mathcal{S}' = \mathcal{S}(\text{id}_s) \leftarrow v \end{array}$$

MAPIP_{PARTIAL}

$$\frac{\Delta, \sigma \vdash e \xrightarrow{e} v \quad v \in_c T \quad \vdash e_i \xrightarrow{e} v_i \quad v_i \in_c \text{nat}(n, m) \quad \Delta_c(\text{id}_s) = \text{array}(T, n, m)}{\Delta, \Delta_c, \sigma, \sigma_c \vdash \text{id}_s(e_i) \Rightarrow e \xrightarrow{\text{mapip}} \langle \mathcal{S}', \mathcal{C}, \mathcal{E} \rangle \quad \mathcal{S}' = \mathcal{S}(\text{id}_s) \leftarrow \text{set_at}(v, v_i, \mathcal{S}(\text{id}_s))}$$

MAPIP_{COMP}

$$\frac{\Delta, \Delta_c, \sigma, \sigma_c \vdash \text{assoc}_{ip} \xrightarrow{\text{mapip}} \sigma'_c \quad \Delta, \Delta_c, \sigma, \sigma'_c \vdash \text{ipmap} \xrightarrow{\text{mapip}} \sigma''_c}{\Delta, \Delta_c, \sigma, \sigma_c \vdash \langle \text{assoc}_{ip}, \text{ipmap} \rangle \xrightarrow{\text{mapip}} \sigma''_c}$$

Remark 5 (Out ports and e). We can not use the e relation to interpret the values of output ports, because output ports are write-only constructs. We append the flag o to the e relation (i.e., e_o) to permit the evaluation of output port identifiers as regular signal identifier expressions.

MAPOP_{OPEN}

$$\frac{}{\Delta, \Delta_c, \sigma, \sigma_c \vdash \text{id}_f \Rightarrow \text{open} \xrightarrow{\text{mapop}} \sigma_c}$$

MAPOP_{SIMPLETOSIMPLE}

$$\frac{\Delta_c, \sigma_c \vdash \text{id}_f \xrightarrow{e_o} v \quad v \in_c T}{\Delta, \Delta_c, \sigma, \sigma_c \vdash \text{id}_f \Rightarrow \text{id}_a \xrightarrow{\text{mapop}} \langle \mathcal{S}', \mathcal{C}, \mathcal{E}' \rangle}$$

$\text{id}_a \in \text{Sigs}(\Delta) \cup \text{Outs}(\Delta)$
 $\Delta(\text{id}_a) = T$
 $\sigma = \langle \mathcal{S}, \mathcal{C}, \mathcal{E} \rangle$
 $\mathcal{S}' = \mathcal{S}(\text{id}_a) \leftarrow v, \mathcal{E}' = \mathcal{E} \cup (\mathcal{S} \neq \mathcal{S}')$

MAPOP_{SIMPLETOPARTIAL}

$$\frac{\vdash e_i \xrightarrow{e} v_i \quad v \in_c T \quad \Delta_c, \sigma_c \vdash \text{id}_f \xrightarrow{e_o} v \quad v_i \in_c \text{nat}(n, m)}{\Delta, \Delta_c, \sigma, \sigma_c \vdash \text{id}_f \Rightarrow \text{id}_a(e_i) \xrightarrow{\text{mapop}} \langle \mathcal{S}', \mathcal{C}, \mathcal{E}' \rangle}$$

$\text{id}_a \in \text{Sigs}(\Delta) \cup \text{Outs}(\Delta)$
 $\Delta(\text{id}_a) = \text{array}(T, n, m)$
 $\sigma = \langle \mathcal{S}, \mathcal{C}, \mathcal{E} \rangle$
 $\mathcal{S}' = \mathcal{S}(\text{id}_a) \leftarrow \text{set_at}(v, v_i, \mathcal{S}(\text{id}_a))$
 $\mathcal{E}' = \mathcal{E} \cup (\mathcal{S} \cap \mathcal{S}')$

MAPOP_{PARTIALTOSIMPLE}

$$\frac{\Delta_c, \sigma_c \vdash \text{id}_f(e'_i) \xrightarrow{e_o} v \quad v \in_c T}{\Delta, \Delta_c, \sigma, \sigma_c \vdash \text{id}_f(e'_i) \Rightarrow \text{id}_a \xrightarrow{\text{mapop}} \langle \mathcal{S}', \mathcal{C}, \mathcal{E}' \rangle}$$

$\text{id}_a \in \text{Sigs}(\Delta) \cup \text{Outs}(\Delta)$
 $\Delta(\text{id}_a) = T$
 $\sigma = \langle \mathcal{S}, \mathcal{C}, \mathcal{E} \rangle$
 $\mathcal{S}' = \mathcal{S}(\text{id}_a) \leftarrow v, \mathcal{E}' = \mathcal{E} \cup (\mathcal{S} \cap \mathcal{S}')$

MAPOP_{PARTIALTOPARTIAL}

$$\frac{\vdash e_i \xrightarrow{e} v_i \quad v \in_c T \quad \Delta_c, \sigma_c \vdash \text{id}_f(e'_i) \xrightarrow{e_o} v \quad v_i \in_c \text{nat}(n, m)}{\Delta, \Delta_c, \sigma, \sigma_c \vdash \text{id}_f(e'_i) \Rightarrow \text{id}_a(e_i) \xrightarrow{\text{mapop}} \langle \mathcal{S}', \mathcal{C}, \mathcal{E}' \rangle}$$

$\text{id}_a \in \text{Sigs}(\Delta) \cup \text{Outs}(\Delta)$
 $\Delta(\text{id}_a) = \text{array}(T, n, m)$
 $\sigma = \langle \mathcal{S}, \mathcal{C}, \mathcal{E} \rangle$
 $\mathcal{S}' = \mathcal{S}(\text{id}_a) \leftarrow \text{set_at}(v, v_i, \mathcal{S}(\text{id}_a))$
 $\mathcal{E}' = \mathcal{E} \cup (\mathcal{S} \cap \mathcal{S}')$

$$\text{MAPOPCOMP} \quad \frac{\Delta, \Delta_c, \sigma, \sigma_c \vdash \text{assoc}_{po} \xrightarrow{\text{mapop}} \sigma' \quad \Delta, \Delta_c, \sigma', \sigma_c \vdash \text{opmap} \xrightarrow{\text{mapop}} \sigma''}{\Delta, \Delta_c, \sigma, \sigma_c \vdash \langle \text{assoc}_{po}, \text{opmap} \rangle \xrightarrow{\text{mapop}} \sigma''}$$

The e_o relation is only defined to retrieve the value of out ports from a store signal S under a design state $\sigma = \langle S, \mathcal{C}, \mathcal{E} \rangle$.

$$\frac{\text{OUTO}}{\Delta, \sigma \vdash \text{id}_s \xrightarrow{e_o} \sigma(\text{id}_s)} \quad \frac{\text{IDXOUTO}}{\Delta, \sigma \vdash \text{id}_s(\text{e}_i) \xrightarrow{e_o} \text{get_at}(i, \sigma(\text{id}_s))} \quad \begin{array}{l} \text{id}_s \in \text{Outs}(\Delta) \\ \text{id}_s \in \sigma \\ \Delta(\text{id}_s) = \text{array}(T, n, m) \\ i = v_i \bmod n \end{array}$$

1.6.8 Evaluation of sequential statements

The ss symbol indicates that the evaluation of the considered sequential statement does not depend on a specific flag (i.e, the c , i , \uparrow or \downarrow flag). In the rules of the ss relation, a ss flag is transferred from the conclusion to the premises when an sequential statement is composed of inner sequential blocks.

Signal assignment statement

A signal assignment generates a new design state with a modified signal store and a new set of events. Note that there are two states on the left side of the thesis symbol. σ represents the state holding the current values of signals, and σ_w holds the new values of signals (i.e. the *written* state).

Premises

The premise $S(id_s) \in_c T$ checks that the value associated to signal id_s in the signal store of σ complies with type T , where T is the type associated with signal id_s in Δ .

$$\text{SIGASSIGN} \quad \frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v \in_c T \quad \text{id}_s \in \text{Sigs}(\Delta) \cup \text{Outs}(\Delta) \quad \Delta(\text{id}_s) = T}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{id}_s \Leftarrow e \xrightarrow{ss} \langle S'_w, \mathcal{C}_w, \mathcal{E}'_w \rangle, \Lambda \quad S'_w = \mathcal{S}_w(id_s) \leftarrow v \quad \mathcal{E}'_w = \mathcal{E}_w \cup (\mathcal{S}_w \setminus S'_w)}$$

$$\text{IDXSIGASSIGN} \quad \frac{\Delta, \sigma, \Lambda \vdash e_i \xrightarrow{e} v_i \quad v_i \in_c T \quad \text{id}_s \in \text{Sigs}(\Delta) \cup \text{Outs}(\Delta) \quad \Delta(\text{id}_s) = \text{array}(T, n, m) \quad \Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v_i \in_c \text{nat}(n, m)}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{id}_s(e_i) \Leftarrow e \xrightarrow{ss} \langle S'_w, \mathcal{C}_w, \mathcal{E}'_w \rangle, \Lambda \quad S'_w = \mathcal{S}_w(id_s) \leftarrow \text{set_at}(v, v_i, \mathcal{S}_w(id_s)) \quad \mathcal{E}'_w = \mathcal{E}_w \cup (\mathcal{S}_w \setminus S'_w)}$$

Variable assignment statement

A variable assignment statement modifies the variable values in the local environment.

VARASSIGN

$$\frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v \in_c T}{\Delta, \sigma, \sigma_w, \Lambda \vdash id_v := e \xrightarrow{ss} \sigma_w, \Lambda(id_v) \leftarrow (T, v)} \quad \begin{array}{l} id_v \in \Lambda \\ \Lambda(id_v) = (T, val) \end{array}$$

IDXVARASSIGN

$$\frac{\Delta, \sigma, \Lambda \vdash e_i \xrightarrow{e} v_i \quad v_i \in_c \text{nat}(n, m) \quad \Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad v \in_c T}{\Delta, \sigma, \sigma_w, \Lambda \vdash id_v(e_i) := e \xrightarrow{ss} \sigma_w, \Lambda(id_v) \leftarrow (T, \text{set_at}(v, v_i, val))} \quad \begin{array}{l} id_v \in \Lambda \\ \Lambda(id_v) = (\text{array}(T, n, m), val) \end{array}$$

If statement

IF \top

$$\frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} \top \quad \Delta, \sigma, \sigma_w, \Lambda \vdash ss \xrightarrow{ss} \sigma'_w, \Lambda'}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{if } (e) ss \xrightarrow{ss} \sigma'_w, \Lambda'} \quad \frac{\text{IF}\perp}{\Delta, \sigma, \sigma_w, \Lambda \vdash e \xrightarrow{e} \perp} \quad \frac{}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{if } (e) ss \xrightarrow{ss} \sigma_w, \Lambda}$$

IFELSE \top

$$\frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{expr} \top \quad \Delta, \sigma, \sigma_w, \Lambda \vdash ss \xrightarrow{ss} \sigma'_w, \Lambda' \quad \text{IF}\perp}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{if } (e) ss ss' \xrightarrow{ss} \sigma'_w, \Lambda'} \quad \frac{\text{IFELSE}\perp}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{if } (e) ss ss' \xrightarrow{ss} \sigma'_w, \Lambda'}$$

Loop statement

LOOP \perp

$$\frac{\Delta, \sigma, \sigma_w, \Lambda_i \vdash ss \xrightarrow{ss} \sigma'_w, \Lambda' \quad \Delta, \sigma, \Lambda_i \vdash id_v = e' \xrightarrow{e} \perp \quad \Delta, \sigma, \sigma'_w, \Lambda' \vdash \text{for } (id_v, e, e') ss \xrightarrow{ss} \sigma''_w, \Lambda''}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{for } (id_v, e, e') ss \xrightarrow{ss} \sigma''_w, \Lambda''} \quad \begin{array}{l} id_v \in \Lambda \\ \Lambda(id_v) = (T, val) \\ \Lambda_i = \Lambda(id_v) \leftarrow (T, val + 1) \end{array}$$

LOOP \top

$$\frac{\Delta, \sigma, \Lambda_i \vdash id_v = e' \xrightarrow{e} \top}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{for } (id_v, e, e') ss \xrightarrow{ss} \sigma_w, \Lambda \setminus (id_v, \Lambda(id_v))} \quad \begin{array}{l} id_v \in \Lambda \\ \Lambda(id_v) = (T, val) \\ \Lambda_i = \Lambda(id_v) \leftarrow (T, val + 1) \end{array}$$

LOOPINIT

$$\frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad \Delta, \sigma, \sigma_w, \Lambda_i \vdash \text{for } (\text{id}_v, e, e') \text{ ss} \xrightarrow{\text{ss}} \sigma'_w, \Lambda' \quad \text{id}_v \notin \Lambda}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{for } (\text{id}_v, e, e') \text{ ss} \xrightarrow{\text{ss}} \sigma'_w, \Lambda'} \quad \Lambda_i = \Lambda \cup (\text{id}_v, (\text{nat}(v, v'), v))$$

Rising and falling edge block statements

$$\frac{\text{RISINGEDGEDEFAULT}}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{rising ss} \xrightarrow{\text{ss}_f} \sigma'_w, \Lambda} \quad f \neq \uparrow \quad \frac{\text{FALLINGEDGEDEFAULT}}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{falling ss} \xrightarrow{\text{ss}_f} \sigma'_w, \Lambda} \quad f \neq \downarrow$$

$$\frac{\text{RISINGEDGEEXEC}}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{ss} \xrightarrow{\text{ss}\uparrow} \sigma'_w, \Lambda'} \quad \frac{\text{FALLINGEDGEEXEC}}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{ss} \xrightarrow{\text{ss}\downarrow} \sigma'_w, \Lambda'} \\ \frac{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{rising ss} \xrightarrow{\text{ss}\uparrow} \sigma'_w, \Lambda'}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{falling ss} \xrightarrow{\text{ss}\downarrow} \sigma'_w, \Lambda'}$$

Rst block statement

$$\frac{\text{RSTDEFAULT}}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{ss}' \xrightarrow{\text{ss}_f} \sigma'_w, \Lambda'} \quad f \neq i \quad \frac{\text{RSTEXEC}}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{ss} \xrightarrow{\text{ss}_i} \sigma'_w, \Lambda'} \\ \frac{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{rst ss ss}' \xrightarrow{\text{ss}_f} \sigma'_w, \Lambda'}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{rst ss ss}' \xrightarrow{\text{ss}_i} \sigma'_w, \Lambda'}$$

Composition of sequential statements and null statement

$$\frac{\text{SEQSTMT}}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{ss} \xrightarrow{\text{ss}} \sigma'_w, \Lambda' \quad \Delta, \sigma, \sigma'_w, \Lambda' \vdash \text{ss}' \xrightarrow{\text{ss}} \sigma''_w, \Lambda''} \quad \frac{}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{ss; ss}' \xrightarrow{\text{ss}} \sigma''_w, \Lambda''} \quad \frac{\text{NULLSTMT}}{\Delta, \sigma, \sigma_w, \Lambda \vdash \text{null} \xrightarrow{\text{ss}} \sigma_w, \Lambda}$$

1.6.9 Evaluation of expressions

$$\frac{\text{NAT}}{\Delta, \sigma, \Lambda \vdash n \xrightarrow{e} n} \quad \frac{n \in \mathbb{N} \quad n \leq \text{NATMAX}}{} \quad \frac{\text{FALSE}}{\Delta, \sigma, \Lambda \vdash \text{false} \xrightarrow{e} \perp} \quad \frac{\text{TRUE}}{\Delta, \sigma, \Lambda \vdash \text{true} \xrightarrow{e} \top}$$

$$\frac{\text{AGGREG}}{\Delta, \sigma, \Lambda \vdash e_i \xrightarrow{e} v_i \quad i = 1, \dots, n}{\Delta, \sigma, \Lambda \vdash (e_1, \dots, e_n) \xrightarrow{e} (v_1, \dots, v_n)}$$

$$\text{SIG} \quad \frac{}{\Delta, \sigma, \Lambda \vdash \text{id}_s \xrightarrow{e} \sigma(\text{id}_s)} \quad \text{id}_s \in Sigs(\Delta) \cup Ins(\Delta)$$

$$\text{VAR} \quad \frac{}{\Delta, \sigma, \Lambda \vdash \text{id}_v \xrightarrow{e} v} \quad \text{id}_v \in \Lambda$$

$$\Lambda(\text{id}_v) = (T, v)$$

$$\text{GEN} \quad \frac{}{\Delta, \sigma, \Lambda \vdash \text{id}_g \xrightarrow{e} v} \quad \text{id}_g \in Gens(\Delta)$$

$$\Delta(\text{id}_g) = (T, v)$$

$$\text{IDXSIG} \quad \frac{\Delta, \sigma, \Lambda \vdash e_i \xrightarrow{e} v_i \quad v_i \in_c \text{nat}(n, m) \quad \text{id}_s \in Sigs(\Delta) \cup Ins(\Delta) \quad \Delta(\text{id}_s) = \text{array}(T, n, m)}{\Delta, \sigma, \Lambda \vdash \text{id}_s(e_i) \xrightarrow{e} \text{get_at}(i, \sigma(\text{id}_s)) \quad i = v_i \bmod n}$$

$$\text{IDXVAR} \quad \frac{\Delta, \sigma, \Lambda \vdash e_i \xrightarrow{e} v_i \quad v_i \in_c \text{nat}(n, m) \quad \text{id}_v \in \Lambda \quad \Delta(\text{id}_v) = (\text{array}(T, n, m), v)}{\Delta, \sigma, \Lambda \vdash \text{id}_v(e_i) \xrightarrow{e} \text{get_at}(i, v) \quad i = v_i \bmod n}$$

where $\text{get_at}(i, a)$ is a function returning the i -th element of array a .

$$\text{NATADD} \quad \frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad \Delta, \sigma, \Lambda \vdash e' \xrightarrow{e} v'}{v +_{\mathbb{N}} v' \leq \text{NATMAX}}$$

$$\Delta, \sigma, \Lambda \vdash e + e' \xrightarrow{e} v +_{\mathbb{N}} v'$$

$$\text{NATSUB} \quad \frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad \Delta, \sigma, \Lambda \vdash e' \xrightarrow{e} v'}{v \geq v'}$$

$$\Delta, \sigma, \Lambda \vdash e - e' \xrightarrow{e} v -_{\mathbb{N}} v'$$

$$\text{ORDOP} \quad \frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad \Delta, \sigma, \Lambda \vdash e' \xrightarrow{e} v' \quad \text{op}_{ordn} \in \{<, \leq, >, \geq\}}{\Delta, \sigma, \Lambda \vdash e \text{ op}_{ordn} e' \xrightarrow{e} v \text{ op}_{ord\mathbb{N}} v'}$$

$$\text{BOOLBINOOP} \quad \frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad \Delta, \sigma, \Lambda \vdash e' \xrightarrow{e} v' \quad \text{op}_{bool} \in \{\text{and}, \text{or}\}}{\Delta, \sigma, \Lambda \vdash e \text{ op}_{bool} e' \xrightarrow{e} v \text{ op}_{\mathbb{B}} v'}$$

$$\text{NOTOP} \quad \frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v}{\Delta, \sigma, \Lambda \vdash \text{not } e \xrightarrow{e} \neg v}$$

$$\text{EQOP} \quad \frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v \quad \Delta, \sigma, \Lambda \vdash e' \xrightarrow{e} v'}{\Delta, \sigma, \Lambda \vdash e = e' \xrightarrow{e} eq(v, v')}$$

$$\text{DIFFOp} \quad \frac{\Delta, \sigma, \Lambda \vdash e = e' \xrightarrow{e} v}{\Delta, \sigma, \Lambda \vdash e \neq e' \xrightarrow{e} \neg v}$$

where eq is the equality relation established for all types defined in the semantics.

$$\text{PARENTH} \quad \frac{\Delta, \sigma, \Lambda \vdash e \xrightarrow{e} v}{\Delta, \sigma, \Lambda \vdash (e) \xrightarrow{e} v}$$

Appendix A

The place design in concrete and abstract VHDL syntax

```

1  entity place is
2    generic(
3      input_arcs_number : natural := 1;
4      output_arcs_number : natural := 1;
5      maximal_marking : natural := 1
6    );
7    port(
8      clock : in std_logic;
9      reset_n : in std_logic;
10     initial_marking : in natural range 0 to maximal_marking;
11     input_arcs_weights : in weight_vector_t(input_arcs_number1 downto 0);
12     output_arcs_types : in arc_vector_t(output_arcs_number1 downto 0);
13     output_arcs_weights : in weight_vector_t(output_arcs_number1 downto 0);
14     input_transitions_fired : in std_logic_vector(input_arcs_number1 downto 0);
15     output_transitions_fired : in std_logic_vector(output_arcs_number1 downto 0);
16     output_arcs_valid : out std_logic_vector(output_arcs_number1 downto 0);
17     priority_authorizations : out std_logic_vector(output_arcs_number1 downto 0);
18     reinit_transitions_time : out std_logic_vector(output_arcs_number1 downto 0);
19     marked : out std_logic
20   );
21 end place;
22
23 architecture place_architecture of place is
24
25   subtype local_weight_t is natural range 0 to maximal_marking;
26
27   signal s_input_token_sum : local_weight_t;
28   signal s_marking : local_weight_t;
29   signal s_output_token_sum : local_weight_t;
30
31 begin
32

```

```

33  input_tokens_sum: process(input_arcs_weights, input_transitions_fired)
34    variable v_internal_input_token_sum: local_weight_t;
35 begin
36   v_internal_input_token_sum := 0;
37
38   for i in 0 to input_arcs_number - 1 loop
39     if (input_transitions_fired(i) = '1') then
40       v_internal_input_token_sum := v_internal_input_token_sum + input_arcs_weights(i)
41         );
42     end if;
43   end loop;
44
45   s_input_token_sum <= v_internal_input_token_sum;
46 end process input_tokens_sum;
47
48 output_tokens_sum: process(output_arcs_types, output_arcs_weights,
49   output_transitions_fired)
50   variable v_internal_output_token_sum: local_weight_t;
51 begin
52   v_internal_output_token_sum := 0;
53
54   for i in 0 to output_arcs_number - 1 loop
55     if (output_transitions_fired(i) = '1' and output_arcs_types(i) = arc_t(BASIC)) then
56       v_internal_output_token_sum := v_internal_output_token_sum +
57         output_arcs_weights(i);
58     end if;
59   end loop;
60
61   s_output_token_sum <= v_internal_output_token_sum;
62 end process output_tokens_sum;
63
64 marking: process(clock, reset_n, initial_marking)
65 begin
66   if (reset_n = '0') then
67     s_marking <= initial_marking;
68   elsif rising_edge(clock) then
69     s_marking <= s_marking + (s_input_token_sum - s_output_token_sum);
70   end if;
71 end process marking;
72
73 determine_marked: process(s_marking)
74 begin
75   if (s_marking = 0) then
76     marked <= '0';
77   else
78     marked <= '1';
79   end if;

```

```

77  end process determine_marked;
78
79 marking_validation_evaluation : process(output_arcs_types, output_arcs_weights,
80   s_marking)
81 begin
82   for i in 0 to output_arcs_number - 1 loop
83     if (((output_arcs_types(i) = arc_t(BASIC)) or (output_arcs_types(i) = arc_t(TEST)))
84       and (s_marking >= output_arcs_weights(i)))
85       or ((output_arcs_types(i) = arc_t(INHIBITOR)) and (s_marking <
86         output_arcs_weights(i)))
87     then
88       output_arcs_valid(i) <= '1';
89     else
90       output_arcs_valid(i) <= '0';
91     end if;
92   end loop;
93 end process marking_validation_evaluation;
94
95 priority_evaluation : process(output_arcs_types, output_arcs_weights,
96   output_transitions_fired, s_marking)
97   variable v_saved_output_token_sum : local_weight_t;
98 begin
99   v_saved_output_token_sum := 0;
100
101   for i in 0 to output_arcs_number - 1 loop
102     if (s_marking >= v_saved_output_token_sum + output_arcs_weights(i)) then
103       priority_authorizations(i) <= '1';
104     else
105       priority_authorizations(i) <= '0';
106     end if;
107
108     if ((output_transitions_fired(i) = '1') and (output_arcs_types(i) = arc_t(BASIC)))
109       then
110         v_saved_output_token_sum := v_saved_output_token_sum + output_arcs_weights(i);
111     end if;
112
113   end loop;
114 end process priority_evaluation;
115
116 reinit_transitions_time_evaluation : process(clock, reset_n)
117 begin
118   if (reset_n = '0') then
119     reinit_transitions_time <= (others => '0');
120   elsif rising_edge(clock) then
121     for i in 0 to output_arcs_number - 1 loop
122       if (((output_arcs_types(i) = arc_t(BASIC)) or (output_arcs_types(i) = arc_t(TEST)))
123           and (s_marking - s_output_token_sum < output_arcs_weights(i)))
124

```

```
119      and (s_output_token_sum > 0))  
120      or output_transitions_fired(i) = '1' )  
121  then  
122    reinit_transitions_time(i) <= '1';  
123  else  
124    reinit_transitions_time(i) <= '0';  
125  end if;  
126  end loop;  
127 end if;  
128 end process reinit_transitions_time_evaluation;  
129  
130 end place_architecture;
```

LISTING A.1: The place design in concrete VHDL syntax.

Appendix B

The transition design in concrete and abstract VHDL syntax

```

1  entity transition is
2    generic(
3      transition_type : transition_t := NOT_TEMPORAL;
4      input_arcs_number : natural := 1;
5      conditions_number : natural := 1;
6      maximal_time_counter : natural := 1
7    );
8    port(
9      clock : in std_logic;
10     reset_n : in std_logic;
11     input_conditions : in std_logic_vector(conditions_number1 downto 0);
12     time_A_value : in natural range 0 to maximal_time_counter;
13     time_B_value : in natural range 0 to maximal_time_counter;
14     input_arcs_valid : in std_logic_vector(input_arcs_number1 downto 0);
15     reinit_time : in std_logic_vector(input_arcs_number1 downto 0);
16     priority_authorizations : in std_logic_vector(input_arcs_number1 downto 0);
17     fired : out std_logic
18   );
19 end transition;
20
21 architecture transition_architecture of transition is
22
23   signal s_condition_combination : std_logic;
24   signal s_enabled : std_logic;
25   signal s_firable : std_logic;
26   signal s_firing_condition : std_logic;
27   signal s_priority_combination : std_logic;
28   signal s_reinit_time_counter : std_logic;
29   signal s_time_counter : natural range 0 to maximal_time_counter;
30
31 begin
32

```

```

33 condition_evaluation: process(input_conditions)
34   variable v_internal_condition: std_logic;
35 begin
36   v_internal_condition := '1';
37
38   for i in 0 to conditions_number - 1 loop
39     v_internal_condition := v_internal_condition and input_conditions(i);
40   end loop;
41
42   s_condition_combination <= v_internal_condition;
43 end process condition_evaluation;
44
45 enable_evaluation: process(input_arcs_valid)
46   variable v_internal_enabled: std_logic;
47 begin
48   v_internal_enabled := '1';
49
50   for i in 0 to input_arcs_number - 1 loop
51     v_internal_enabled := v_internal_enabled and input_arcs_valid(i);
52   end loop;
53
54   s_enabled <= v_internal_enabled;
55 end process enable_evaluation;
56
57 reinit_time_counter_evaluation: process(reinit_time, s_enabled)
58   variable v_internal_reinit_time_counter: std_logic;
59 begin
60   v_internal_reinit_time_counter := '0';
61
62   for i in 0 to input_arcs_number - 1 loop
63     v_internal_reinit_time_counter := v_internal_reinit_time_counter or reinit_time(i);
64   end loop;
65
66   s_reinit_time_counter <= v_internal_reinit_time_counter;
67 end process reinit_time_counter_evaluation;
68
69 time_counter: process(reset_n, clock)
70 begin
71   if (reset_n = '0') then
72     s_time_counter <= 0;
73   elsif falling_edge(clock) then
74     if ((s_enabled = '1') and (transition_type /= transition_t(NOT_TEMPORAL))) then
75       if (s_reinit_time_counter = '0') then
76         if (s_time_counter < maximal_time_counter) then
77           s_time_counter <= s_time_counter + 1;
78         end if;

```

```

79      else
80          s_time_counter <= 1;
81      end if;
82      else
83          s_time_counter <= 0;
84      end if;
85      end if;
86  end process time_counter;
87
88  firing_condition_evaluation : process (s_enabled, s_condition_combination,
89                                         s_reinit_time_counter, s_time_counter)
90  begin
91      if ((s_condition_combination = '1')
92          and (s_enabled = '1')
93          and ((transition_type = transition_t(NOT_TEMPORAL))
94
95              or ((transition_type = transition_t(TEMPORAL_A_B))
96                  and (s_reinit_time_counter = '0')
97                  and (s_time_counter >= (time_A_value1))
98                  and (s_time_counter < time_B_value)
99                  and (time_A_value /= 0)
100                 and (time_B_value /= 0)))
101
102              or ((s_reinit_time_counter = '0')
103                  and (time_A_value /= 0)
104                  and (((transition_type = transition_t(TEMPORAL_A_A))
105                      and (s_time_counter = (time_A_value1)))
106                      or ((transition_type = transition_t(TEMPORAL_A_INFINITE))
107                          and (s_time_counter >= (time_A_value1)) )
108
109                  or ((transition_type /= transition_t(NOT_TEMPORAL))
110                      and (s_reinit_time_counter = '1')
111                      and (time_A_value = 1))
112
113 ) then
114     s_firing_condition <= '1';
115     else
116         s_firing_condition <= '0';
117     end if;
118  end process firing_condition_evaluation;
119
120  priority_authorization_evaluation : process(priority_authorizations)
121    variable v_priority_combination : std_logic;
122  begin
123    v_priority_combination := '1';
124

```

```

125   for i in 0 to input_arcs_number - 1 loop
126     v_priority_combination := v_priority_combination and priority_authorizations(i);
127   end loop;
128
129   s_priority_combination <= v_priority_combination;
130 end process priority_authorization_evaluation;
131
132 firable: process(reset_n, clock)
133 begin
134   if (reset_n = '0') then
135     s_firable <= '0';
136   elsif falling_edge(clock) then
137     s_firable <= s_firing_condition;
138   end if;
139 end process firable;
140
141 fired_evaluation: process (s_firable, s_priority_combination)
142 begin
143   fired <= s_firable and s_priority_combination;
144 end process fired_evaluation;
145
146 end transition_architecture;

```

LISTING B.1: The transition design in concrete VHDL syntax.

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