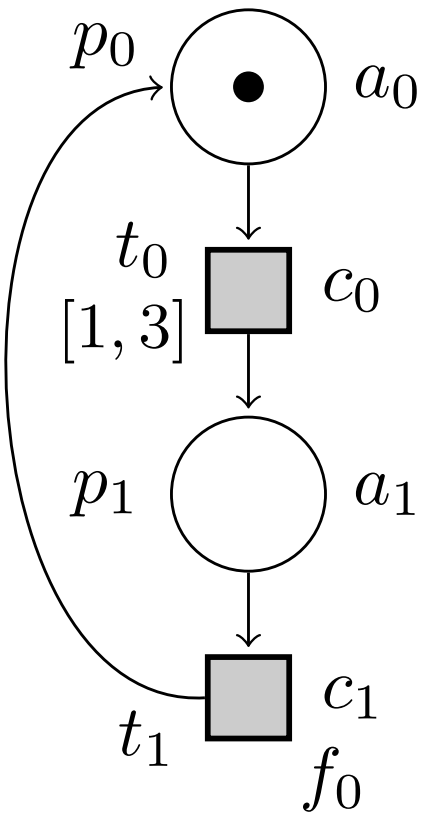
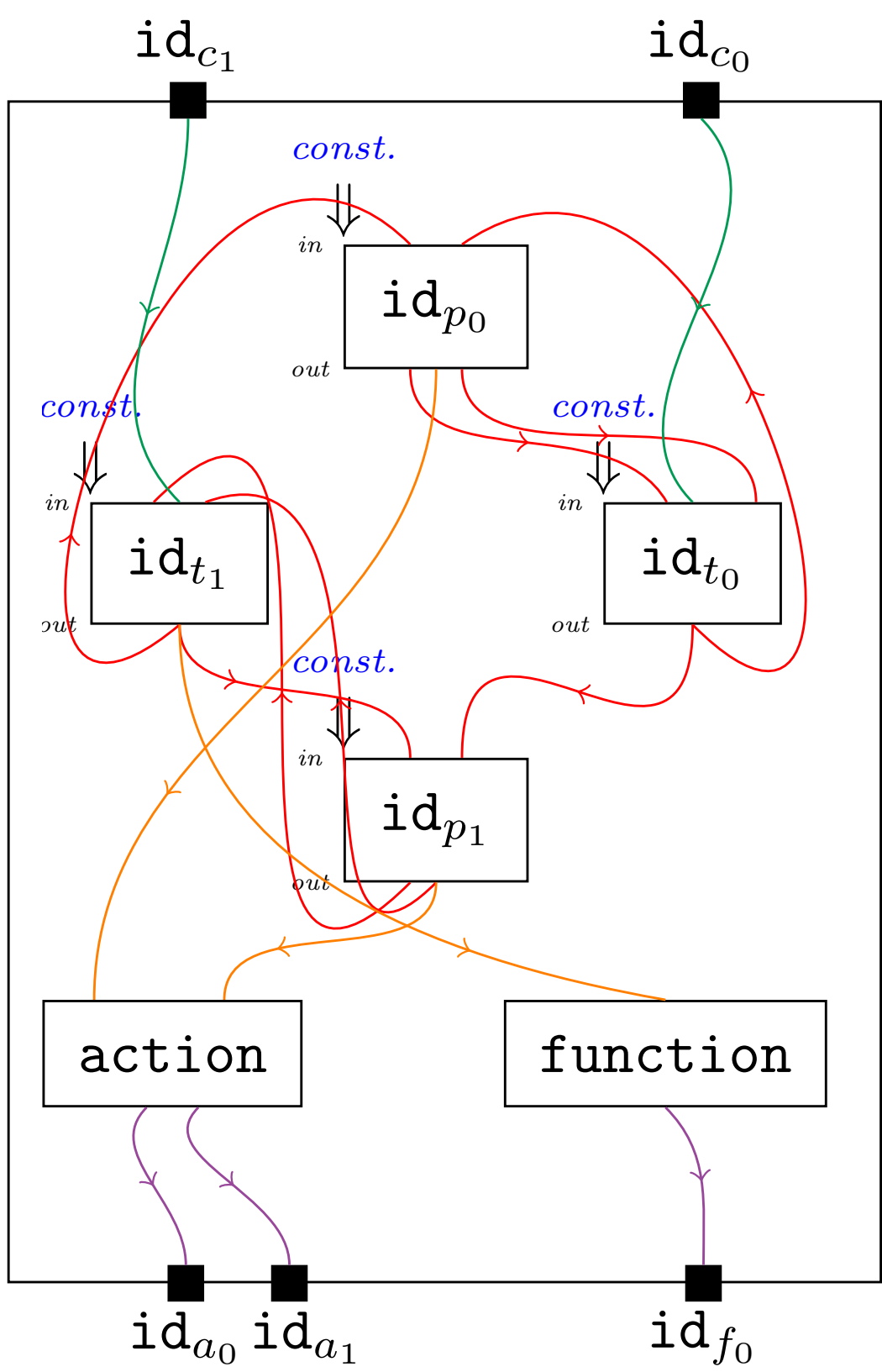


SITPN

Transformation



$\mathcal{H}$-VHDL top-level design