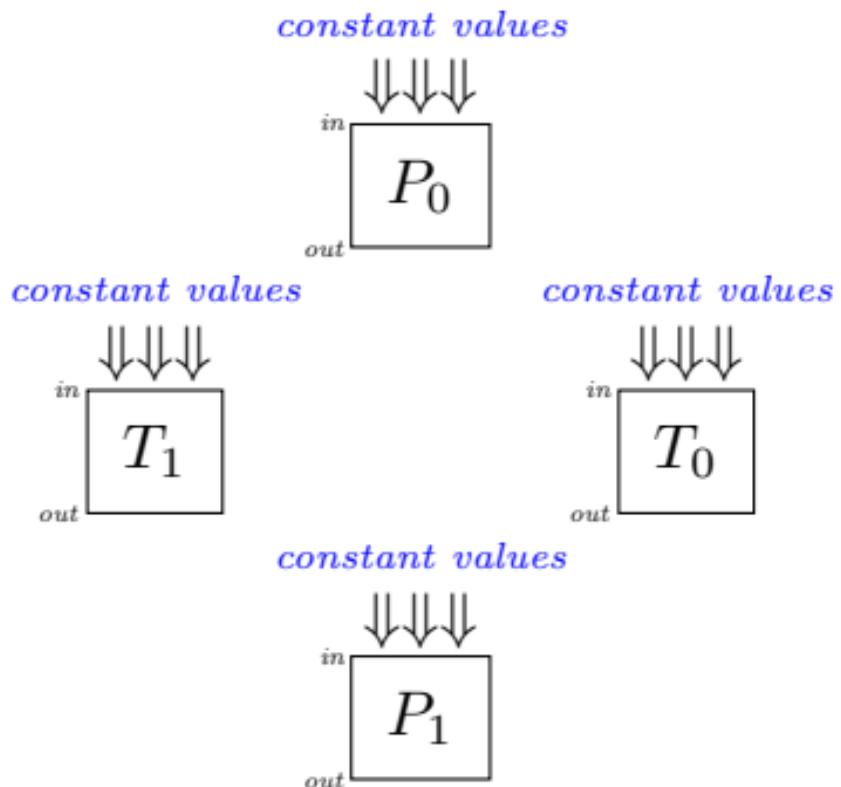


Transformation \Rightarrow



SITPN

VHDL top-level design