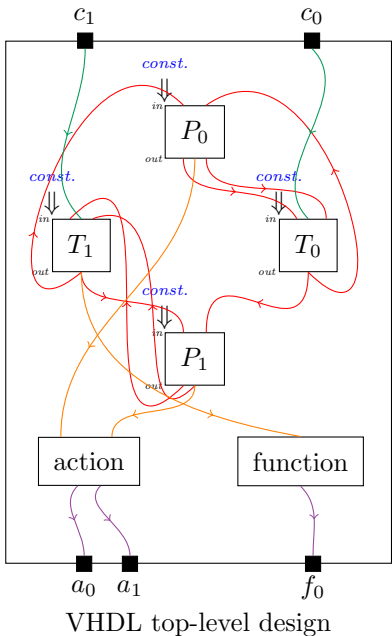


SITPN

Transformation  
 $\Longrightarrow$



VHDL top-level design