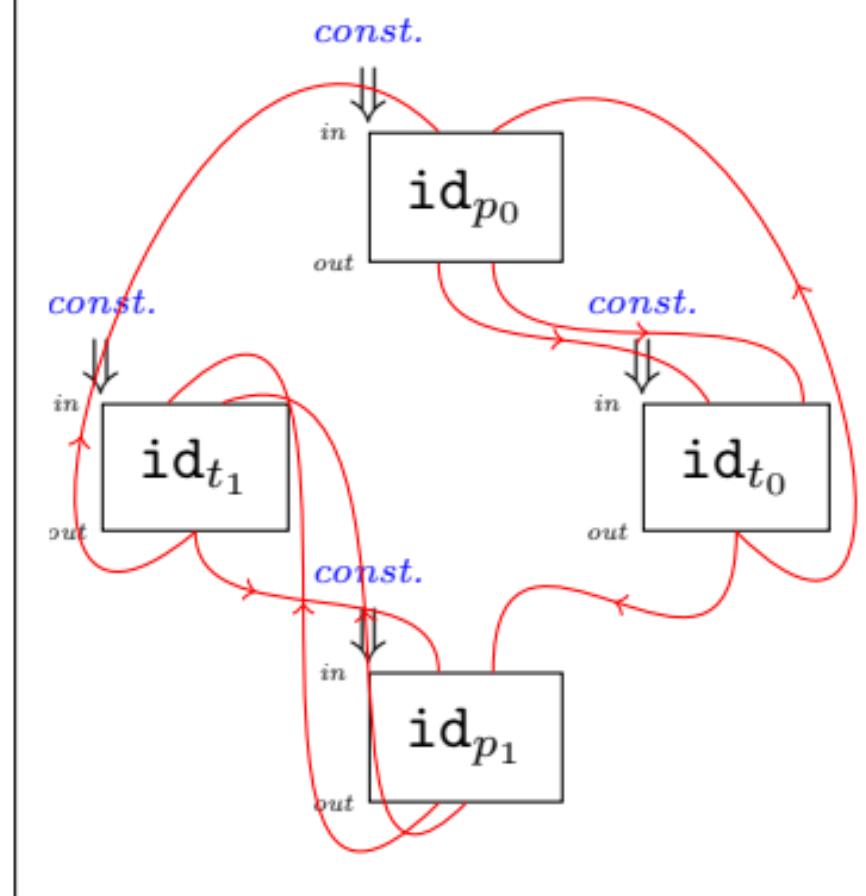


Transformation



SITPN

\mathcal{H} -VHDL top-level design