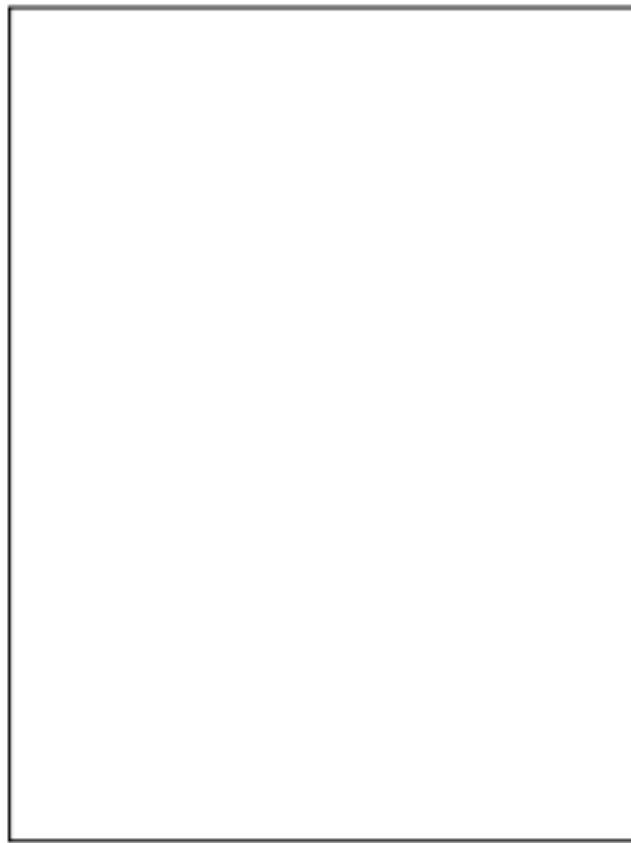


Transformation  
→



SITPN

VHDL top-level design