Stacy Gaikovaia

4A Computer Engineering
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Summary of Qualifications

Availability: 4 month work term starting September 2020
Languages: C/C++, Python, Bash, Verilog, SystemVerilog, Java, Coq
Tools: Git, perforce, vim, gdb, Unix/Linux, gcc, make
Frameworks/Libraries: OpenCL, FFmpeg, Intel Intrinsics (AVX, AVX2), AWS

Prior Experience

Apple Inc, ASIC Design Engineer – Verilog, SystemVerilog
September 2019 – December 2019

Worked on the hardware microarchitecture of the pixel pipeline for various display panels.

- Re-architected interconnect fabric for tone mapping component, fixing a critical timing bug
- Worked with a senior engineer to verify feature set of tone mapping component, allowing project to move onto the next phase of development
- Created re-usable hardware components that will be available for future designs
- Improved the ability of the timing control module to handle odd-valued timing intervals

IDT/Renesas, Firmware Developer - C
January 2019 – April 2019

Developed firmware for R11F, a high density video transcoder on FPGA avalible on AWS.

- Wrote custom bitstream filter converting CABAC-formatted H264 files to the CAVLC format for the FFmpeg project, which sped up decode time by ~12%
- Bitstream filter involved multiple concurrent processes and communicating across CPU/FPGA memory interface
- Modified FPGA hardware abstraction view to account for new hardware features
- Migrated project from AWS 2017.1 to 2017.4

IDT, Firmware Developer - C
May 2018 – August 2018

Developed firmware for R12C, a CPU-based video transcoder.

- Re-wrote firmware throttle controller to balance CPU usage between different transcoder components, providing finer control over transport stream multiplexing
- Wrote FFmpeg regression test suite to find system performance discrepencies

Alert Labs, Software Developer – Python, Java
January 2017 – April 2017

Analyzed water use patterns in the company backend to ensure sensor performance and develop new functionality.

- Developed and implemented feature detection algorithms to detect and report anomalous water use patterns
- Automated mechanical performance analysis of water sensor during company's first bulk sale period

Centre for Theoretical Neuroscience, Research Assistant – Python
April 2016 – August 2016

Wrote high-level neural simulations using the *nengo* Python software package.

- Modeled the process of object categorization and adaptation to visual distortion in monkey brains
- Wrote optimization scripts to find recursive network connection strengths that mapped accurately to known biological phenomena, such as response latency and neuron spiking patterns

Education

B.A.Sc. University of Waterloo
September 2015 – April 2021

Candidate for Bachelor of Applied Science, Honours Computer Engineering
Combinatorics and Optimization Minor