

CSE 232: Assignment 2

```
vibhor@LAPTOP-QVQGB6UI:/mnt/c/Users/Vibhor Aggarwal/Documents/5thSem/CN/A2/assignment2/assignment2/build$ ctest
Test project /mnt/c/Users/Vibhor Aggarwal/Documents/5thSem/CN/A2/assignment2/assignment2/build
  Start 1: wrapping_integers_cmp ..... Passed    0.03 sec
1/23 Test #1: wrapping_integers_cmp ..... Passed    0.03 sec
  Start 2: wrapping_integers_unwrap ..... Passed    0.03 sec
2/23 Test #2: wrapping_integers_unwrap ..... Passed    0.03 sec
  Start 3: wrapping_integers_wrap ..... Passed    0.03 sec
3/23 Test #3: wrapping_integers_wrap ..... Passed    0.03 sec
  Start 4: wrapping_integers_roundtrip ..... Passed    0.53 sec
4/23 Test #4: wrapping_integers_roundtrip ..... Passed    0.53 sec
  Start 5: byte_stream_construction ..... Passed    0.03 sec
5/23 Test #5: byte_stream_construction ..... Passed    0.03 sec
  Start 6: byte_stream_one_write ..... Passed    0.03 sec
6/23 Test #6: byte_stream_one_write ..... Passed    0.03 sec
  Start 7: byte_stream_two_writes ..... Passed    0.03 sec
7/23 Test #7: byte_stream_two_writes ..... Passed    0.03 sec
  Start 8: byte_stream_capacity ..... Passed    0.58 sec
8/23 Test #8: byte_stream_capacity ..... Passed    0.58 sec
  Start 9: byte_stream_many_writes ..... Passed    0.03 sec
9/23 Test #9: byte_stream_many_writes ..... Passed    0.03 sec
  Start 10: recv_connect ..... Passed    0.05 sec
10/23 Test #10: recv_connect ..... Passed    0.05 sec
  Start 11: recv_transmit ..... Passed    0.11 sec
11/23 Test #11: recv_transmit ..... Passed    0.11 sec
  Start 12: recv_window ..... Passed    0.04 sec
12/23 Test #12: recv_window ..... Passed    0.04 sec
  Start 13: recv_reorder ..... Passed    0.05 sec
13/23 Test #13: recv_reorder ..... Passed    0.05 sec
  Start 14: recv_close ..... Passed    0.05 sec
14/23 Test #14: recv_close ..... Passed    0.05 sec
  Start 15: recv_special ..... Passed    0.03 sec
15/23 Test #15: recv_special ..... Passed    0.03 sec
  Start 16: fsm_stream_reassembler_cap ..... Passed    0.13 sec
16/23 Test #16: fsm_stream_reassembler_cap ..... Passed    0.13 sec
  Start 17: fsm_stream_reassembler_single ..... Passed    0.03 sec
17/23 Test #17: fsm_stream_reassembler_single ..... Passed    0.03 sec
  Start 18: fsm_stream_reassembler_seq ..... Passed    0.03 sec
18/23 Test #18: fsm_stream_reassembler_seq ..... Passed    0.03 sec
  Start 19: fsm_stream_reassembler_dup ..... Passed    0.04 sec
19/23 Test #19: fsm_stream_reassembler_dup ..... Passed    0.04 sec
  Start 20: fsm_stream_reassembler_holes ..... Passed    0.03 sec
20/23 Test #20: fsm_stream_reassembler_holes ..... Passed    0.03 sec
  Start 21: fsm_stream_reassembler_many ..... Passed    0.13 sec
21/23 Test #21: fsm_stream_reassembler_many ..... Passed    0.13 sec
  Start 22: fsm_stream_reassembler_overlapping ..... Passed    0.03 sec
22/23 Test #22: fsm_stream_reassembler_overlapping ... Passed    0.03 sec
  Start 23: fsm_stream_reassembler_win ..... Passed    0.13 sec
23/23 Test #23: fsm_stream_reassembler_win ..... Passed    0.13 sec

100% tests passed, 0 tests failed out of 23

Total Test time (real) = 2.67 sec
vibhor@LAPTOP-QVQGB6UI:/mnt/c/Users/Vibhor Aggarwal/Documents/5thSem/CN/A2/assignment2/assignment2/build$
```

Output for test cases