IT301: Data Communication & Computer Network(DCCN)

Class: B. Tech (CS) Sec A
Semester : V
Teacher: Dr. Amritanjali

Week 5

Syllabus

Module I

- **Data Communications and Networking**: Overview A Communications Model, Data Communications, Data Communication Networking, The Need for Protocol Architecture, A Simple Protocol Architecture, OSI, The TCP/IP Protocol Architecture, Data Transmission Concepts and Terminology, Analog and Digital Data Transmission, Transmission Impairments, Channel Capacity. (8L)

Module II

- **Transmission Media and Signal Encoding Techniques:** Guided Transmission Media, Wireless Transmission, Wireless Propagation, Line-of-Sight Transmission. Digital Data Digital Signals, Digital Data Analog Signals, Analog Data Digital Signals, Analog Data Analog Signals. (8L)

Module III

- **Digital Data Communication Techniques and Data Link Control:** Asynchronous and Synchronous Transmission, Types of Errors, Error Detection, Error Correction, Line Configurations, Interfacing, Flow Control, Error Control, High-Level Data Link Control (HDLC). (8L)

Module IV

- Multiplexing, Circuit Switching and Packet Switching Multiplexing Frequency Division Multiplexing, Synchronous Time Division Multiplexing, Statistical Time Division Multiplexing, Switching Networks, Circuit-Switching Networks, Circuit-Switching Concepts, Control Signaling, Soft switch Architecture, Packet-Switching Principles, X.25, and Frame Relay. (8L)

Module V

- Asynchronous Transfer Model Protocol Architecture, ATM Logical Connections, ATM Cells, Transmission of ATM Cells, ATM Service Categories, ATM Adaptation Layer. Routing in Switched Networks Routing in Circuit-Switching Networks, Routing in Packet-Switching Networks, Least-Cost Algorithms. (8L)

Text Book: Stallings W., Data and Computer Communications, 10^{th} Edn., Pearson Education, PHI, New Delhi, 2014.(T1)

Reference Book: Forouzan B. A., Data Communications and Networking, 5thEdn. TMH, New Delhi, 2017.(R1)

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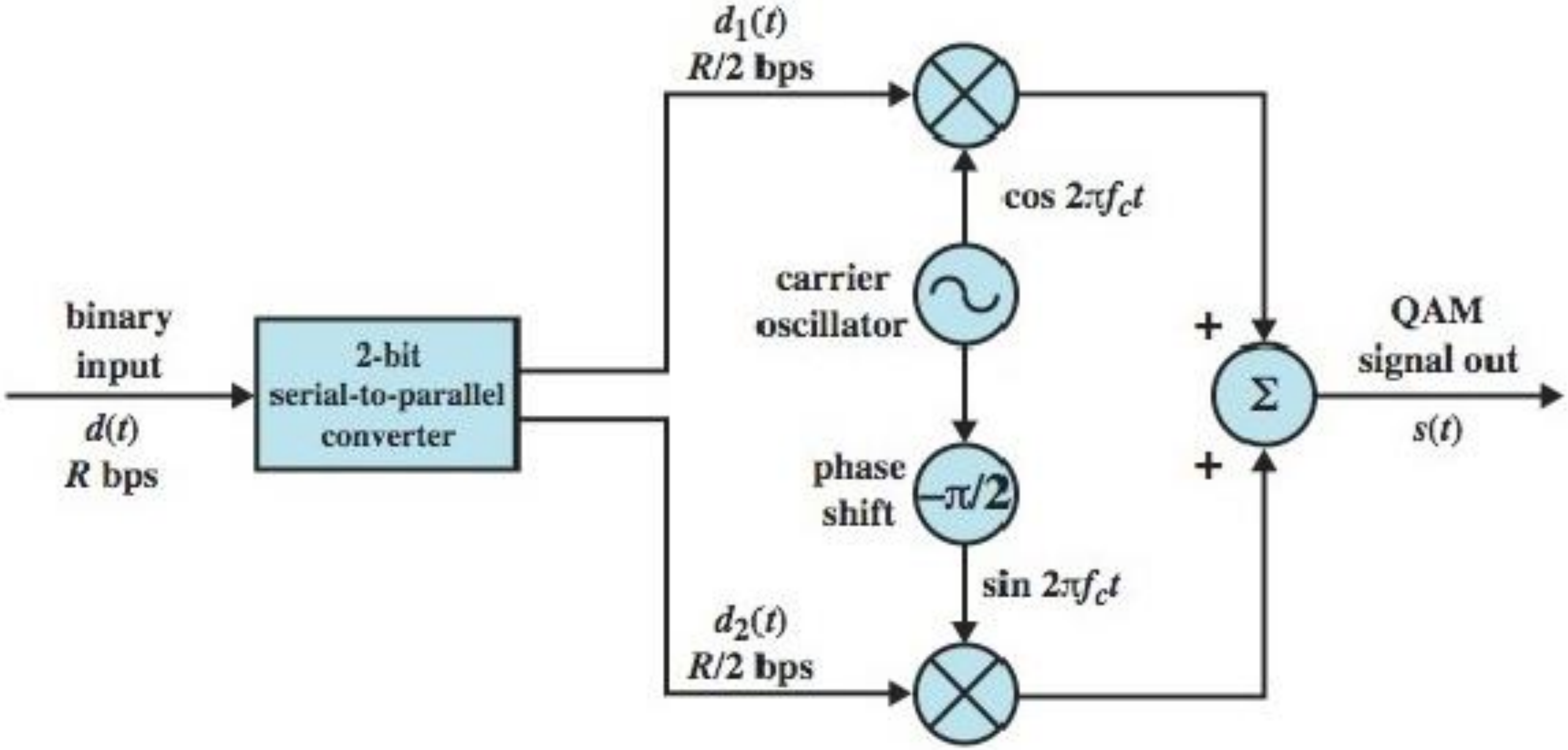
Quadrature Amplitude Modulation (QAM)

- Combination of ASK and PSK
- ASK modulation of two copies of the carrier signal with phase difference of 90^0

$$s(t) = d_1(t)\cos 2\pi f_c t + d_2(t)\sin 2\pi f_c t$$

- As the number of states is increased, data rate increase but error probability also increases due to noise and attenuation

QAM Modulator



Analog Data Digital Signals

- Allows analog data to be transmitted over digital communication system
- Requires digitization of analog data

Digitization

- Analog data is converted to digital data

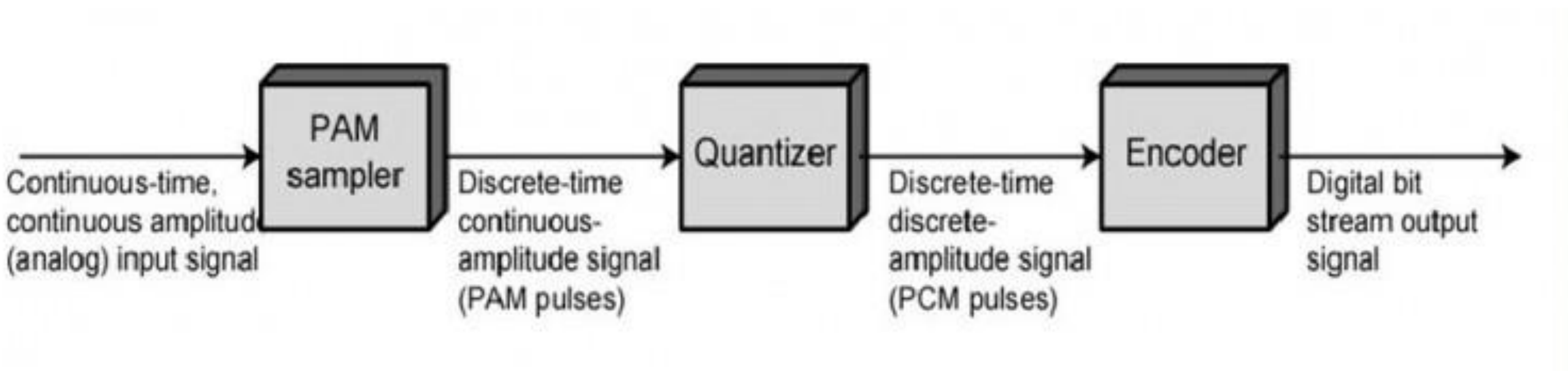
Sampling Theorem

- If a signal f(t) is sampled at regular intervals of time and at a rate higher than the twice the highest signal frequency, then the sample contain all the necessary information of the original signal.

Pulse Code Modulation

Pulse Code Modulation process has three steps

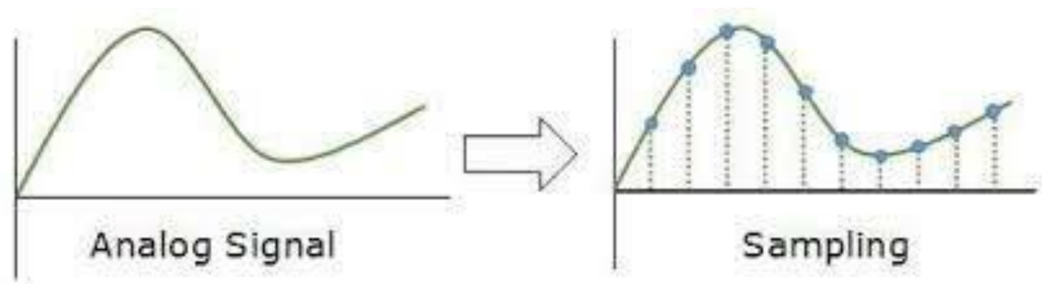
- Sampling
- Quantization
- Coding



Sampling

Pulse Amplitude Modulation Sampler

- Converts the continuous amplitude signal into discrete-time-continuous signal (PAM pulses)
- Amplitude of the analog signal is measured at regular intervals of time
- Number of samples per second is several times the maximum frequency



Quantization

- Analog sample with an amplitude is converted into a digital sample with an amplitude that takes one of a specifically defined set of quantization values
- Range of possible values of the analog samples is divided into some number of levels
- Quantization approximates the analog sample values with the nearest quantization values
- Small difference between the original value and the quantized value is known as quantization error

Coding

- Encoder encodes the quantized samples
- Each quantized sample is encoded into binary

PCM

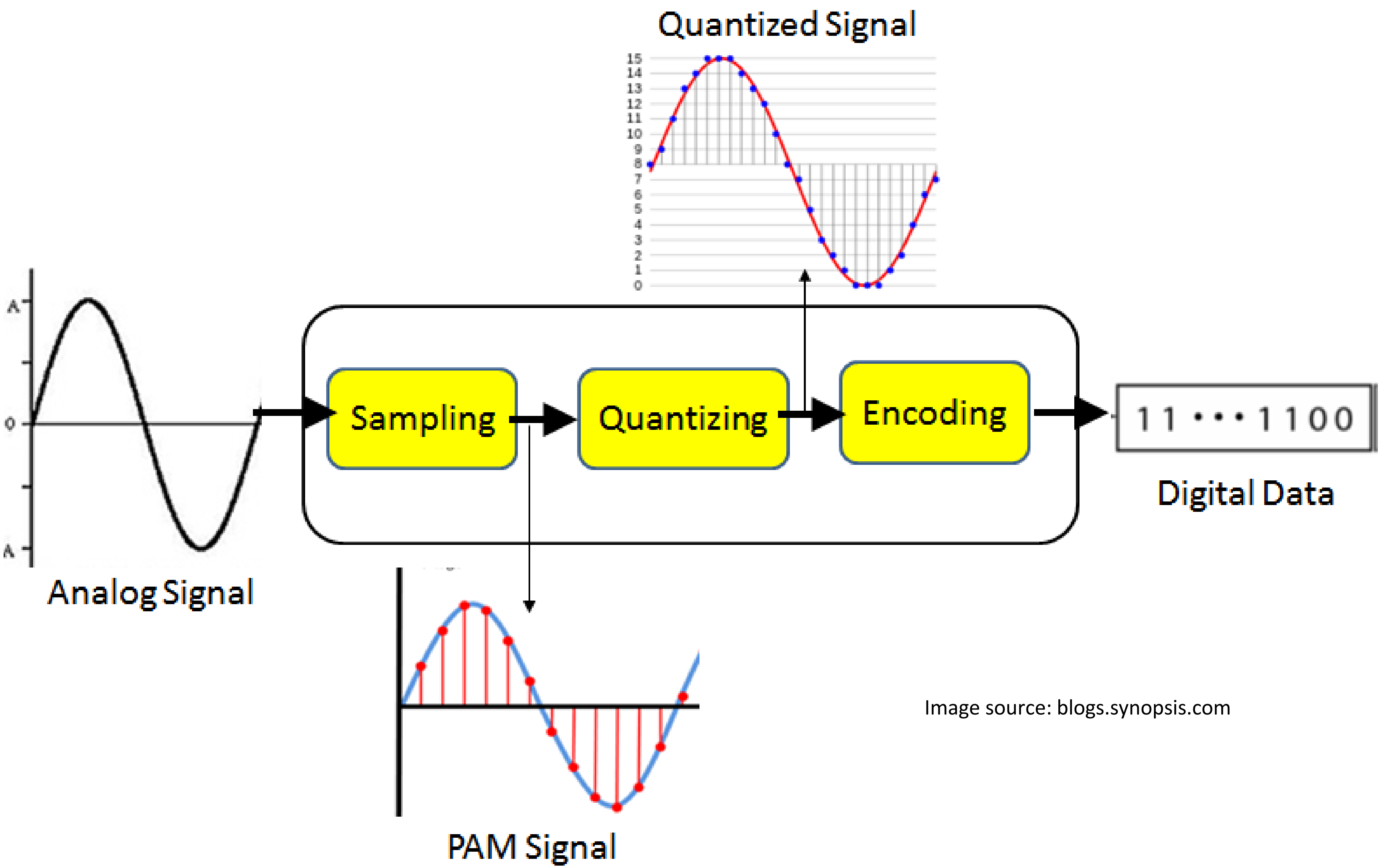
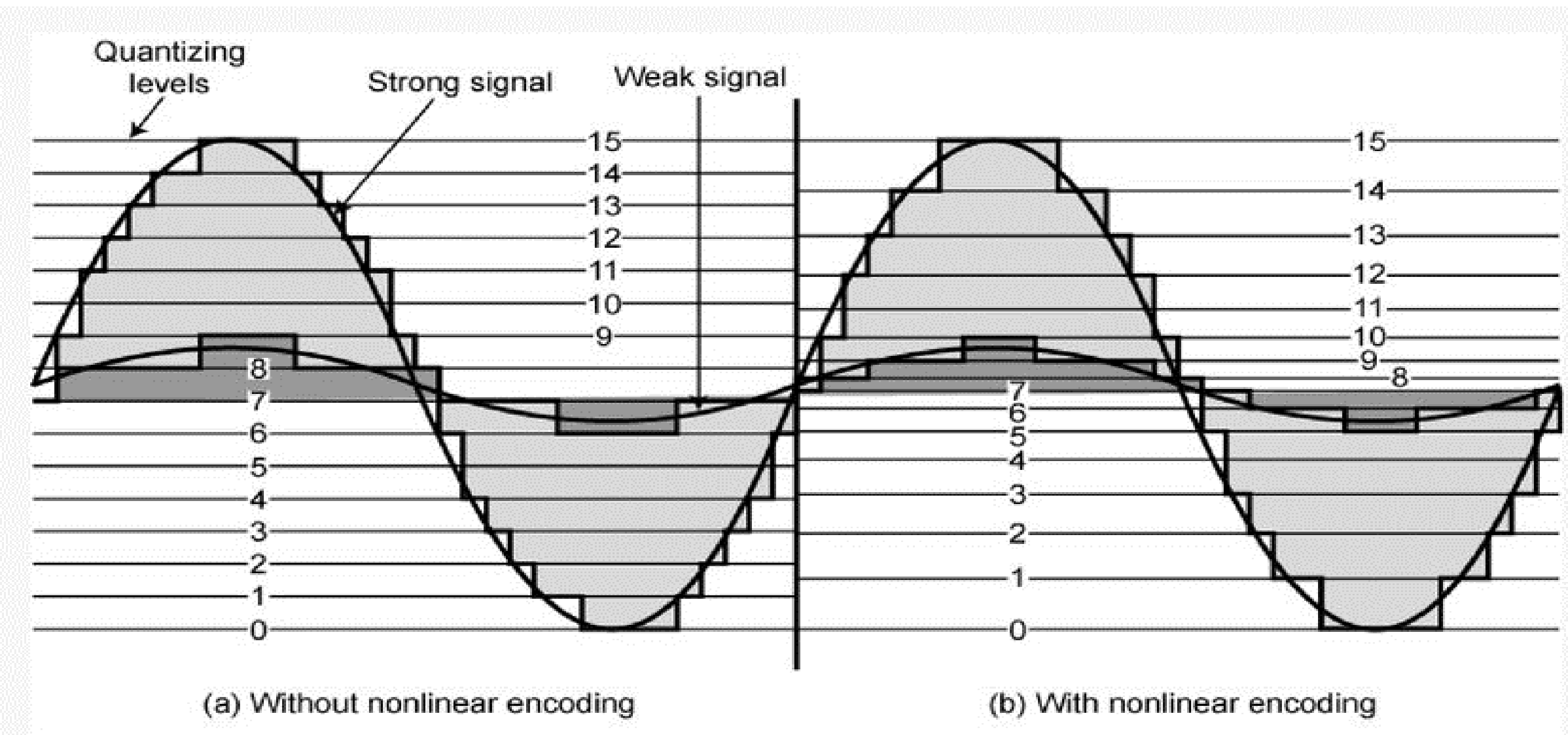


Image source: blogs.synopsis.com

Non linear Encoding

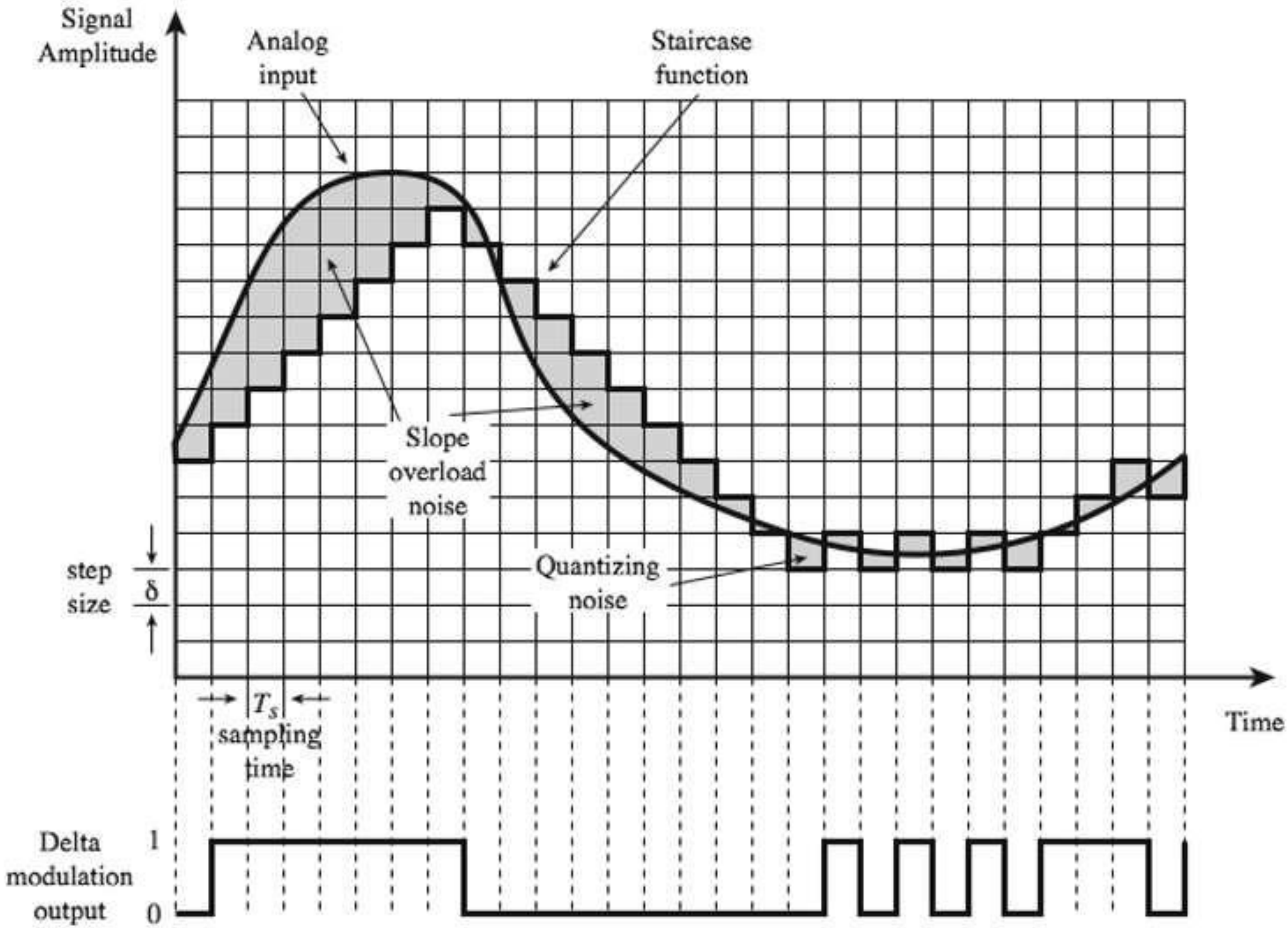
- Quantization levels are not equally spaced
- Reduces signal distortion



Delta Modulation

- Staircase function is used to closely track the analog input waveform
- Staircase function moves up or down by one quantization level (δ) at each sampling interval
- Output is represented by a single binary digit, for each sample
- Receiver
- Reconstructs the staircase function from the received digital data
- Generates analog approximation of the original analog input using some type of integration process or low pass filters
- Performance depends upon- step size (δ) and sampling rate

Delta Modulation



Analog Data Analog Signals

- Amplitude Modulation
- Angle modulation
  - Frequency Modulation
  - Phase Modulation

Amplitude Modulation

- The modulated signal can be expressed as

  $s(t) = [1+ m(t)/A_c]\cos 2\pi f_c t$

  $= [1+(A_m/A_c).\cos 2\pi f_m t]\cos 2\pi f_c t$

  $=[1+n_a. \cos 2\pi f_m t]\cos 2\pi f_c t$

  $=[1+n_a. x(t)]\cos 2\pi f_c t$

  n_a is modulation index

- After expansion

  $s(t) = \cos 2\pi f_c t + n_a/2 \cos 2\pi(f_c-f_m)t + n_a/2 \cos 2\pi(f_c+f_m)t$
- This scheme is also known as double sideband transmitted carrier (DSBTC)

Angle Modulation

- The modulated signal can be expressed as

  $s(t) = A_c \cos[2\pi f_c t + \phi(t)]$

Phase Modulation

$\phi(t) = n_p m(t)$

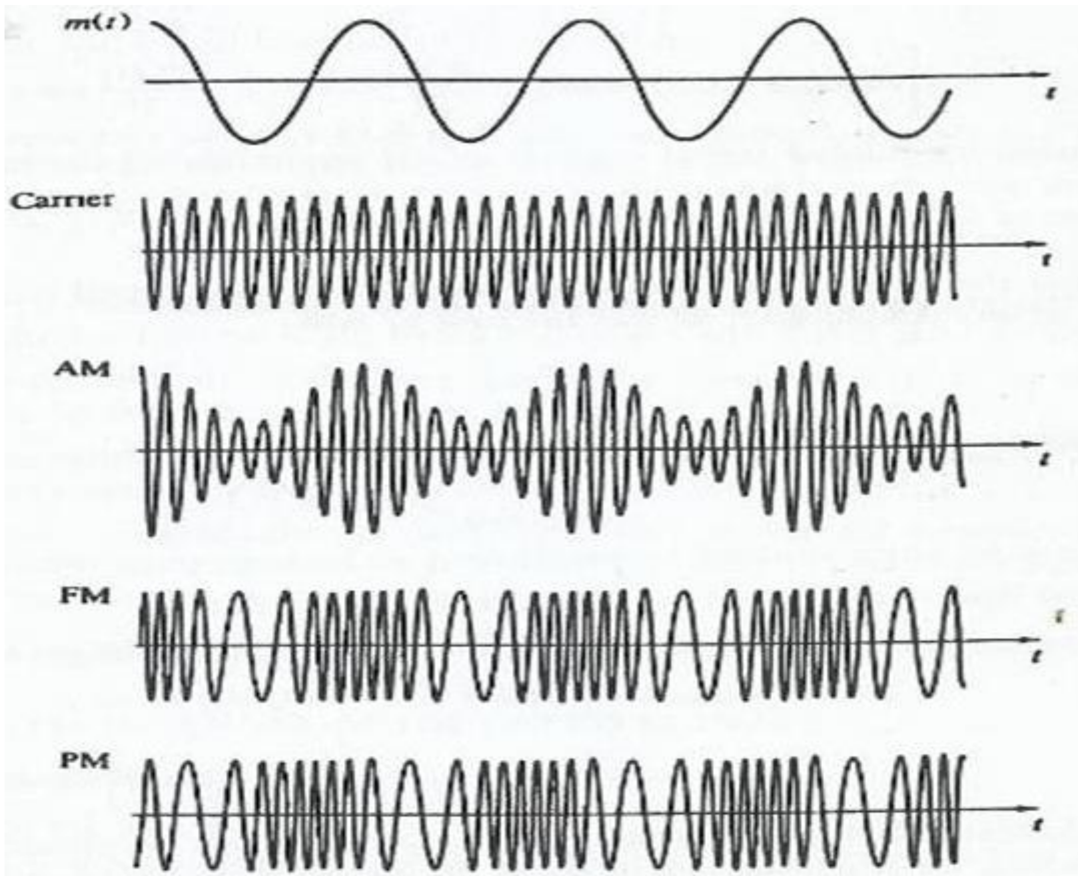
n_p is phase modulation index

Frequency Modulation

$\phi'(t) = n_f m(t)$

n_f is frequency modulation index

Amplitude, Frequency and Phase Modulation



Transmission Bandwidth

$$\text{AM:} \qquad B_T = 2B$$

$$\text{PM / FM:} \qquad B_T = 2(\beta + 1)B$$

$$\text{where} \qquad \beta = \begin{cases} A_m n_p & \text{for PM} \\ A_m n_f \big/ 2\pi B & \text{for FM} \end{cases}$$

and $\quad A_m$ is the maximum value of $m(t)$

Module III

- Digital Data Communication
  - Synchronization
  - Error Detection
  - Error Correction

Synchronization

For proper sampling receiver should know

- Arrival Time
- Bit Duration

Serial Transmission

Signal elements are transmitted serially

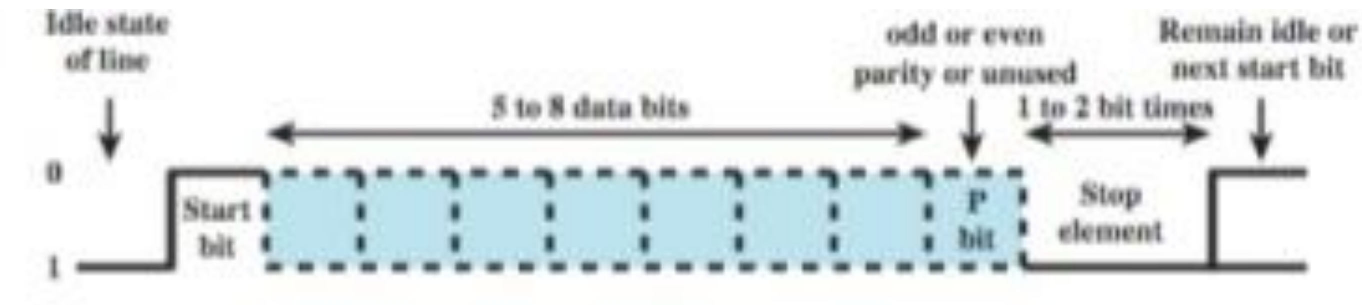
Each signal element may be

- Less than one bit
- One bit
- More than one bit

Asynchronous Transmission

- Transmission takes place character by character
- Each character begins with a start bit (binary 0)
- Bits of the character are transmitted (followed by a parity bit) starting with LSB
- Idle state, stop element is transmitted which is signal element for binary 1
- Minimum length of stop element is fixed

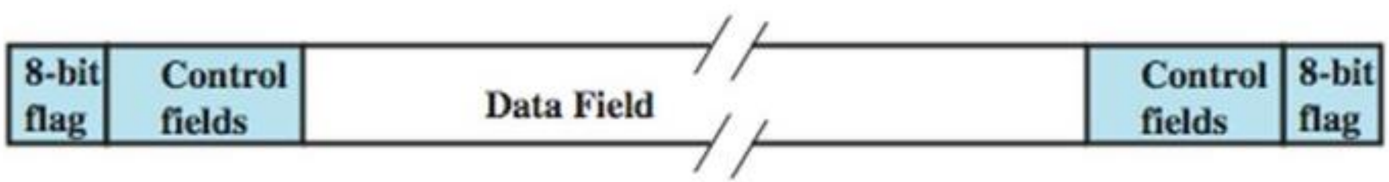
Asynchronous Transmission



- Inefficient transmission (overhead of 2-3 bits per character)
- Noise can cause false appearance of start bit
- Sometimes, there can be framing error

Synchronous Transmission

- A block of bits is transmitted in a stream
- Synchronization between sender and receiver clock is achieved either by sending separate clock signal or by embedding clocking information in the data signal
- Each block begins with preamble bit pattern and ends with postamble bit pattern
- Block also contains link layer control information



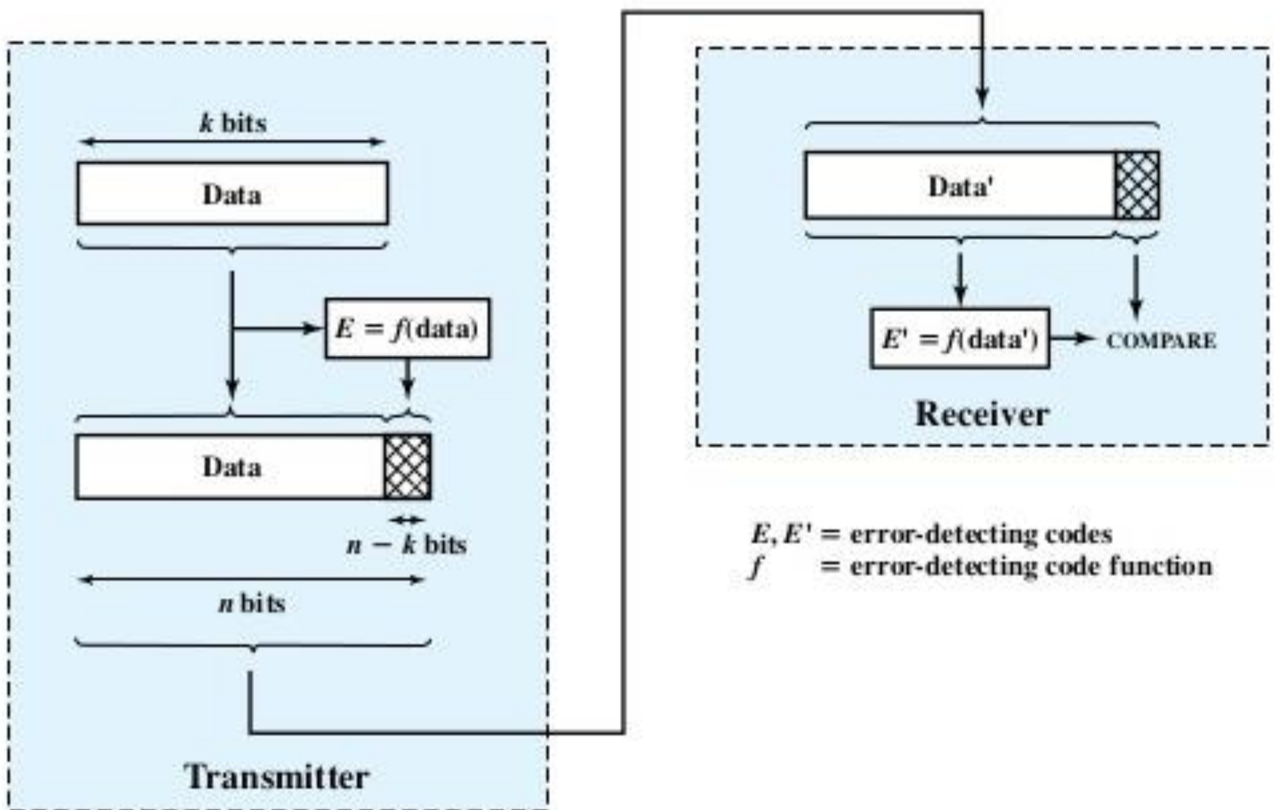
Types of Errors

- Bits get altered due to transmission errors
- Single Bit Error- occurs in the presence of white noise
- Burst Error- when a contiguous sequence of bits gets affected or a cluster of bits with a number of error bits in the cluster
- Burst errors are caused by impulse noise and its effects are more at higher data rates

Error Detection

- Error Detection Codes/ Check Bits- Additional bits for error detection added to a given frame of bits
- Code is calculated as a function of transmitted bits
- Receiver performs error detection code calculation on the data bits and compares the result with the received check bits
- If there is mismatch then there is error, otherwise either there in no error or error is undetected

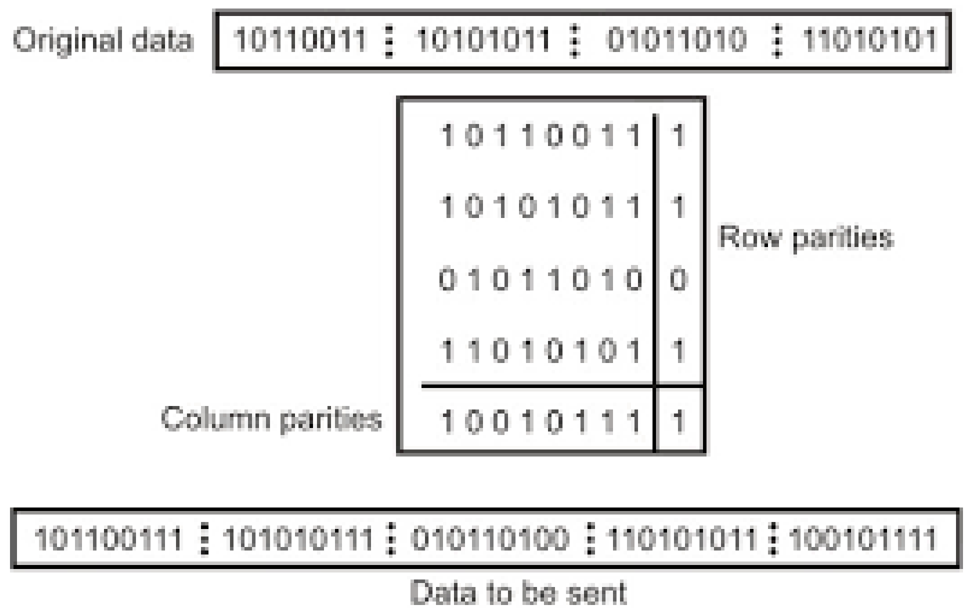
Error Detection Process



Parity Check

- Even Parity- A parity bit is added to the end of data block to make the total number of 1’s even
- Odd Parity- A parity bit is added to the end of data block to make the total number of 1’s odd

Block parity can be used for sending frames with multiple characters



Cyclic Redundancy Check

Cyclic Redundancy Check (CRC)

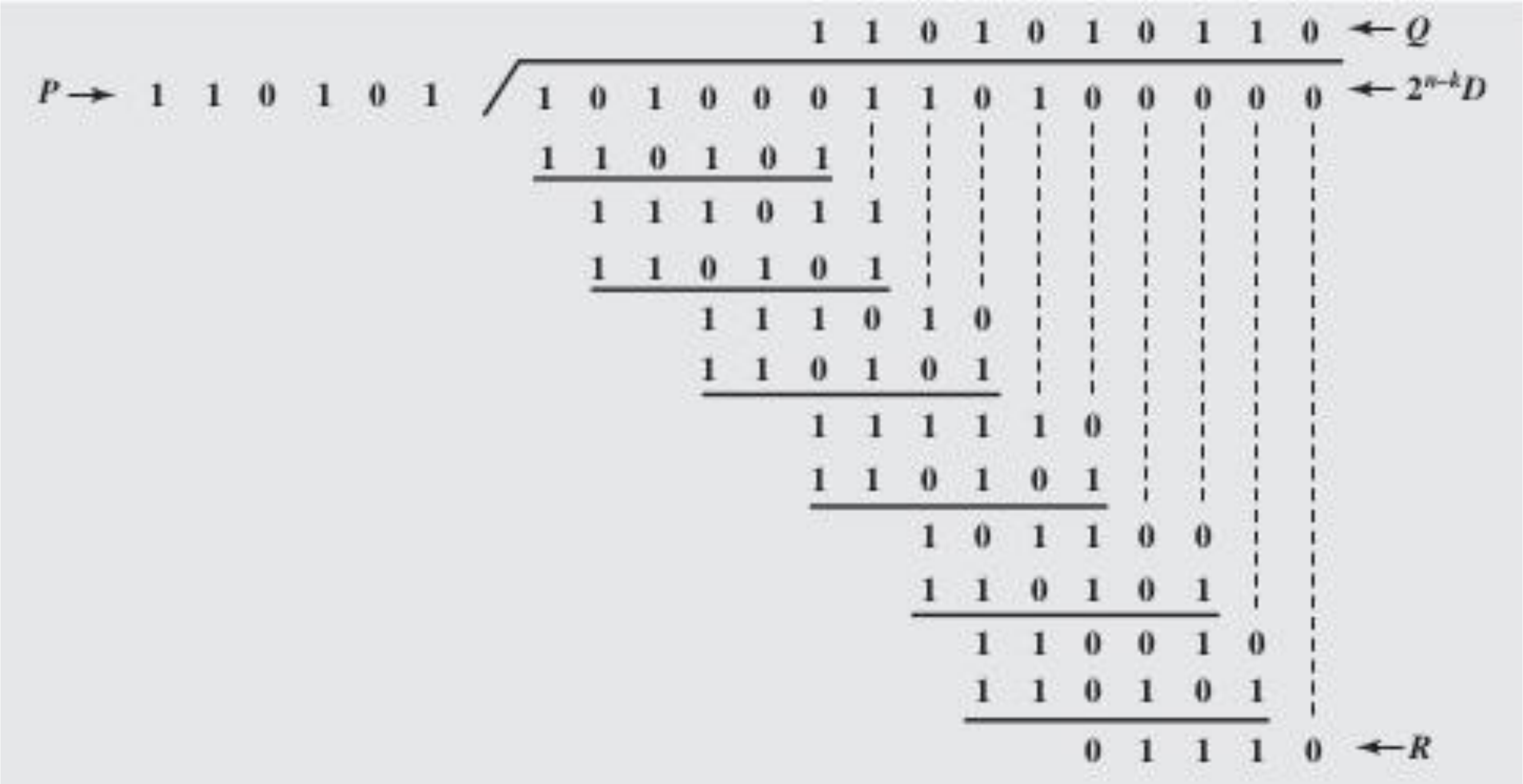
- One of the most powerful error detection codes
- To the k bits of data (n-k) bits frame check sequence (FCS) is appended, so that the resulting n bits is exactly divisible by a predetermined divisor
- To detect error, receiver divides the received frame of n bits by the same divisor
- Assumes no error if the remainder is 0

Frame Check Sequence

FCS Calculation

- Left Shift k-bits of data by (n-k) bits
- Divide by P, predetermined divisor of (n-k)+1 bits
- Remainder R of length (n-k) bits is FCS

FCS Calculation



Error Detection using CRC