112 Fall EE3235 Analog Integrated Circuit Analysis and Design I

Final Project

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In this project, we are to design and analyze a 6-bit analog-to-digital converter (ADC) combined with a bandgap reference as the supply, the system architecture is shown below:

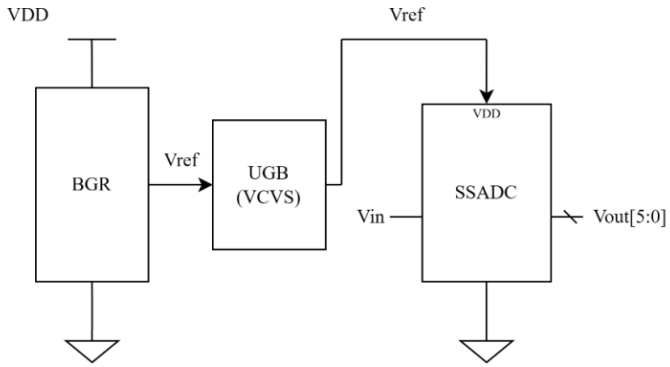


Fig. 1. ADC and bandgap reference.

PART I – Bandgap Reference

Bandgap reference circuits are widely used to generate a 'temperature-independent' voltage supply for power-sensitive circuits, in this part, we will design a bandgap reference circuit based on the schematic shown below and try to meet all specifications in table. 1.

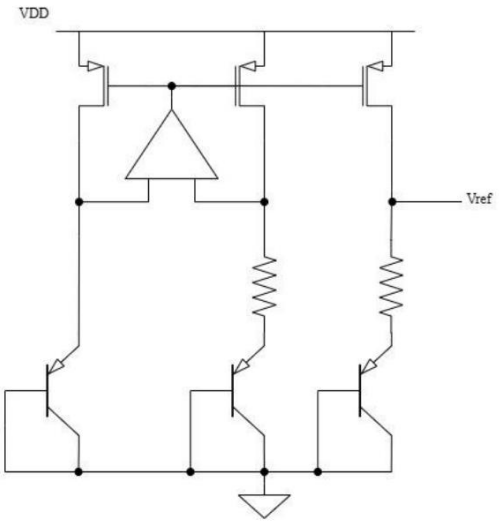


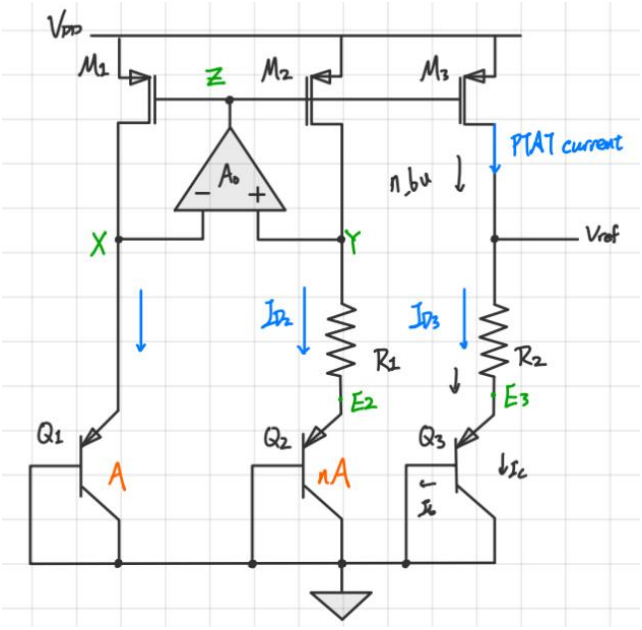
Fig. 2. Opamp-based BGR.

Bandgap Reference							
Working Item	SPEC			Your Work			
Supply Voltage V_{DD}	1.98V	1.8V	1.62V		1.98V	1.8V	1.62V
T.C from -40~125℃ (ppm/℃)	<20ppm/℃			TT	15.93	15.34	16.92
				SS	15.66	15.21	16.89
				FF	15.61	15.16	17.01
Bandgap Voltage (V)				TT	1.3653	1.3643	1.3621
V_{DD}	1.8V, -40~125℃						
PSR @ DC (dB)	< -40dB			TT	-40.3965~-45.3518		
				SS	-40.433 ~-45.9916		
				FF	-40.5761~-45.2817		
PSR @ 10KHz (dB)	<-30dB			TT	-40.3892~-45.5718		
				SS	-40.4304~-46.9277		
				FF	-40.560 ~-45.3433		
V_{DD}	1.8V, 27℃, TT						
Power Consumption (μW)	<50μW			34.2511μ			

Table. 1. Bandgap reference SPECs

1. Design Consideration

- ***Bandgap Reference***



(a) Determine the ratio of the two resistors through calculation and calculate the expected V_{ref}. (Here I use ideal op-amp first to ensure that the BGR meet the SPEC of T.C. The op-amp will be design later.)

Assume Q_1 and Q_2 are identical ($I_{c1} = I_{c2}$):

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln\left(\frac{nI_{c1}}{I_s}\right) - V_T \ln\left(\frac{I_{c2}}{I_s}\right) = V_T \ln n$$

And since the current mirror:

$$I_{D1} \approx I_{D2} = \frac{V_T \ln n}{R_1}$$

Then we can get:

$$V_{ref} = V_{BE3} + \frac{R_2}{R_1} V_T \ln n$$

For zero T.C. we need to satisfy:

$$\frac{\partial V_{ref}}{\partial T} = 0 = \alpha_1 \frac{\partial V_{BE3}}{\partial T} + \alpha_2 \frac{\partial V_T}{\partial T} \ln n \ , where\ \alpha_1 = 1 \ , \alpha_2 = \frac{R_2}{R_1}$$

After running the operation point analysis on a single BJT, we get $V_{BE} \approx$ 0.65~0.68, then we can get $\frac{\partial V_{BE}}{\partial T} \approx -1.9mV/°K$, $\frac{\partial V_T}{\partial T} \approx 0.087mV/°K$

So, we need to satisfy $\alpha_2 \ln n = \frac{\partial V_{BE}}{\partial T} \div \frac{\partial V_T}{\partial T} \approx 24.6$.

Choose n=8, then $\alpha_2 = \frac{R_2}{R_1} \approx 12.3$

Here we should decide the resistance, let's move on to part (b) for deciding the resistance of R_1 and R_2 then back to (a) for calculating V_{ref} .

From (b) $R_1 = 100k\Omega$ then we can get:

$$V_{BE3} = V_T \ln\left(\frac{I_{c3}}{I_s}\right) = V_T \ln\left(\frac{V_T \ln n}{R_1} * \frac{\beta}{1+\beta} * \frac{1}{I_s}\right) \approx 0.67V$$

Then,

$$V_{ref} = V_{BE3} + \frac{R_2}{R_1} V_T \ln n \approx 1.3596V$$

(b) Power consumption <$50\mu W$

For power consumption, we should satisfy:

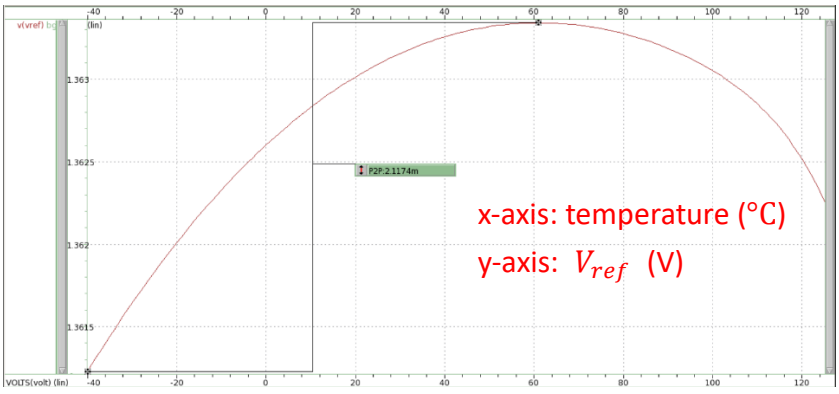
$$(I_{D1} + I_{D2} + I_{D3}) * 1.8 < 50\mu W \rightarrow I_{D1} \approx I_{D2} \approx I_{D3} < 9.26\mu A$$

Since we also have to consider the power of start-up circuit with gm-biasing, so our power in this part can't be too high. We need to choose bigger resistance.

Choose $R_1 = 100k\Omega$, $I_{D1,2,3} \approx \frac{V_T \ln n}{R_1} \approx 0.54\mu A$

Choose $R_2 = 1230k\Omega$ since $\alpha_2 = 12.3$.

But since the T.C may be sensitive to the ratio of resistance, we should fine-tune the resistance of R_2 to get the result close to zero T.C.



$T.C. \approx 15.2ppm$

Final value: $R_2 = 1232k\Omega$

(c) Sizing the transistors ($M_1 \sim M_3$)

We assume that $M_1 \sim M_3$ are identical for above analysis. Assume that the mobility ratio between electrons and holes to be 1:3, set the width of NMOS and PMOS to be 1:3. By channel length modulation, we can know that L is inversely proportional to λ, and by $r_o = \frac{1}{\lambda I_D}$, we can know that increase L will linearly increase r_o. Since the schematic like a two-stage cascade amplifier, we may assume the gain formula:

$g_m r_o = \frac{2I_D}{V_{in}-V_{th}} \times \frac{1}{\lambda I_D} = \frac{2}{\lambda(V_{in}-V_{th})}$ with $g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L}}$, we know that the effect of L to g_m is smaller than λ, so increase L can also increase A_v also decrease the effect of channel length modulation.

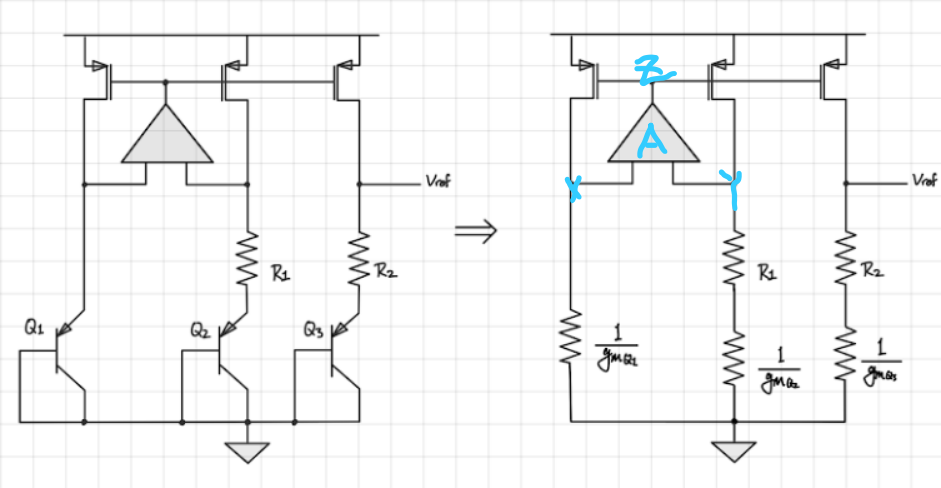
I let the size of PMOS $M_1 \sim M_3$ be 27u/9u. The reason why I use the larger length is that it can decrease the channel length modulation and enhance stability by some characteristics. Like the lower sensitivity to process variations. Larger transistors are generally less sensitive to manufacturing process variations, like oxide thickness, doping levels. It also can reduce the short-channel effects. We can know that short-channel effects become more prominent in smaller transistors, and it can impact the stability of the transistor's operation. So larger transistors with longer channel lengths, are less affected by these short-channel effects, providing more stable characteristics. In addition, it can also reduce parasitic capacitance since the larger transistors tend to have lower parasitic capacitances.

(d) PSR (Power Supply Rejection) is an important indicator for evaluating the quality of a bandgap reference circuit.

At **DC**: Power Supply Rejection Ratio

At **AC**: Power Supply Ripple Rejection Ratio

Please analyze the aspects through which PSR can be improved and how the gain of the op-amp would affect PSR. Here we re-construct the circuit like below:



Let's compute the resistance see from emitter to collector of BJT, assuming that $r_\pi \to \infty$, then the input resistance of BJT, R_{in} reduces to $\frac{1}{g_{m,Q}}$. Since a MOSFET is similar to a BJT with a r_π infinite, this makes a BJT have the similar input resistance like MOSFET $\frac{1}{g_{m,Mos}}$. Now we can start to discuss the circuit above:

$$\Delta V_X = g_{m1}(\Delta V_Z - \Delta V_{DD})(\frac{1}{g_{m,Q1}} \parallel r_{o1})$$

$$\Delta V_Y = g_{m2}(\Delta V_Z - \Delta V_{DD})(R_1 + \frac{1}{g_{m,Q2}} \parallel r_{o2})$$

Then,

$$(\Delta V_Y - \Delta V_X) * (A\text{: } Gain\ of\ Opamp) = \Delta V_Z$$

$$\to g_m(\Delta V_Z - \Delta V_{DD})R_1 * A = \Delta V_Z$$

$$\to (g_m R_1 * A - 1) * \Delta V_Z = g_m R_1 * A * \Delta V_{DD}$$

$$\to \frac{\Delta V_Z}{\Delta V_{DD}} = \frac{g_m R_1 * A}{g_m R_1 * A - 1} \to (\Delta V_Z - \Delta V_{DD}) = \frac{\Delta V_{DD}}{g_m R_1 * A - 1}$$

Then we can get the formula:

$$\Delta V_{ref} = g_{m3}(\Delta V_Z - \Delta V_{DD})(R_2 + \frac{1}{g_m} \parallel r_{o3})$$

After all, we can use the formula of PSR, if we want to achieve:

$$PSR = 20\log\frac{\Delta V_{ref}}{\Delta V_{DD}} < -40dB$$

Our ratio $\frac{\Delta V_{ref}}{\Delta V_{DD}}$ should be smaller than 0.01.

$$\frac{\Delta V_{ref}}{\Delta V_{DD}} = g_{m3}\left(\frac{1}{g_m R_1 * A - 1}\right)\left(R_2 + \frac{1}{g_m} \parallel r_{o3}\right) \approx \frac{g_{m3}R_2}{g_m R_1 * A - 1} < 0.01$$

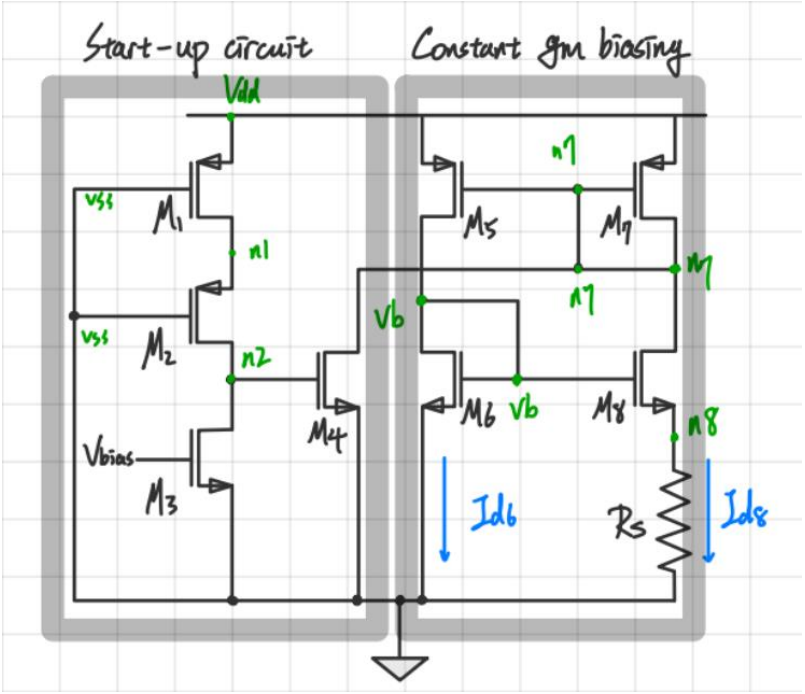
$$\frac{1}{g_m R_1 * A - 1} < 8.2521 * 10^{-4}, with\ g_{m3} = 9.8361\mu, R_2 = 1232k\Omega$$

By the formula above, we can derive the minimal gain we've to achieve:

$$A > 1010.6773\ v/v$$

Thus, for the ideal simulation of BGR, I used E-element of gain 4500, as this not only exceeds the calculation minimum, but also closed to the two-stage op-amp gain from previous homework.

- ***Start-up Circuit with Constant-gm Biasing***

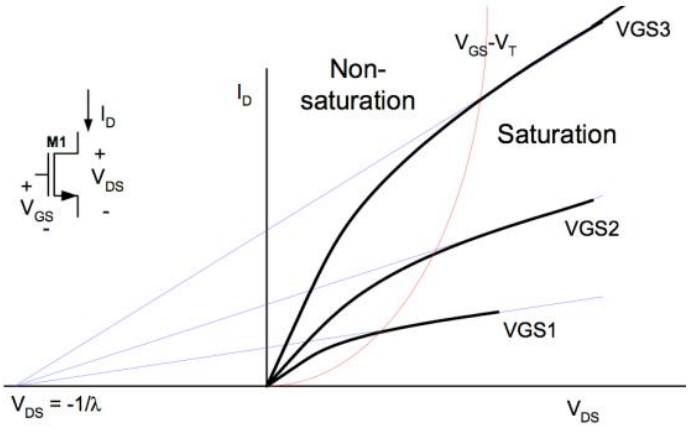


Let's divide this circuit to 2 parts (start-up circuit, constant-gm biasing).

1. *Start-up Circuit*

According to the operation of start-up circuits at low source voltages V_{DD}, the transistors ($M_1 \sim M_4$) would turn-on (into saturation region or subthreshold) to increase the rate of turning on in the constant-gm circuit. The upper two PMOS in the start-up circuit (M_1, M_2) will turn OFF (drop to linear region) when the MOS in the constant-gm biasing circuit turn ON, and they will have the large V_{ov} (since the gate voltage approach to V_{DD}), and according to the formula of drain current in triode region below:

$$I_D = \mu_{n(p)} C_{ox}[(V_{gs} - V_{th})V_{ds} - \left(\frac{V_{ds}}{2}\right)^2](1 \pm \lambda V_{ds})$$

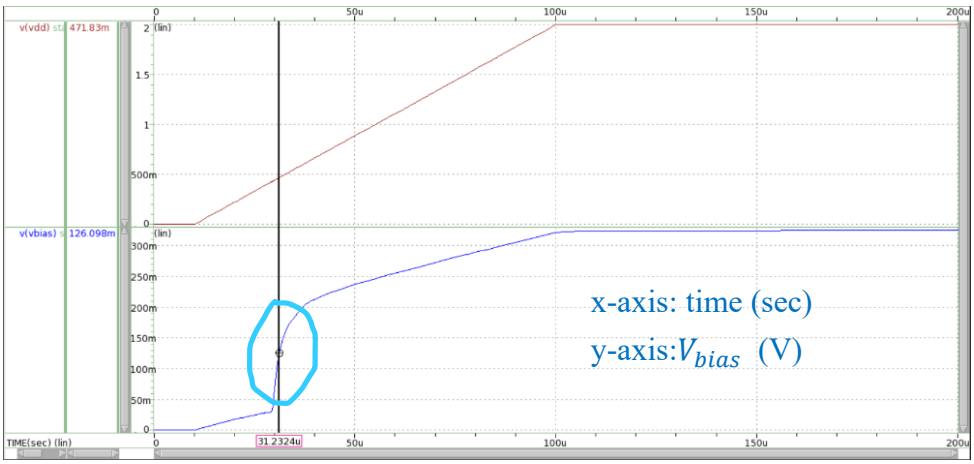


the current will be very large. Thus, by the formula of power below:

$$Power = V_{DD} * I_{total}$$

The power will be large, too. Therefore, I let my W/L be 1/40 for the smaller current and power. For some consideration about area, I let the size of $M_{1,2}$ be 0.9u/12u and $M_{3,4}$ be 0.3/12u, still follows the 3:1 size of PMOS to NMOS from carrier mobility.

If we run a simulation of start-up circuit with constant-gm biasing itself (with voltage divider) to test the operation of this start-up circuit design, we can see the highlight part below; the curve increases rapidly since the start-up circuit turn **ON** at that moment:



We can see that when V_{DD} is around 0.3~0.9V, the V_{bias} has a rapid increase.

Region of start-up transistors currently:

subckt	xstart	xstart	xstart	xstart
element	1:m1	1:m2	1:m3	1:m4
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1
region	Subth	Subth	Saturation	Subth
id	-1.9795n	-1.9792n	1.9800n	226.3956f
ibs	3.810e-25	1.8808a	-1.290e-24	-1.560e-28
ibd	1.8808a	35.3172a	-1.0224a	-1.2248a
vgs	-435.0000m	-412.4135m	321.1024m	10.8814m

2. *Constant-gm Biasing*

Assume that the size of the transistors M_8 is 4 times of M_6, and satisfying the square law, then $V_{ov8} = \frac{1}{2}V_{ov6}$, $I_{d8} = I_{d6} = \frac{V_{ov8}}{R_s}$. By the analysis above, we get $g_{m8} = \frac{2I_{d8}}{V_{ov8}} = 2g_{m6}$.

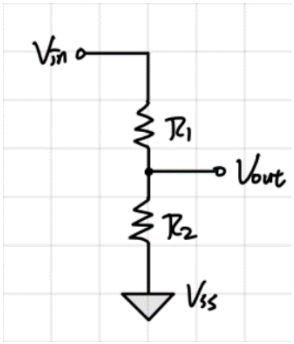
Thus, we can know that our current has the stable g_m. The propose of this biasing method is to maintain a constant transconductance (g_m) for a field-effect transistor or a bipolar junction transistor over variations in temperature and process parameters. The constant-gm biasing circuit adjusts the biasing of the transistor to compensate for variations in temperature and manufacturing process. By keeping the constant, the circuit can achieve better performance in terms of gain, linearity, and overall stability.

By the analysis above, I let the size of PMOS (M_5, M_7) be 3u/1u, NMOS (M_6) be

1u/1u, still follows the 3:1 size of PMOS to NMOS from carrier mobility, and M_8 be 4u/1u by the analysis of constant-gm biasing above.

After running simulations, we get the biasing voltage $V_{bias} \approx 600mV \sim 700mV$. We may need a voltage divider to get a proper biasing voltage for the two-stage op-amp.

- ***Voltage Divider***

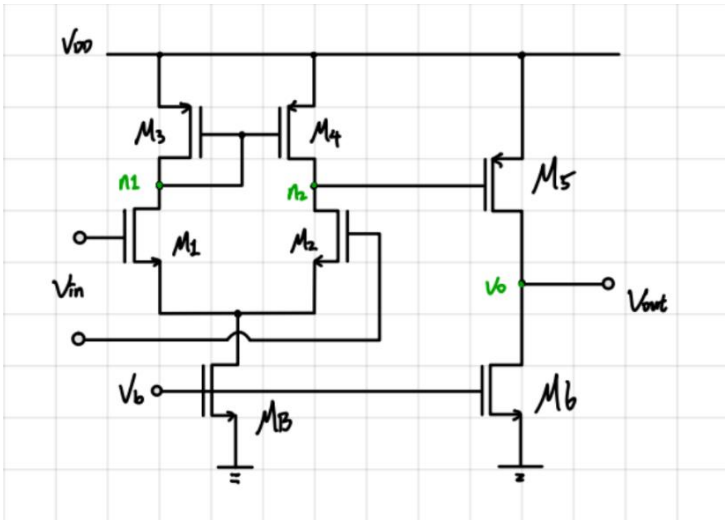


Since we only get one output voltage from constant-gm biasing with start-up circuit, we may have to design a single-ended two-state op-amp with single-biasing voltage. The output from constant-gm core with start-up circuit is around 600mV to 700mV, and since our output voltage is going to biasing the tail transistor in the two-stage op-amp from the next part, we need to lower the output to prevent the power going to high. To get $V_{out} \approx 300mV \sim 350mV$, I let $R_{1,2} = 10M\Omega$, considering the situation that if the resistances of $R_{1,2}$ are too small, it may impact the output resistance of constant-gm biasing circuit. The larger resistance will minimize the current flow, consequently, lowers the unstable effect on the constant-gm biasing circuit. It may also lower the noise on the final output.

- ***Two-stage Op-amp***

Here I design a two-stage op-amp with single-ended and single biasing voltage because we only get single voltage supply from constant-gm biasing circuit.

Upper transistors (M_3, M_4) using the self-biasing voltage.



I used the output voltage from voltage divider we've mention above to lower the biasing voltage, the goal is to make it closer to the threshold voltage V_{TH}, such that we can get the better performance (lower power) by the formula below:

$$I_D = \frac{1}{2}\mu_{n(p)}C_{ox}\left(V_{gs} - V_{th}\right)^2(1 \pm \lambda V_{ds})$$

The two-stage op-amp gain formula:

$$A_v \approx A_{v_{stage1}} \times A_{v_{stage1}} = g_{m4,5}r_{o5,6} \times g_{m8,9}\left(r_{o3,4} \parallel r_{o8,9}\right)$$

Since I used e-element with assuming the output gain >4k, and by the analysis about PSR at previous part, we should try to achieve the output gain of 4k.

I let the length of all PMOS and NMOS be 1u. Following the 3:1 size of PMOS to NMOS from carrier mobility, I set the width of $M_{3,4}: M_{1,2}$ and $M_5: M_6$ be 3:1.

Since we use a voltage divider to get the biasing voltage $V_b \approx 300\sim350mV$ from constant-gm biasing circuit, and satisfying the condition of MOS in saturation:

$$V_{GS} - V_{TH} > 0\,, V_{DS} > V_{GS} - V_{TH}$$

I let the size of M_B be 2u/1u. We can check our gain and operation region now:

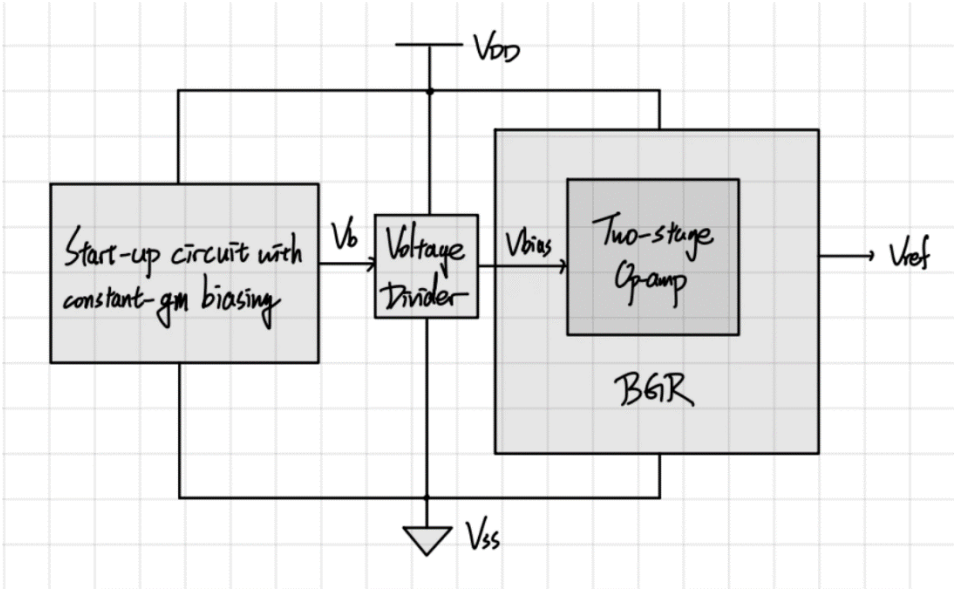
```
****     small-signal transfer characteristics

     v(vo)/vdf                                 =   -4.8119k
     input resistance at             vdf       =  1.000e+20
     output resistance at v(vo)                =   67.9831x
```

xopamp 3:m1 0:n_18.1 Subth	xopamp 3:m2 0:n_18.1 Subth	xopamp 3:m3 0:p_18.1 Subth	xopamp 3:m4 0:p_18.1 Subth	subckt element model region	xopamp 3:m5 0:p_18.1 Subth	xopamp 3:m6 0:n_18.1 Subth	xopamp 3:mb 0:n_18.1 Subth
42.2033n	42.2033n	-42.2050n	-42.2050n	id	-43.1825n	43.1820n	84.4077n
-41.1050a	-41.1050a	5.126e-24	5.126e-24	ibs	5.245e-24	-1.287e-23	-1.877e-23
-198.4930a	-198.4930a	72.7011a	72.7011a	ibd	135.4537a	-147.1497a	-61.3305a
363.1942m	363.1942m	-415.0364m	-415.0364m	vgs	-415.0364m	309.9810m	309.9810m
1.0982	1.0982	-415.0364m	-415.0364m	vds	-773.2786m	1.0267	286.8058m
-286.8058m	-286.8058m	0.	0.	vbs	0.	0.	0.
451.3549m	451.3549m	-498.3869m	-498.3869m	vth	-498.3869m	396.7650m	395.0126m
44.4177m	44.4177m	-47.1166m	-47.1166m	vdsat	-47.1159m	43.1976m	43.1831m
-88.1608m	-88.1608m	83.3504m	83.3504m	vod	83.3504m	-86.7840m	-85.0317m
309.0570u	309.0570u	215.3544u	215.3544u	beta	215.3545u	306.9180u	617.5747u
514.9231m	514.9231m	557.0847m	557.0847m	gam eff	557.0847m	507.4459m	507.4459m
1.1437u	1.1437u	993.2314n	993.2314n	gm	1.0157u	1.1556u	2.2612u
13.3396n	13.3396n	3.0432n	3.0432n	gds	2.5357n	12.1699n	26.8077n
200.7873n	200.7873n	300.6434n	300.6434n	gmb	307.6005n	241.4947n	480.2762n
1.3003f	1.3003f	3.7527f	3.7527f	cdtot	3.4971f	1.3616f	2.9976f
2.3411f	2.3411f	8.4397f	8.4397f	cgtot	8.4380f	2.5529f	5.1213f
1.7666f	1.7666f	5.7938f	5.7938f	cstot	5.7938f	1.9397f	3.7719f
3.4953f	3.4953f	11.1942f	11.1942f	cbtot	10.9389f	3.8865f	7.8992f
576.4336a	576.4336a	2.3798f	2.3798f	cgs	2.3779f	605.9198a	1.2431f
386.9322a	386.9322a	1.0764f	1.0764f	cgd	1.0762f	386.9667a	773.9254a

We can see that the gain has achieve over 4.8k v/v, satisfy the specification we gave from previous part, which is about the calculation of PSR. And our transistors are working at subthreshold region, which is acceptable.

- ***Overall Block Diagram of BGR:***

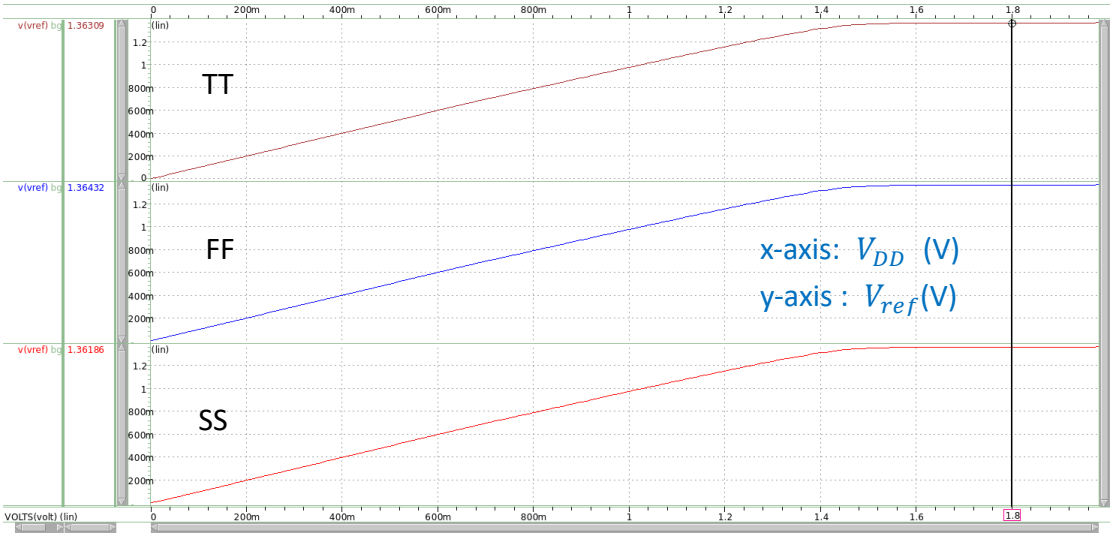


Device Size (Part I)			
Bandgap Reference			
M1 (W/L, m)	(27u/9u, 1)	Q1 (m)	1
M2 (W/L, m)	(27u/9u, 1)	Q2 (m)	8
M3 (W/L, m)	(27u/9u, 1)	Q3 (m)	1
R1 (Ω)	100k	R2 (Ω)	1232k
Start-up Circuit with Constant-gm Biasing			
M1 (W/L, m)	(0.9u/12u, 1)	M5 (W/L, m)	(3u/1u, 1)
M2 (W/L, m)	(0.9u/12u, 1)	M6 (W/L, m)	(1u/1u, 1)
M3 (W/L, m)	(0.3u/12u, 1)	M7 (W/L, m)	(3u/1u, 1)
M4 (W/L, m)	(0.3u/12u, 1)	M8 (W/L, m)	(4u/1u, 1)
Rs (Ω)	110k	----------	----------
Two-stage Op-amp			
M1 (W/L, m)	(1u/1u, 1)	M5 (W/L, m)	(3u/1u, 1)
M2 (W/L, m)	(1u/1u, 1)	M6 (W/L, m)	(1u/1u, 1)
M3 (W/L, m)	(3u/1u, 1)	MB (W/L, m)	(2u/1u, 1)
M4 (W/L, m)	(3u/1u, 1)	----------	----------
Voltage Divider			
R1 (Ω)	10M	R2 (Ω)	10M

2. Simulation Result

(a) .DC

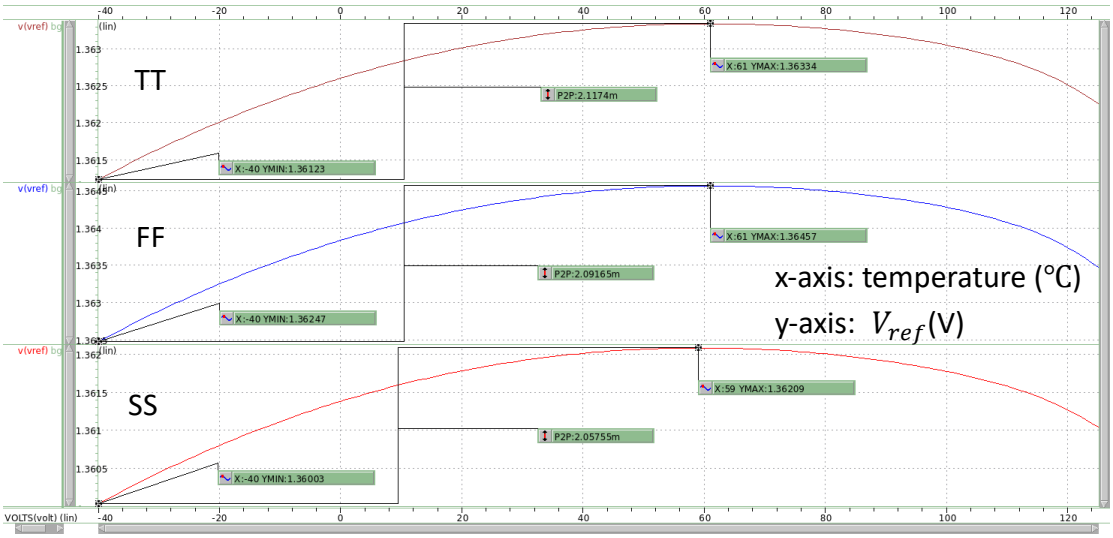
■ Sweep V_{DD} from 0V to 1.98V



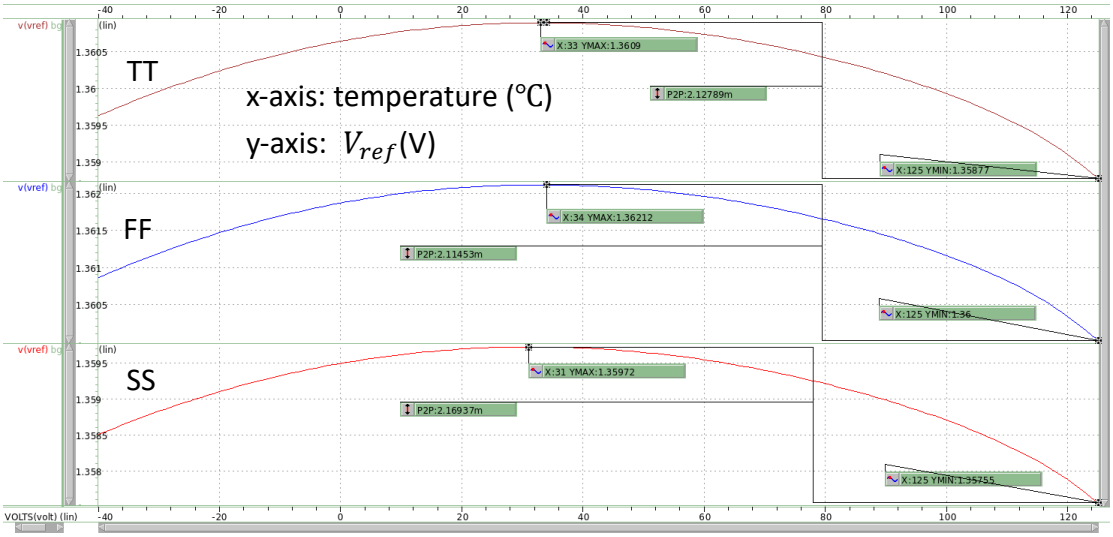
We can see that when V_{DD} is around 1.62V~1.98V, V_{ref} is around 1.36V with a small difference. It shows that the output from BGR is nearly independent to the supply voltage when supply voltage is around 1.62V~1.98V.

■ Sweep the temperature from -40℃ to 125℃ to derive the temperature coefficient.

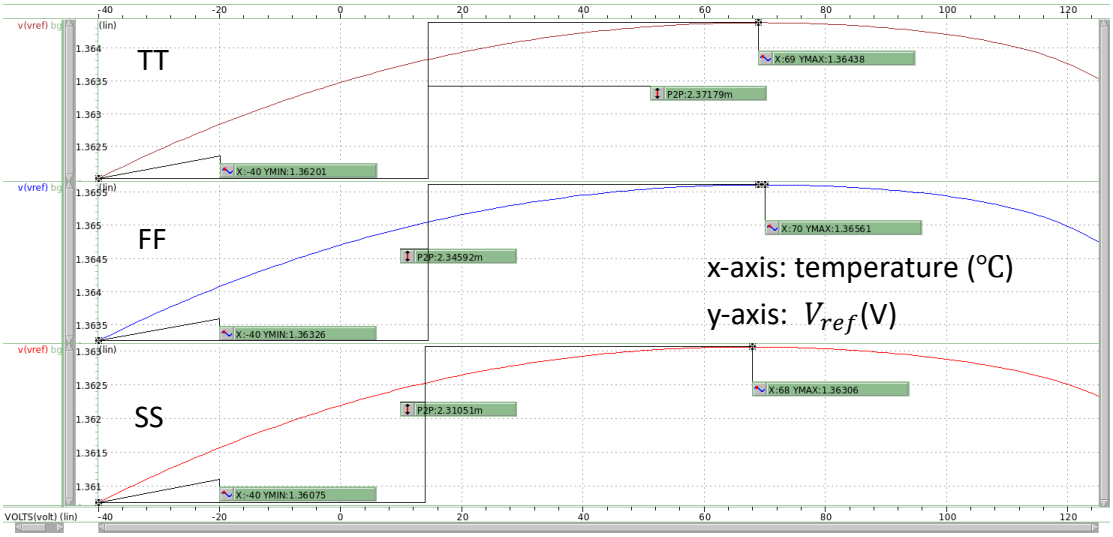
At $V_{DD} = 1.8V$:



At $V_{DD} = 1.62V$:



At $V_{DD} = 1.98V$:



We can observe the 3 figures above and see that whether our design meet the

T.C. requirements by calculate the T.C. using the following formula:

$$Temp.Coeff.(T.C.) = \frac{1}{V_{ref}} \times \frac{V_{max} - V_{min}}{T_{max} - T_{min}}$$

Using the V_{ref} at 27°C:

T.C. = 15.34ppm ($@V_{DD} = 1.8V, TT\ corner$)

T.C. = 15.16ppm ($@V_{DD} = 1.8V, FF corner$)

T.C. = 15.21ppm ($@V_{DD} = 1.8V, SS\ corner$)

T.C. = 16.92ppm ($@V_{DD} = 1.62V, TT\ corner$)

T.C. = 17.01ppm ($@V_{DD} = 1.62V, FFcorner$)

T.C. = 16.89ppm ($@V_{DD} = 1.62V, SS\ corner$)

T.C. = 15.93ppm ($@V_{DD} = 1.98V, TT\ corner$)

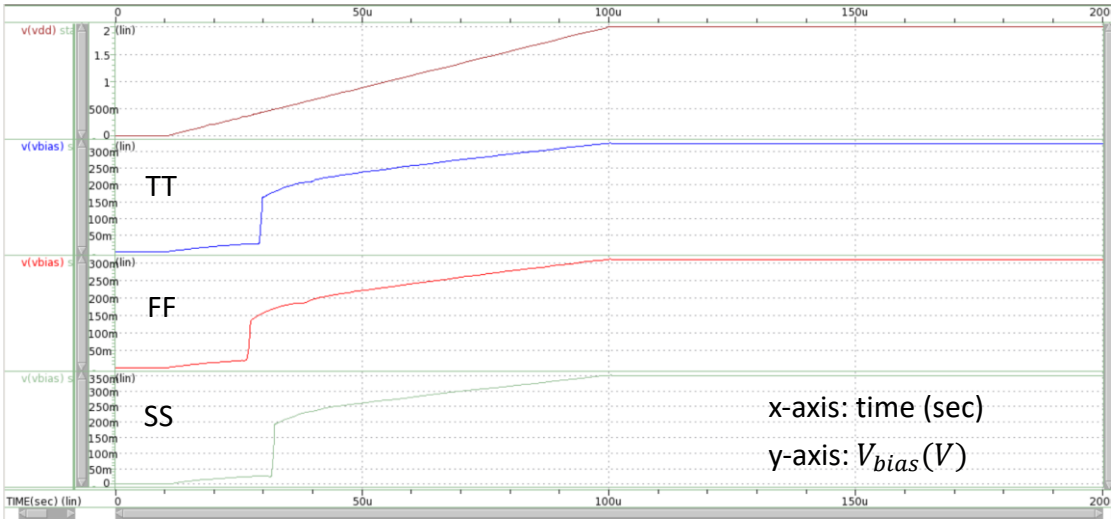
T.C. = 15.61ppm ($@V_{DD} = 1.98V, FFcorner$)

T.C. = 15.66ppm ($@V_{DD} = 1.98V, SS\ corner$)

(b) .Tran

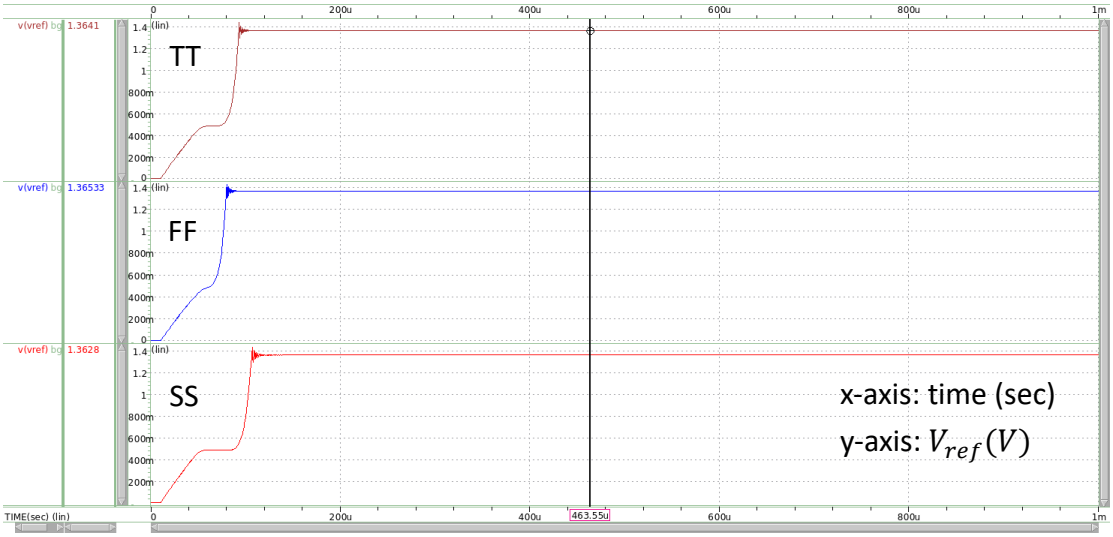
- Check the start-up condition and ensure that the reference voltage is indeed stable.

First, look at the waveform of start-up circuit with constant-gm biasing circuit:



We can see that our V_{bias} have a sharp rise when the supply voltage V_{DD} is around 0.35V to 0.45V, it means that our start-up circuit is operating, increasing the voltage of V_{bias}. Its purpose is to start-up the constant-gm circuit to reach a stable output voltage V_{bias} sooner.

Second, let's look at the output voltage V_{ref} from the overall BGR circuit:



The voltage V_{ref} at three corners stabilizes after $t > 100\mu\ (sec)$. The curvature region is the region which start-up circuit start operating. And we can see the oscillate (unstable) region, constant-gm core circuit will stabilize V_{ref}, and finally remain around 1.364V.

(c) .AC

- Identify the main feedback loop and test the loop stability by the method in HW6.

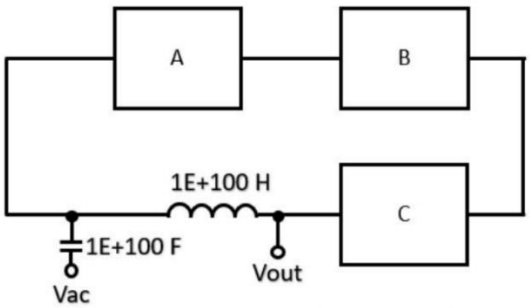
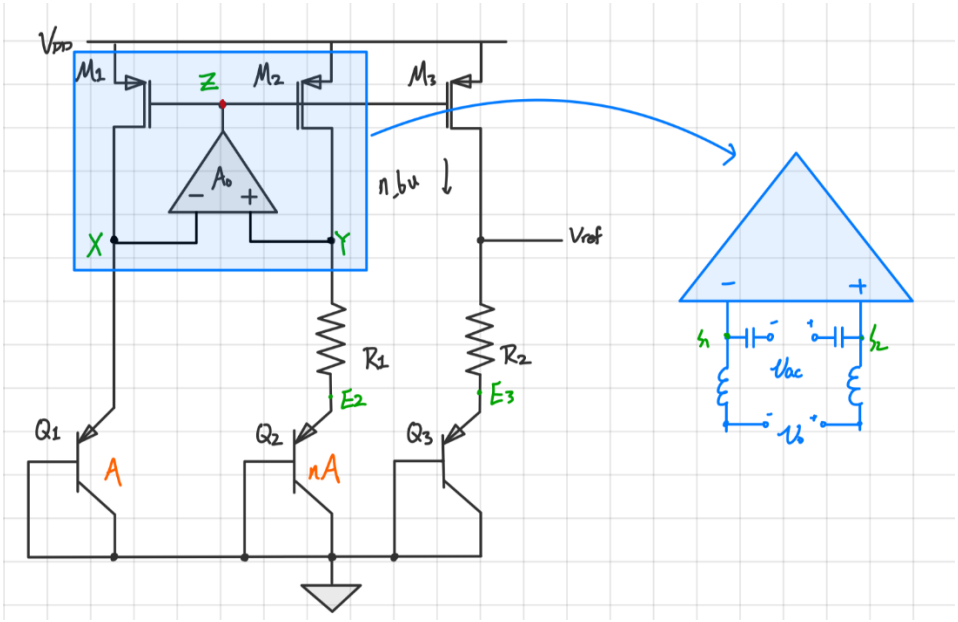


Fig. 4. Frequency Analysis of a Feedback Loop

The way we test the loop stability is shown above. By analyzing the feedback loop of the BGR circuit, the main loop is the loop from two-stage op-amp output V_Z, through the PMOS M_1 and finally back to the input point V_X. To test the stability, we construct our circuit like below.

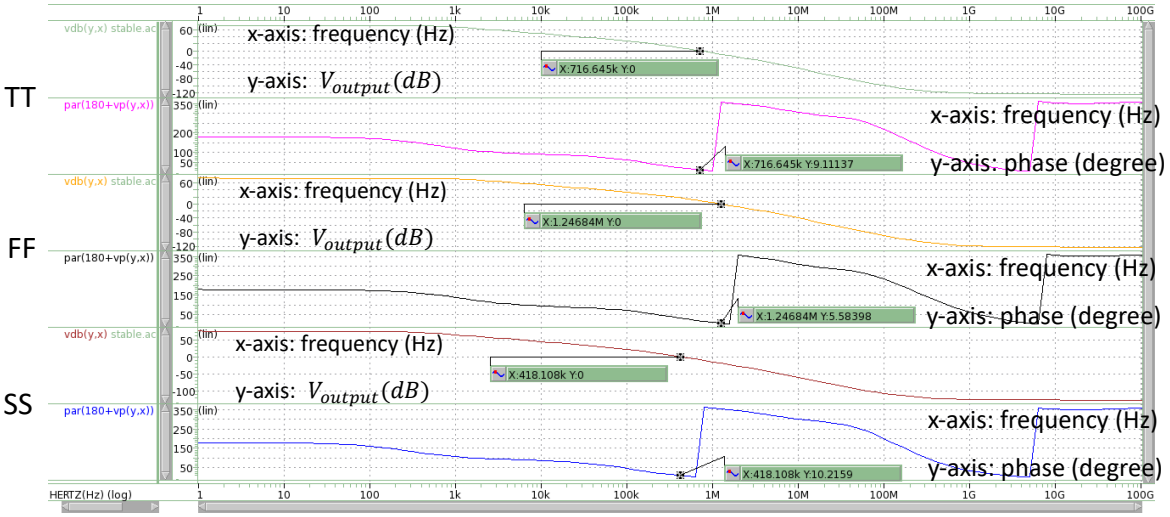


And measure the phase margin:

```
*** Measure the Op-amp output voltage phase margin
.measure ac phase_margin FIND par('180+vp(y, x)') when vdb(y, x)=0
```

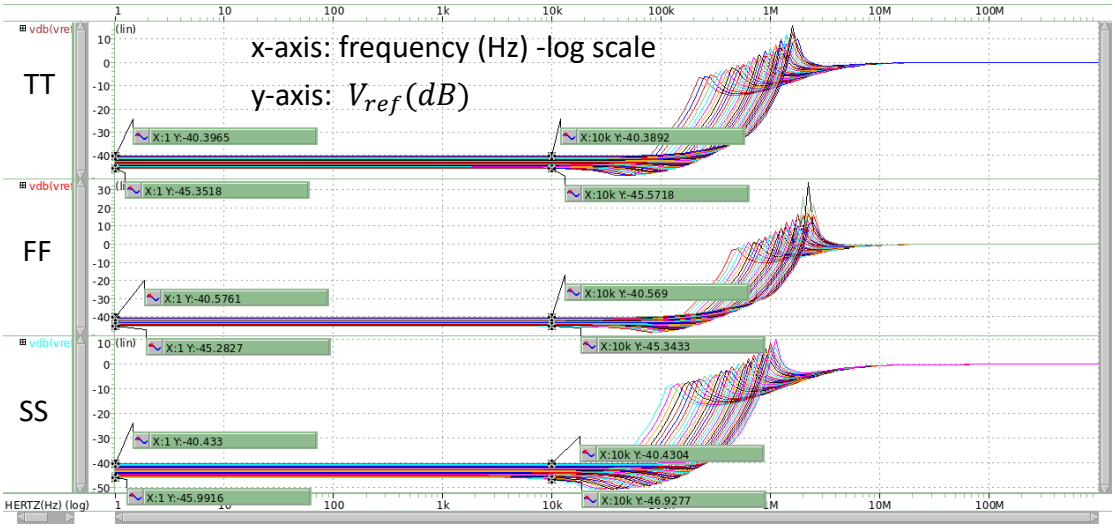
phase_margin	temper	phase_margin	temper	phase_margin	temper
9.1114	27.0000	5.5841	27.0000	10.2159	27.0000

TT FF SS



From the figure above, we can see that before/after gain reaches 0dB, the phase is always positive, ensures that our design remains negative feedback, and place the gain crossover well below the phase crossover, providing stability in the output node.

■ Measure the PSR under different corners and temperatures.



From the previous analysis, we need to design a two-stage op-amp which gain is larger than 1010.6773v/v in order to guarantee the sufficient PSR. We can see the figure above, our design meets the SPEC at 3 different corners (TT, FF, SS).

Part II – Single Slope ADC (SSADC)

Single Slope ADC is a type of ADC with a small area and simple design. In this part, we are to utilize the V_{ref} generated by the bandgap reference designed in Part I as the power supply voltage to design the Single Slope ADC. The block diagram of the SSADC is shown below:

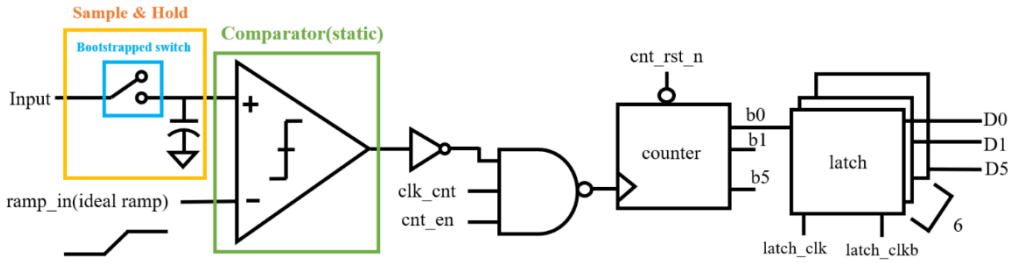


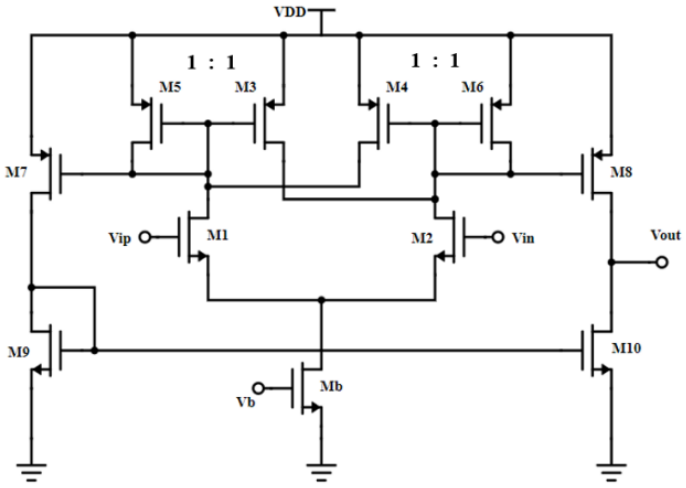
Fig. 5. The block diagram of the Single Slope ADC

In this part, we are about to design a comparator and combine it with the bandgap reference circuit in Part I, eventually, try to meet all the specifications in table. 2

Bandgap Reference + SSADC						
Working Item	SPEC			My Work		
Single Slop ADC input range	$0.95V_{ref}$~$0.25V_{ref}$ (Round to the second decimal place.)					
Supply Voltage V_{DD}	1.8V	1.62V	1.98V	1.8V	1.62V	1.98V
Sampling rate	20kHz					
ENOB	>5bits			5.366	5.366	5.364

Table. 2

1. Design Consideration



(a) Observe the operation of the SSADC and discuss the operational requirements that the comparator must meet.

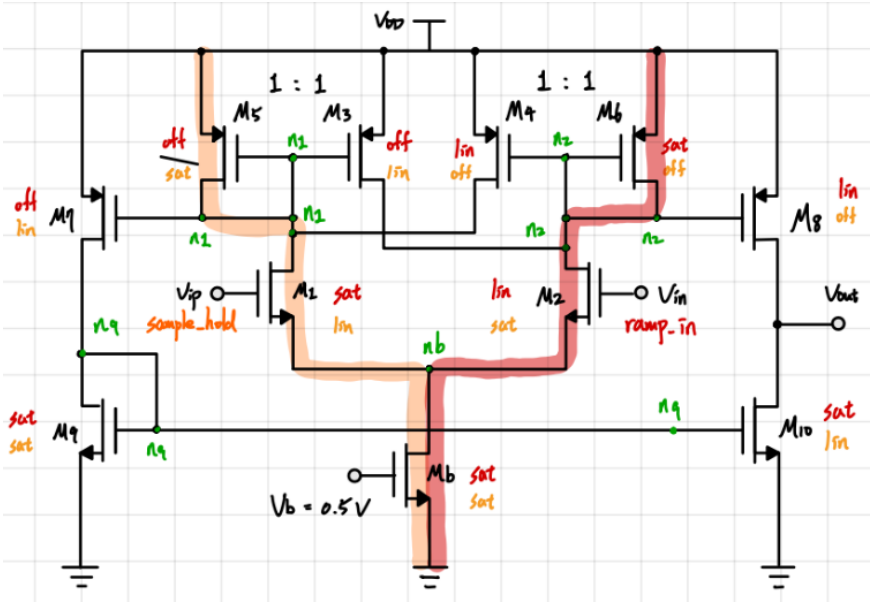
In this part, we are to design a comparator circuit, it scheme is looks like a two-stage amplifier. We can design it like we design amplifier but with the DC input, since when the input voltage to an amplifier is DC, the amplifier can exhibit behavior similar to a comparator under certain conditions. Following the SPEC of the BGR + SSADC, we can see that the given input is around $0.95V_{ref}$~$0.25V_{ref}$, and our V_{ref} output is close to 1.364V, so the input range should be around 0.34V~1.3V. So we need to change the input range in 'final_tb.sp', with 'ramp_max=1.3', 'ramp_min=0.35'.

For the requirement of settling time of the comparator design, we should shorten the output transition time of comparator, which is limited by the period of 'clk'. We should design our comparator with short rise time. The shorter rise time, the better correctness of output. We can take a look at the defined clock frequency:

```
.param cnt_freq=1.594x
```

$f_{clk} = 1.594MHz$, which means that the clock cycle is 627.4n second. So, our goal is to design a comparator with output rise time smaller than 627.4n sec.

(b) Design Flow of Comparator:



The comparator circuit is shown above, it can be seen from that configuration that there is a current-series negative feedback due to the tail transistor at the common source node of $M_{1,2}$ and another voltage-shunt positive feedback due to the cross coupled pair $M_{3,4}$.

When $V_{ramp\_in} \gg V_{sample}$(the red path), M_2 flows more current than M_1, which makes $M_{4,6}$ ON and let $M_{3,5}$ turn OFF. The voltage across M_5 ($V_{DS,5}$) close to zero, which makes the voltage at node n_1 (V_{n1}) be larger.

The secondary gain stage amplifies the differential voltage at node n_1 and n_2 ($V_{n1,n2}$), returns a single ended output voltage at V_{out}.

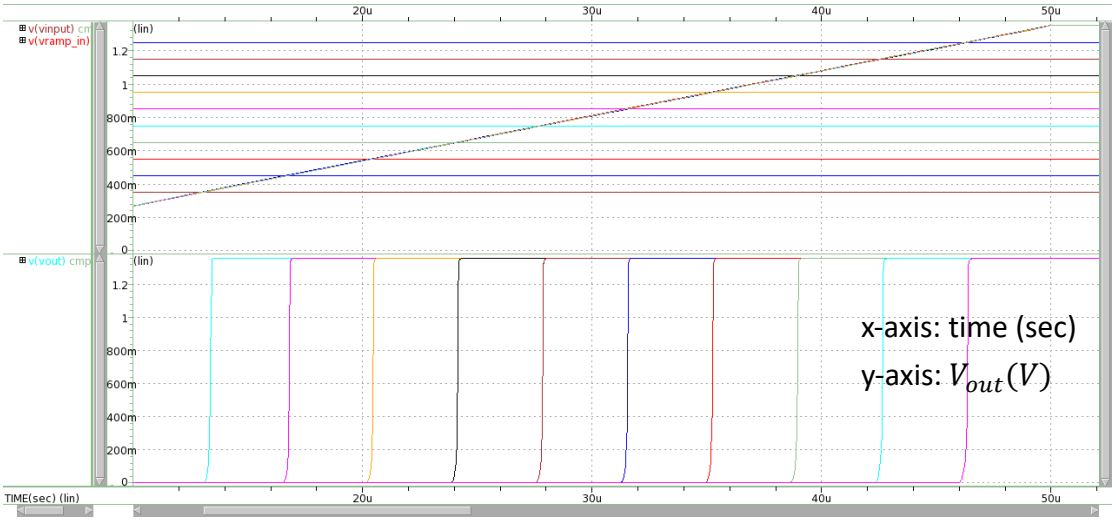
V_{out} will be HIGH, since $V_{n1} > V_{n2}$. And $I_{D,6}$ is approximately equal to tail current.

When $V_{ramp_{in}} \ll V_{sample}$(the orange path), M_1 flows more current than M_2, which makes $M_{3,5}$ ON and let $M_{4,6}$ OFF. And since the voltage across $M_{3,5}$ will lower the voltage at node n_1 (V_{n1}), which makes $V_{n1} < V_{n2}$. Eventually pulls V_{out} to negative rail potential. And I_{D5} is approximately equal to tail current.

When sizing the transistors, we want to maintain a relatively same pull up and down ratio for each node, this prevents a too high or low operating voltage that minimizes the performance of the comparator. By the following formula:

$$I_D = \frac{1}{2}\mu_{n(p)}C_{ox}\left(V_{gs} - V_{th}\right)^2(1 \pm \lambda V_{ds})$$

We may assume that the mobility ratio between electrons and holes to be 1:3 and set the width of NMOS and PMOS to be 1:3 for a fixed current flow through each transistor with similar V_{ov}. Since we want the transistors at second stage be more sensitive such that we can shorten the rise/fall time of V_{out}, I let the size of $M_{7,8}$ be 9u/0.3u and $M_{9,10}$ be 0.3u/9u, such that the PMOS $M_{7,8}$ will have the larger variation (current) according to the current formula. I chose a unit size of 0.3um as a smaller transistor shrinks the distance that a carrier needs to move between gates, increasing the switching speeds of the comparator. We can run some simulations to check whether comparators acting normally at the input range of 0.35V to 1.3V:



From the figure above, since I want to prevent the situation that comparator can't have the sufficient short rising/falling time, I run a simulation of transient response to see whether comparator have the similar rising/falling rime at every point in the range from 0.35V~1.3V. From the result we can see that the rise time

of V_{out} is similar and the delay time is minimum under different V_{input}. This means that our comparator design is capable of operating at different V_{input} voltages with almost no effect in performance.

Size of Transistors in Comparator			
M1 (W/L, m)	(3u/0.3u, 1)	M7 (W/L, m)	(9u/0.3u, 1)
M2 (W/L, m)	(3u/0.3u, 1)	M8 (W/L, m)	(9u/0.3u, 1)
M3 (W/L, m)	(9u/0.3u, 1)	M9 (W/L, m)	(0.3u/9u, 1)
M4 (W/L, m)	(9u/0.3u, 1)	M10 (W/L, m)	(0.3u/9u, 1)
M5 (W/L, m)	(9u/0.3u, 1)	MB (W/L, m)	(9u/9u, 1)
M6 (W/L, m)	(9u/0.3u, 1)	----------	----------

2. Measure the ENOB

Utilize the provided 'final_tb.sp' file to run the .tran simulation and use WaveView to export waveform simulation data. Finally, use the provided MATLAB code to calculate ENOB (Effective Number of Bits)

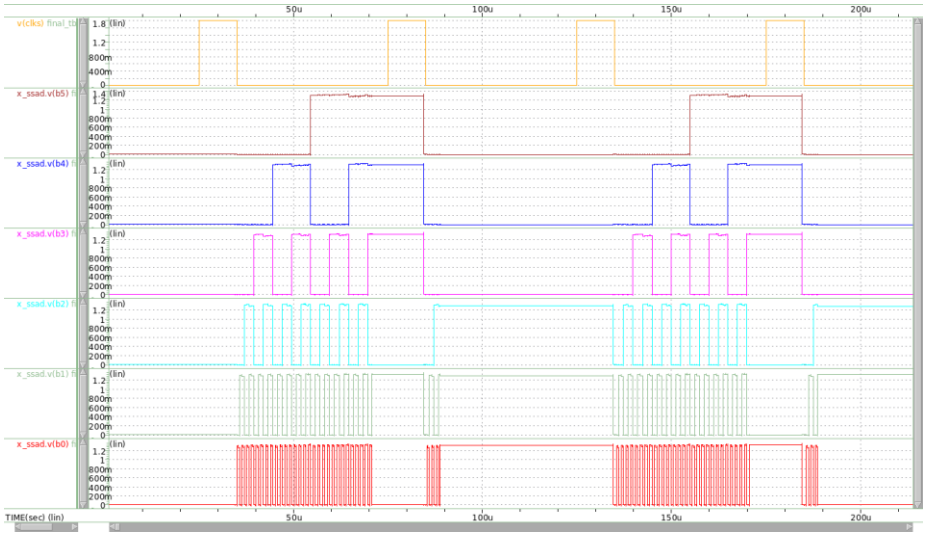
All following measurements are using the same testbench value with NFIN=511; NSAMPLE=1024, with VCNT_EN and VCNT_ENb set to 0.78*Ts for avoidance of overflow.

Following figure shows the waveforms of sample&hold with the ramp_in signal, and the output of comparator:

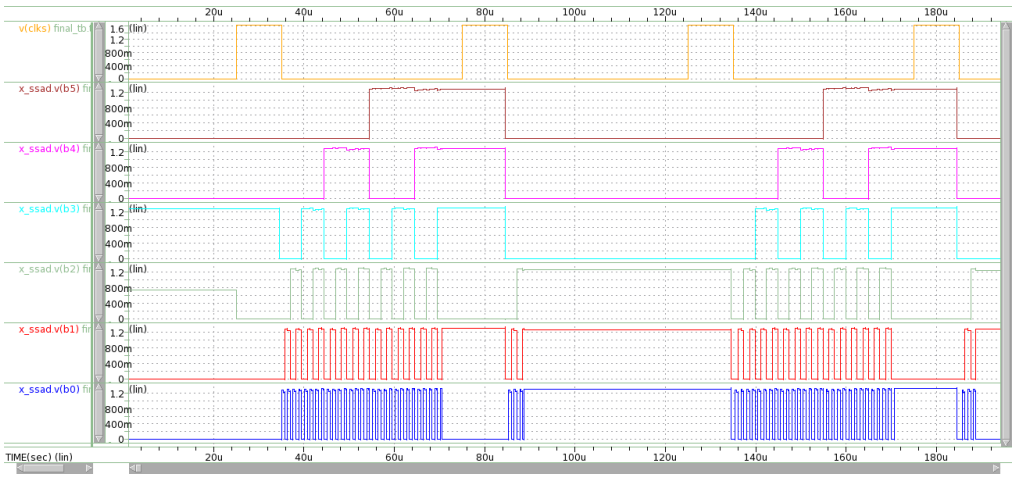
We can see the rise time of comparator is 150.579n (sec).

Grab the signals (b5~b0) to see the pattern:

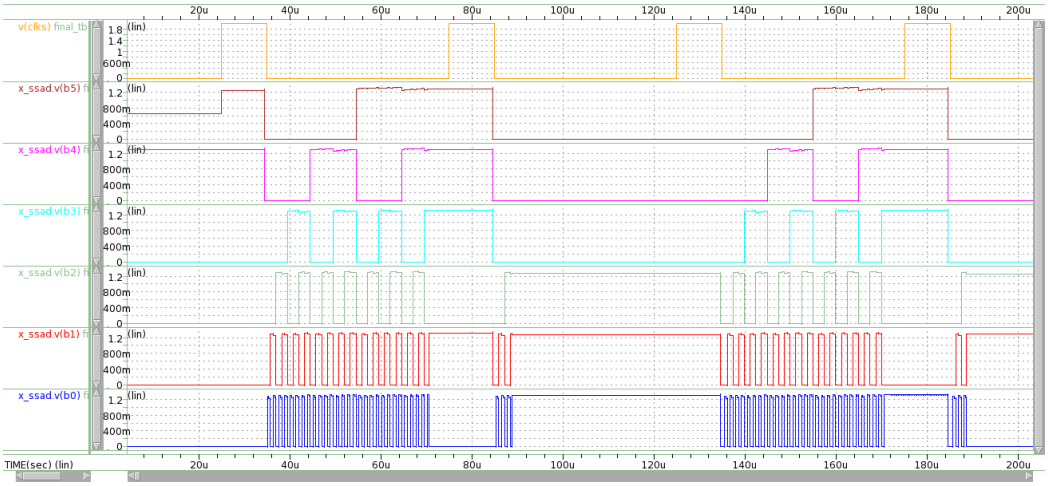
At $V_{DD} = 1.8V$



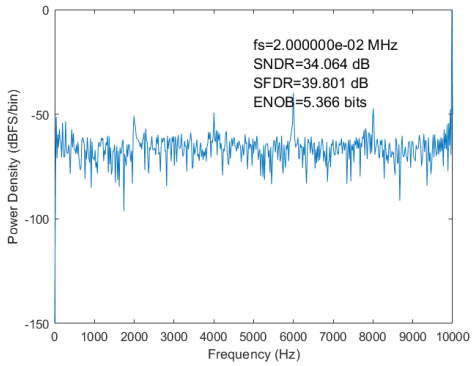
At $V_{DD} = 1.62V$



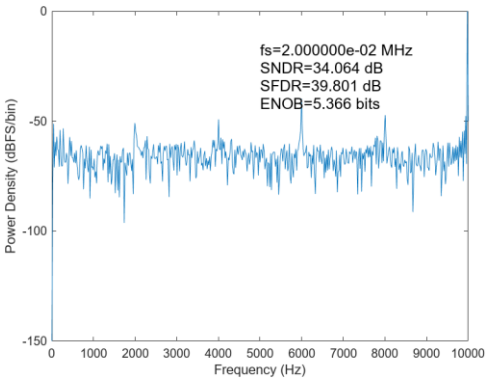
At $V_{DD} = 1.98V$



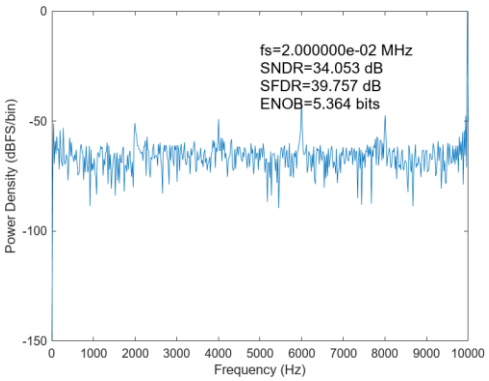
The following simulation exhibit 1028 data points, which is bigger than the request (1024).



$V_{DD} = 1.8V$
ENOB 5.366 bits



$V_{DD} = 1.62V$
ENOB 5.366 bits



$V_{DD} = 1.98V$
ENOB 5.364 bits

From the measurements and MATLAB calculations above, we can see that our results are very close to each other. Its possible reason is because that our output voltage V_{ref} of BGR is almost the same when the supply voltage V_{DD} is different (1.62V, 1.8V, 1.98V). This proves that our effectiveness of BGR and performance of comparator design.

Part III – Experience Sharing

I put in a tremendous amount of effort into our final project, particularly during the HSPICE testbench simulations. Due to various issues with EE workstations, I ended up running the 'final_tb.sp' simulation a total of fifteen times. The process was truly agonizing, with challenges of different magnitudes arising each time. However, the immense sense of accomplishment I felt when seeing the correct results made it all worthwhile.

As the semester draws to a close, I reflect upon the enriching experience of delving into the intricacies of electronic circuits. The journey encompassed various crucial concepts such as MOSFETT, Gain Stage, Operational Amplifier, and Bandgap Reference, which are relative to every homework this semester.

The HSPICE testbench simulations proved to be a formidable challenge. Running the simulations multiple times, a total of fifteen to be exact, become a test of patience and perseverance. Issues ranging from workstation unexpected errors, and some problems about testbench setup added layers of complexity. But the design flow, couple with some challenges encountered in HSPICE simulations has been a transformative experience.

I extend my gratitude to the professors, course TAs, and peers who contributed to this enriching learning experience. Their guidance and collaboration have played a pivotal role in shaping my understanding and enthusiasm for electronic circuits.