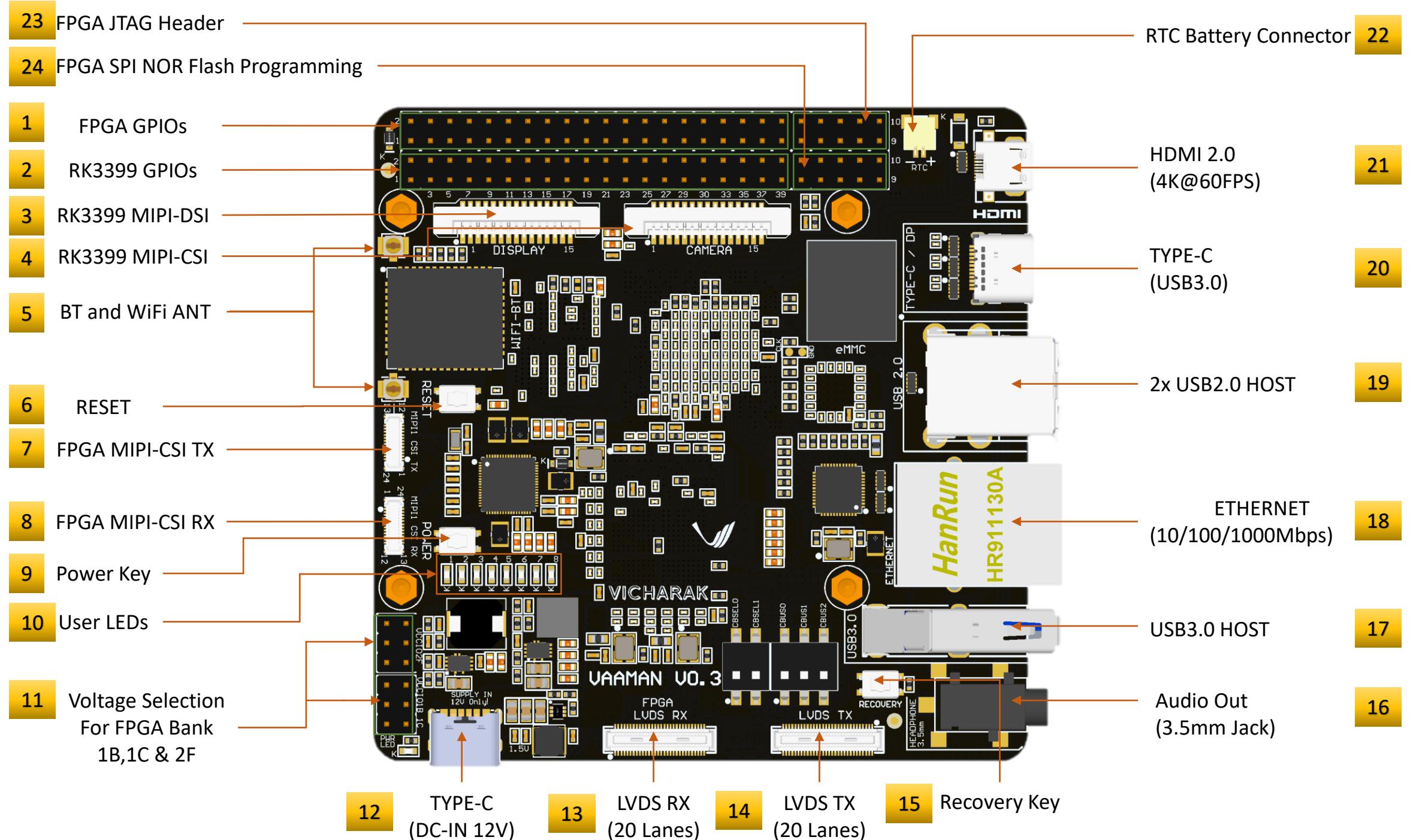
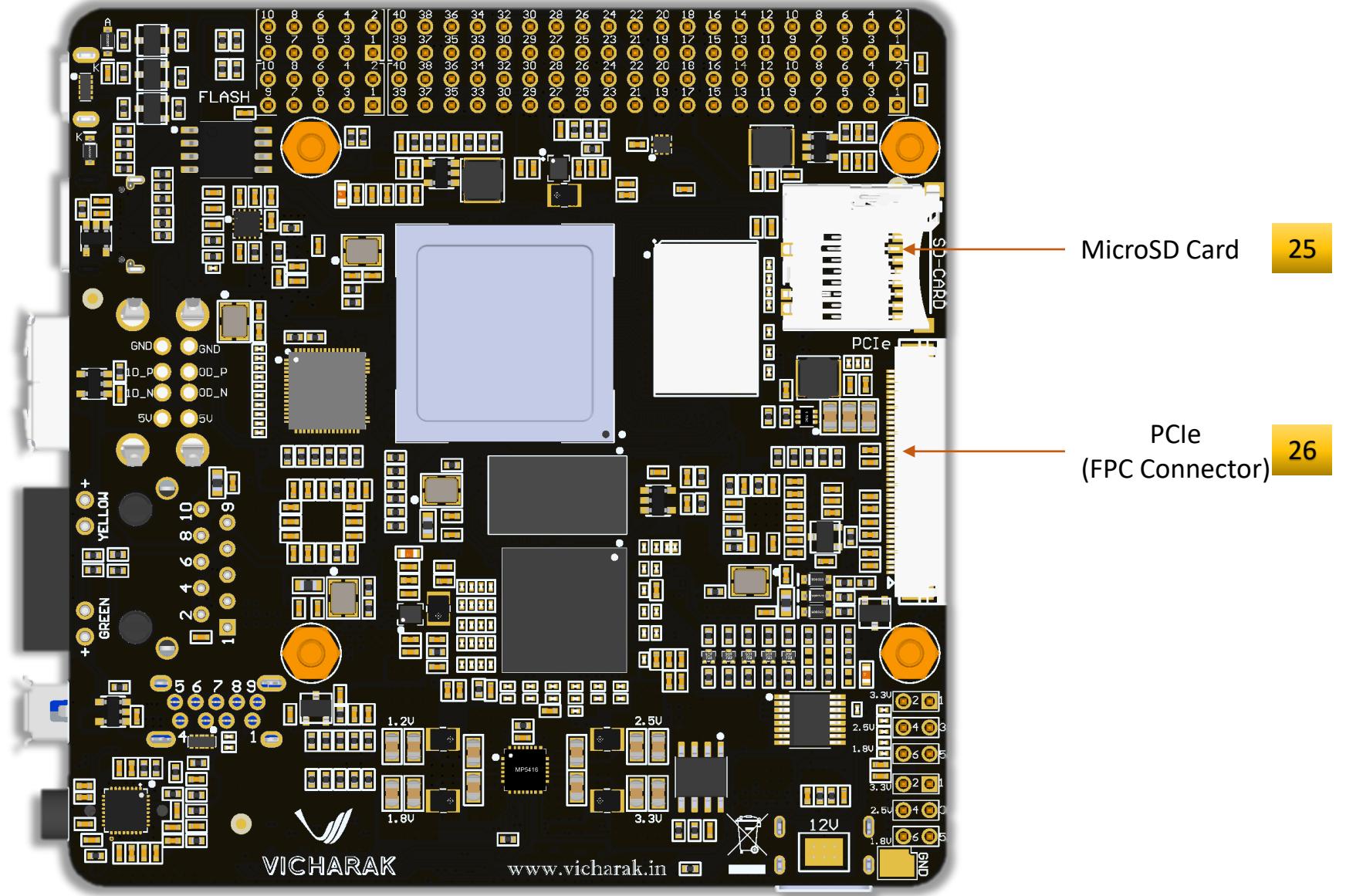


# Revision History

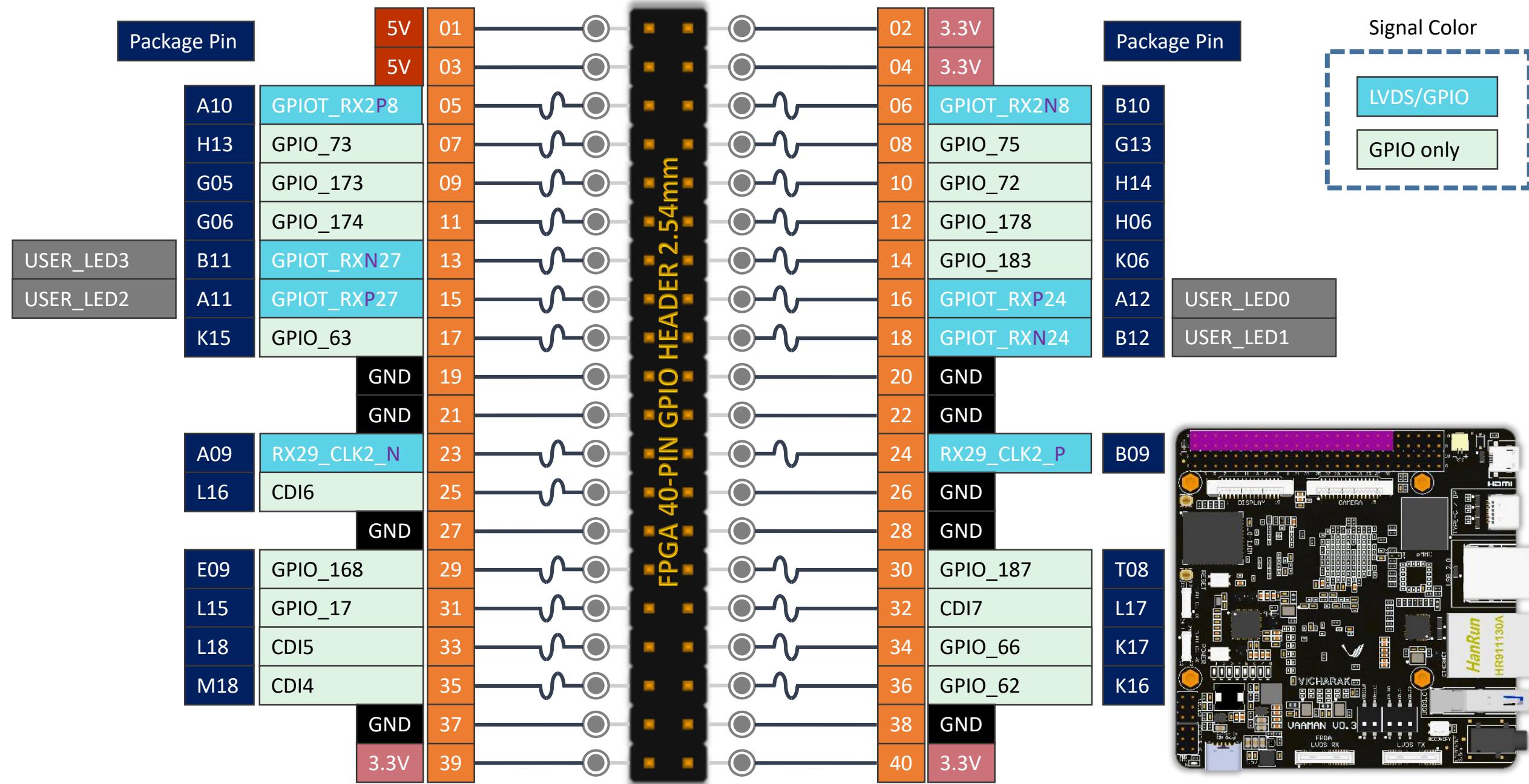
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Document Number	Revision Number	Description	Revision Date
	001	Initial Release	May 2023
	002	Updated RK3399 GPIOs Header pins	July 2023
	003	Page added FPGA Internal Clock Sources	Oct 2023





## 1 FPGA GPIOs



## 2 RK399 GPIOs

Package Pin

G30

H28

H31

AF5

AL3

AK1

G31

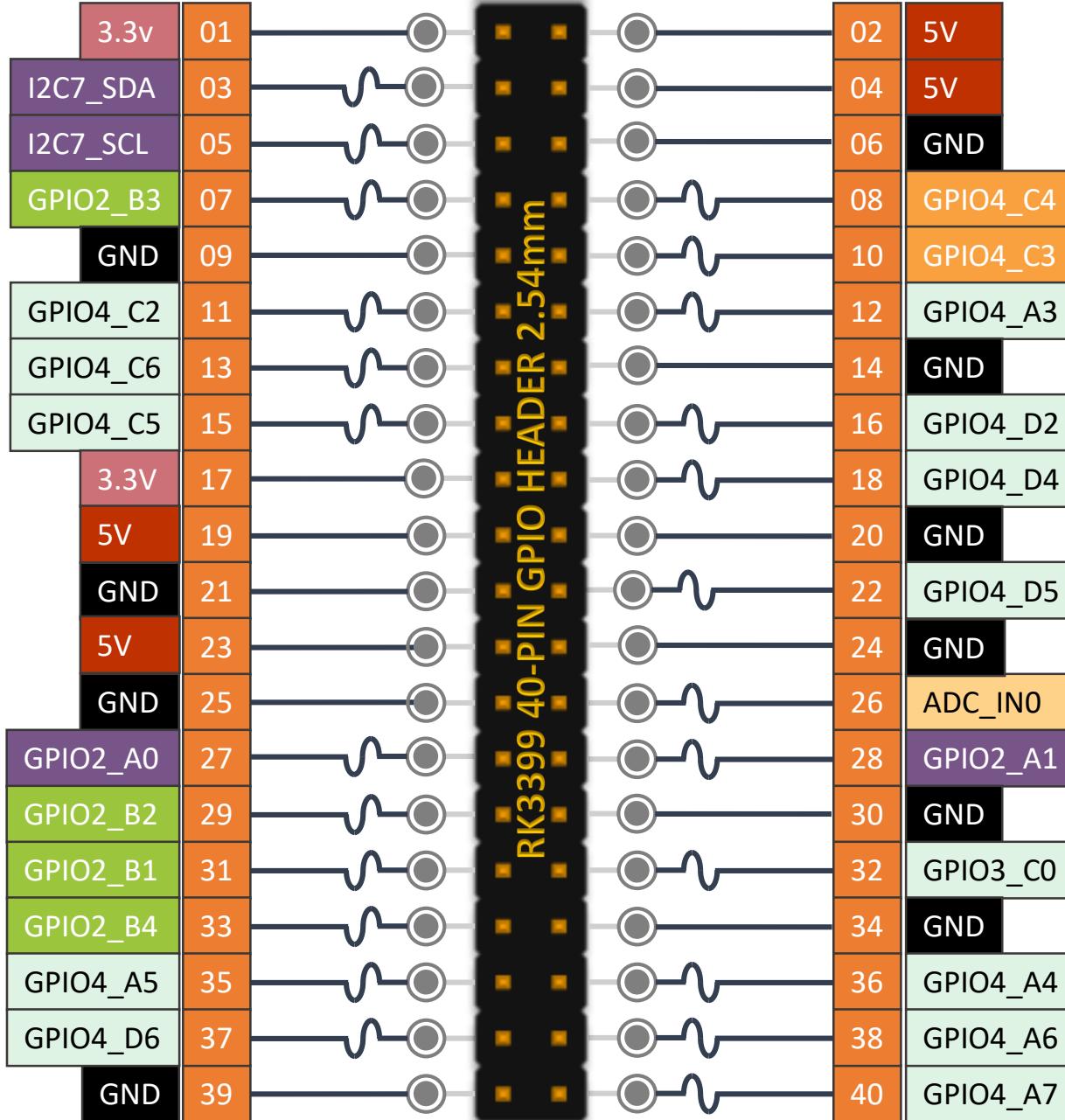
H24

F30

F31

AJ1

AG4



Package Pin

AJ4

AK2

AF3

AH3

AH5

AJ3

AG26

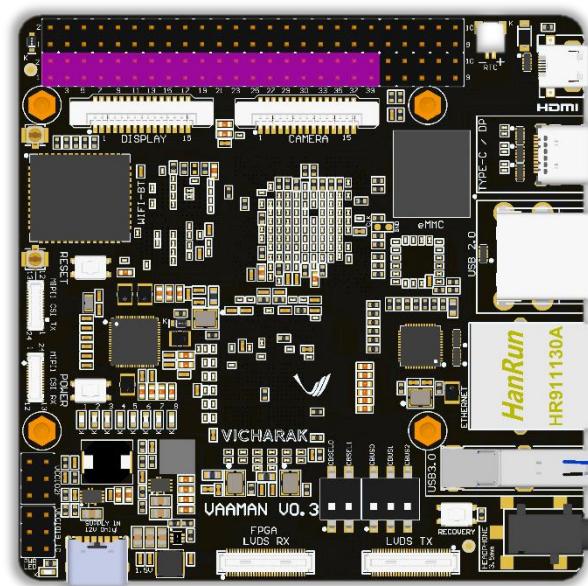
H25

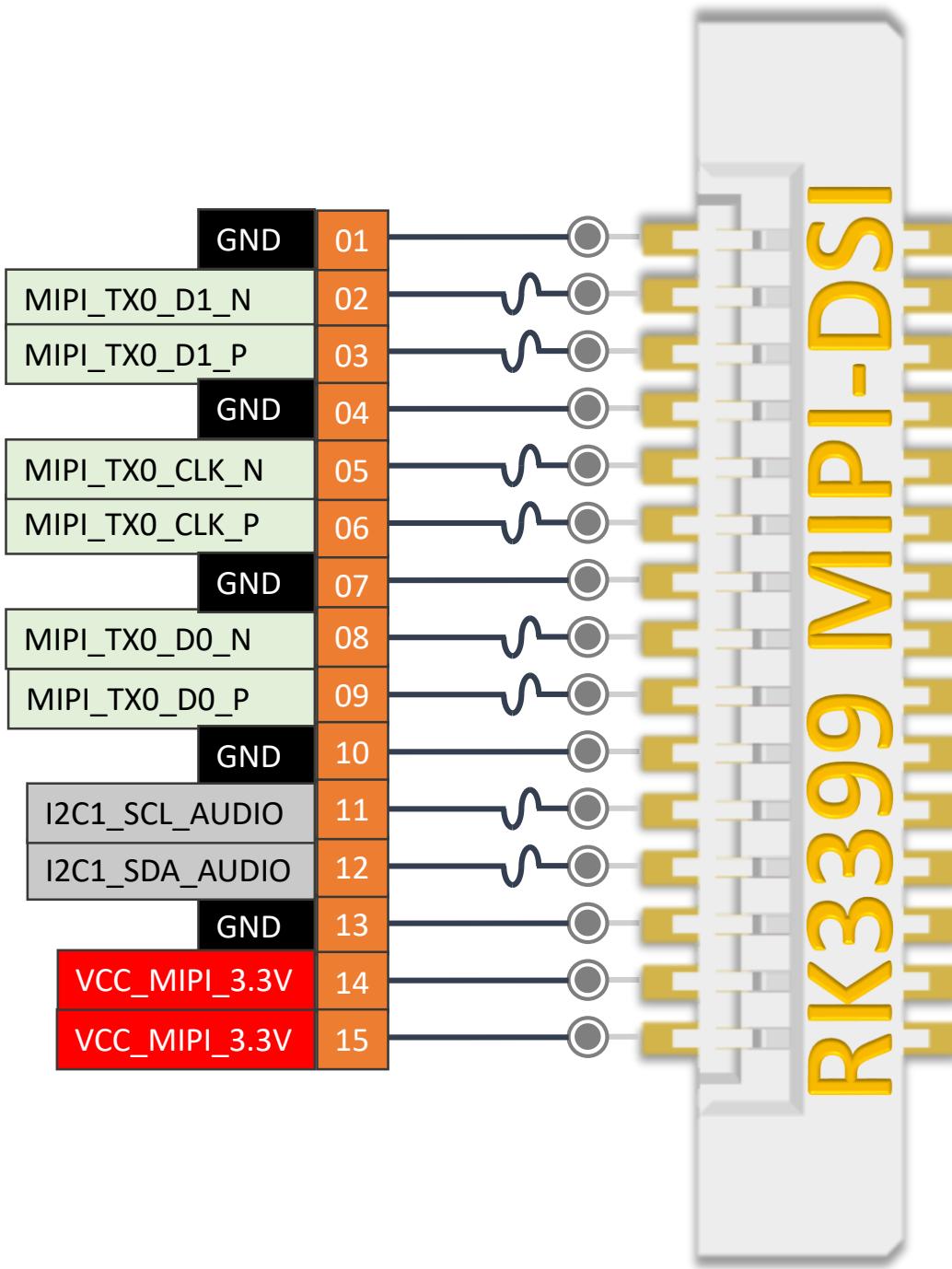
D27

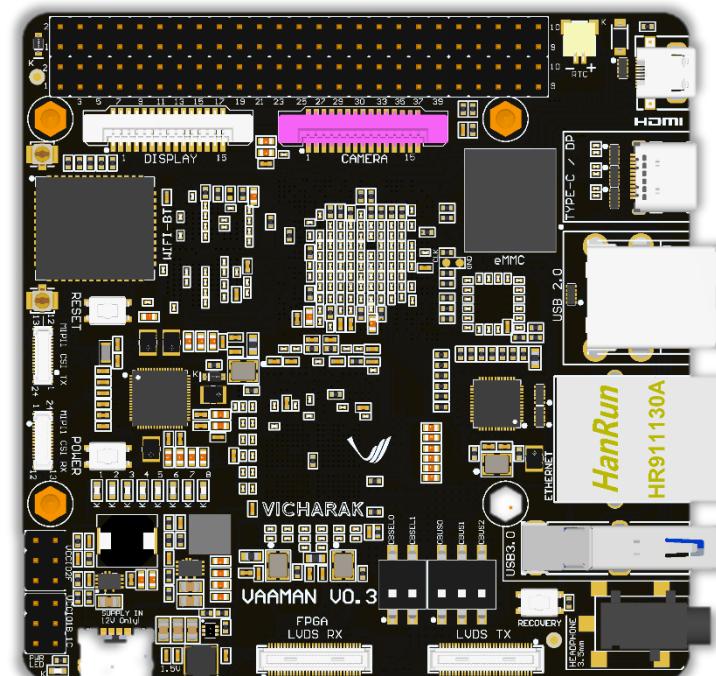
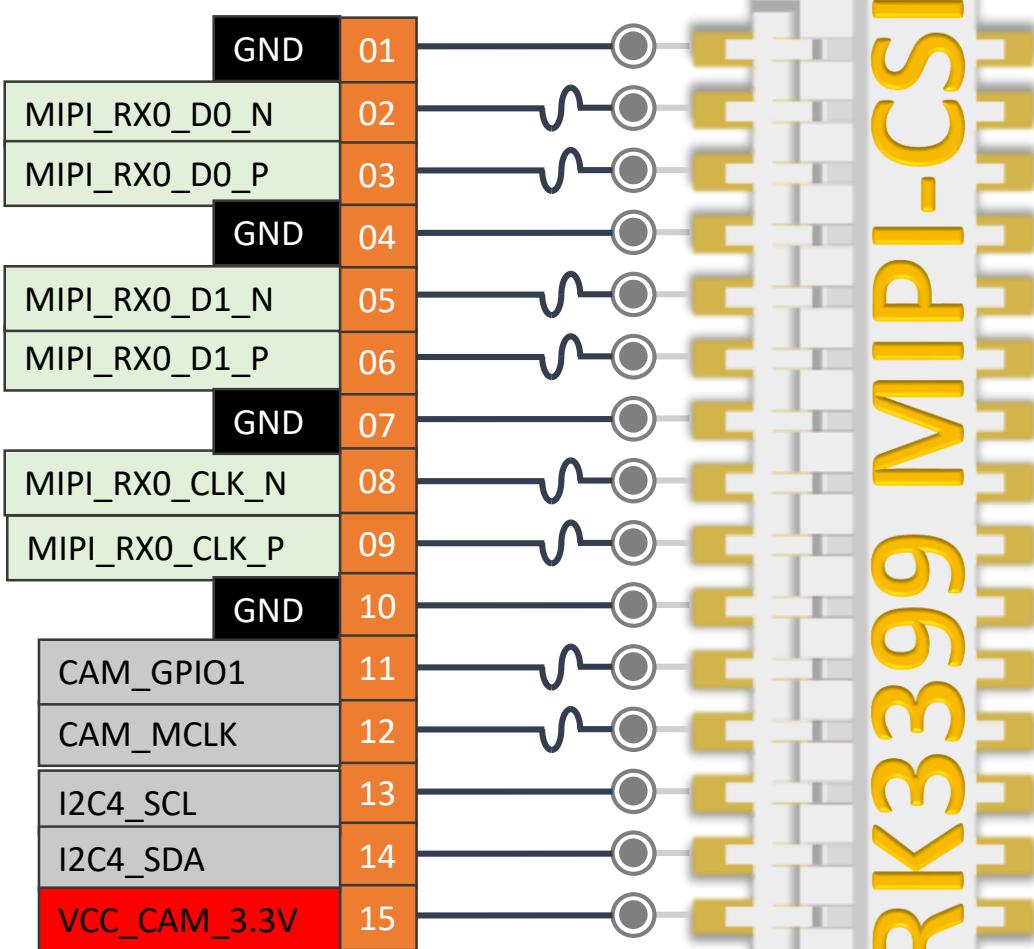
AA7

AD6

AC6

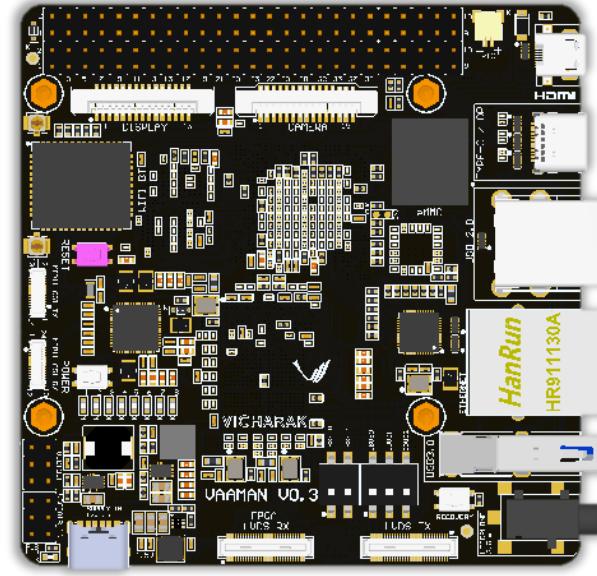


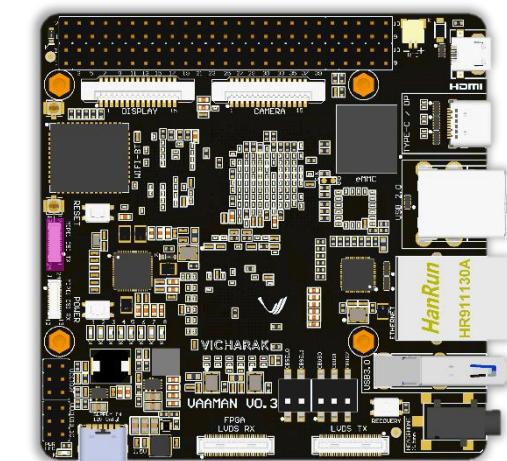
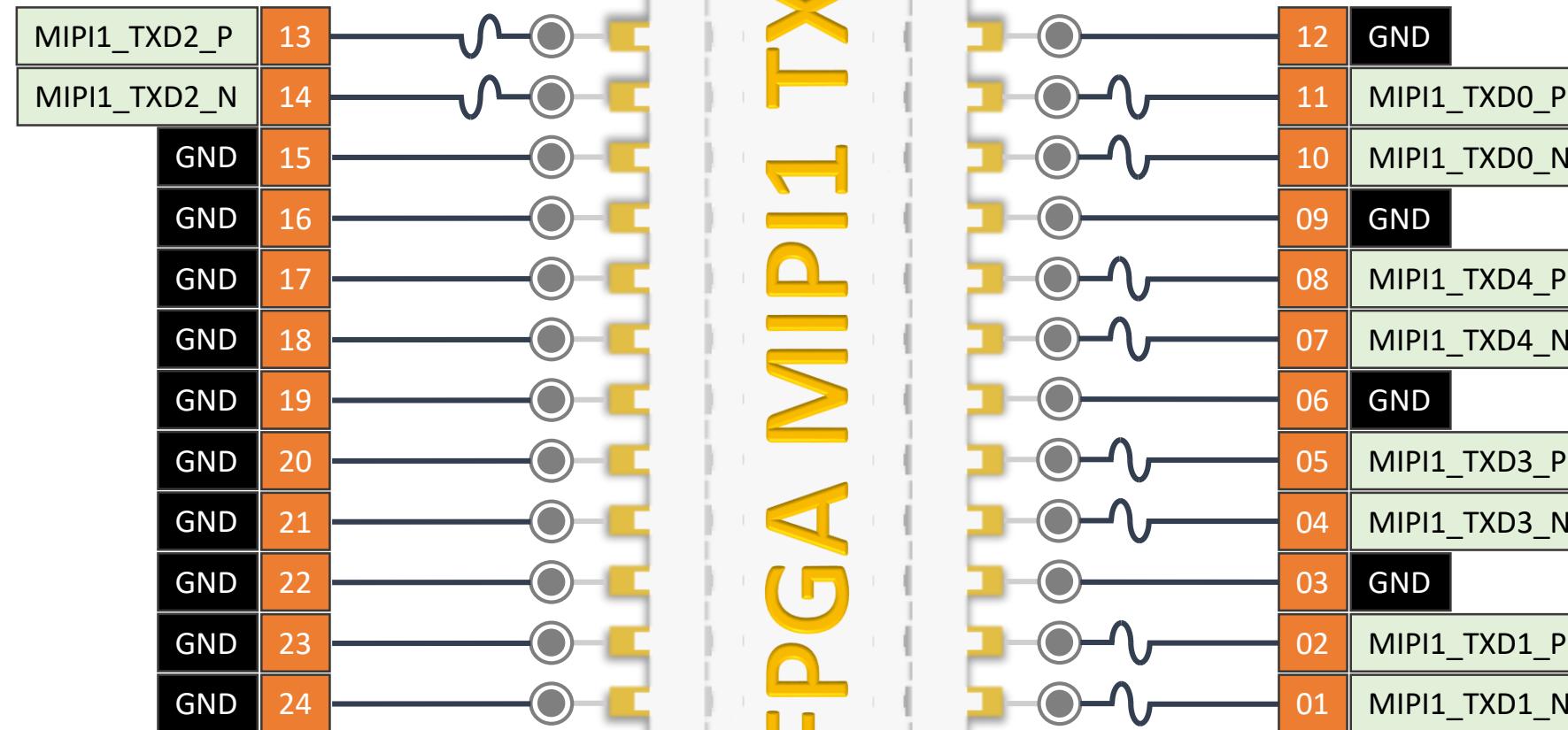


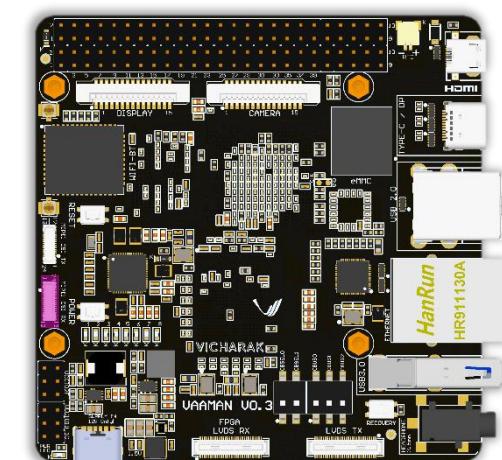
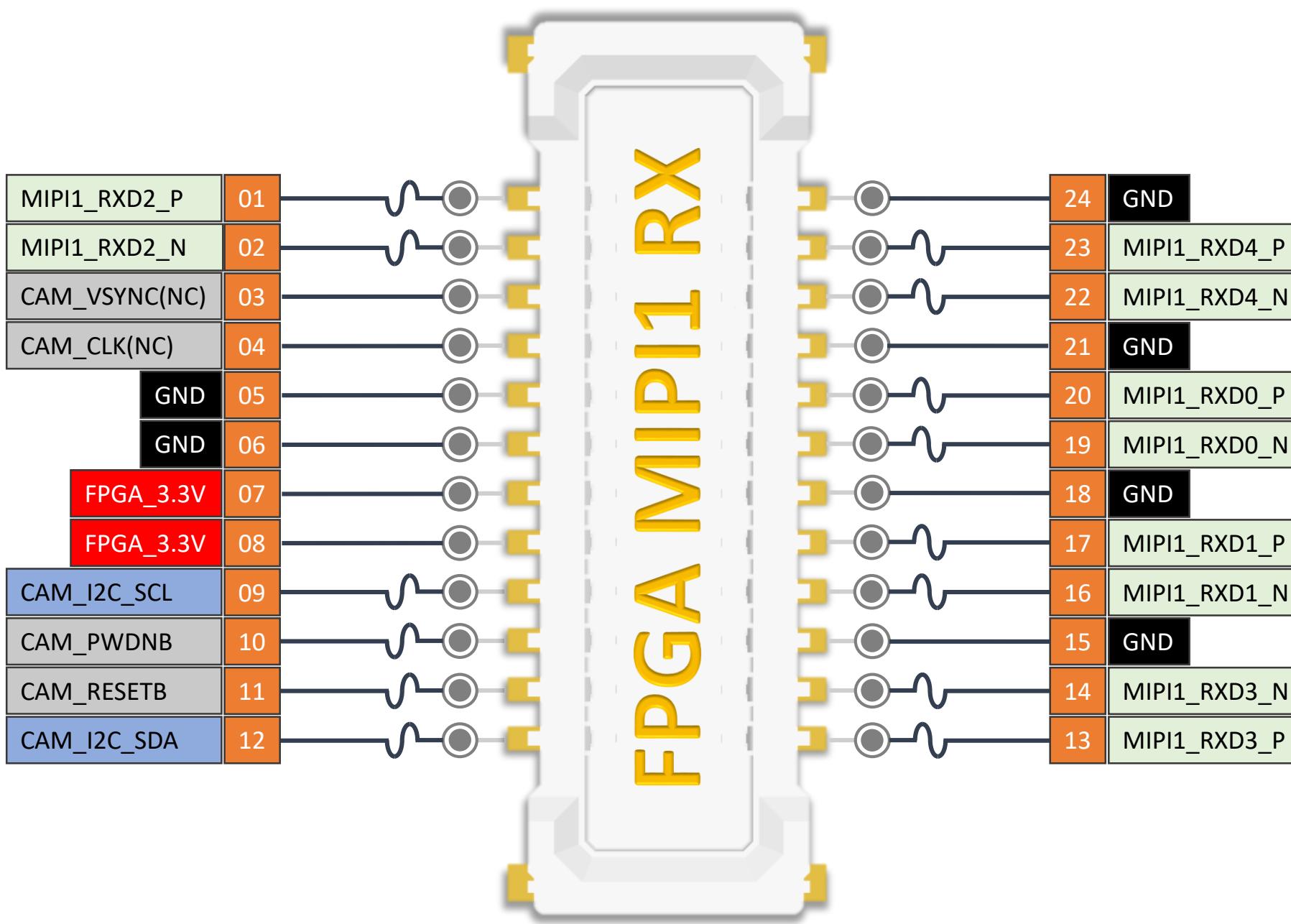




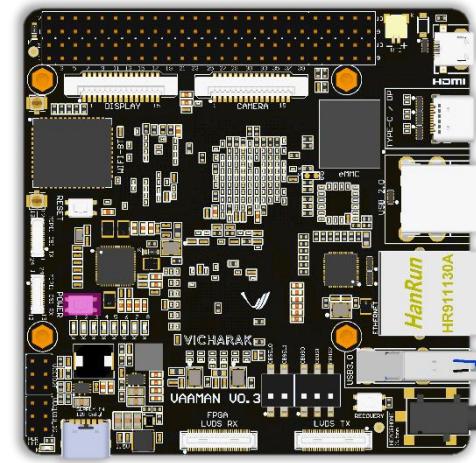
Board **Reset** Push-Button

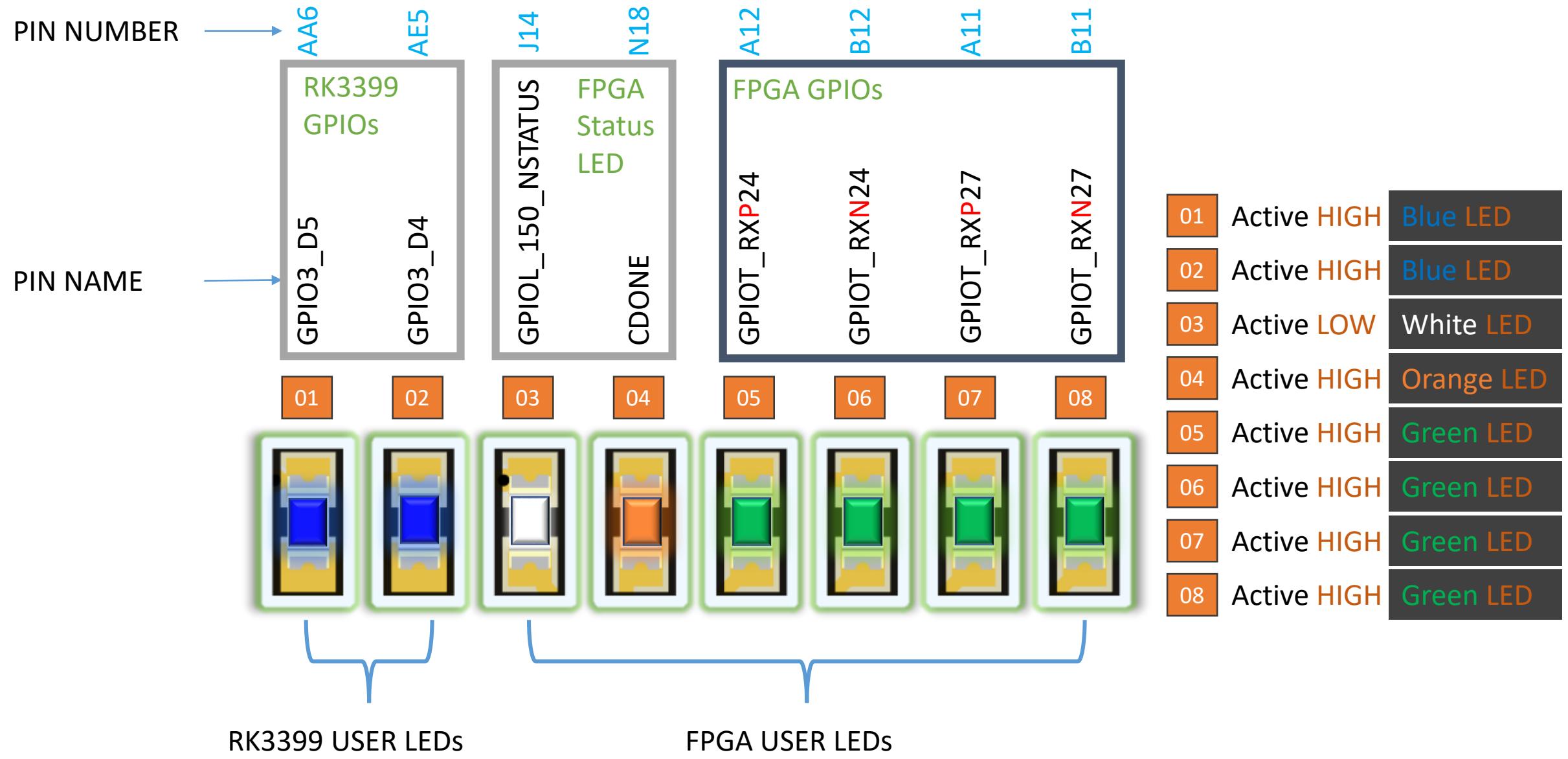


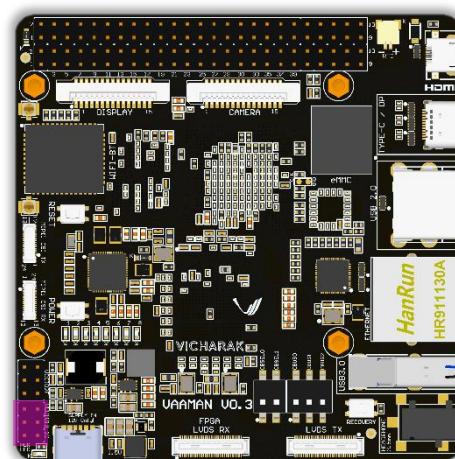
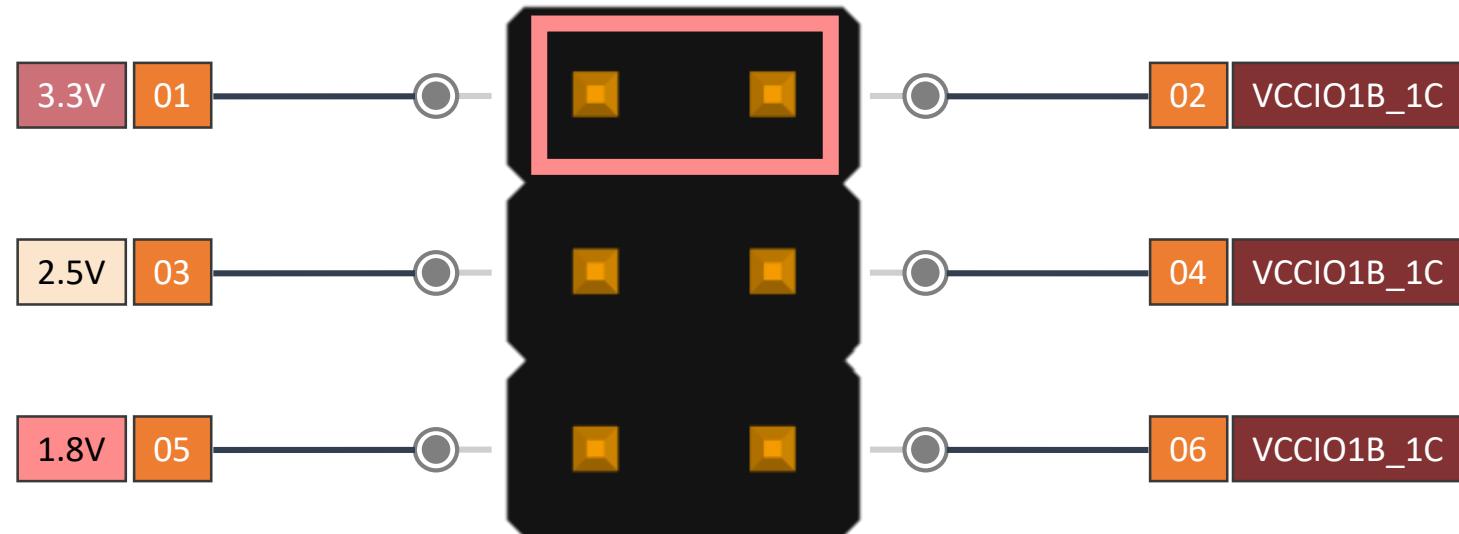
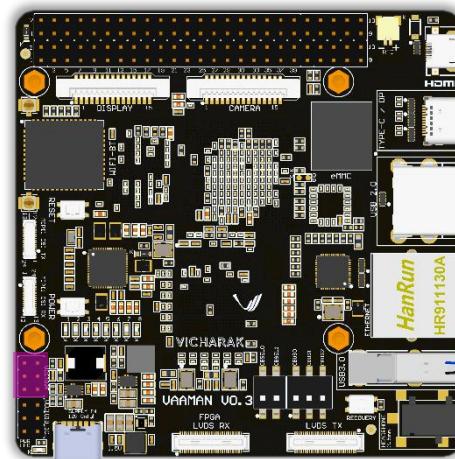
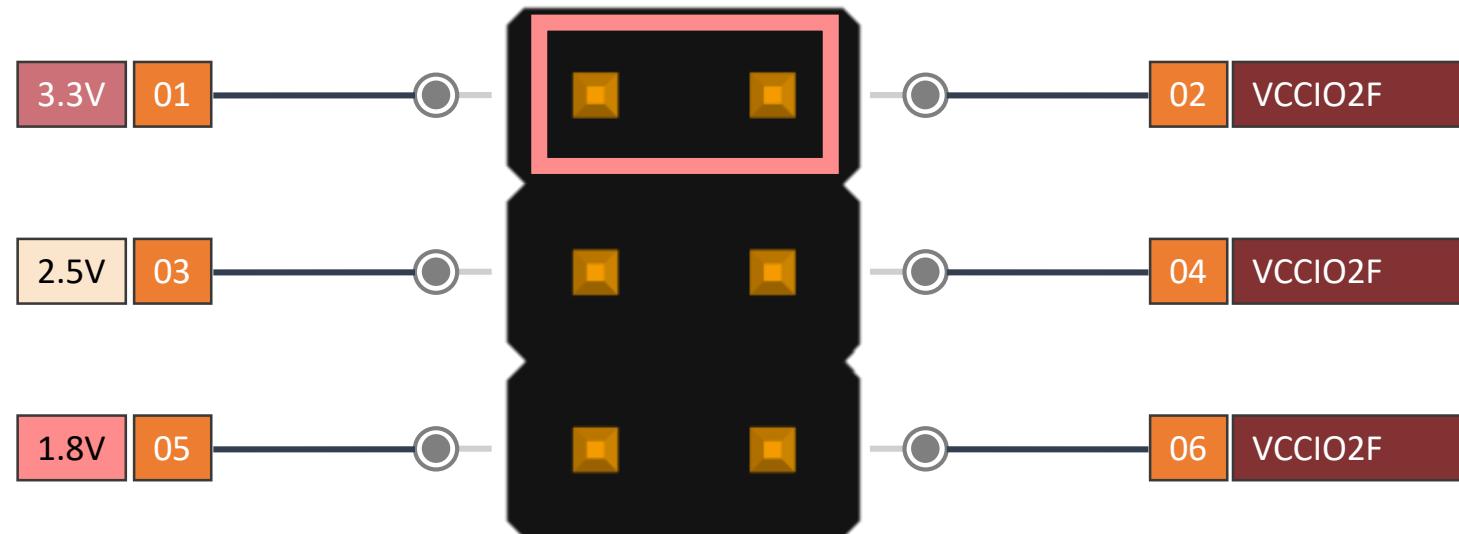




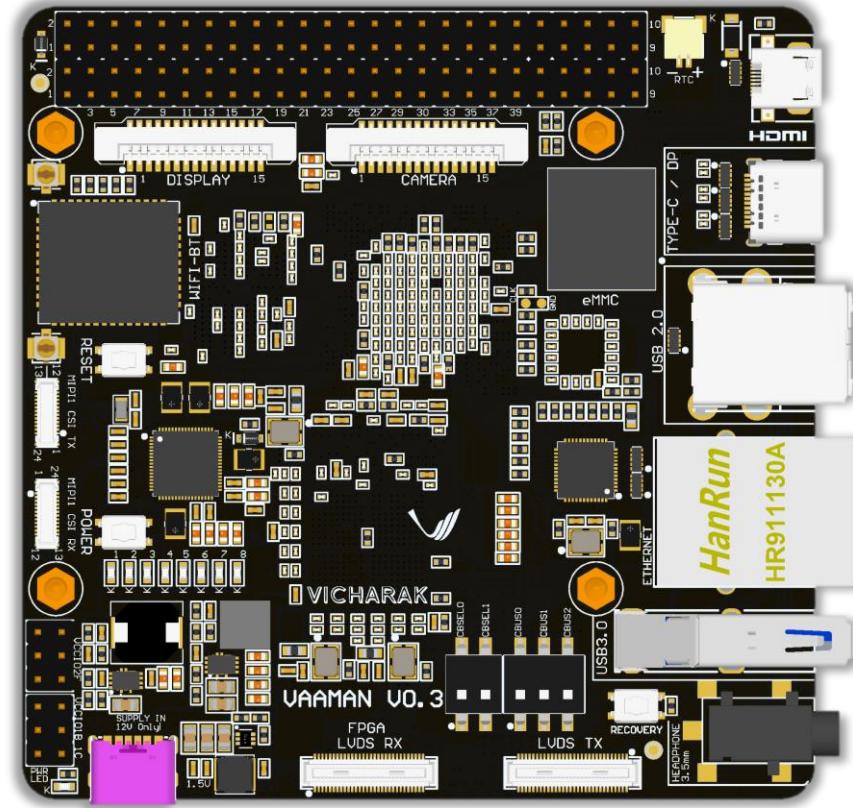
## 9 Power Key







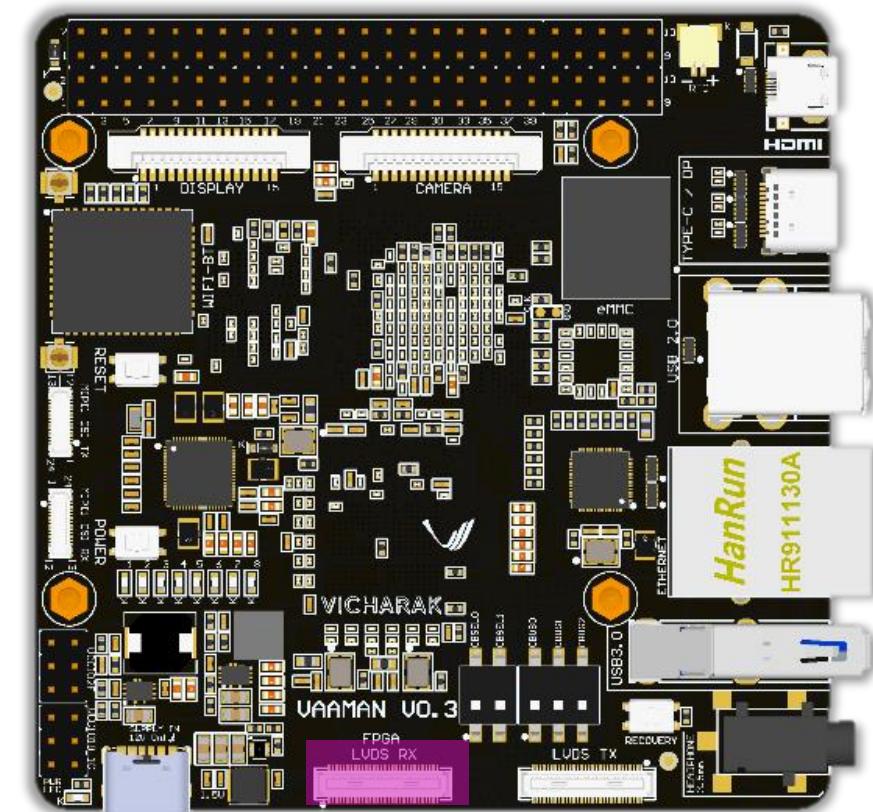
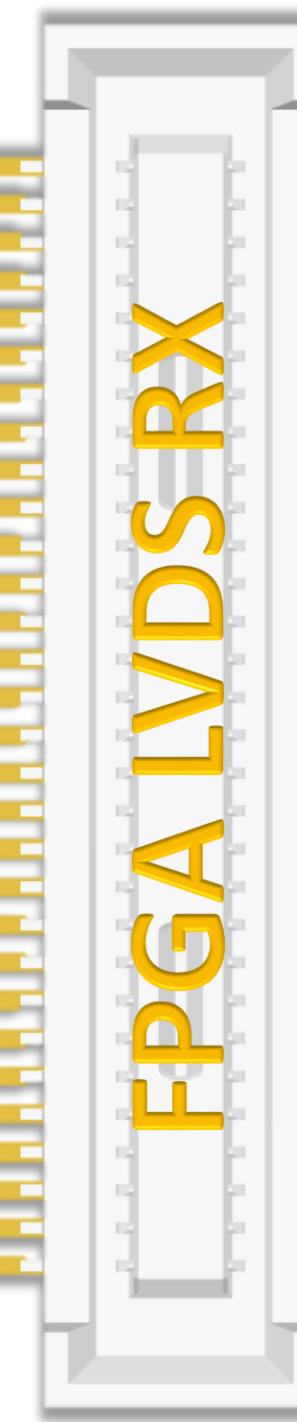
Jumper	VCCIO1B_1C (J2)	VCCIO2F (J3)
Connect pins 1 and 2	3.3 V (default)	3.3 V (default)
Connect pins 3 and 4	2.5 V	2.5 V
Connect pins 5 and 6	1.8 V	1.8 V



USB PD, support USB Type C PD 2.0, 9V/2A, 12V/2A

Qualcomm® Quick ChargeTM: Supports QC 3.0/2.0 adapter, 9V/2A, 12V/1.5A

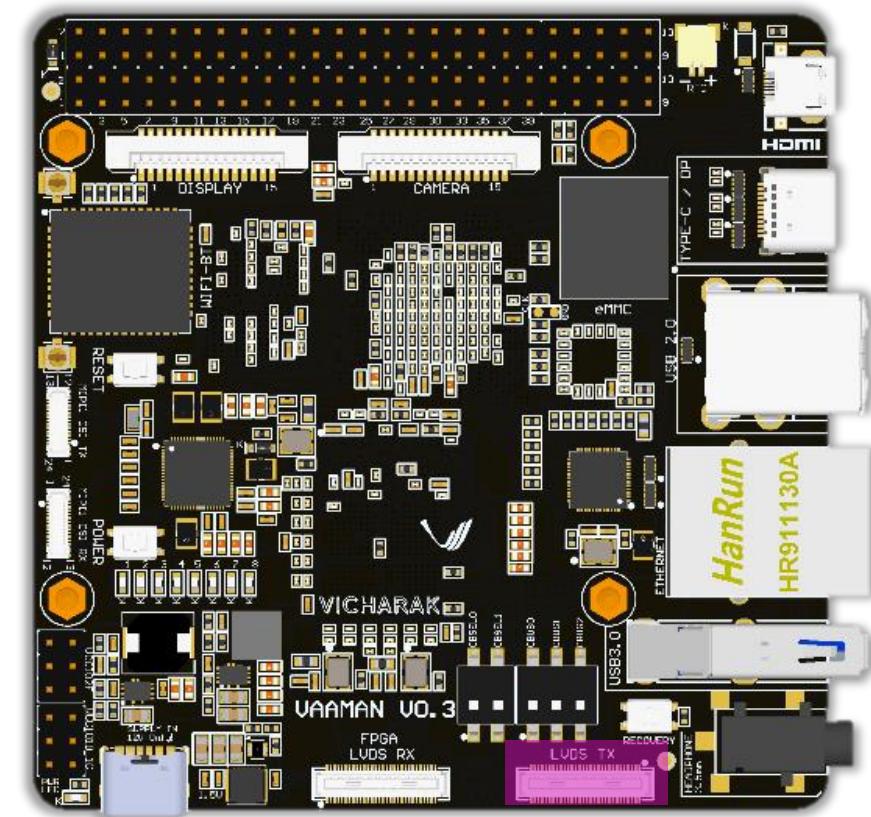
GPIO_RX14_N	31			30	GND
GPIO_RX14_P	32			29	GPIO_RX13_N
GND	33			28	GPIO_RX13_P
GPIO_RX12_N	34			27	GND
GPIO_RX12_P	35			26	GPIO_RX11_N
GND	36			25	GPIO_RX11_P
GPIO_RX17_P	37			24	GND
GPIO_RX17_N	38			23	GPIO_RX07_N
GND	39			22	GPIO_RX07_P
GPIO_RX09_CLK0_N	40			21	GND
GPIO_RX09_CLK0_P	41			20	GPIO_RX04_N
GND	42			19	GPIO_RX04_P
GPIO_RX16_N	43			18	GND
GPIO_RX16_P	44			17	GPIO_RX02_N
GND	45			16	GPIO_RX02_P
GPIO_RX15_N	46			15	GND
GPIO_RX15_P	47			14	GPIO_RX19_CLK1_N
GND	48			13	GPIO_RX19_CLK1_P
GPIO_RX20_P	49			12	GND
GPIO_RX20_N	50			11	GPIO_RX18_N
GND	51			10	GPIO_RX18_P
GPIO_RX05_N	52			09	GND
GPIO_RX05_P	53			08	GPIO_RX_21_P
GND	54			07	GPIO_RX_21_N
GPIO_RX01_P	55			06	GND
GPIO_RX01_N	56			05	GPIO_RX08_N
GND	57			04	GPIO_RX08_P
GPIO_RX06_N	58			03	GND
GPIO_RX06_P	59			02	GPIO_RX03_N
GND	60			01	GPIO_RX03_P

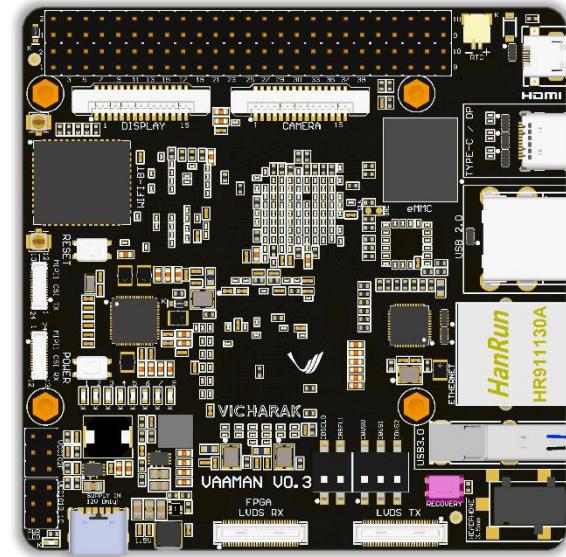


GPIOB_TX13_N	31		
GPIOB_TX13_P	32		
GND	33		
GPIOB_TX02_N	34		
GPIOB_TX02_P	35		
GND	36		
GPIOB_TX00_N	37		
GPIOB_TX00_P	38		
GND	39		
GPIOB_TX01_N	40		
GPIOB_TX01_P	41		
GND	42		
GPIOB_TX08_N	43		
GPIOB_TX08_P	44		
GND	45		
GPIOB_TX07_P	46		
GPIOB_TX07_N	47		
GND	48		
GPIOB_TX11_N	49		
GPIOB_TX11_P	50		
GND	51		
GPIOB_TX15_P	52		
GPIOB_TX15_N	53		
GND	54		
GPIOB_TX14_N	55		
GPIOB_TX14_P	56		
GND	57		
GPIOB_TX19_P	58		
GPIOB_TX19_N	59		
GND	60		

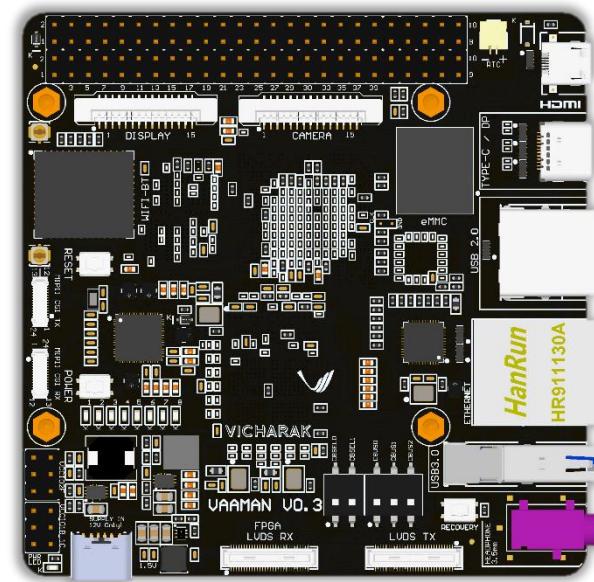
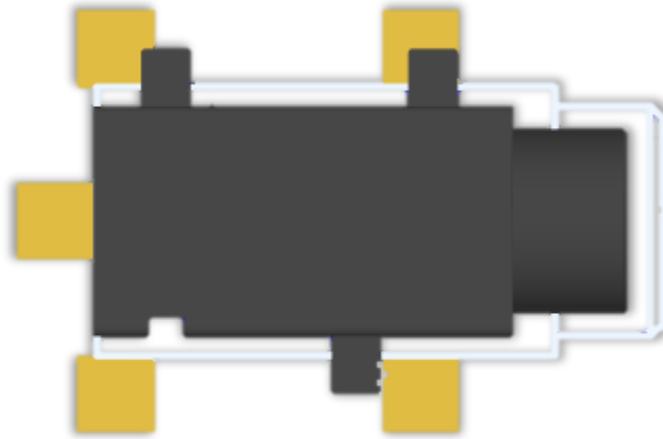


		30	GND
		29	GPIOB_TX05_N
		28	GPIOB_TX05_P
		27	GND
		26	GPIOB_TX03_N
		25	GPIOB_TX03_P
		24	GND
		23	GPIOB_TX04_P
		22	GPIOB_TX04_N
		21	GND
		20	GPIOB_TX06_N
		19	GPIOB_TX06_P
		18	GND
		17	GPIOB_TX09_P
		16	GPIOB_TX09_N
		15	GND
		14	GPIOB_TX10_N
		13	GPIOB_TX10_P
		12	GND
		11	GPIOB_TX18_N
		10	GPIOB_TX18_P
		09	GND
		08	GPIOB_TX12_P
		07	GPIOB_TX12_N
		06	GND
		05	GPIOB_TX17_N
		04	GPIOB_TX17_P
		03	GND
		02	GPIOB_TX16_N
		01	GPIOB_TX16_P

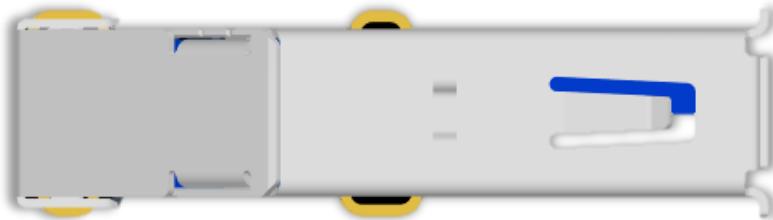




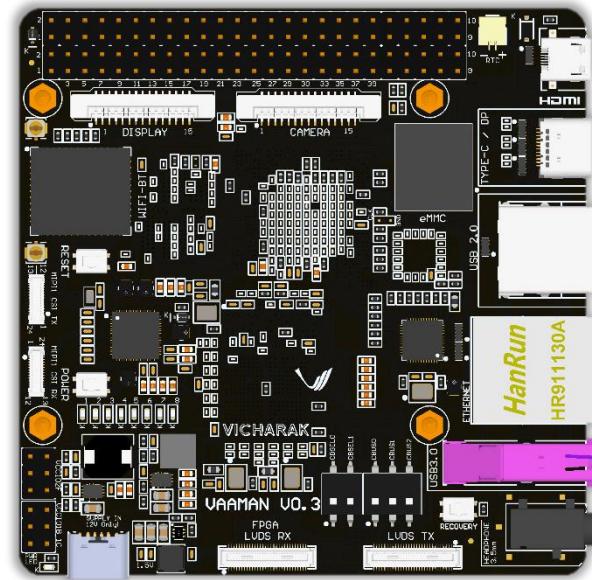
RECOVERY push button to allow user to easily flash over USB the on-board eMMC storage.



3.5mm jack with mic HD codec that supports up to 24-bit/96KHz audio.

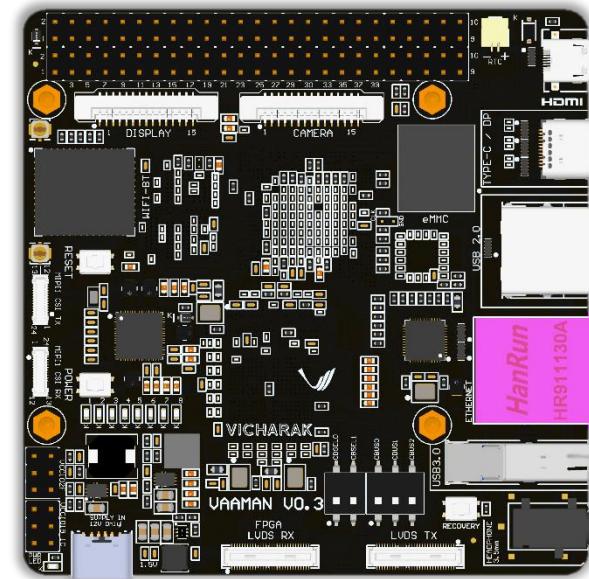


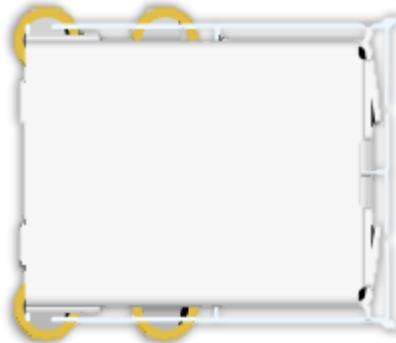
USB3.0 HOST



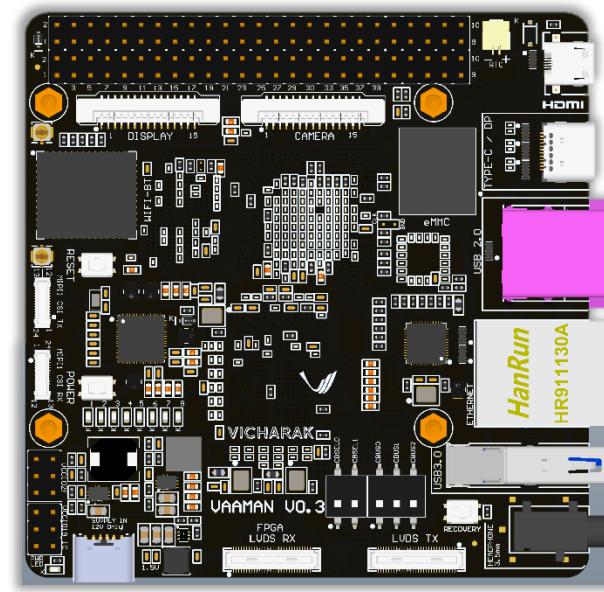


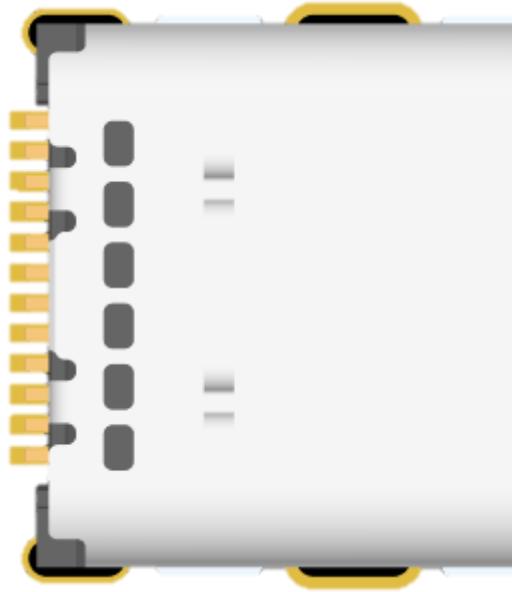
ETHERNET (10/100/1000Mbps)



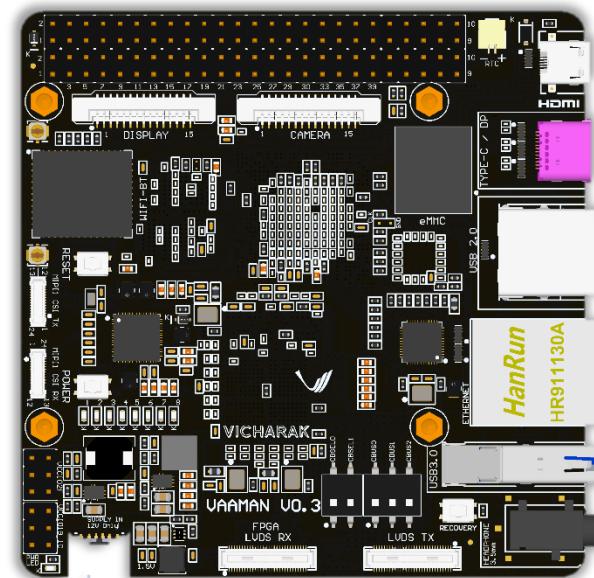


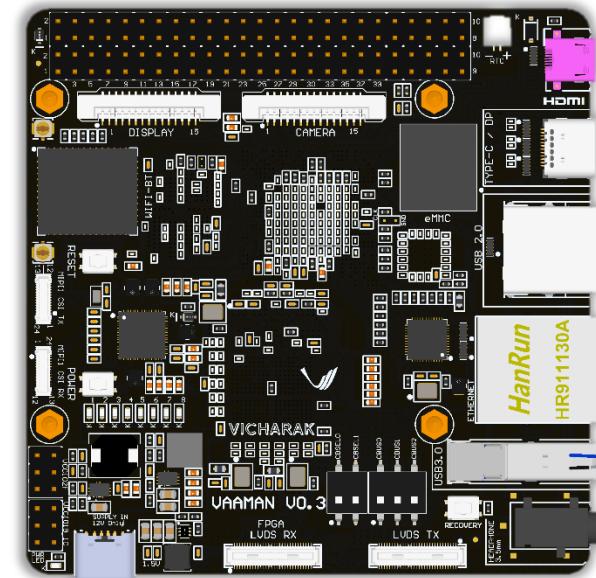
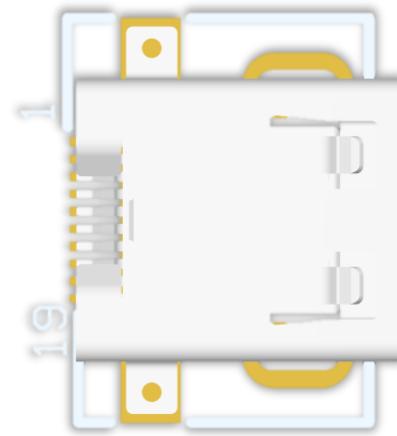
2x USB2.0 HOST

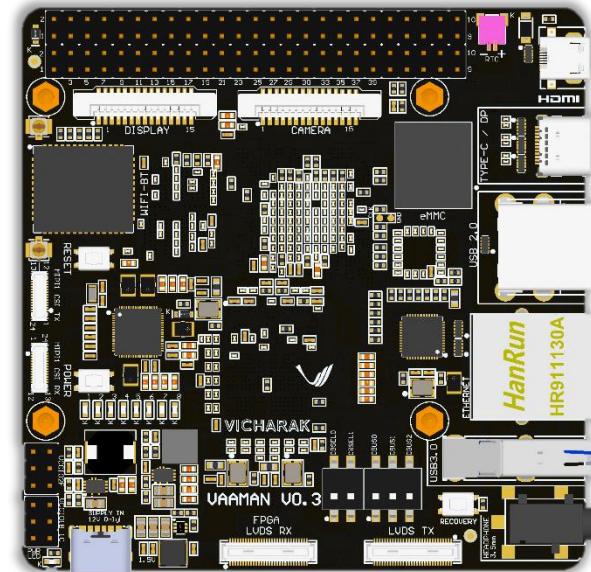
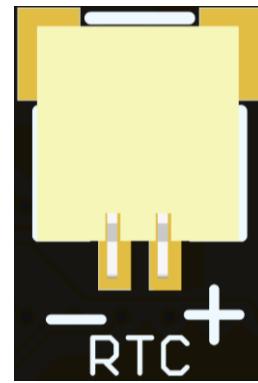


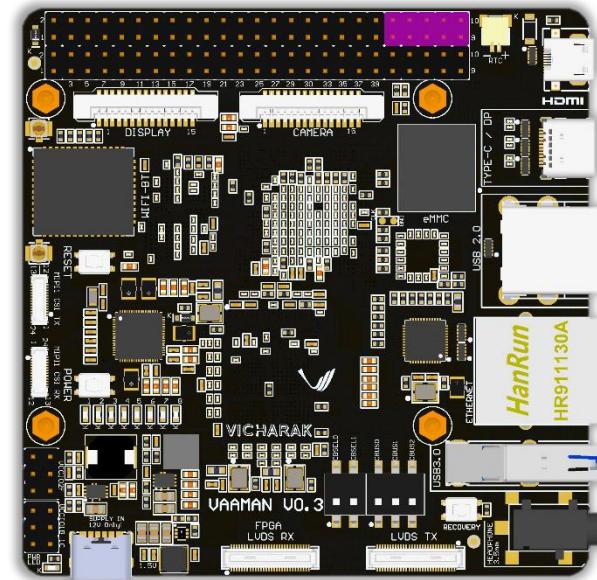
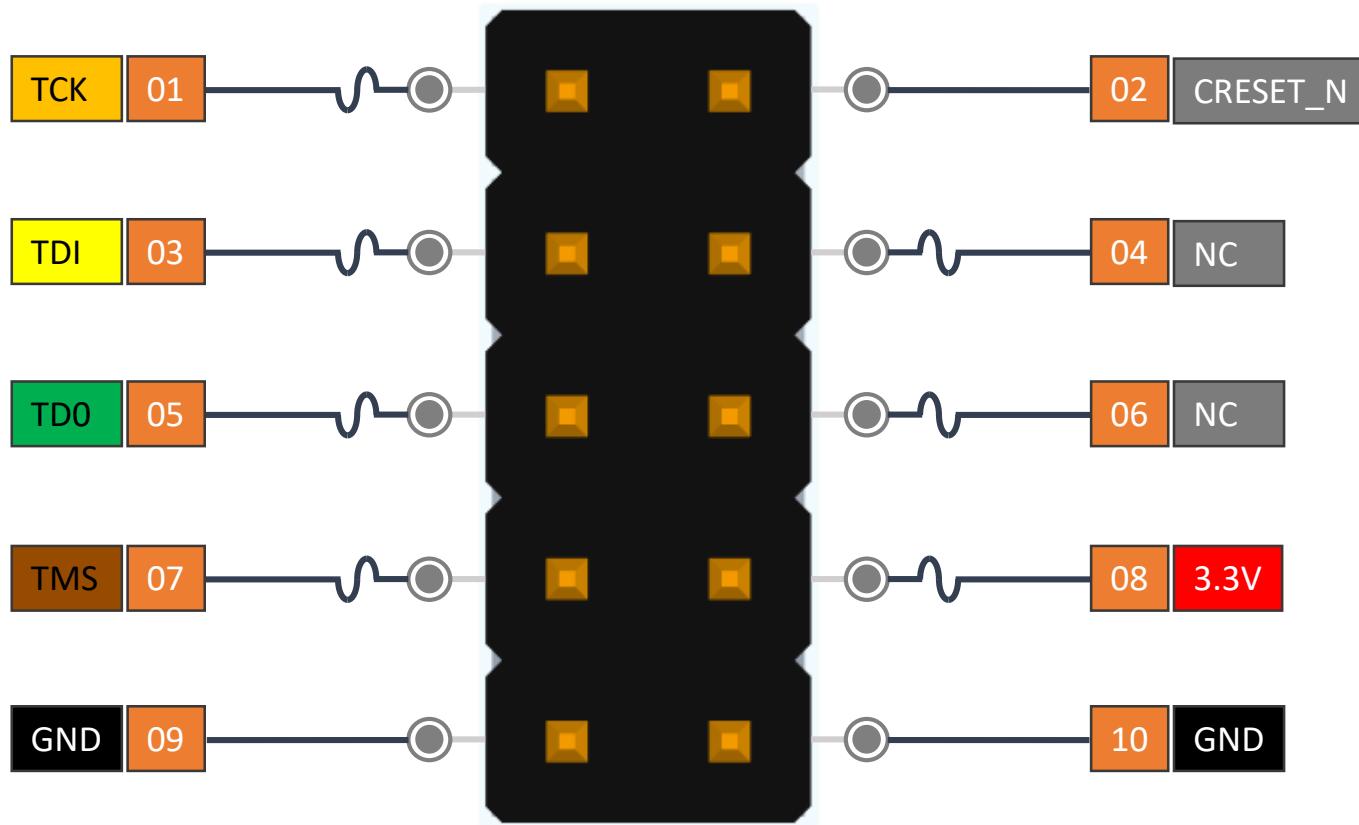


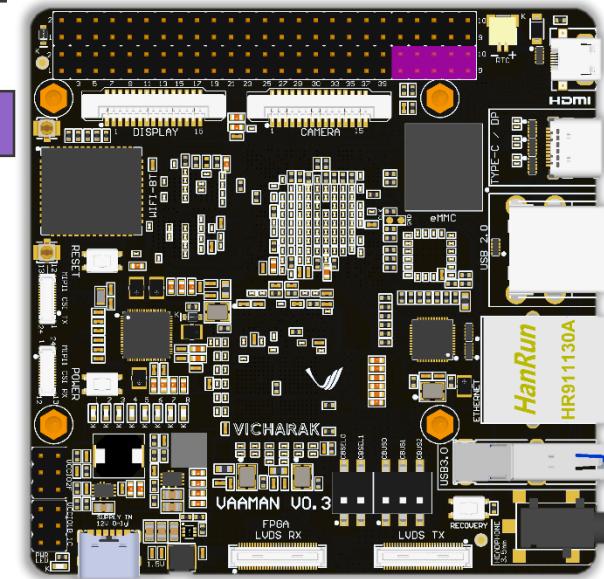
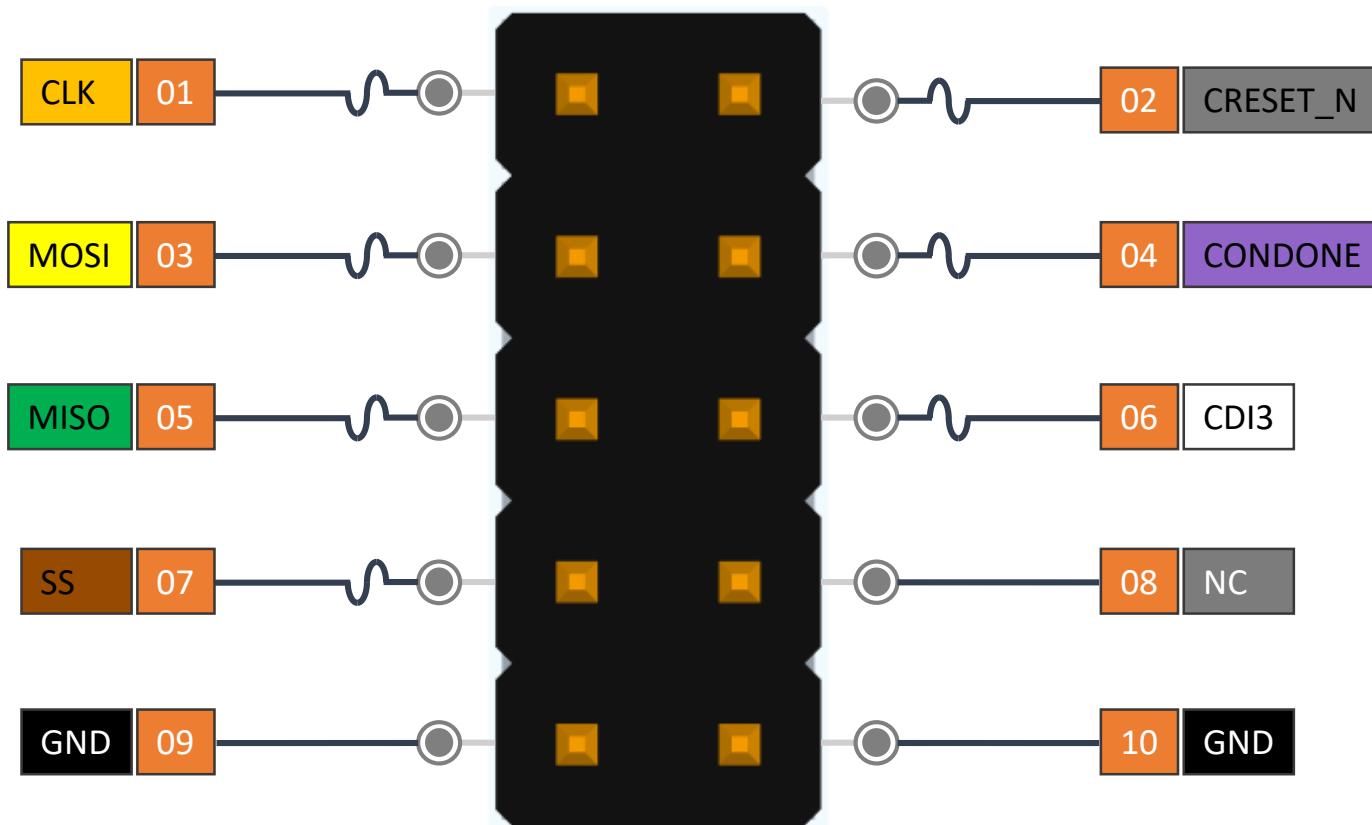
TYPE-C(USB3.0) / DisplayPort

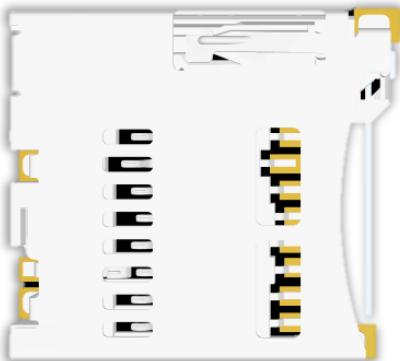




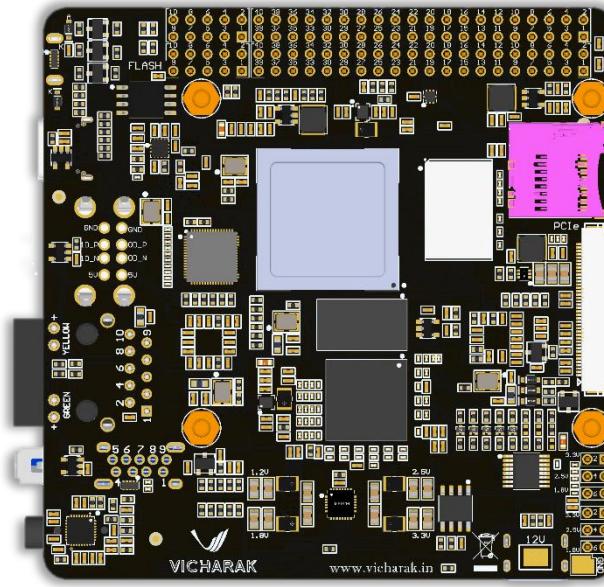


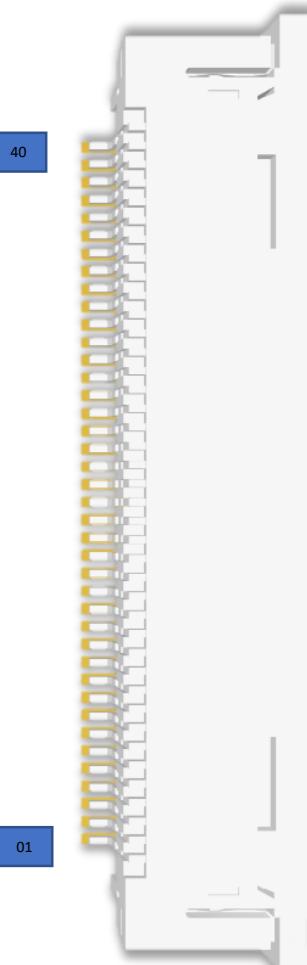




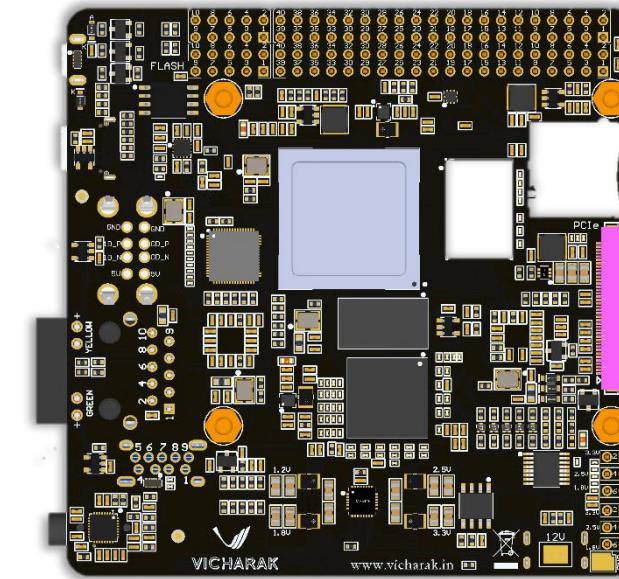


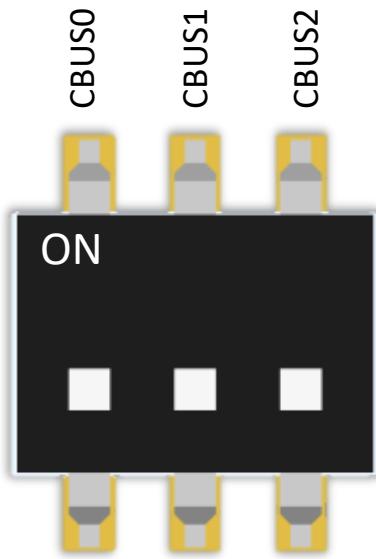
MicroSD Card





01	PCIE_CLKREQ_
02	GND
03	PCIE_TX3_P
04	PCIE_TX3_N
05	GND
06	PCIE_RX3_P
07	PCIE_RX3_N
08	GND
09	PCIE_TX0_P
10	PCIE_TX0_N
11	GND
12	PCIE_PERST_L
13	GND
14	PCIE_TX1_P
15	PCIE_TX1_N
16	GND
17	PCIE_RX0_P
18	PCIE_RX0_N
19	GND
20	PCIE_RX1_P
21	PCIE_RX1_N
22	GND
23	PCIE_TX2_P
24	PCIE_TX2_N
25	GND
26	PCIE_REF_CLK
27	PCIE_REF_CLK
28	GND
29	PCIE_RX2_P
30	PCIE_RX2_N
31	GND
32-40	VCC3V3_PCIE





*Table 5: SPI Hardware Settings*

If you do not make any connections, the default mode is x1 SPI active.

Configuration Mode	Parallel/Serial	TEST_N	SS_N	CBUS2, CBUS1, CBUS0	Width
SPI Active	Serial	1	1	3'b111	x1
	Parallel	1	1	3'b110	x2
	Parallel	1	1	3'b101	x4
SPI Passive	Serial	1	0	3'b111	x1
	Parallel	1	0	3'b110	x2
	Parallel	1	0	3'b101	x4
	Parallel	1	0	3'b100	x8
	Parallel	1	0	3'b011	x16
	Parallel	1	0	3'b010	x32

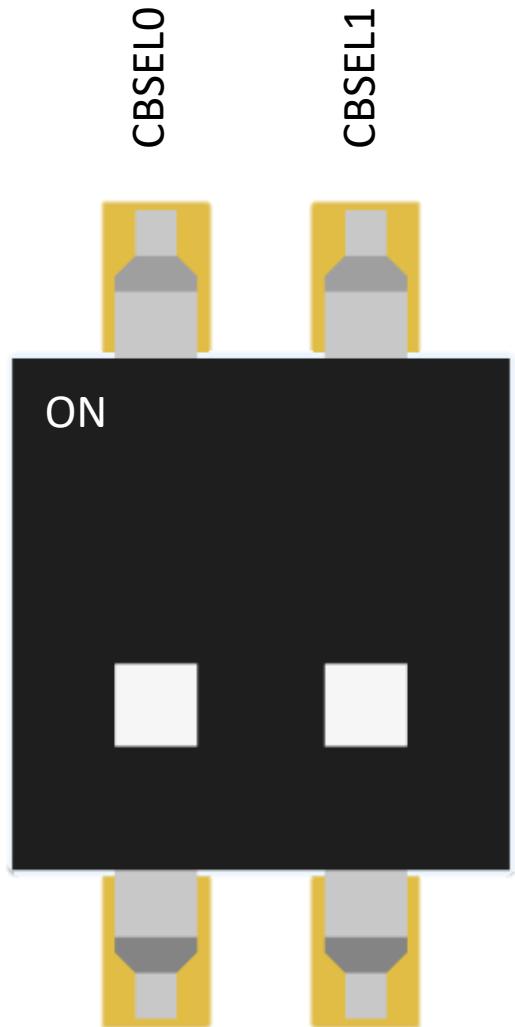
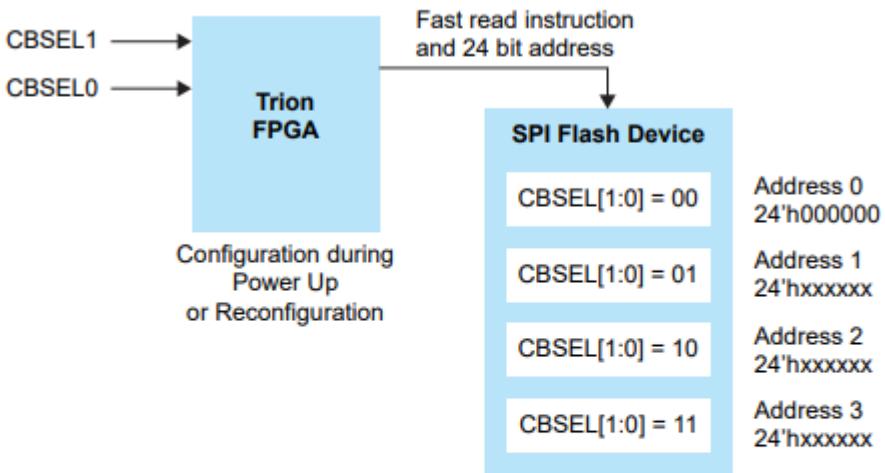


Figure 20: Configuration Setup for Multiple Images



Connect CBSEL [1:0] for the image you want to use:

- 00 for image 1
- 01 for image 2
- 10 for image 3
- 11 for image 4

You use the Efinity Programmer to combine multiple images into a single hex file.

**Note:** If the flash device does not have a valid image in the location the FPGA expects based on the CBSEL[1:0] setting, the FPGA looks at the image locations in ascending order until it finds a valid image. For example, if CBSEL[1:0] is 11 and the flash device has images for 00 and 01, the FPGA loads the image at 00.

