MC68332 Microcontroller - Detailed Overview

1. System Integration Module (SIM) - Detailed Explanation

The SIM handles the core system functions of the MC68332 and acts as a bridge between the CPU3

Main Responsibilities:

- Clock signal management (System Clock generation and distribution)
- Chip Select and External Bus Interface
- Watchdog Timer functionality
- Interrupt control and arbitration
- System protection features (like bus error handling)

Key Components of SIM:

- External Bus Interface (EBI): Controls address/data multiplexing, read/write control signals, and bus access timing.
- Chip Select Logic: Generates up to 7 chip select signals for memory-mapped peripherals or external RAM/ROM.
- Watchdog Timer (WDT): Ensures system reliability by resetting the MCU if it becomes unresponsive.
- Clock System: Works with an external oscillator and internal PLL to generate the system clock.

2. QSM (Queued Serial Module) - Detailed Block Diagram & Functionality

QSM includes two major interfaces:

- SCI (Serial Communications Interface): UART-style asynchronous serial communication.
- SPI (Serial Peripheral Interface): Full-duplex, synchronous communication.

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QSM Block Diagram Includes:

- Transmit and Receive shift registers for SCI and SPI
- Baud rate generator (SCI)
- Clock generator and chip select logic (SPI)
- Interrupt control for each interface
- Queues/buffers to allow background transfers

SCI Frame Format: Start bit + 8/9 data bits + optional parity + 1/2 stop bits

SPI Frame Format: Continuous stream of bits (8/16) clocked by master with Chip Select

3. IMB (Intermodule Bus) - Internal Architecture

Role: The IMB is a fast internal data bus connecting the CPU32 with internal modules like TPU, SIM

Characteristics:

- Parallel 16-bit or 32-bit data path
- Supports internal address decoding
- Arbitration logic allows shared access (e.g., CPU and TPU both accessing RAM)

4. SRAM (Static RAM) - Internal Memory Role

The MC68332 includes 2KB of on-chip SRAM:

- Used for general-purpose storage by the CPU
- Used by the TPU during emulation mode (stores microcode)
- Dual-access via IMB by both CPU and TPU

- Retains data in standby mode (as long as power is present)

5. Watchdog Timer

- Ensures system recovery in case of software failure or infinite loops

- Can be configured for different timeout periods
- If not reset within the set interval, it triggers a system reset

Key Registers:

- WCR (Watchdog Control Register)
- WSR (Watchdog Service Register)

6. External Bus Interface (EBI)

Used to interface external memory (RAM, ROM) and peripherals.

Signals Generated:

- Address lines (A0-A23)
- Data lines (D0-D15)
- Control signals: R/W, AS (Address Strobe), DS (Data Strobe), CS (Chip Select), RESET, BERR (Bus Error)

7. Chip Select & Timing Logic

Function: Simplifies interfacing with external devices by auto-generating chip select signals based

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Configurable Parameters:

- Base address
- Address mask
- Wait states
- Access size (byte/word)

Supports:

- Up to 7 chip selects
- Glueless interface to ROM, RAM, EEPROM, etc.

8. Baud Rate Generator (SCI Submodule)

Used to generate the timing for asynchronous SCI communication.

- Divides system clock to produce baud rate
- Configurable via SCI baud rate register
- Common baud rates: 9600, 19200, 38400, etc.

9. Interrupt Handling

MC68332 supports multiple interrupt sources:

- TPU Channel Interrupts
- QSM (SCI/SPI) Interrupts
- Watchdog Timeout
- External IRQ Pins (IRQ7-IRQ1)

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Interrupt Features:

- Prioritization
- Vector base register to point to interrupt vector table
- Masking and nesting supported

10. Memory Map

Address Range	Description
0x000000 - 0x0007FF	2KB Internal SRAM
0xY00000 - 0xYFFFFF	External RAM/ROM via CS lines
0xFFF000 - 0xFFFFFF	Internal Peripheral Registers

Memory-mapped access to TPU, SIM, QSM, etc.

Flexible due to programmable chip select logic

11. Pinouts Overview

The MC68332 comes in various packages (e.g., 132-pin PQFP). Key pins include:

Power & Clock: VCC, GND, EXTAL, XTAL

Bus Interface: A0-A23, D0-D15, R/W, AS, DS, BERR

Control: RESET, HALT, IRQ1-IRQ7

Communication: SCI TXD/RXD, SPI MISO/MOSI/SCK/CS

TPU I/O Pins: 16 channels configurable for input/output timing functions

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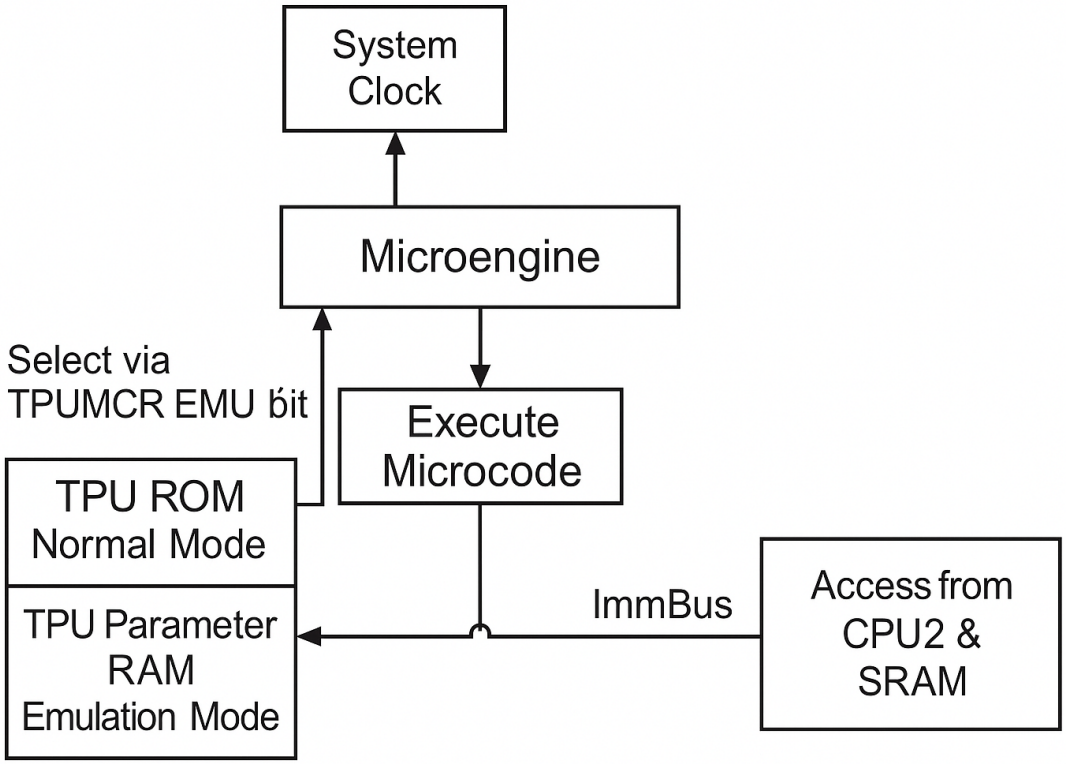
Diagram



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Diagram