CS M51A and EE M16 Spring 2015 Section 1

Logic Design of Digital Systems

Dr. Yutao He

Verilog Lab #2 - Design of Combinational Systems

Due: May 13rd, 2015

(1) **Name:** Lai (Last) Victor (First)

Student ID: 404274720

Signature: Victor Lai

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Signature:

Date: May 13, 2015

Result	
Correctness	
Creativity	
Report	
Total Score	