

CS M51A and EE M16 Spring 2015 Section 1

Logic Design of Digital Systems

Dr. Yutao He

Verilog Lab #3 - Design of Sequential Systems

Due: June 2, 2015

Team ID: 01

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Last First

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Signature: Victor Lai

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Date: June 2, 2015

Result	
Correctness	
Creativity	
Report	
Total Score	