CS M51A and EE M16 Spring 2015 Section 1 Logic Design of Digital Systems

Dr. Yutao He

Verilog Lab#3 - Design of Sequential Systems

Due: June 2, 2015

Tear	m ID: _	01	
(1)	Name	: Lai Last	Victor First
	Student ID: 404274720 Signature: La		
(2)	Name	: <u>Gahm</u>	Dennis
		Last	First
Student ID: 704016107			1016107 0.4 1
Signature: Demin Lahm			
Date:June 2, 2015			
		\mathbf{Result}	
		Correctness	
		Creativity	
		Report	
		Total Score	