



# **The Errata of IMX623-AAQV-W Datasheet**

May 18, 2022

Sony Semiconductor Solutions Corporation

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# Affected Documents(1)

ID	ET No	Document	Date	Revision	Remarks
1	ET-00054	Datasheet	August 24, 2020	0.0.1	<ul style="list-style-type: none"> <li>1. Recommended CRA</li> <li>2. Rename the power supply pins ,GND pins, Sync pins and GPIO pin.</li> <li>3. AC specification</li> <li>4. Serial communication</li> <li>5. Output Mode(MIPI serial)</li> <li>6. Example of Peripheral Circuit</li> </ul>
2	ET-00060	Datasheet	September 29, 2020	0.0.2	<ul style="list-style-type: none"> <li>1. Update the Example of Peripheral Circuit</li> <li>2. Update the Pixel Arrangement</li> </ul>
3	ET-00072	Datasheet	December 15, 2020	0.1.0	<ul style="list-style-type: none"> <li>1. Update the Input Clock Specifications</li> <li>2. Update the Pin List(I/O type)</li> <li>3. Update the Pin List(Symbol)</li> <li>4. Update the Example of Peripheral Circuit</li> </ul>
4	ET-00083	Datasheet	April 20, 2021	0.1.1	<ul style="list-style-type: none"> <li>1. Update Table 11-3 Pin State.</li> <li>2. Update Table 12-1 DC Characteristics.</li> <li>3. Update Master Clock (OSCI).</li> <li>4. Update AC Characteristics</li> <li>5. Update Spot Pixel Specifications.</li> </ul>
5	ET-00087	Datasheet	May 17, 2021	0.1.2	<ul style="list-style-type: none"> <li>1. Updated Fig. 7-1 Optical Center (Top View).</li> <li>2. Updated Frame Sync (FSYNC) Input.</li> <li>3. Updated System reset signal (XCLR).</li> <li>4. Updated Package Outline.</li> </ul>

# Affected Documents(2)

ID	ET No	Document	Date	Revision	Remarks
6	ET-00108	Datasheet	May 18, 2022	22505	<ul style="list-style-type: none"><li>1. Updated Table 11-2 Equivalent Circuit.</li><li>2. Updated AC Characteristics.</li><li>3. Updated Table 12-7 Current Consumption.</li><li>4. Updated Fig. 13-1 Spectral Sensitivity Characteristics.</li><li>5. Updated Image Sensor Characteristics.</li><li>6. Updated Table 17-2 List of Output Mode (MIPI CSI-2 4-lane).</li><li>7. Updated Example of Peripheral Circuit.</li><li>8. Updated Table 20-2 Spot Pixel Specification (Sub-pixel2).</li><li>9. Updated Notice on White Pixels Specifications.</li><li>10. Updated Marking.</li><li>11. Updated Package Outline.</li></ul>

# Purpose

This report is intended to provide application developers with errata information about the IMX623-AAQV-W documents as follows:

- The IMX623-AAQV-W DataSheet

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# Errata 1-1. Recommended CRA

## Revision 0.0.0:

### 2. Feature

Delete Recommended CRA

### 2. Features

- ◆ CMOS active pixel type
- ◆ Number of recommended recording pixels: 1920 (H) × 1536 (V) approx. 2.95 M pixels
- ◆ Recommended CRA: 21.8 degrees
- ◆ Input frequency (OSCI clock): 18 / 24 / 30 MHz (Oscillator / Crystal resonator) (T.B.D.)
- ◆ External communication interface : I2C communication

## Revision 0.0.1:

### 2. Feature

Delete Recommended CRA .

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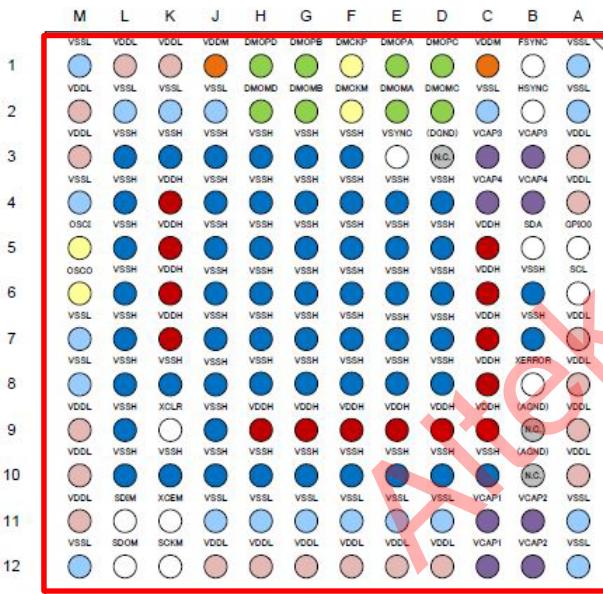
# Errata 1-2. Rename the power supply pins ,GND pins, Sync pins and GPIO pin ①

## Revision 0.0.0:

### 5. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 3.3 V)	V <sub>DDH</sub>	3.135	3.30	3.465	V
Supply voltage (interface 1.8 V)	V <sub>DDM</sub>	1.70	1.80	1.90	V
Supply voltage (digital 1.1 V)	V <sub>DOL</sub>	1.00	1.10	1.20	V
Operating temperature	Topr	Ta = -40 to +105 and T <sub>j</sub> = -40 to +125			°C
Storage temperature	Tstg	Ta = -40 to +125			°C

### 10. Pin Configuration



## Revision 0.0.1:

### 5. Recommended Operating Conditions

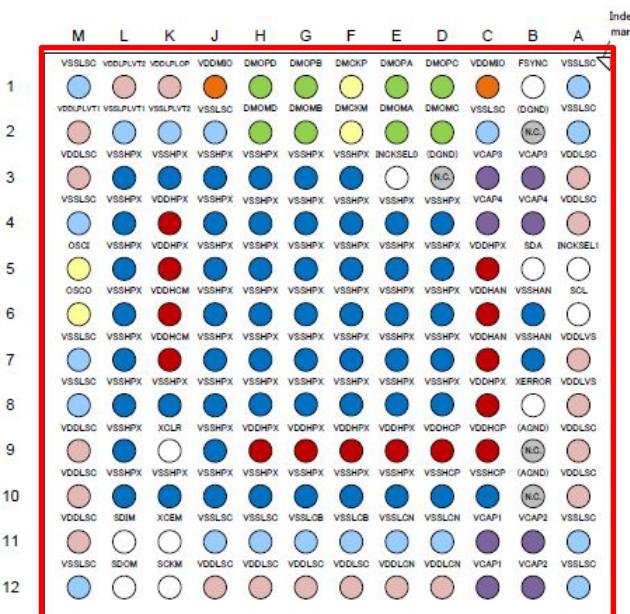
Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 3.3 V)	A <sub>V<sub>DD</sub></sub> <sup>1</sup>	3.135	3.30	3.465	V
Supply voltage (interface 1.8 V)	O <sub>V<sub>DD</sub></sub> <sup>2</sup>	1.70	1.80	1.90	V
Supply voltage (digital 1.1 V)	D <sub>V<sub>DD</sub></sub> <sup>3</sup>	1.00	1.10	1.20	V
Operating temperature	Topr	Ta = -40 to +105 and T <sub>j</sub> = -40 to +125			°C
Storage temperature	Tstg	Ta = -40 to +125			°C

\*1 AV<sub>DD</sub>: VDDHPX, VDDHAN, VDDHDA, VDDHCP, VDDHCM

\*2 OV<sub>DD</sub>: VDDMIO

\*3 DV<sub>DD</sub>: VDDLSC, VDDLGN, VDDLVS, VDDLPLOP, VDDLPVT1, VDDLPVT2

### 10. Pin Configuration



# Errata 1-2. Rename the power supply and GPIO pin②

## Revision 0.0.0:

11. Pin Description

Table 11-1 Pin List

No.	Pin No.	I/O	Analog/Digital	Symbol
1	A1	GND	Digital	VSSL
2	A2	GND	Digital	VSSL
3	A3	Power	Digital	VDDL
4	A4	Power	Digital	VDDL
5	A5	I/O	Digital	GPIO0
6	A6	I/O	Digital	SCI
7	A7	Power	Digital	VDDL
8	A8	Power	Digital	VDDL
9	A9	Power	Digital	VDDL
10	A10	Power	Digital	VDDL
11	A11	GND	Digital	VSSL
12	A12	GND	Digital	VSSL
13	B1	I/O	Digital	FSYNC
14	B2	-	Digital	VCMIC
15	B3	Input	Analog	VCAP3
16	B4	Output	Analog	VCAP4
17	B5	I/O	Digital	SDA
18	B6	GND	Analog	VSSH
19	B7	GND	Analog	VSSH
20	B8	Output	Digital	XERROR
21	B9	-	-	N.C.
22	B10	-	-	N.C.
23	B11	Output	Analog	VCAP2
24	B12	Output	Analog	VCAP2
25	C1	Power	Digital	VDDM
26	C2	GND	Digital	VSSL
27	C3	Input	Analog	VCAP3
28	C4	Output	Analog	VCAP4
29	C5	Power	Analog	VDDH
30	C6	Power	Analog	VDDH
31	C7	Power	Analog	VDDH
32	C8	Power	Analog	VDDH
33	C9	Power	Analog	VDDH
34	C10	GND	Analog	VSSH
35	C11	Output	Analog	VCAP1
36	C12	Output	Analog	VCAP1
37	D1	Output	Digital	DMOPC
38	D2	Output	Digital	DMOMC
39	D3	-	-	N.C.
40	D4	GND	Analog	VSSH
41	D5	GND	Analog	VSSH
42	D6	GND	Analog	VSSH
43	D7	GND	Analog	VSSH
44	D8	GND	Analog	VSSH
45	D9	Power	Analog	VDDH
46	D10	GND	Analog	VSSH
47	D11	GND	Digital	VSSL
48	D12	Power	Digital	VDDL
49	E1	Output	Digital	DMOPA
50	E2	Output	Digital	DMOMA
51	E3	I/O	Digital	INCKSEL

## Revision 0.0.1:

11. Pin Description

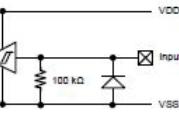
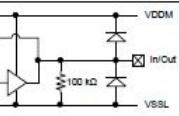
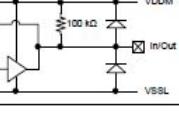
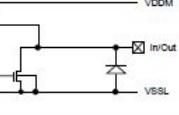
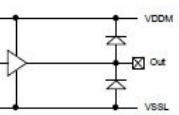
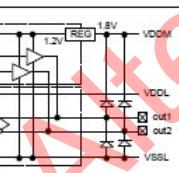
Table 11-1 Pin List

No.	Pin No.	I/O	Analog/Digital	Symbol
1	A1	GND	Digital	VSSLSC
2	A2	GND	Digital	VSSLSC
3	A3	Power	Digital	VDDLSC
4	A4	Power	Digital	VDDLSC
5	A5	Input	Digital	INCKSEL
6	A6	I/O	Digital	SCL
7	A7	Power	Digital	VDDLVS
8	A8	Power	Digital	VDDLSC
9	A9	Power	Digital	VDDLSC
10	A10	Power	Digital	VDDLSC
11	A11	GND	Digital	VSSLSC
12	A12	GND	Digital	VSSLSC
13	B1	I/O	Digital	FSYNC
14	B2	-	-	N.C.
15	B3	Input	Analog	VCAP3
16	B4	Output	Analog	VCAP4
17	B5	I/O	Digital	SDA
18	B6	GND	Analog	VSSHAN
19	B7	GND	Analog	VSSHAN
20	B8	Output	Digital	XERROR
21	B9	-	-	N.C.
22	B10	-	-	N.C.
23	B11	Output	Analog	VCAP2
24	B12	Output	Analog	VCAP2
25	C1	Power	Digital	VDDMIO
26	C2	GND	Digital	VSSLSC
27	C3	Input	Analog	VCAP3
28	C4	Output	Analog	VCAP4
29	C5	Power	Analog	VDDHPX
30	C6	Power	Analog	VDDHAN
31	C7	Power	Analog	VDDHAN
32	C8	Power	Analog	VDDHPX
33	C9	Power	Analog	VDDHCP
34	C10	GND	Analog	VSSHCP
35	C11	Output	Analog	VCAP1
36	C12	Output	Analog	VCAP1
37	D1	Output	Digital	DMOPC
38	D2	Output	Digital	DMOMC
39	D3	-	-	N.C.
40	D4	GND	Analog	VSSH
41	D5	GND	Analog	VSSH
42	D6	GND	Analog	VSSH
43	D7	GND	Analog	VSSH
44	D8	GND	Analog	VSSH
45	D9	Power	Analog	VDDH
46	D10	GND	Analog	VSSH
47	D11	GND	Digital	VSSL
48	D12	Power	Digital	VDDL
49	E1	Output	Digital	DMOPA
50	E2	Output	Digital	DMOMA
51	E3	Input	Digital	INCKSEL
52	E4	GND	Analog	VSSH
53	E5	GND	Analog	VSSH
54	E6	GND	Analog	VSSH
55	E7	GND	Analog	VSSH
56	E8	GND	Analog	VSSH
57	E9	Power	Analog	VDDH
58	E10	GND	Analog	VSSH
59	E11	GND	Digital	VSSL
60	E12	Power	Digital	VDDL
61	F1	Output	Digital	DMCKP
62	F2	Output	Digital	DMCKM
63	F3	GND	Analog	VSSH
64	F4	GND	Analog	VSSH
65	F5	GND	Analog	VSSH
66	F6	GND	Analog	VSSH
67	F7	GND	Analog	VSSH
68	F8	GND	Analog	VSSH
69	F9	Power	Analog	VDDH
70	F10	GND	Analog	VSSH
71	F11	GND	Digital	VSSL
72	F12	Power	Digital	VDDL
73	G1	Output	Digital	DMOPB
74	G2	Output	Digital	DMOMB
75	G3	GND	Analog	VSSH
76	G4	GND	Analog	VSSH
77	G5	GND	Analog	VSSH
78	G6	GND	Analog	VSSH
79	G7	GND	Analog	VSSH
80	G8	GND	Analog	VSSH
81	G9	Power	Analog	VDDH
82	G10	GND	Analog	VSSH
83	G11	GND	Digital	VSSL
84	G12	Power	Digital	VDDL
85	H1	Output	Digital	DMOPD
86	H2	Output	Digital	DMOMD
87	H3	GND	Analog	VSSH
88	H4	GND	Analog	VSSH
89	H5	GND	Analog	VSSH
90	H6	GND	Analog	VSSH
91	H7	GND	Analog	VSSH
92	H8	GND	Analog	VSSH
93	H9	Power	Analog	VDDH
94	G10	GND	Analog	VSSH
95	H11	GND	Digital	VSSL
96	H12	Power	Digital	VDDM
97	J1	Power	Digital	VDDM
98	J2	GND	Digital	VSSL
99	J3	GND	Analog	VSSH
100	J4	GND	Analog	VSSH
101	J5	GND	Analog	VSSH
102	J6	GND	Analog	VSSH
103	J7	GND	Analog	VSSH
104	J8	GND	Analog	VSSH
105	J9	GND	Analog	VSSH
106	J10	GND	Analog	VSSH
107	J11	GND	Digital	VSSL
108	J12	Power	Digital	VDDL
109	K1	Power	Digital	VDDL
110	K2	GND	Digital	VSSL
111	K3	GND	Analog	VSSH
112	K4	Power	Analog	VDDH
113	K5	Power	Analog	VDDH
114	K6	Power	Analog	VDDH
115	K7	Power	Analog	VDDH
116	K8	GND	Analog	VSSH
117	K9	Input	Digital	XCLR
118	K10	GND	Analog	VSSH
119	K11	I/O	Digital	XCEM
120	K12	I/O	Digital	SCKM
121	L1	Power	Digital	VDDL
122	L2	GND	Digital	VSSL
123	L3	GND	Analog	VSSH
124	L4	GND	Analog	VSSH
125	L5	GND	Analog	VSSH
126	L6	GND	Analog	VSSH
127	L7	GND	Analog	VSSH
128	L8	GND	Analog	VSSH
129	L9	GND	Analog	VSSH
130	L10	GND	Analog	VSSH
131	L11	I/O	Digital	SDIM
132	L12	I/O	Digital	SDIM
133	M1	GND	Digital	VSSL
134	M2	Power	Digital	VDDL
135	M3	Power	Digital	VDDL
136	M4	GND	Digital	VSSL
137	M5	Input	Digital	OSCI
138	M6	Output	Digital	OSCO
139	M7	GND	Digital	VSSLSC
140	M8	GND	Digital	VSSLSC
141	M9	Power	Digital	VDDHAN
142	M10	Power	Digital	VDDHAN
143	M11	Power	Digital	VDDHAN
144	M12	GND	Digital	VSSLSC
145	H1	GND	Analog	VSSH
146	H2	Output	Digital	DMOPD
147	H3	GND	Analog	VSSH
148	H4	GND	Analog	VSSH
149	H5	GND	Analog	VSSH
150	H6	GND	Analog	VSSH
151	H7	GND	Analog	VSSH
152	H8	GND	Analog	VSSH
153	H9	Power	Analog	VDDHPX
154	H10	GND	Analog	VSSH
155	H11	GND	Digital	VSSLSC
156	H12	Power	Digital	VDDLSC
157	J1	Power	Digital	VDDMIO
158	J2	GND	Digital	VSSLSC
159	J3	GND	Analog	VSSH
160	J4	GND	Analog	VSSH
161	J5	GND	Analog	VSSH
162	J6	GND	Analog	VSSH
163	J7	GND	Analog	VSSH
164	J8	GND	Analog	VSSH
165	J9	GND	Analog	VSSH

# Errata 1-2. Rename the power supply pins ,GND pins, Sync pins and GPIO pin③

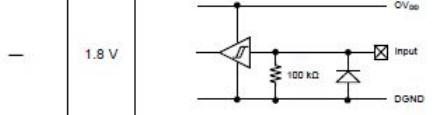
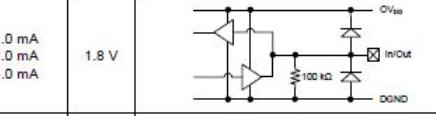
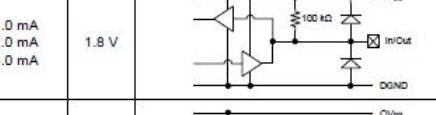
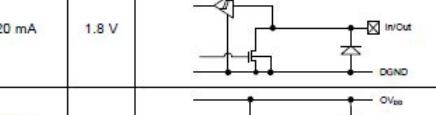
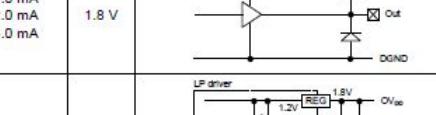
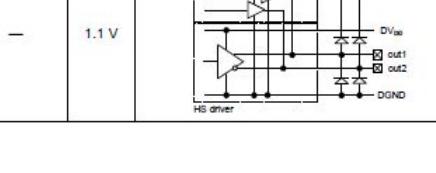
## Revision 0.0.0:

Table 11-2 Equivalent Circuit (T.B.D.)

Symbol	Remarks	Drive Capability	I/F voltage	Equivalent circuit
OSCI OSCO	—	—	1.8 V	T.B.D.
XCLR	Schmitt	—	1.8 V	
HSYNC VSYNC FSYNC GPIO0 SDIM SDOM	Pull-down	1.0 mA 2.0 mA 4.0 mA	1.8 V	
SCKM XCEM	Pull-up	1.0 mA 2.0 mA 4.0 mA	1.8 V	
SDA SCL	Schmitt	20 mA	1.8 V	
XERROR	—	1.0 mA 2.0 mA 4.0 mA	1.8 V	
DMOPA DMOMA DMOPB DMOMB DMOPC DMOMC DMOPD DMOMD DMCKP DMCKM	MIPi CSI-2 output	—	1.1 V	

## Revision 0.0.1:

Table 11-2 Equivalent Circuit (T.B.D.)

Symbol	Remarks	Drive Capability	I/F voltage	Equivalent circuit
OSCI OSCO	—	—	1.8 V	T.B.D.
XCLR	Schmitt	—	1.8 V	
SDIM SDOM FSYNC	Pull-down	1.0 mA 2.0 mA 4.0 mA	1.8 V	
SCKM XCEM	Pull-up	1.0 mA 2.0 mA 4.0 mA	1.8 V	
SDA SCL	Schmitt	20 mA	1.8 V	
XERROR	—	1.0 mA 2.0 mA 4.0 mA	1.8 V	
DMOPA DMOMA DMOPB DMOMB DMOPC DMOMC DMOPD DMOMD DMCKP DMCKM	MIPi CSI-2 output	—	1.1 V	

Pin name and I/O were incorrect.  
 VSYNC→Delete  
 HSYNC→Delete  
 GPIO0 → Delete

# Errata 1-2. Rename the power supply pins ,GND pins, Sync pins and GPIO pin ④

## Revision 0.0.0:

Table 11-3 Pin Status (T.B.D.)

Symbol	I/O	Reset	After Reset	Normal Operating
OSCI	I	T.B.D.	T.B.D.	T.B.D.
OSCO	O	T.B.D.	T.B.D.	T.B.D.
XCLR	I	T.B.D.	T.B.D.	T.B.D.
SCKM	I/O	T.B.D.	T.B.D.	T.B.D.
SDIM	I/O	T.B.D.	T.B.D.	T.B.D.
SDOM	I/O	T.B.D.	T.B.D.	T.B.D.
XCEM	I/O	T.B.D.	T.B.D.	T.B.D.
XERROR	O	T.B.D.	T.B.D.	T.B.D.
SDA	I/O	T.B.D.	T.B.D.	T.B.D.
SCL	I/O	T.B.D.	T.B.D.	T.B.D.
FSYNC	I/O	T.B.D.	T.B.D.	T.B.D.
VSYNC	I/O	T.B.D.	T.B.D.	T.B.D.
Hsync	I/O	T.B.D.	T.B.D.	T.B.D.
GPIO0	I/O	T.B.D.	T.B.D.	T.B.D.
DMOPC	O	T.B.D.	T.B.D.	T.B.D.
DMOMC	O	T.B.D.	T.B.D.	T.B.D.
DMOPA	O	T.B.D.	T.B.D.	T.B.D.
DMOMA	O	T.B.D.	T.B.D.	T.B.D.
DMCKP	O	T.B.D.	T.B.D.	T.B.D.
DMCKM	O	T.B.D.	T.B.D.	T.B.D.
DMOPB	O	T.B.D.	T.B.D.	T.B.D.
DMOMB	O	T.B.D.	T.B.D.	T.B.D.
DMOPD	O	T.B.D.	T.B.D.	T.B.D.
DMOMD	O	T.B.D.	T.B.D.	T.B.D.

## Revision 0.0.1:

Table 11-3 Pin Status (T.B.D.)

Symbol	I/O	Reset	After Reset	Normal Operating
OSCI	I	T.B.D.	T.B.D.	T.B.D.
OSCO	O	T.B.D.	T.B.D.	T.B.D.
XCLR	I	T.B.D.	T.B.D.	T.B.D.
SCKM	I/O	T.B.D.	T.B.D.	T.B.D.
SDIM	I/O	T.B.D.	T.B.D.	T.B.D.
SDOM	I/O	T.B.D.	T.B.D.	T.B.D.
XCEM	I/O	T.B.D.	T.B.D.	T.B.D.
XERROR	O	T.B.D.	T.B.D.	T.B.D.
SDA	I/O	T.B.D.	T.B.D.	T.B.D.
SCL	I/O	T.B.D.	T.B.D.	T.B.D.
FSYNC	I/O	T.B.D.	T.B.D.	T.B.D.
INCKSEL0	I	T.B.D.	T.B.D.	T.B.D.
INCKSEL1	I	T.B.D.	T.B.D.	T.B.D.
DMOPC	O	T.B.D.	T.B.D.	T.B.D.
DMOMC	O	T.B.D.	T.B.D.	T.B.D.
DMOPA	O	T.B.D.	T.B.D.	T.B.D.
DMOMA	O	T.B.D.	T.B.D.	T.B.D.
DMCKP	O	T.B.D.	T.B.D.	T.B.D.
DMCKM	O	T.B.D.	T.B.D.	T.B.D.
DMOPB	O	T.B.D.	T.B.D.	T.B.D.
DMOMB	O	T.B.D.	T.B.D.	T.B.D.
DMOPD	O	T.B.D.	T.B.D.	T.B.D.
DMOMD	O	T.B.D.	T.B.D.	T.B.D.

Pin name and I/O were incorrect.  
VSYNC→INCKSEL0  
Hsync→Delete  
GPIO0 →INCKSEL1

# Errata 1-2. Rename the power supply pins ,GND pins, Sync pins and GPIO pin ⑥

## Revision 0.0.0:

Table 11-3 Pin Status (T.B.D.)

Symbol	I/O	Reset	After Reset	Normal Operating
OSCI	I	T.B.D.	T.B.D.	T.B.D.
OSCO	O	T.B.D.	T.B.D.	T.B.D.
XCLR	I	T.B.D.	T.B.D.	T.B.D.
SCKM	I/O	T.B.D.	T.B.D.	T.B.D.
SDIM	I/O	T.B.D.	T.B.D.	T.B.D.
SDOM	I/O	T.B.D.	T.B.D.	T.B.D.
XCEM	I/O	T.B.D.	T.B.D.	T.B.D.
XERROR	O	T.B.D.	T.B.D.	T.B.D.
SDA	I/O	T.B.D.	T.B.D.	T.B.D.
SCL	I/O	T.B.D.	T.B.D.	T.B.D.
FSYNC	I/O	T.B.D.	T.B.D.	T.B.D.
VSYNC	I/O	T.B.D.	T.B.D.	T.B.D.
Hsync	I/O	T.B.D.	T.B.D.	T.B.D.
GPIO0	I/O	T.B.D.	T.B.D.	T.B.D.
DMOPC	O	T.B.D.	T.B.D.	T.B.D.
DMOMC	O	T.B.D.	T.B.D.	T.B.D.
DMOPA	O	T.B.D.	T.B.D.	T.B.D.
DMOMA	O	T.B.D.	T.B.D.	T.B.D.
DMCKP	O	T.B.D.	T.B.D.	T.B.D.
DMCKM	O	T.B.D.	T.B.D.	T.B.D.
DMOPB	O	T.B.D.	T.B.D.	T.B.D.
DMOMB	O	T.B.D.	T.B.D.	T.B.D.
DMOPD	O	T.B.D.	T.B.D.	T.B.D.
DMOMD	O	T.B.D.	T.B.D.	T.B.D.

## Revision 0.0.1:

Table 11-3 Pin Status (T.B.D.)

Symbol	I/O	Reset	After Reset	Normal Operating
OSCI	I	T.B.D.	T.B.D.	T.B.D.
OSCO	O	T.B.D.	T.B.D.	T.B.D.
XCLR	I	T.B.D.	T.B.D.	T.B.D.
SCKM	I/O	T.B.D.	T.B.D.	T.B.D.
SDIM	I/O	T.B.D.	T.B.D.	T.B.D.
SDOM	I/O	T.B.D.	T.B.D.	T.B.D.
XCEM	I/O	T.B.D.	T.B.D.	T.B.D.
XERROR	O	T.B.D.	T.B.D.	T.B.D.
SDA	I/O	T.B.D.	T.B.D.	T.B.D.
SCL	I/O	T.B.D.	T.B.D.	T.B.D.
FSYNC	I/O	T.B.D.	T.B.D.	T.B.D.
INCKSEL0	I	T.B.D.	T.B.D.	T.B.D.
INCKSEL1	I	T.B.D.	T.B.D.	T.B.D.
DMOPC	O	T.B.D.	T.B.D.	T.B.D.
DMOMC	O	T.B.D.	T.B.D.	T.B.D.
DMOPA	O	T.B.D.	T.B.D.	T.B.D.
DMOMA	O	T.B.D.	T.B.D.	T.B.D.
DMCKP	O	T.B.D.	T.B.D.	T.B.D.
DMCKM	O	T.B.D.	T.B.D.	T.B.D.
DMOPB	O	T.B.D.	T.B.D.	T.B.D.
DMOMB	O	T.B.D.	T.B.D.	T.B.D.
DMOPD	O	T.B.D.	T.B.D.	T.B.D.
DMOMD	O	T.B.D.	T.B.D.	T.B.D.

Pin name and I/O were incorrect.  
VSYNC→INCKSEL0  
Hsync→Delete  
GPIO0 →INCKSEL1

# Errata 1-2. Rename the power supply pins ,GND pins, Sync pins and GPIO pin ⑤

## Revision 0.0.0:

### 12.1. DC Characteristics

Table 12-1 DC Characteristics (T.B.D.)

Item	Pins	Condition	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDDH	—	V <sub>DDH</sub>	3.315	3.30	3.485	V
	VDDM	—	V <sub>DDM</sub>	1.70	1.80	1.90	V
	VDDL	—	V <sub>DDL</sub>	1.00	1.10	1.20	V
Digital input voltage	OSCI XCLR HYSNC VSYNC FSYNC GPIO0 SDIM SDOM	—	V <sub>IH</sub>	0.75 × V <sub>DDM</sub>	—	—	V
		—	V <sub>IL</sub>	—	—	0.25 × V <sub>DDM</sub>	V
Digital output voltage	XCEM SCKM SDOM SDIM HYSNC VSYNC FSYNC XERROR GPIO0	IOH= -4mA IOH= -2mA IOH= -1mA	V <sub>OH</sub>	V <sub>DDM</sub> - 0.2	—	—	V
		IOL= 4mA IOL= 2mA IOL= 1mA	V <sub>OL</sub>	—	—	0.2	V

### 12.3. Current Consumption (T.B.D.)

Table 12-8 Current Consumption

Item	Pins	Symbol	Typ.	Max.	Unit
Operating current <sup>3</sup>	VDDH	I <sub>VDDH</sub>	T.B.D.	T.B.D.	mA
	VDDM	I <sub>VDDM</sub>	T.B.D.	T.B.D.	mA
	VDDL	I <sub>VDDL</sub>	T.B.D.	T.B.D.	mA

Operating current: (Typ.) Supply voltage 3.3 V / 1.8 V / 1.1 V, T<sub>j</sub> = 25 °C, the light condition: T.B.D.  
(Max.) T.B.D. the light condition: at signal saturated.

## Revision 0.0.1:

### 12.1. DC Characteristics

Table 12-1 DC Characteristics (T.B.D.)

Item	Pins	Condition	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDDHPX	—	A <sub>VDD</sub>	3.315	3.30	3.485	V
	VDDHAN	—					
	VDDHCP	—					
Interface	VDDHCM	—					
	VDDMIO	—	O <sub>VDD</sub>	1.70	1.80	1.90	V
Digital	VDDLSC	—					
	VDDLGN	—					
Digital input voltage	VDDLVS	—					
	VDDLPLVT1	—					
Digital output voltage	VDDLPLVT2	—					
	VDDLPLOP	—					
OSCI XCLR FSYNC INCKSEL0 INCKSEL1	—	V <sub>IH</sub>	0.8 × O <sub>VDD</sub>	—	—	—	V
	SDIM SDOM	—	V <sub>IL</sub>	—	—	0.2 × O <sub>VDD</sub>	V
Digital output voltage	XCEM SCKM SDOM SDIM FSYNC XERROR	IOH= -4mA IOH= -2mA IOH= -1mA	V <sub>OH</sub>	O <sub>VDD</sub> - 0.2	—	—	V
		IOL= 4mA IOL= 2mA IOL= 1mA	V <sub>OL</sub>	—	—	0.2	V

### 12.3. Current Consumption (T.B.D.)

Table 12-6 Current Consumption

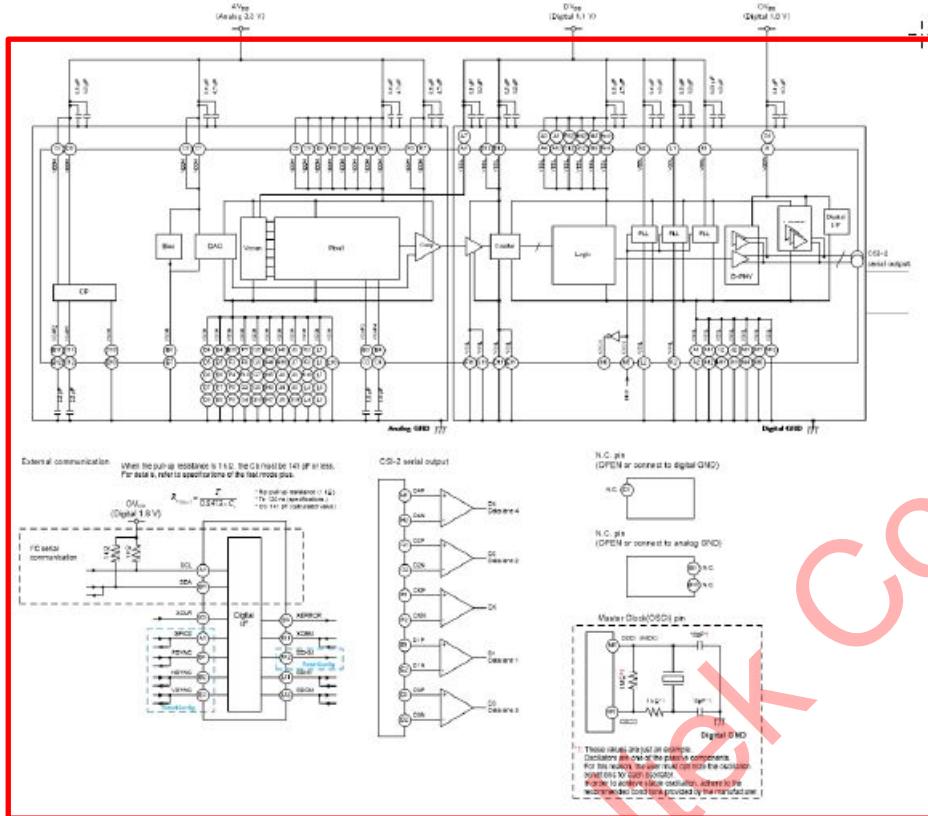
Item	Pins	Symbol	Typ.	Max.	Unit
Operating current <sup>3</sup>	VDDHPX	I <sub>A<sub>VDD</sub></sub>	T.B.D.	T.B.D.	mA
	VDDHAN				
	VDDHCP				
Interface	VDDHCM				
	VDDMIO	I <sub>O<sub>VDD</sub></sub>	T.B.D.	T.B.D.	mA
Digital	VDDLSC				
	VDDLGN				
Digital input voltage	VDDLVS				
	VDDLPLVT1				
Digital output voltage	VDDLPLVT2				
	VDDLPLOP				

Operating current: (Typ.) Supply voltage 3.3 V / 1.8 V / 1.1 V, T<sub>j</sub> = 25 °C, the light condition: T.B.D.  
(Max.) T.B.D. the light condition: at signal saturated.

# Errata 1-2. Rename the power supply pins ,GND pins, Sync pins and GPIO pin ⑥

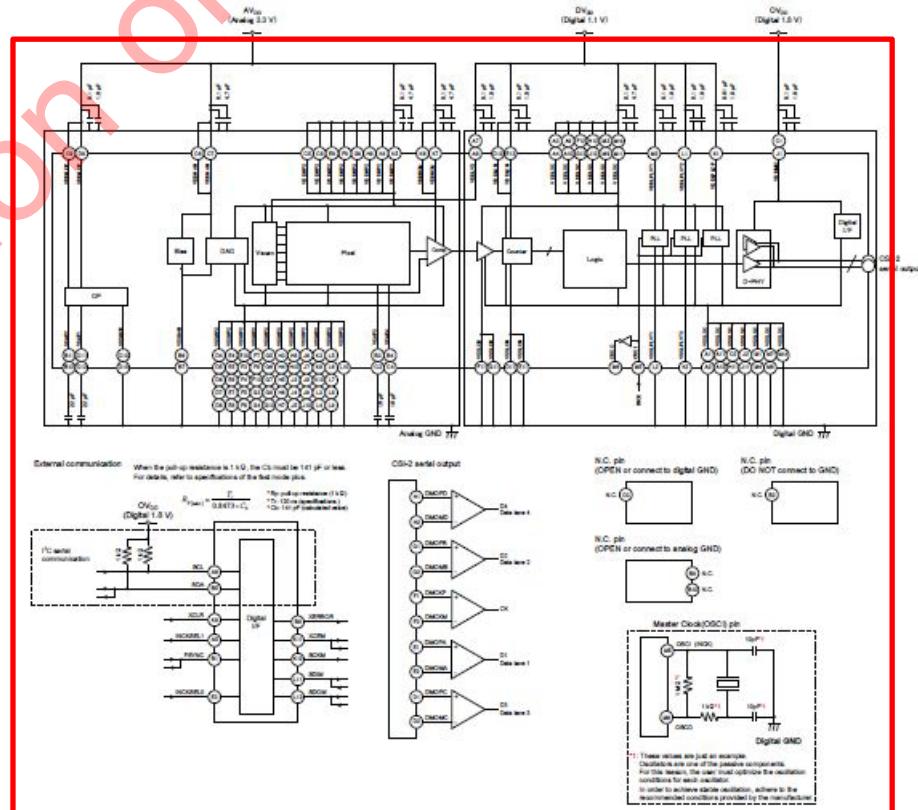
## Revision 0.0.0:

18. Example of Peripheral Circuit (T.B.D.)



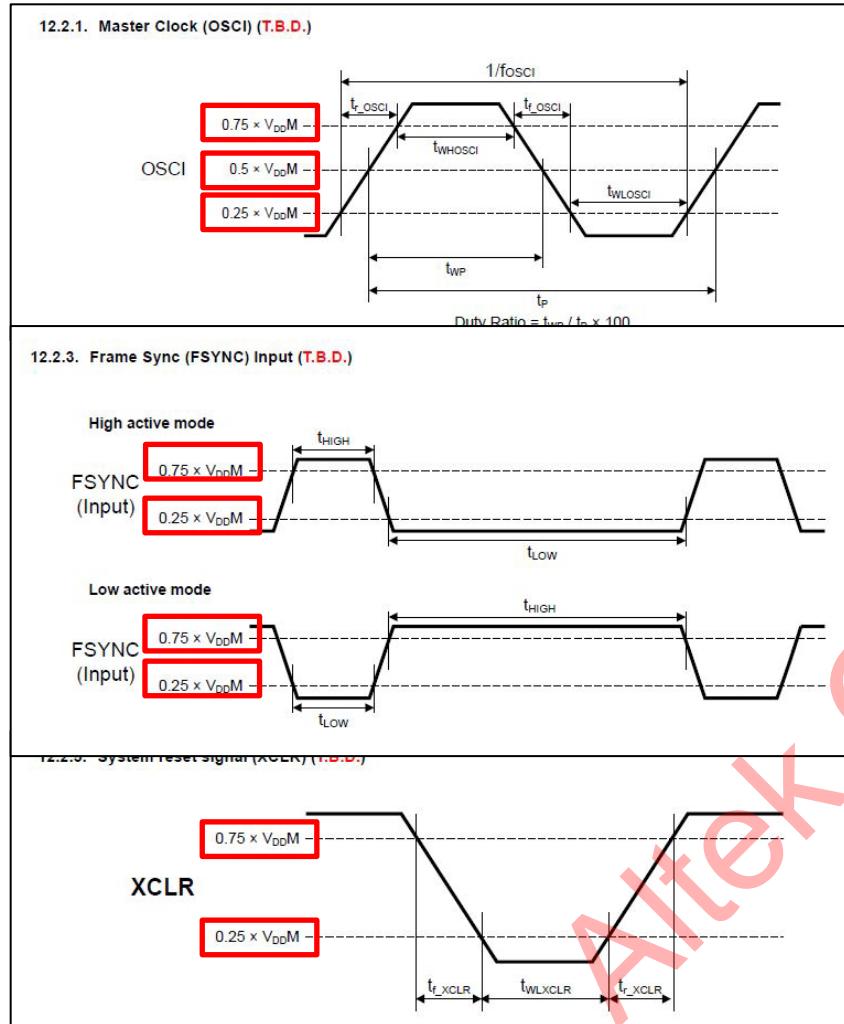
## Revision 0.0.1:

18. Example of Peripheral Circuit (T.B.D.)

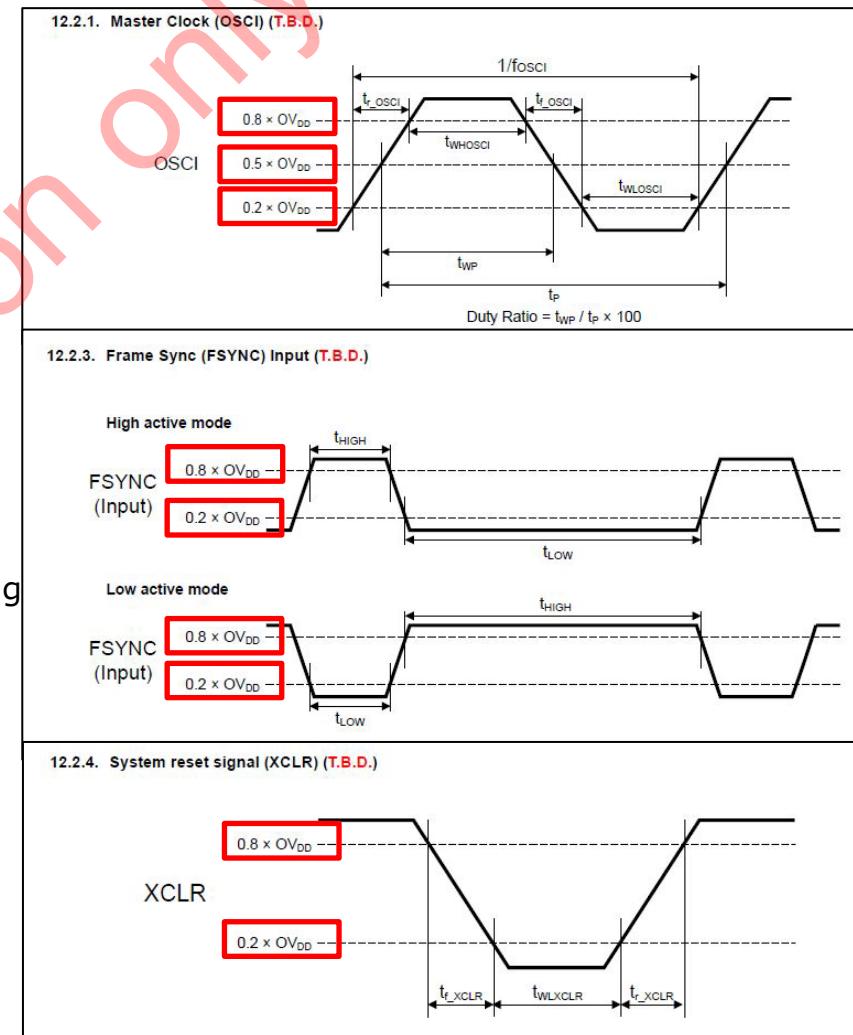


# Errata 1-3. AC specification

## Revision 0.0.0:

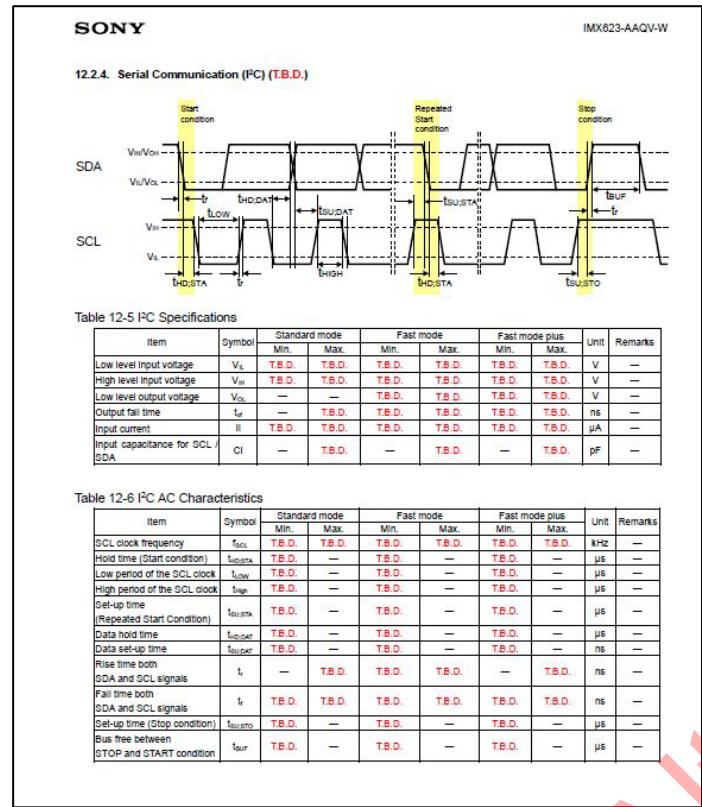


## Revision 0.0.1:



# Errata 1-4. Serial communication

## Revision 0.0.0:



## Revision 0.0.1:

Removed to comply with I<sub>C</sub> communication.

# Errata 1-5. Output Mode(MIPI serial)

## Revision 0.0.0:

17.6.1 Output Mode(MIPI serial).

Table 17-2 List of Output Mode (MIPI CSI-2 4-lane) (T.B.D.)

Output Mode	HDR Combine	Frame Rate [frames/s]	AD bit	Output Format	Valid Size		Total Size		Data rate [Mbps/lane]
					H [pixels]	V [lines]	H [pixels]	V [lines]	
Normal Output	Uncombined	60	10	RAW12	2214	1626	648		
		30	12		2400	1750	378		
		60	10		2214	1626	756		
		30	12		2400	1750	441		
		60	10	RAW16	2214	1626	864		
		30	12		2200	1750	462		
		60	10		2214	1626	1080		
		30	12		2400	1750	630		
		60	10	RAW20	2214	1626	1296		
		30	12		2200	1750	693		
HDR Combined Output	Combined	60	10		2214	1626	648		
		30	12		2400	1750	378		
		60	10		2214	1626	756		
		30	12		2400	1750	441		
		60	10		2214	1626	864		
		30	12		2200	1750	462		
		60	10		2214	1626	1080		
		30	12		2400	1750	630		
		60	10		2214	1626	1296		
		30	12		2200	1750	693		
HDR Uncombined Output (Line / Line)	Uncombined	60	10	RAW12x2	2460	3252	1440		
		30	12	RAW12x4	2200	3500	693		
		30	10	RAW12x4	6224	2270	7000	1430.1	

## Revision 0.0.1:

17.6.1 Output Mode(MIPI serial).

Table 17-3 List of Output Mode (MIPI CSI-2 2-lane) (T.B.D.)

Output Mode	HDR Combine	Frame Rate [frames/s]	AD bit	Output Format	Valid Size		Total Size		Data rate [Mbps/lane]
					H [pixels]	V [lines]	H [pixels]	V [lines]	
Normal Output	Uncombined	60	10	RAW12	2214	1626	648		
		30	12		2400	1750	378		
		60	10		2152.5	1626	1470		
		30	12		2400	1750	882		
		60	10	RAW16	-	-	-	-	
		30	12		2200	1750	924		
		60	10		-	-	-	-	
		30	12		2400	1750	1260		
		60	10	RAW20	-	-	-	-	
		30	12		2200	1750	1386		
HDR Combined Output	Combined	60	10		2214	1626	648		
		30	12		2400	1750	378		
		60	10		2091	1626	1428		
		30	12		2400	1750	882		
		60	10		-	-	-	-	
		30	12		2200	1750	924		
		60	10		-	-	-	-	
		30	12		2400	1750	1260		
		60	10	RAW24	-	-	-	-	
		30	12		2200	1750	1386		
HDR Uncombined Output (Line / Line)	Uncombined	60	10		2214	1626	648		
		30	12		2400	1750	378		
		30	12		3112	2200	3500	1386	

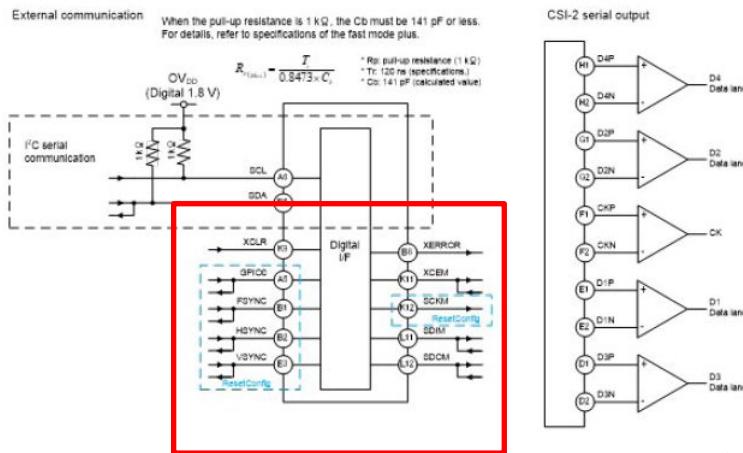
AD bit of HDR uncombined output mode is incorrect.

# Errata 1-6. Example of Peripheral Circuit

## Revision 0.0.0:

### 18. Example of Peripheral Circuit

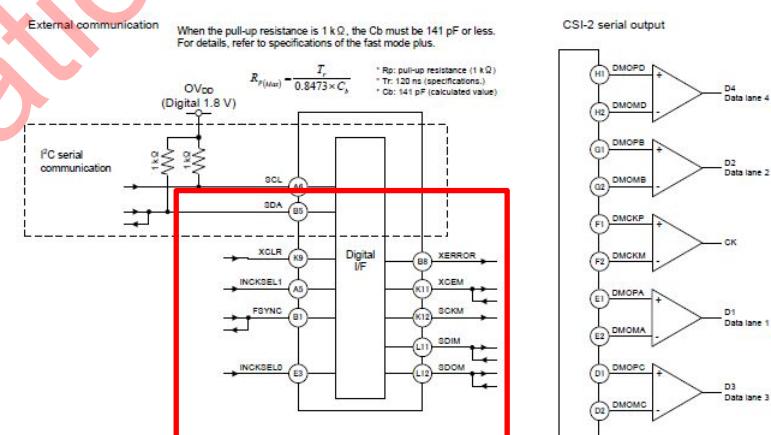
Delete Reset configuration information.



## Revision 0.0.1:

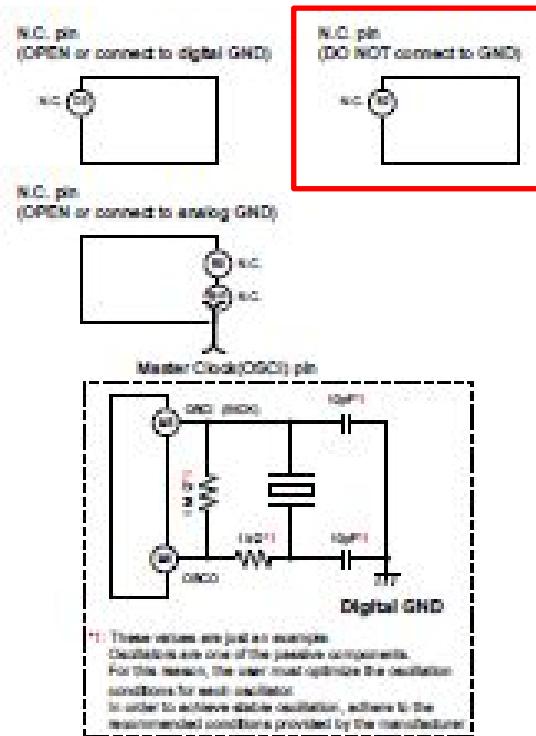
### 18. Example of Peripheral Circuit

Delete Recommended CRA .

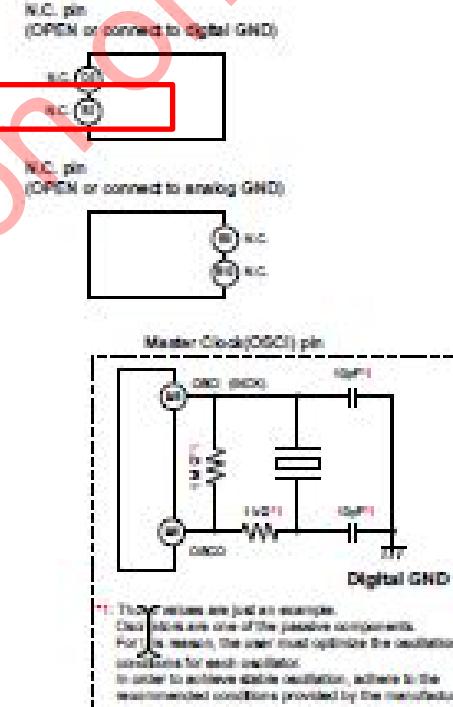


# Errata 2-1. update the Example of Peripheral Circuit

## Revision 0.0.1:

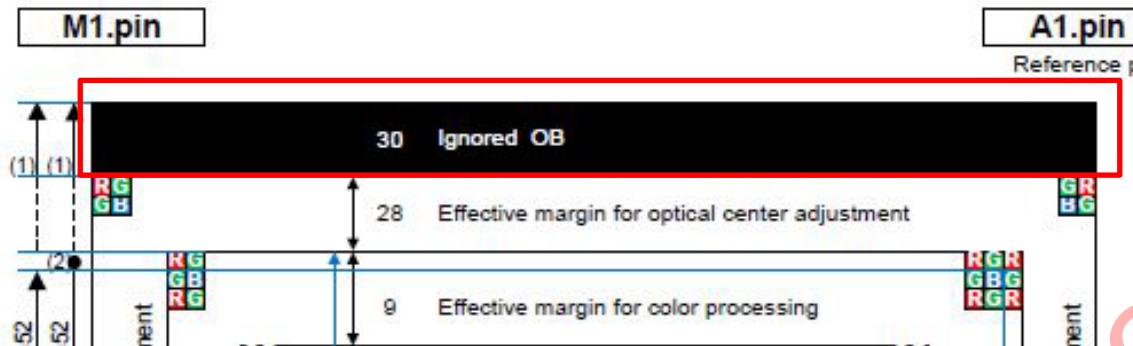


## Revision 0.0.2:

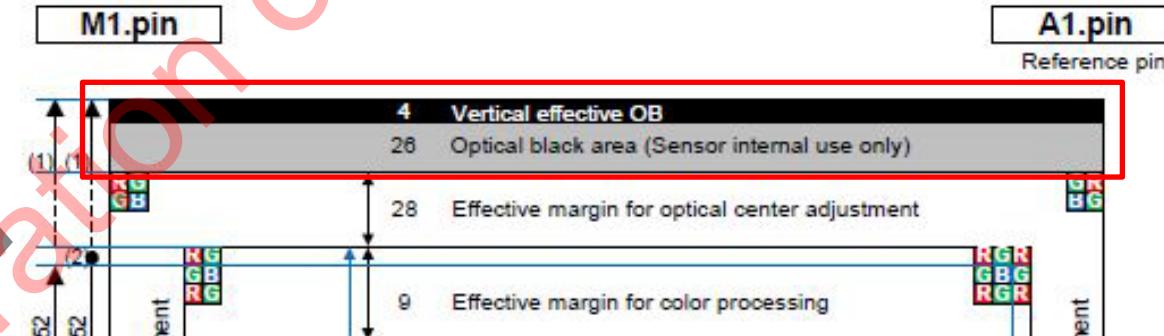


## **Errata 2-2. update the Pixel Arrangement**

# Revision 0.0.1:



## Revision 0.0.2:



Revision 0.0.2

**A1.pin**  
Reference pin

in for optical center adjustment

in for color processing

**M1.pin**

4 V<sub>DD</sub>  
26 GND  
28 E<sub>IN</sub>  
9 E<sub>OUT</sub>

Pinout details:  
 - A1.pin: Reference pin, in for optical center adjustment, in for color processing.  
 - M1.pin: Pin 4 is V<sub>DD</sub>, Pin 26 is GND, Pin 28 is E<sub>IN</sub>, Pin 9 is E<sub>OUT</sub>.  
 - Both pins have a red box around them, and a large red arrow points from A1.pin to M1.pin.

# Errata 3-1. Update the Input Clock Specifications①

## Revision 0.0.2:

- ◆ Input frequency (OSCI clock): 18 / 24 / 30 MHz (Oscillator / Crystal resonator) (T.B.D.)



## Revision 0.1.0:

- ◆ Input frequency (OSCI clock): 18 - 30 MHz (Oscillator / Crystal resonator), recommended frequencies are 18/24/30MHz.

Table 12-2 Input Clock Specifications

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
OSCI clock frequency <sup>*1</sup>	foscI	foscIx0.98(T.B.D.)	foscI	foscIx1.02(T.B.D.)	MHz	foscI = 18 / 24 / 30 MHz
OSCI low level pulse width	tW <sub>OSCI</sub>	10(T.B.D.)	—	—	ns	foscI = 18 / 24 / 30 MHz
OSCI high level pulse width	tW <sub>HOSCI</sub>	10(T.B.D.)	—	—	ns	foscI = 18 / 24 / 30 MHz
OSCI clock duty	Duty ratio	45(T.B.D.)	50(T.B.D.)	55(T.B.D.)	%	Define with 0.5 × CV <sub>DD</sub>
OSCI rise time	t <sub>r</sub> <sub>_osci</sub>	—	—	5(T.B.D.)	ns	20% to 80%
OSCI fall time	t <sub>f</sub> <sub>_osci</sub>	—	—	5(T.B.D.)	ns	20% to 80%

\*1 Any deviations in OSCI fluctuation affects the frame rate.

Table 12-2 Input Clock Specifications

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
OSCI clock frequency <sup>*1</sup>	foscI	foscIx0.98(T.B.D.)	foscI	foscIx1.02(T.B.D.)	MHz	foscI = 18 to 30 MHz
OSCI low level pulse width	tW <sub>OSCI</sub>	10(T.B.D.)	—	—	ns	foscI = 18 to 30 MHz
OSCI high level pulse width	tW <sub>HOSCI</sub>	10(T.B.D.)	—	—	ns	foscI = 18 to 30 MHz
OSCI clock duty	Duty ratio	45(T.B.D.)	50(T.B.D.)	55(T.B.D.)	%	Define with 0.5 × CV <sub>DD</sub>
OSCI rise time	t <sub>r</sub> <sub>_osci</sub>	—	—	5(T.B.D.)	ns	20% to 80%
OSCI fall time	t <sub>f</sub> <sub>_osci</sub>	—	—	5(T.B.D.)	ns	80% to 20%

\*1 Recommended frequencies of OSCI clock are 18/24/30MHz.

\*1 Any deviations in OSCI fluctuation affect the frame rate.

# Errata 3-1. Update the Input Clock Specifications②

## Revision 0.0.2:

Table 17-2 List of Output Mode (MIPI CSI-2 4-lane)

Output Mode	HDR Combine	Frame Rate [frames/s]	AD bit	I
...	...	...	...	...
...	...	...	...	...
...	...	...	...	...
...	...	...	...	...

Table 17-3 List of Output Mode (MIPI CSI-2 2-lane)

Output Mode	HDR Combine	Frame Rate [frames/s]	AD bit	I
...	...	...	...	...
...	...	...	...	...
...	...	...	...	...
...	...	...	...	...

## Revision 0.1.0:

Table 17-2 List of Output Mode (MIPI CSI-2 4-lane)

Output Mode	HDR Combine	Frame Rate [frames/s] <sup>*1</sup>	AD bit	I
...	...	...	...	...
...	...	...	...	...
...	...	...	...	...
...	...	...	...	...

\*1 When using the recommended frequency of OSCI.

Table 17-3 List of Output Mode (MIPI CSI-2 2-lane)

Output Mode	HDR Combine	Frame Rate [frames/s] <sup>*1</sup>	AD bit	I
...	...	...	...	...
...	...	...	...	...
...	...	...	...	...
...	...	...	...	...

\*1 When using the recommended frequency of OSCI.

## Errata 3-2. Update the Pin List(I/O type)

Revision 0.0.2:

5	A5	Input	Digital	INCKSEL1
51	E3	Input	Digital	INCKSEL0

Revision 0.1.0:

5	A5	I/O	Digital	INCKSEL1
51	E3	I/O	Digital	INCKSEL0



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# Errata 3-3. Update the Pin List(Symbol)

Revision 0.0.2:

58	E10	GND	Analog	VSSHCP	Analog GND
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Revision 0.1.0:

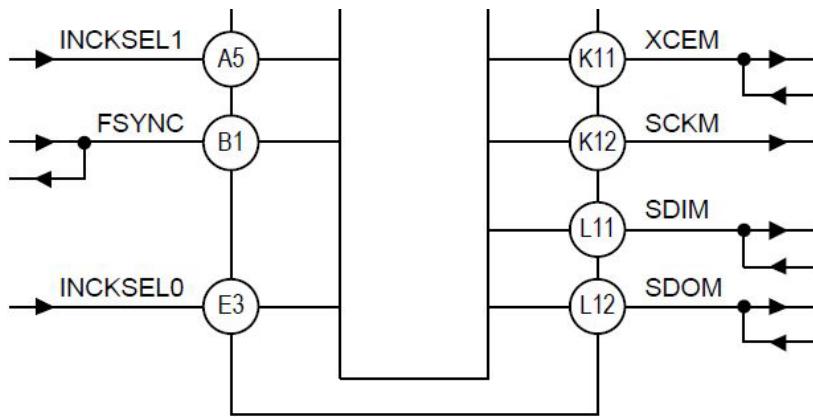
58	E10	GND	Analog	VSSHPX	Analog GND
----	-----	-----	--------	--------	------------



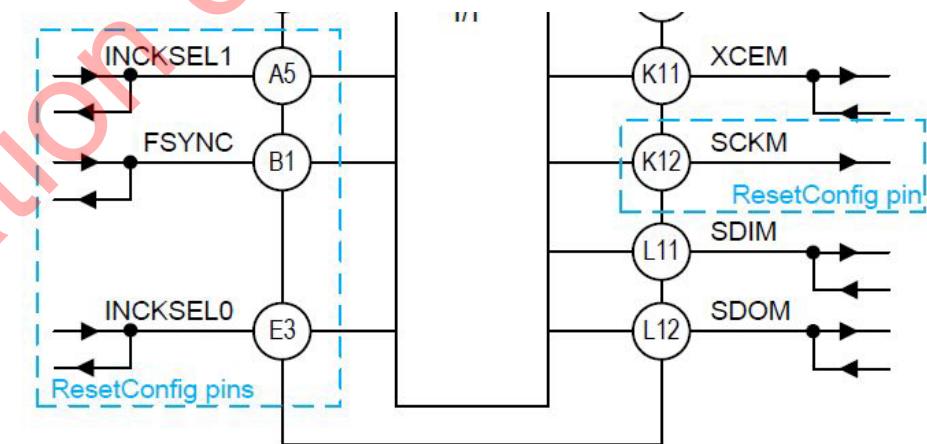
Altek Corporation Only

# Errata 3-4. Update the Example of Peripheral Circuit

Revision 0.0.2:



Revision 0.1.0:



# Errata 4-1. Update the Table 11-3 Pin State

## Revision 0.1.0:

		INPUT L	INPUT H	INPUT H
XCLR	I	INPUT L	INPUT H	INPUT H
SCKM	I/O	INPUT (pull-up)	OUTPUT (SCKM)	OUTPUT (SCKM)
SDIM	I/O	INPUT (pull-down)	INOUT (SDIO1(SDIM))	INOUT (SDIO1(SDIM))
SDOM	I/O	INPUT (pull-down)	INOUT (SDIO0(SDOM))	INOUT (SDIO0(SDOM))
XCEM	I/O	INPUT (pull-up)	OUTPUT (XCEM)	OUTPUT (XCEM)
XERROR	O	OUTPUT L	OUTPUT (XERROR)	OUTPUT (XERROR)
SDA	I/O	INPUT (External pull-up)	INPUT (External pull-up)	INPUT (External pull-up)
SCL	I/O	INPUT (External pull-up)	INPUT (External pull-up)	INPUT (External pull-up)
FSYNC	I/O	INPUT (pull-down)	INPUT (pull-down)	INPUT(FSYNC)
INCKSEL0	I/O	INPUT (pull-down)	INPUT (pull-down)	OUTPUT (INCKSEL0)
INCKSEL1	I/O	INPUT (pull-down)	INPUT (pull-down)	OUTPUT (INCKSEL1)

## Revision 0.1.1:

XCLR	I	INPUT L	INPUT H	INPUT H
SCKM	I/O	INPUT (pull-up)	INOUT OUTPUT <sup>*1</sup> (SCKM)	INOUT OUTPUT <sup>*1</sup> (SCKM)
SDIM	I/O	INPUT (pull-down)	INOUT (SDIO1(SDIM))	INOUT (SDIO1(SDIM))
SDOM	I/O	INPUT (pull-down)	INOUT (SDIO0(SDOM))	INOUT (SDIO0(SDOM))
XCEM	I/O	INPUT (pull-up)	INOUT OUTPUT <sup>*1</sup> (XCEM)	INOUT OUTPUT <sup>*1</sup> (XCEM)
XERROR	O	OUTPUT L	OUTPUT (XERROR)	OUTPUT (XERROR)
SDA	I/O	INPUT (External pull-up)	INPUT (External pull-up)	INPUT (External pull-up)
SCL	I/O	INPUT (External pull-up)	INPUT (External pull-up)	INPUT (External pull-up)
FSYNC	I/O	INPUT (pull-down)	INPUT (pull-down)	INPUT(FSYNC)
INCKSEL0	I/O	INPUT (pull-down)	INPUT (pull-down)	INPUT (INCKSEL0)
INCKSEL1	I/O	INPUT (pull-down)	INPUT (pull-down)	OUTPUT (INCKSEL1)

\*1 When using Serial-NOR-Flash.

# Errata 4-2. Update the Table 12-1 DC Characteristics

## Revision 0.1.0:

Table 12-1 DC Characteristics (T.B.D.)

Item	Pins	Condition	Symbol	Min.	Typ.	Max.	Unit	
Supply voltage	Analog	VDDHPX VDDHAN VDDHCP VDDHCM	—	AV <sub>DD</sub>	3.315	3.30	3.465	V
	Interface	VDDMIO	—	OV <sub>DD</sub>	1.70	1.80	1.90	V
	Digital	VDDLSC VDDLCN VDDLVS VDDLPLVT1 VDDLPLVT2 VDDLPLOP	—	DV <sub>DD</sub>	1.00	1.10	1.20	V
		OSCI XCLR FSYNC INCKSEL0 INCKSEL1 SDIM SDOM	—	V <sub>IH</sub>	0.8 × OV <sub>DD</sub>	—	—	V
Digital input voltage	OSCI XCLR FSYNC INCKSEL0 INCKSEL1 SDIM SDOM	V <sub>IL</sub>	—	—	0.2 × OV <sub>DD</sub>	—	V	
		XCEM SCKM SDOM SDIM FSYNC XERROR	IOH= -4mA IOH= -2mA IOH= -1mA	V <sub>OH</sub>	OV <sub>DD</sub> - 0.2	—	—	V
Digital output voltage	XCEM SCKM SDOM SDIM FSYNC XERROR	IOL= 4mA IOL= 2mA IOL= 1mA	V <sub>OL</sub>	—	—	0.2	V	

## Revision 0.1.1:

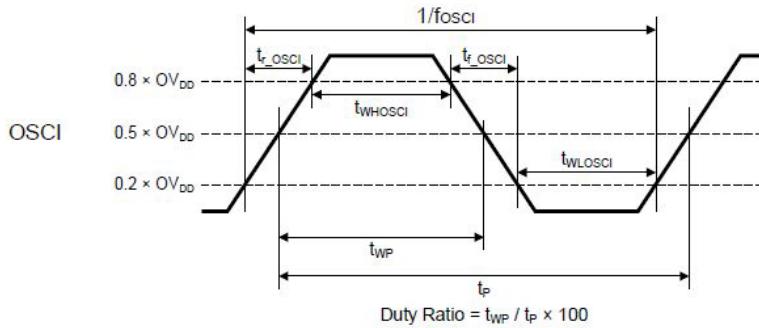
Table 12-1 DC Characteristics

Item	Pins	Condition	Symbol	Min.	Typ.	Max.	Unit	
Supply voltage	Analog	VDDHPX VDDHAN VDDHCP VDDHCM	—	AV <sub>DD</sub>	3.315	3.30	3.465	V
	Interface	VDDMIO	—	OV <sub>DD</sub>	1.70	1.80	1.90	V
	Digital	VDDLSC VDDLCN VDDLVS VDDLPLVT1 VDDLPLVT2 VDDLPLOP	—	DV <sub>DD</sub>	1.00	1.10	1.20	V
		OSCI XCLR FSYNC INCKSEL0 INCKSEL1 SDIM SDOM	—	V <sub>IH</sub>	0.7 × OV <sub>DD</sub>	—	—	V
Digital input voltage	OSCI XCLR FSYNC INCKSEL0 INCKSEL1 SDIM SDOM	V <sub>IL</sub>	—	—	—	0.3 × OV <sub>DD</sub>	V	
		XCEM SCKM SDOM SDIM FSYNC XERROR	IOH= -4mA IOH= -2mA IOH= -1mA	V <sub>OH</sub>	OV <sub>DD</sub> - 0.2	—	—	V
Digital output voltage	XCEM SCKM SDOM SDIM FSYNC XERROR	IOL= 4mA IOL= 2mA IOL= 1mA	V <sub>OL</sub>	—	—	0.2	V	

# Errata 4-3. Update the Master Clock (OSCI)

## Revision 0.1.0:

12.2.1. Master Clock (OSCI)



## Revision 0.1.1:

12.2.1. Master Clock (OSCI)

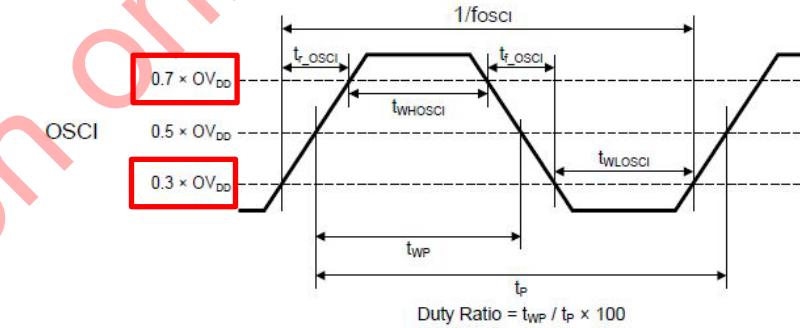


Table 12-2 Input Clock Specifications

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
OSCI clock frequency <sup>*1</sup>	foscI	foscIx0.98(T.B.D.)	foscI	foscIx1.02(T.B.D.)	MHz	foscI = 18 to 30 MHz
OSCI low level pulse width	tWLOSCI	10(T.B.D.)	—	—	ns	foscI = 18 to 30 MHz
OSCI high level pulse width	tWOSCI	10(T.B.D.)	—	—	ns	foscI = 18 to 30 MHz
OSCI clock duty	Duty ratio	45(T.B.D.)	50(T.B.D.)	55(T.B.D.)	%	Define with $0.5 \times OV_{DD}$
OSCI rise time	$t_r_{OSCI}$	—	—	5(T.B.D.)	ns	20% to 80%
OSCI fall time	$t_f_{OSCI}$	—	—	5(T.B.D.)	ns	80% to 20%

\*1 Recommended frequencies of OSCI clock are 18/24/30MHz.

\*1 Any deviations in OSCI fluctuation affect the frame rate.

Table 12-2 Input Clock Specifications

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
OSCI clock frequency <sup>*1</sup>	foscI	foscIx0.98(T.B.D.)	foscI	foscIx1.02(T.B.D.)	MHz	foscI = 18 to 30 MHz
OSCI low level pulse width	tWLOSCI	10(T.B.D.)	—	—	ns	foscI = 18 to 30 MHz
OSCI high level pulse width	tWOSCI	10(T.B.D.)	—	—	ns	foscI = 18 to 30 MHz
OSCI clock duty	Duty ratio	40	50	60	%	Define with $0.5 \times OV_{DD}$
OSCI rise time	$t_r_{OSCI}$	—	—	5(T.B.D.)	ns	30% to 70%
OSCI fall time	$t_f_{OSCI}$	—	—	5(T.B.D.)	ns	70% to 30%

\*1 Recommended frequencies of OSCI clock are 18/24/30MHz.

\*1 Any deviations in OSCI fluctuation affect the frame rate.

# Errata 4-4. Update the AC Characteristics

## Revision 0.1.0:

### Contents

1. Description
2. Features
3. Device Structure
4. Absolute Maximum Ratings
5. Recommended Operating Conditions
6. USE RESTRICTION NOTICE
7. Optical Center
8. Pixel Arrangement
9. Block Diagram
10. Pin Configuration
11. Pin Description
12. Electrical Characteristics
  - 12.1. DC Characteristics
  - 12.2. AC Characteristics
    - 12.2.1. Master Clock (OSCI)
    - 12.2.2. Frame Sync (FSYNC) Output
    - 12.2.3. Frame Sync (FSYNC) Input
    - 12.2.4. System reset signal (XCLR)
  - 12.3. Current Consumption



12.2.4. System reset signal (XCLR)

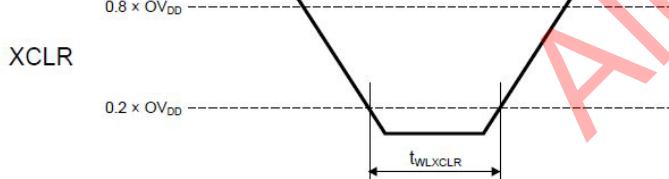


Table 12-5 XCLR Output Specifications

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XCLR Low level pulse width	$t_{WLXCLR}$	100(T.B.D.)	—	—	μs	—

## Revision 0.1.1:

### Contents

1. Description
2. Features
3. Device Structure
4. Absolute Maximum Ratings
5. Recommended Operating Conditions
6. USE RESTRICTION NOTICE
7. Optical Center
8. Pixel Arrangement
9. Block Diagram
10. Pin Configuration
11. Pin Description
12. Electrical Characteristics
  - 12.1. DC Characteristics
  - 12.2. AC Characteristics
    - 12.2.1. Master Clock (OSCI)
    - 12.2.2. Frame Sync (FSYNC) Output
    - 12.2.3. Frame Sync (FSYNC) Input
    - 12.2.4. Serial Communication (I<sup>2</sup>C)
    - 12.2.5. MIPI Output
    - 12.2.6. Serial-NOR-Flash I/F
    - 12.2.7. System reset signal (XCLR)
  - 12.3. Current Consumption

#### 12.2.4. Serial Communication (I<sup>2</sup>C)

Refer to the following I<sup>2</sup>C Standard:  
• UM10204 I<sup>2</sup>C-bus Specification, Version 6.0, 4th of April 2014

#### 12.2.5. MIPI Output

Refer to the following MIPI Standard:  
• MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.2  
• MIPI Alliance Specification for D-PHY Version 1.2

#### 12.2.6. Serial-NOR-Flash I/F

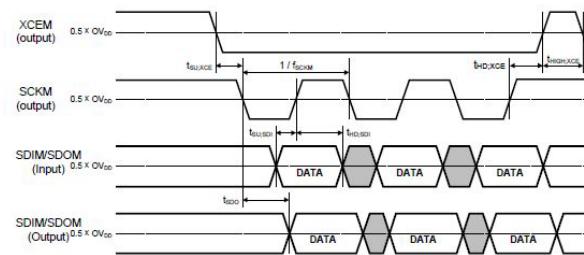


Table 12-5 Serial-NOR-Flash I/F Input / Output Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCKM clock frequency	$f_{SCKM}$	—	—	63.78(T.B.D.)	MHz	60.75 MHz + 5%
SCKM Duty ratio	Duty ratio	45(T.B.D.)	50(T.B.D.)	55(T.B.D.)	%	—
XCEM High time	$t_{HIGH,XCE}$	20(T.B.D.)	—	—	ns	—
XCEM setup time	$t_{SUS,XCE}$	10(T.B.D.)	—	—	ns	—
XCEM hold time	$t_{HOLD,XCE}$	10(T.B.D.)	—	—	ns	—
SDIM / SDOM setup time	$t_{SUS,SDI}$	0(T.B.D.)	—	—	ns	—
SDIM hold time	$t_{HOLD,SDI}$	10(T.B.D.)	—	—	ns	—
SDIM / SDOM output delay	$t_{SDI}$	-2(T.B.D.)	—	2(T.B.D.)	ns	(Maximum capacitance: 15 pF)

SC

# Errata 4-5. Update the Spot Pixel Specifications

## Revision 0.1.0:

Table 20-1 Spot Pixel Specification (Sub-pixel1) (T.B.D.)

(AV<sub>DD</sub> = 3.3V, OV<sub>DD</sub> = 1.8V, DV<sub>DD</sub> = 1.1V, T<sub>j</sub>=85°C, A/D 12-bit, Gain 0dB)

Type of spot pixels		Level of spot pixels		Maximum spot pixels in each zone		Measurement method
		Active pixel area	Effective OB			
Black or white pixels at high light	SP1L	30 % $\leq$ D		*1	No evaluation criteria applied	1
White pixels in the dark (Exposure time: 1/30 s)	SP1L	31.7 mV $\leq$ D		*2		3
Black pixels at signal saturated	SP1H	D $\leq$ 126 mV		*3	No evaluation criteria applied	4
	SP1L	D $\leq$ 480 mV				

Sum of \*1, \*2 and \*3 is less than equal to 1000 pixels.

Table 20-2 Spot Pixel Specification (Sub-pixel2) (T.B.D.)

(AV<sub>DD</sub> = 3.3V, OV<sub>DD</sub> = 1.8V, DV<sub>DD</sub> = 1.1V, T<sub>j</sub>=85°C, A/D 12-bit, Gain 0dB)

Type of spot pixels		Level of spot pixels		Maximum spot pixels in each zone		Measurement method
		Active pixel area	Effective OB			
Black or white pixels at high light	SP2L	30 % $\leq$ D		*4	No evaluation criteria applied	2
White pixels in the dark (Exposure time: 1/30 s)	SP2H	5.6 mV $\leq$ D		*5		3
	SP2L	180 mV $\leq$ D				
Black pixels at signal saturated	SP2H	D $\leq$ 26 mV		*6	No evaluation criteria applied	5
	SP2L	D $\leq$ 886 mV				

Sum of \*4, \*5 and \*6 is less than equal to 1000 pixels.

## Revision 0.1.1:

Table 20-1 Spot Pixel Specification (Sub-pixel1) (T.B.D.)

(AV<sub>DD</sub> = 3.3V, OV<sub>DD</sub> = 1.8V, DV<sub>DD</sub> = 1.1V, T<sub>j</sub>=85°C, A/D 12-bit, Gain 0dB)

Type of spot pixels		Level of spot pixels		Maximum spot pixels in each zone		Measurement method
		Active pixel area	Effective OB			
Black or white pixels at high light	SP1L	30 % $\leq$ D		*1	No evaluation criteria applied	1
White pixels in the dark (Exposure time: 1/30 s)	SP1L	31.7 mV $\leq$ D		*2		3
Black pixels at signal saturated	SP1H	D $\leq$ 126 mV		*3	No evaluation criteria applied	4
	SP1L	D $\leq$ 480 mV				

Sum of \*1, \*2 and \*3 is less than equal to 500 pixels. (T.B.D.)

Table 20-2 Spot Pixel Specification (Sub-pixel2) (T.B.D.)

(AV<sub>DD</sub> = 3.3V, OV<sub>DD</sub> = 1.8V, DV<sub>DD</sub> = 1.1V, T<sub>j</sub>=85°C, A/D 12-bit, Gain 0dB)

Type of spot pixels		Level of spot pixels		Maximum spot pixels in each zone		Measurement method
		Active pixel area	Effective OB			
Black or white pixels at high light	SP2L	30 % $\leq$ D		*4	No evaluation criteria applied	2
White pixels in the dark (Exposure time: 1/30 s)	SP2H	5.6 mV $\leq$ D		*5		3
	SP2L	180 mV $\leq$ D				
Black pixels at signal saturated	SP2H	D $\leq$ 26 mV		*6	No evaluation criteria applied	5
	SP2L	D $\leq$ 886 mV				

Sum of \*4, \*5 and \*6 is less than equal to 500 pixels. (T.B.D.)

# Errata 5-1. Update the Fig.7-1 Optical Center(Top View)

## Revision 0.1.1:

### 7. Optical Center

- Package center
- Optical center
- Package reference (H, V)

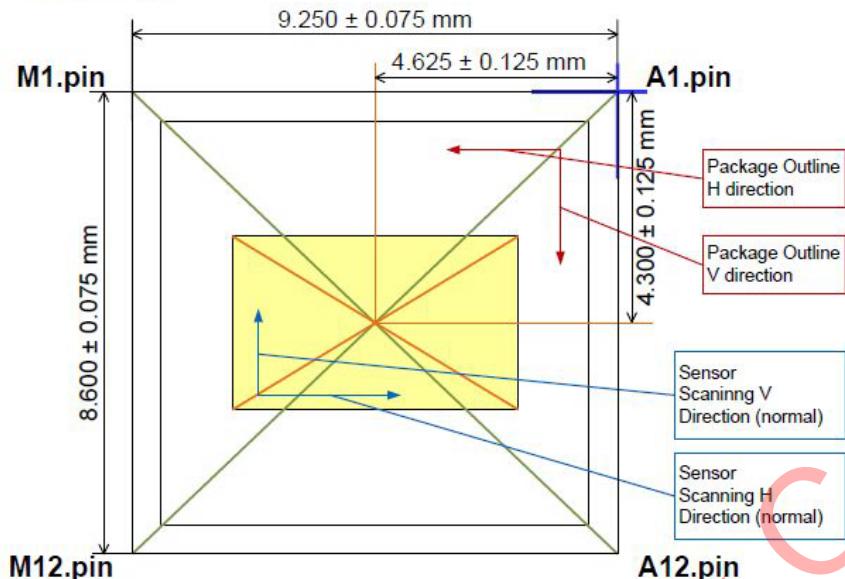


Fig. 7-1 Optical Center (Top View) \*1

\*1 The optical center above is position when the Optical Center Adjustment is default setting. (Shift amount of H and V are 0.)

## Revision 0.1.2:

### 7. Optical Center

- Package center
- Optical center
- Package reference (H, V)

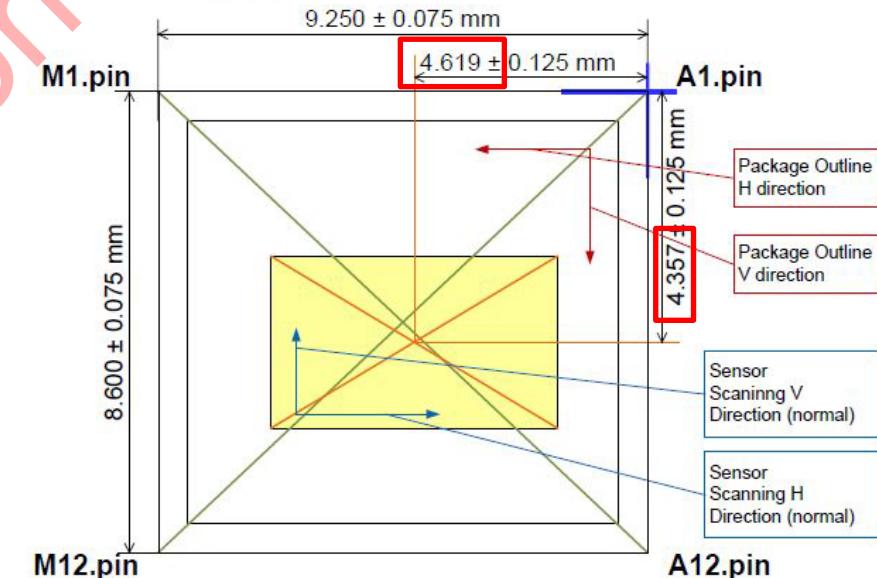


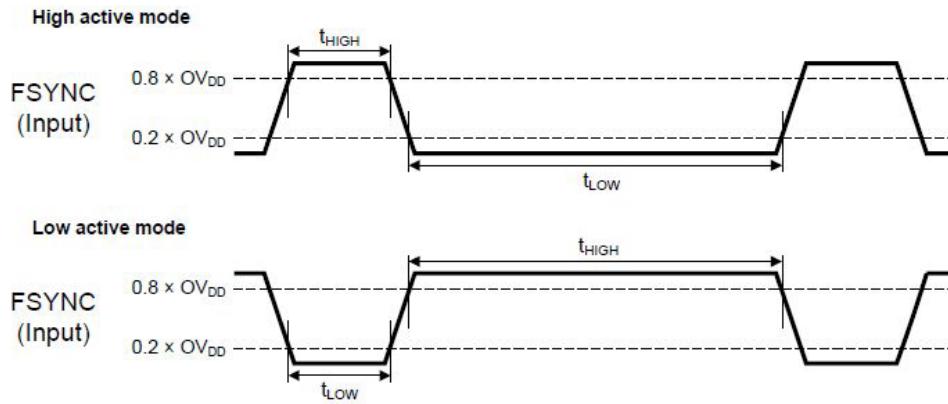
Fig. 7-1 Optical Center (Top View) \*1

\*1 The optical center above is position when the Optical Center Adjustment is default setting. (Shift amount of H and V are 0.)

# Errata 5-2. Frame Sync (FSYNC) Input

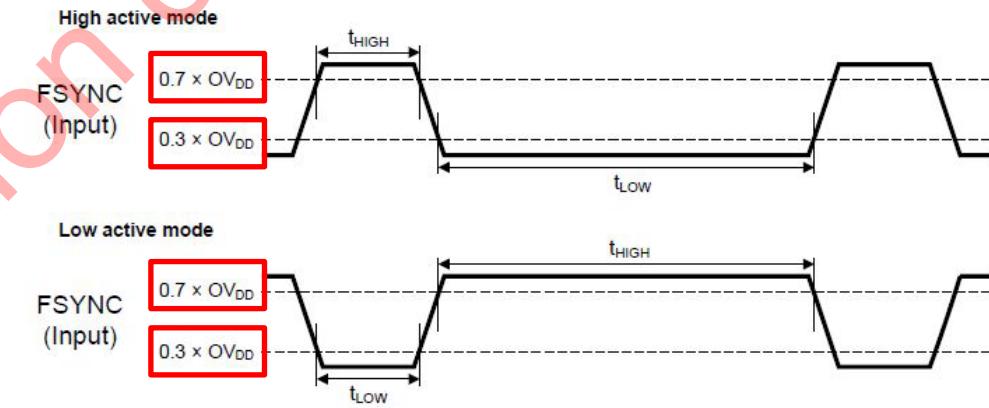
## Revision 0.1.1:

### 12.2.3. Frame Sync (FSYNC) Input



## Revision 0.1.2:

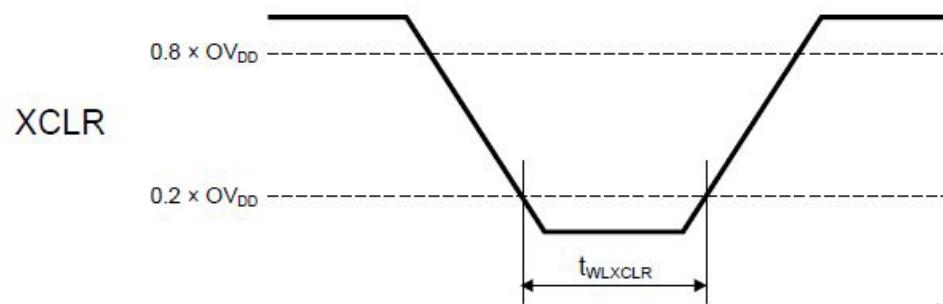
### 12.2.3. Frame Sync (FSYNC) Input



# Errata 5-3. System reset signal (XCLR)

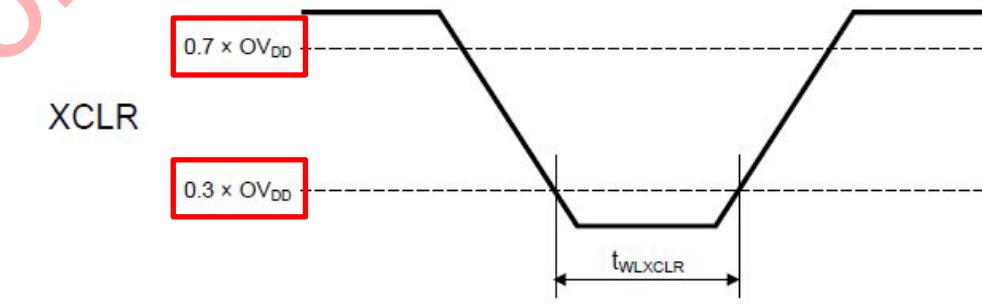
Revision 0.1.1:

12.2.7. System reset signal (XCLR)



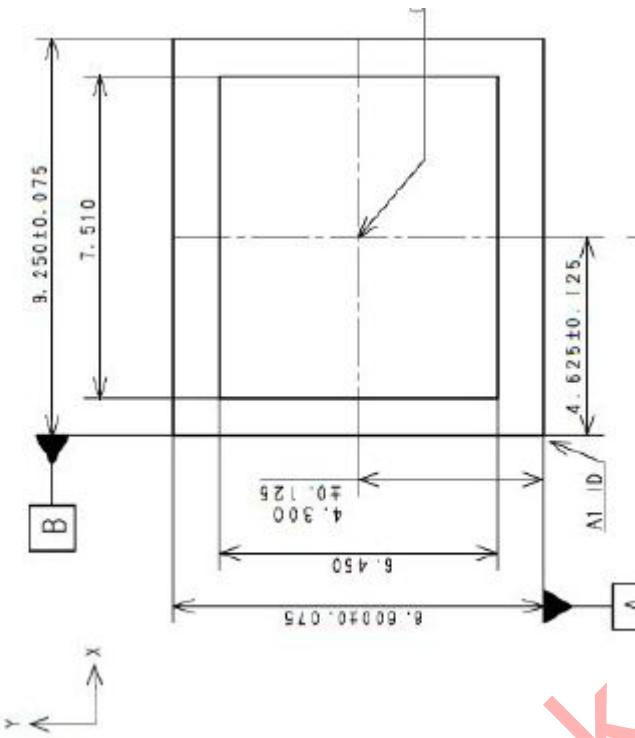
Revision 0.1.2:

12.2.7. System reset signal (XCLR)



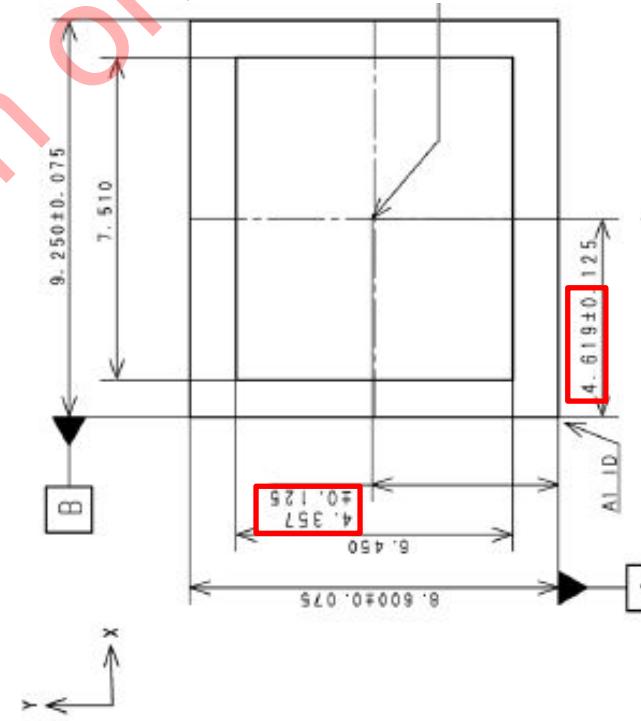
# Errata 5-4. Update the Package Outline

Revision 0.1.1:



INTATIVE

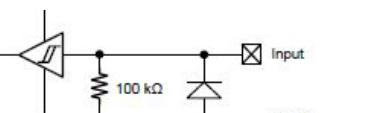
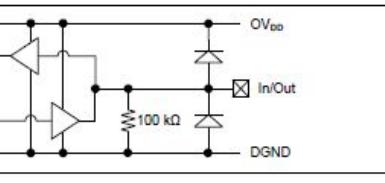
Revision 0.1.2:



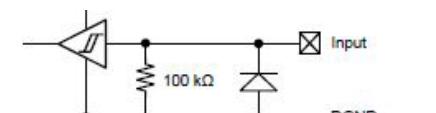
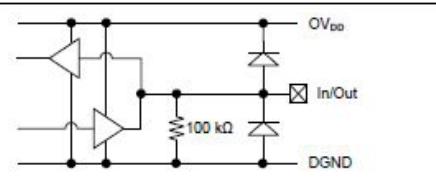
INTATIVE

# Errata 6-1. Updated the Table 11-2 Equivalent Circuit

Revision 0.1.2:

XCLR	Schmitt	—	1.8 V	
SDIM SDOM FSYNC	Pull-down	1.0 mA 2.0 mA 4.0 mA	1.8 V	

Revision 22505:

XCLR	Schmitt	—	1.8 V	
INCKSEL0 INCKSEL1 SDIM SDOM FSYNC	Pull-down	1.0 mA 2.0 mA 4.0 mA	1.8 V	

Altek Corporation only

# Errata 6-2. Updated the AC Characteristics

## Revision 0.1.2:

Table 12-2 Input Clock Specifications

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
OSCI clock frequency <sup>1)</sup>	fosc <sub>i</sub>	fosc <sub>i</sub> ×0.98(T.B.D.)	fosc <sub>i</sub>	fosc <sub>i</sub> ×1.02(T.B.D.)	MHz	fosc <sub>i</sub> = 18 to 30 MHz
OSCI low level pulse width	t <sub>W</sub> OSCI	10(T.B.D.)	—	—	ns	fosc <sub>i</sub> = 18 to 30 MHz
OSCI high level pulse width	t <sub>W</sub> OSCI	10(T.B.D.)	—	—	ns	fosc <sub>i</sub> = 18 to 30 MHz
OSCI clock duty	Duty ratio	40	50	60	%	Define with 0.5 × OV <sub>DD</sub>
OSCI rise time	t <sub>r</sub> _osc <sub>i</sub>	—	—	5(T.B.D.)	ns	30% to 70%
OSCI fall time	t <sub>f</sub> _osc <sub>i</sub>	—	—	5(T.B.D.)	ns	70% to 30%

\*1 Recommended frequencies of OSCI clock are 18/24/30MHz.

\*1 Any deviations in OSCI fluctuation affect the frame rate.

Table 12-5 Serial-NOR-Flash I/F Input / Output Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCKM clock frequency	f <sub>SCKM</sub>	—	—	63.78(T.B.D.)	MHz	60.75 MHz + 5%
SCKM Duty ratio	Duty ratio	45(T.B.D.)	50(T.B.D.)	55(T.B.D.)	%	—
XCEM High time	t <sub>HIGH</sub> XCE	20(T.B.D.)	—	—	ns	—
XCEM setup time	t <sub>SU</sub> XCE	10(T.B.D.)	—	—	ns	—
XCEM hold time	t <sub>HD</sub> XCE	10(T.B.D.)	—	—	ns	—
SDIM / SDOM setup time	t <sub>SU</sub> :SDI	0(T.B.D.)	—	—	ns	—
SDIM hold time	t <sub>HD</sub> :SDI	10(T.B.D.)	—	—	ns	—
SDIM / SDOM output delay	t <sub>SDO</sub>	-2(T.B.D.)	—	2(T.B.D.)	ns	—

(Maximum capacitance: 15 pF)

## Revision 22505:

Table 12-2 Input Clock Specifications

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
OSCI clock frequency <sup>1)</sup>	fosc <sub>i</sub>	fosc <sub>i</sub> ×0.98	fosc <sub>i</sub>	fosc <sub>i</sub> ×1.02	MHz	fosc <sub>i</sub> = 18 to 30 MHz
OSCI low level pulse width	t <sub>W</sub> OSCI	8	—	—	ns	fosc <sub>i</sub> = 18 to 30 MHz
OSCI high level pulse width	t <sub>W</sub> OSCI	8	—	—	ns	fosc <sub>i</sub> = 18 to 30 MHz
OSCI clock duty	Duty ratio	40	50	60	%	Define with 0.5 × OV <sub>DD</sub>
OSCI rise time	t <sub>r</sub> _osc <sub>i</sub>	—	—	5	ns	30% to 70%
OSCI fall time	t <sub>f</sub> _osc <sub>i</sub>	—	—	5	ns	70% to 30%
OSCI jitter	—	—	—	600	ps	cycle to cycle jitter

\*1 Recommended frequencies of OSCI clock are 18/24/30MHz.

\*1 Any deviations in OSCI fluctuation affect the frame rate.

Table 12-5 Serial-NOR-Flash I/F Input / Output Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCKM clock frequency	f <sub>SCKM</sub>	—	—	62.4	MHz	60 MHz + 4.04%
SCKM Duty ratio	Duty ratio	45	50	55	%	—
XCEM High time	t <sub>HIGH</sub> XCE	20	—	—	ns	—
XCEM setup time	t <sub>SU</sub> XCE	10	—	—	ns	—
XCEM hold time	t <sub>HD</sub> XCE	10	—	—	ns	—
SDIM / SDOM setup time	t <sub>SU</sub> :SDI	0	—	—	ns	—
SDIM hold time	t <sub>HD</sub> :SDI	8	—	—	ns	—
SDIM / SDOM output delay	t <sub>SDO</sub>	-1.8	—	4.8	ns	—

(Maximum capacitance: 15 pF)

# Errata 6-3. Updated Table 12-7 Current Consumption

## Revision 0.1.2:

Table 12-7 Current Consumption

Item	Pins	Symbol	Typ.	Max.	Unit
Operating current *1 All-pixel scan 3Mpixels (1920 × 1536) 10-bit 60 frames/s MIPI 4-lane PWL20 / HDR combined	VDDHPX				
	VDDHAN				
	VDDHCP				
	VDDHCM				
	VDDMIO	IOV <sub>DD</sub>	9(T.B.D.)	11(T.B.D.)	mA
	VDDLSC				
	VDDLCN				
	VDDLVS				
	VDDLPLVT1				
	VDDLPLVT2				
Operating current *1 All-pixel scan 3Mpixels (1920 × 1536) 12-bit 30 frames/s MIPI 4-lane PWL20 / HDR combined	VDDLPLOP				
	VDDHPX				
	VDDHAN				
	VDDHCP				
	VDDHCM				
	VDDMIO	IOV <sub>DD</sub>	8(T.B.D.)	9(T.B.D.)	mA
	VDDLSC				
	VDDLCN				
	VDDLVS				
	VDDLPLVT1				
	VDDLPLVT2				
	VDDLPLOP				

\*1 Operating current: (Typ.) Supply voltage 3.3 V / 1.8 V / 1.1 V, T<sub>j</sub> = 25 °C  
The light condition: luminous intensity when the sensor outputs 1/3 of the maximum output.  
(Max.) Supply voltage 3.465 V / 1.9 V / 1.2 V, T<sub>j</sub> = 125 °C  
The worst condition of the internal circuit operating current consumption.

## Revision 22505:

Table 12-7 Current Consumption

Item	Pins	Symbol	Typ.	Max.	Unit
Operating current *1 All-pixel scan 3Mpixels (1920 × 1536) 10-bit 60 frames/s MIPI 4-lane PWL20 / HDR combined	VDDHPX				
	VDDHAN				
	VDDHCP				
	VDDHCM				
	VDDMIO	IOV <sub>DD</sub>	3	4	mA
	VDDLSC				
	VDDLCN				
	VDDLVS				
	VDDLPLVT1				
	VDDLPLVT2				
Operating current *1 All-pixel scan 3Mpixels (1920 × 1536) 12-bit 30 frames/s MIPI 4-lane PWL20 / HDR combined	VDDLPLOP				
	VDDHPX				
	VDDHAN				
	VDDHCP				
	VDDHCM				
	VDDMIO	IOV <sub>DD</sub>	3	4	mA
	VDDLSC				
	VDDLCN				
	VDDLVS				
	VDDLPLVT1				
	VDDLPLVT2				
	VDDLPLOP				

\*1 Operating current: (Typ.) Supply voltage 3.3 V / 1.8 V / 1.1 V, T<sub>j</sub> = 25 °C  
(Max.) Supply voltage 3.465 V / 1.9 V / 1.2 V, T<sub>j</sub> = 125 °C

# Errata 6-4. Updated Fig. 13-1 Spectral Sensitivity Characteristics

Revision 0.1.2:

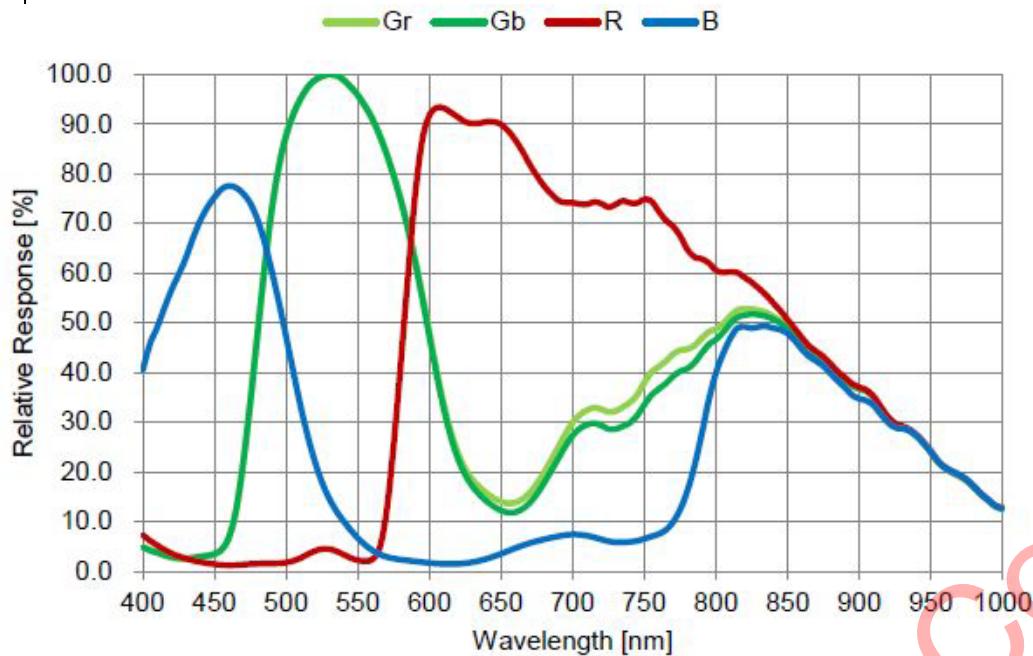


Fig. 13-1 Spectral Sensitivity Characteristics (T.B.D.)

Revision 22505:

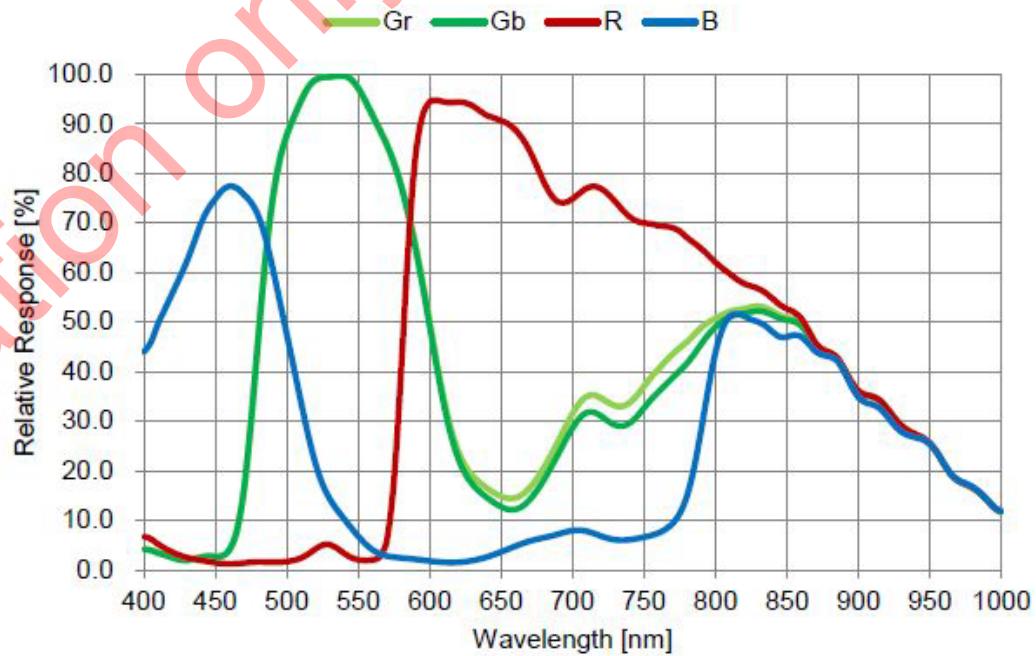


Fig. 13-1 Spectral Sensitivity Characteristics

# Errata 6-5. Updated Image Sensor Characteristics

## Revision 0.1.2:

### 14. Image Sensor Characteristics

Table 14-1 List of Image Sensor Characteristics (T.B.D.)

(AV<sub>DD</sub> = 3.3 V, OV<sub>DD</sub> = 1.8 V, DV<sub>DD</sub> = 1.1 V, T<sub>J</sub> = 85°C, A/D: 12 bit output, Gain: 0 dB)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity	Sg	8251 (1711)	10933 (2267)	—	LSB (mV)	1	Exposure time: 1/30 s Sub-pixel1 HCG mode
		2450 (508)	3062 (635)	—			Exposure time: 1/30 s Sub-pixel1 LCG mode
		14 (3)	29 (6)	—			Exposure time: 1/30 s Sub-pixel2 High
Sub-pixel Sensitivity ratio (Green)	GSP1H / GSP1L	RsHL	—	3.57	—	2	Sub-pixel1 HCG mode / Sub-pixel1 LCG mode
	GSP1L / GSP2H	RsL2	—	118	—		Sub-pixel1 LCG mode / Sub-pixel2 High
Color Sensitivity ratio	R <sub>SPI1</sub> / G <sub>SPI1</sub>	RG	0.46	—	0.59	—	Sub-pixel1 LCG mode
	B <sub>SPI1</sub> / G <sub>SPI1</sub>	BG	0.31	—	0.47		
Saturation signal	Vsat	2566 (532)	—	—	LSB (mV)	4	Sub-pixel1 LCG mode
		2375 (985)	—	—			Sub-pixel2 Low

1. 1 LSB (Least Significant Bit) = T.B.D. mV (A/D: 12-bit) / T.B.D. mV (A/D: 10-bit)

2. The characteristics above apply to "physical active pixel area."

## Revision 22505:

### 14. Image Sensor Characteristics

Table 14-1 List of Image Sensor Characteristics

(AV<sub>DD</sub> = 3.3 V, OV<sub>DD</sub> = 1.8 V, DV<sub>DD</sub> = 1.1 V, T<sub>J</sub> = 85°C, A/D: 12 bit output, Gain: 0 dB)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity	Sg	8224 (1711)	10897 (2267)	—	LSB (mV)	1	Exposure time: 1/30 s Sub-pixel1 HCG mode
		2442 (508)	3052 (635)	—			Exposure time: 1/30 s Sub-pixel1 LCG mode
		14 (3)	29 (6)	—			Exposure time: 1/30 s Sub-pixel2 High
Sub-pixel Sensitivity ratio (Green)	GSP1H / GSP1L	RsHL	—	3.57	—	—	Sub-pixel1 HCG mode / Sub-pixel1 LCG mode
	GSP1L / GSP2H	RsL2	—	118	—		Sub-pixel1 LCG mode / Sub-pixel2 High
Color Sensitivity ratio	R <sub>SPI1</sub> / G <sub>SPI1</sub>	RG	0.46	—	0.59	—	Sub-pixel1 LCG mode
	B <sub>SPI1</sub> / G <sub>SPI1</sub>	BG	0.31	—	0.47		
Saturation signal	Vsat	2557 (532)	—	—	LSB (mV)	4	Sub-pixel1 LCG mode
		2367 (985)	—	—			Sub-pixel2 Low

1. 1 LSB Sub-pixel1 HCG mode (SP1H), Sub-pixel1 LCG mode (SP1L), Sub-pixel2 High (SP2H):  
208.04 µV (A/D 12-bit), 832.77 µV (A/D 10-bit)

1 LSB Sub-pixel2 Low (SP2L):  
416.08 µV (A/D 12-bit), 1665.54 µV (A/D 10-bit)

2. The characteristics above apply to "physical active pixel area."

# Errata 6-6. Updated Table 17-2 List of Output Mode (MIPI CSI-2 4-lane)

## Revision 0.1.2:

Table 17-2 List of Output Mode (MIPI CSI-2 4-lane)

Output Mode	HDR Combine	Frame Rate [frames/s] <sup>*1</sup>	AD bit	Output Format	Valid Size		Total Size		Data rate [Mbps/lane]
					H [pixels]	V [lines]	H [pixels]	V [lines]	
Normal Output	Uncombined	60	10	RAW12	2214	1626	648		
			12		2400	1750	378		
			10		2214	1626	756		
			12	RAW14	2400	1750	441		
			10		2214	1626	864		
			12		2200	1750	462		
		30	10	RAW16	2214	1626	1080		
			12		2400	1750	630		
			10		2214	1626	1296		
			12	RAW20	2200	1750	693		
			10		2214	1626	1296		
			12		2200	1750	693		
HDR Combined Output	Combined	60	10	RAW12	2214	1626	648		
			12		2400	1750	378		
			10		2214	1626	756		
			12	RAW14	2400	1750	441		
			10		2214	1626	864		
			12		2200	1750	462		
		30	10	RAW16	2214	1626	1080		
			12		2400	1750	630		
			10		2214	1626	1296		
			12	RAW20	2200	1750	693		
			10		2214	1626	1296		
			12		2200	1750	693		
HDR Uncombined Output (Line / Line)	Uncombined	60	10	RAW12x2	2460	3252	1440		
			12		2200	3500	693		
		30	12		6224	2270	7000	1430.1	
		30	12	RAW12x4					

## Revision 22505:

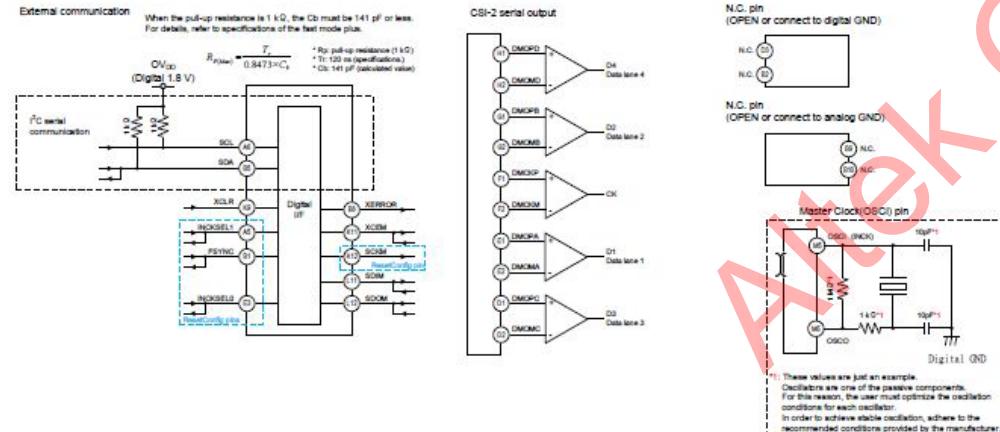
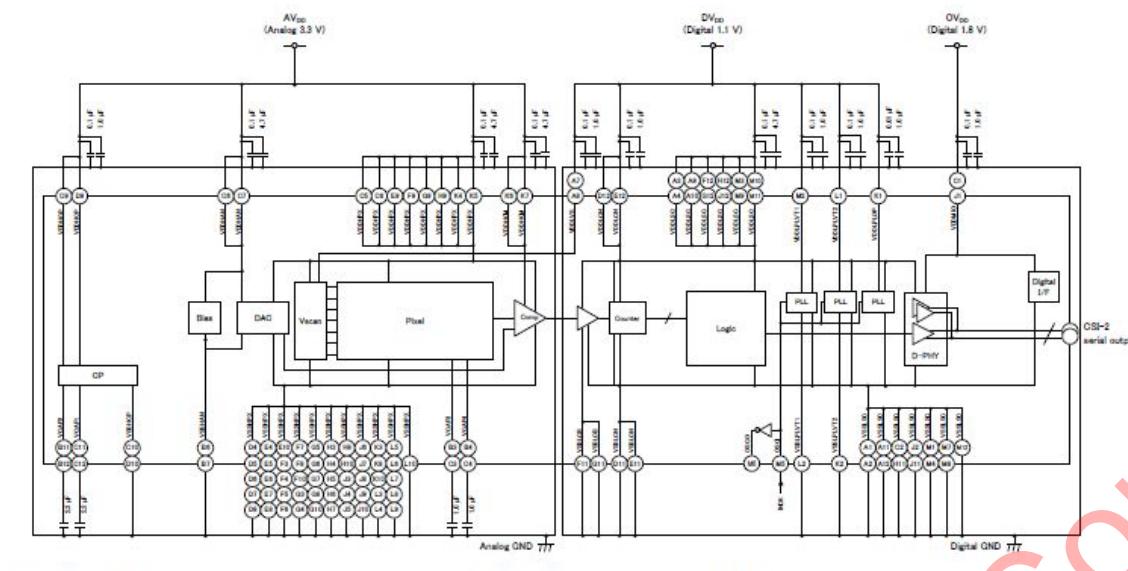
Table 17-2 List of Output Mode (MIPI CSI-2 4-lane)

Output Mode	HDR Combine	Frame Rate [frames/s] <sup>*1</sup>	AD bit	Output Format	Valid Size		Total Size		Data rate [Mbps/lane]
					H [pixels]	V [lines]	H [pixels]	V [lines]	
Normal Output	Uncombined	60	10	RAW12	2214	1626	648		
			12		2400	1750	378		
			10		2214	1626	756		
			12	RAW14	2400	1750	441		
			10		2214	1626	864		
			12		2200	1750	462		
		30	10	RAW16	2214	1626	1080		
			12		2400	1750	630		
			10		2214	1626	1296		
			12	RAW20	2200	1750	693		
			10		2214	1626	1296		
			12		2200	1750	693		
HDR Combined Output	Combined	30	10	RAW12	2214	1626	648		
			12		2400	1750	378		
			10		2214	1626	756		
			12	RAW14	2400	1750	441		
			10		2214	1626	864		
			12		2200	1750	462		
HDR Uncombined Output (Line / Line)	Uncombined	60	10	RAW16	2214	1626	1080		
			12		2400	1750	630		
			10		2214	1626	1296		
		30	10	RAW20	2200	1750	693		
			12		2214	1626	1296		
			10		2200	1750	693		
HDR Uncombined Output (Line / Line)	Uncombined	60	10	RAW12x2	2460	3252	1440		
			12		2200	3500	693		
		30	12	RAW12x4	6224	2270	7000	1470	

# Errata 6-7. Updated Example of Peripheral Circuit

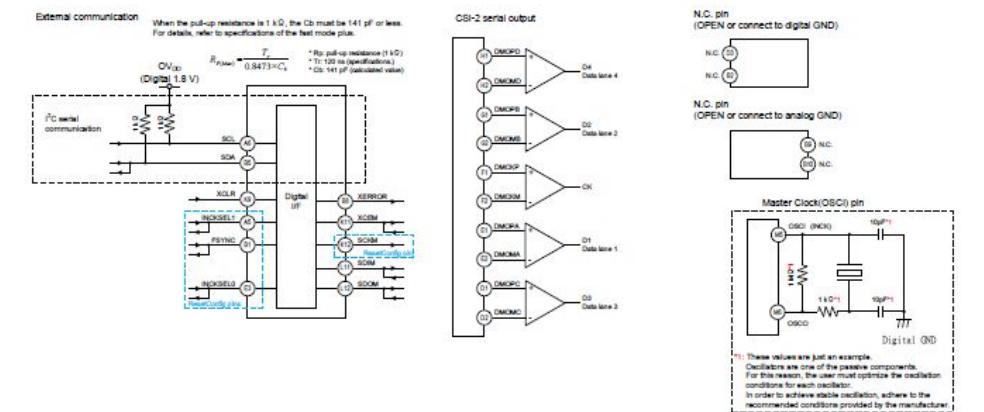
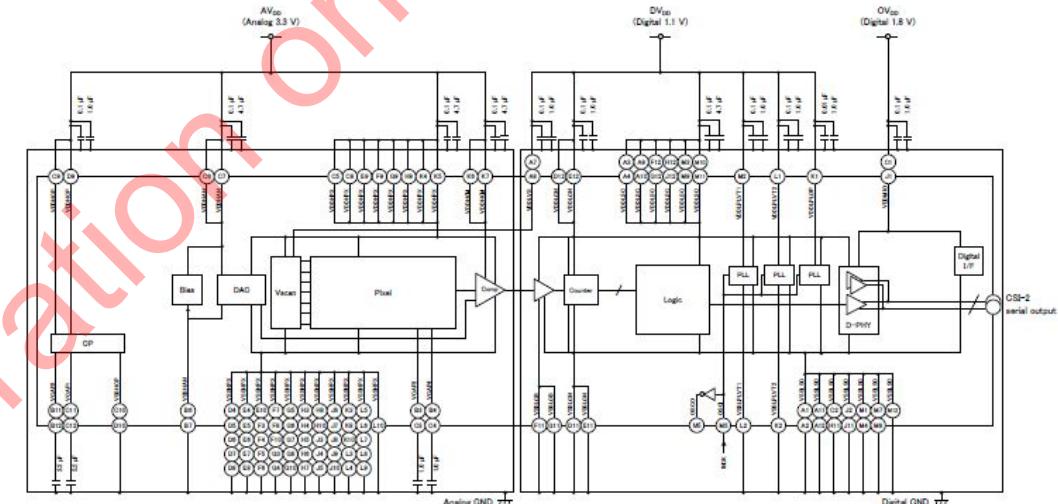
## Revision 0.1.2:

### 18. Example of Peripheral Circuit



## Revision 22505:

### 18. Example of Peripheral Circuit



\* For the design guideline of the printed circuit board layout and mount, please refer to the support package.

Application circuits shown are typical examples illustrating the operation of the devices.  
Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of  
these circuits or for any infringement of third party and other right due to same.

# Errata 6-8. Updated Table 20-2 Spot Pixel Specification (Sub-pixel2)

Revision 0.1.2:

Revision 22505:

Table 20-2 Spot Pixel Specification (Sub-pixel2) (T.B.D.)

(AV<sub>DD</sub> = 3.3V, OV<sub>DD</sub> = 1.8V, DV<sub>DD</sub> = 1.1V, Tj=85°C, A/D 12-bit, Gain 0dB)

Type of spot pixels		Level of spot pixels		Maximum spot pixels in each zone		Measurement method
				Active pixel area	Effective OB	
Black or white pixels at high light	SP2L	30 %	≤ D	*4	No evaluation criteria applied	2
White pixels in the dark (Exposure time: 1/30 s)	SP2H	5.6 mV	≤ D	*5	3	
	SP2L	180 mV	≤ D			
Black pixels at signal saturated	SP2H	D	≤ 26 mV	*6	No evaluation criteria applied	5
	SP2L	D	≤ 886 mV			

Sum of \*4, \*5 and \*6 is less than equal to 500 pixels. (T.B.D.)

Table 20-2 Spot Pixel Specification (Sub-pixel2)

(AV<sub>DD</sub> = 3.3V, OV<sub>DD</sub> = 1.8V, DV<sub>DD</sub> = 1.1V, Tj=85°C, A/D 12-bit, Gain 0dB)

Type of spot pixels		Level of spot pixels		Maximum spot pixels in each zone		Measurement method
				Active pixel area	Effective OB	
Black or white pixels at high light	SP2L	30 %	≤ D	*4	No evaluation criteria applied	2
White pixels in the dark (Exposure time: 1/30 s)	SP2H	5.6 mV	≤ D	*5	3	
	SP2L	180 mV	≤ D			
Black pixels at signal saturated	SP2H	D	≤ 36 mV	*6	No evaluation criteria applied	5
	SP2L	D	≤ 886 mV			

Sum of \*4, \*5 and \*6 is less than equal to 500 pixels.

# Errata 6-9. Updated Notice on White Pixels Specifications

Revision 0.1.2:

Revision 22505:

Example of Annual Number of Occurrence

White Pixel Level (in the case of integration time = 1/30 s) (T <sub>j</sub> = 60 °C)	Annual number of occurrence	
	Sub-pixel1 LCG mode	Sub-pixel2 High
5.6 mV or higher	5.0 (T.B.D.) pcs	0.8 (T.B.D.) pcs
10.0 mV or higher	3.0 (T.B.D.) pcs	0.1 (T.B.D.) pcs
24.0 mV or higher	0.8 (T.B.D.) pcs	0.1 (T.B.D.) pcs
50.0 mV or higher	0.5 (T.B.D.) pcs	0.0 (T.B.D.) pcs
72.0 mV or higher	0.4 (T.B.D.) pcs	0.0 (T.B.D.) pcs

Example of Annual Number of Occurrence

White Pixel Level (in the case of integration time = 1/30 s) (T <sub>j</sub> = 60 °C)	Annual number of occurrence	
	Sub-pixel1 LCG mode	Sub-pixel2 High
5.6 mV or higher	2.8 pcs	0.5 pcs
10.0 mV or higher	1.7 pcs	0.1 pcs
24.0 mV or higher	0.5 pcs	0.1 pcs
50.0 mV or higher	0.3 pcs	0.0 pcs
72.0 mV or higher	0.3 pcs	0.0 pcs

# Errata 6-10. Updated Marking

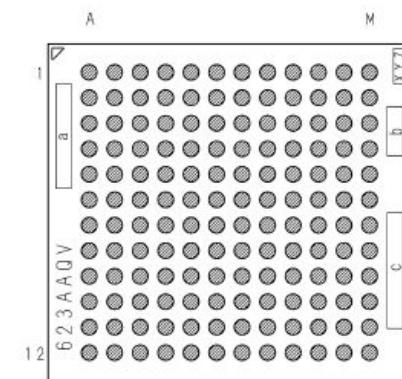
## Revision 0.1.2:

### 22. Marking

T.B.D.

## Revision 22505:

### 22. Marking



a : Lot No. (Max7)



Control No.

Week manufactured

Year manufactured

b : Substrate serial No. (Max. 3)

c : Internal Assy Lot No. (Max. 8)

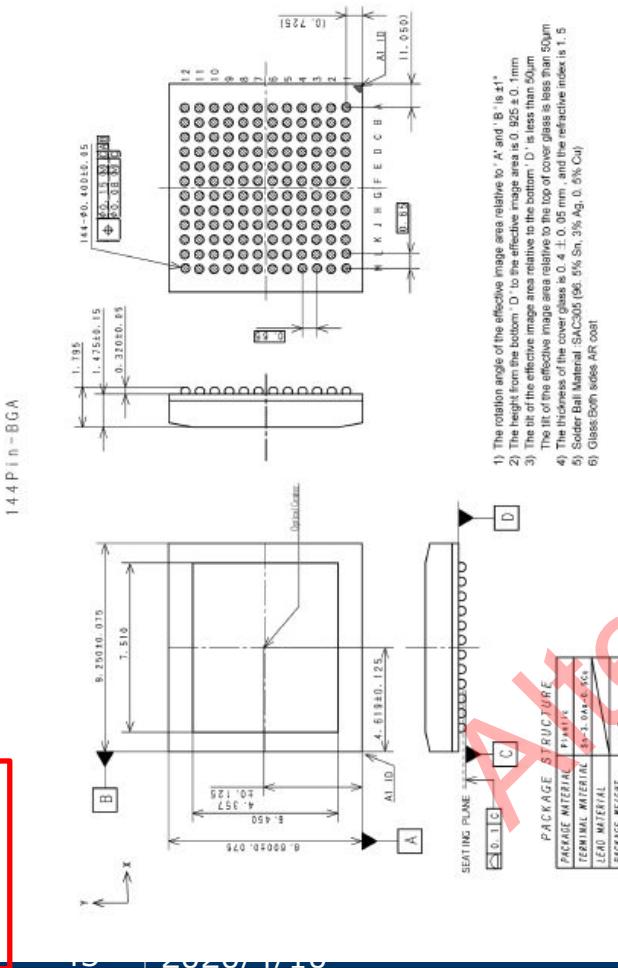
Note : Numbers enter into X to Z (Plating)

# **Errata 6-11. Updated Package Outline**

## **Revision 0.1.2:**

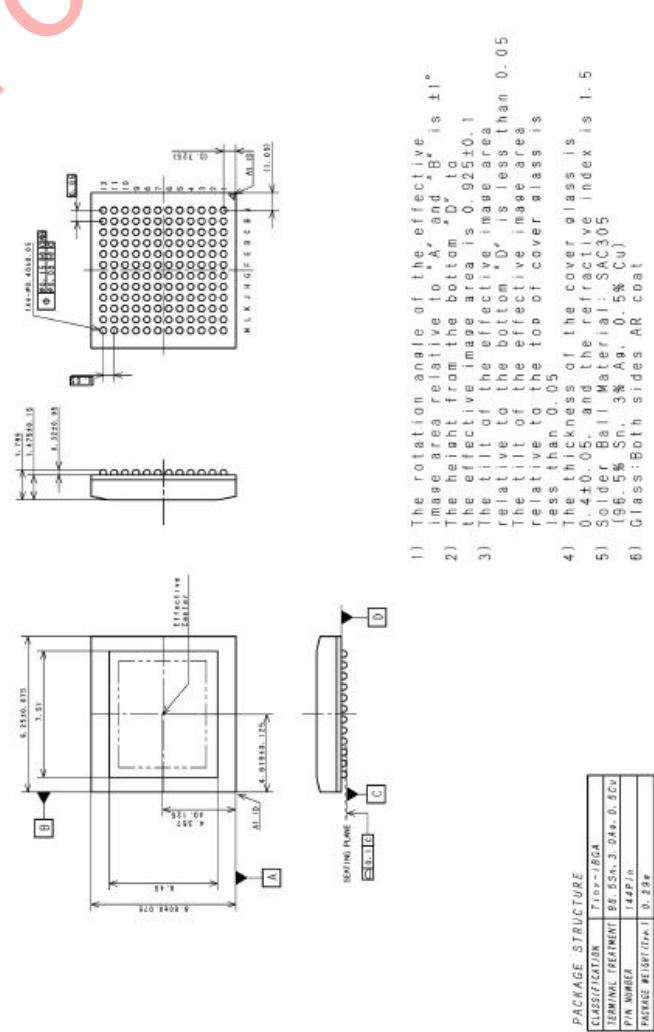
## 24. Package Outline

(Unit: mm)



Revision 22505:

## 24. Package Outline



- 1) The rotation angle of the effective image area relative to  $A_x$  and  $B_y$  is 1°.
- 2) The height from the bottom  $D_y$  to the effective image area is 0.925 mm. The tilt of the effective image area is 0.1°.
- 3) The tilt of the effective image area relative to the bottom  $D_y$  is less than 0.05°. The tilt of the effective image area relative to the top of cover glass is less than 0.05°.
- 4) The thickness of the cover glass is 0.4±0.05, and the refractive index is 1.5.
- 5) Solder Ball Material: SAC305 (96% Sn, 3% Ag, 0.5% Cu).
- 6) Glass/Both sides AR coat

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