

IMX623-AAQV Application Note

CMOS Image Sensor

Altek Corporation Only

Sony Semiconductor Solutions Corporation

Revision History

Date	Revision	Remarks
April 19, 2021	0.1.0	Tentative Edition Official Release <ul style="list-style-type: none">• “1.2 The Sensor’s Signal Process Flow”<ul style="list-style-type: none">- Added the signal process flow in “Figure 1-2.”• “2.1.5 Reset Configuration”<ul style="list-style-type: none">- Updated the method for setting the sensor’s slave address.• “2.1.5.1 Setting the Master Clock Frequency”<ul style="list-style-type: none">- Updated the INCK frequency process flow.• “2.2.2 Regional Allocation of Serial NOR Flash Device”<ul style="list-style-type: none">- Added the descriptions of the capacity of the Serial NOR Flash device.• “2.2.3 Pin Assignment When No Serial NOR Flash Device Is Used”<ul style="list-style-type: none">- Changed the recommended pin assignment of the SDIM pin.• “2.2.4 The State of the Serial NOR Flash Device”<ul style="list-style-type: none">- Added the descriptions of how to confirm the state of the Serial NOR Flash device connected to the sensor.• “2.4.1 MIPI CSI-2 Pins and Supported Specifications”<ul style="list-style-type: none">- Added the descriptions of the maximum bit rate for each lane.• “3.1.1 Register Categories”<ul style="list-style-type: none">- Added the register category (SM_CONST).• “3.4.3 The Sensor’s Undefined Regions”<ul style="list-style-type: none">- Added the descriptions of the sensor’s undefined regions.• “3.5.2 Examples of Command and Subcommand Usage”<ul style="list-style-type: none">- Updated the descriptions.• “4.8 The Registers That Can Be Changed While the Sensor Is in Streaming State”<ul style="list-style-type: none">- Added the descriptions of the registers which can be changed while the sensor is in Streaming State.• “5.1.3.3 Compositing Gain”<ul style="list-style-type: none">- Updated the equation to calculate the compositing gain for SP2.• “5.2.3.2.3 Long Exposure”<ul style="list-style-type: none">- Added the descriptions of the conditions under which the sensor performs long exposure.• “5.2.3.4.6 Light Metering Region Mask Function”<ul style="list-style-type: none">- Added the descriptions of the IR_OP_OIF_AE_MSK_SEL register.• “5.2.3.5.5 Two-Tracking Speed Control”<ul style="list-style-type: none">- Added the descriptions of the two-tracking speed control for AE.• “5.2.3.6.1 Detecting Flickering”<ul style="list-style-type: none">- Added the descriptions of the automatic flicker detection and the detection sensitivity.• “5.2.3.6.2 Flickerless AE Function’s Operating Modes”<ul style="list-style-type: none">- Added the descriptions of the exposure time settings for Flickerless AE.• “5.2.3.7.2 Full ME”<ul style="list-style-type: none">- Added the descriptions of digital gains for non-HDR output.• “5.2.4 Conditions”<ul style="list-style-type: none">- Added the descriptions of the available range for the sensor’s exposure time settings.• “5.3.2 Functional Overview”<ul style="list-style-type: none">- Added the descriptions of the
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		<p>Aitek Corporation All rights reserved.</p> <ul style="list-style-type: none">• AWB_WBCLIP_SPS_OFT_ON register.• “5.3.3.1 Selecting a Method of Adjusting White Balance Gain”<ul style="list-style-type: none">- Added the description of the setting when the white balance gain is not applied.• “5.3.3.2.1 Configuring the Settings for Convergence Operations”<ul style="list-style-type: none">- Added the descriptions of the settings for the AWB convergence operations.• “5.3.3.2.2 Auto Tracking White Balance (ATW)”<ul style="list-style-type: none">- Added the description of switching of WB scenes.- Added the descriptions of the ATW_FRM_CHK_F register.- Added the descriptions of determination of an Operation Area error.- Added the descriptions of the convergence speed.• “5.3.3.5.2 Light Metering Region Mask Function”<ul style="list-style-type: none">- Added the descriptions of the IR_OP_OIF_AWB_MSK_SEL register.- Added the descriptions of the threshold for light metering.- Added the descriptions of determination of a light metering error.- Added the descriptions of the coefficient of the IIR filter.• “5.4 Clamp Function”<ul style="list-style-type: none">- Added the descriptions of the OB Area related to the Clamp function.- Added the descriptions of the processing of the Digital Clamp function.• “6.1.3.2.1 Setting a Data Output Timing Delay”<ul style="list-style-type: none">- Added the descriptions of the adjustment of the time when the sensor begins internal processing in external pulse-based sync.• “6.1.4 Conditions”<ul style="list-style-type: none">- Added the description of the restriction on External Pulse-Based Synchronization.• “6.3.3.1 Setting the Horizontal/Vertical Flip Function’s Control Registers”<ul style="list-style-type: none">- Added the descriptions of the settings for horizontal flipping.• “6.6.3.1.1 Setting interlocking source(s)”<ul style="list-style-type: none">- Added the interlocking source information.• “6.7 Context Switch Function”<ul style="list-style-type: none">- Changed the function name from the “Scene Select function” to the “Context Switch function.”• “6.7.3.1.2 Event Region”<ul style="list-style-type: none">- Added an example of setting the Event Region.• “6.9.3.5 Front Embedded Data”<ul style="list-style-type: none">- Added the descriptions of the time when the information is transmitted to the Front Embedded Data.- Added the descriptions of the OB information.• “6.9.3.5.4 Information Regarding Host-Selected Register(s)”<ul style="list-style-type: none">- Added the description of the registers, the information about which cannot be transmitted by the host.• “6.9.3.5.25 Clamp Information”<ul style="list-style-type: none">- Added the information about the black level’s offset value.• “6.9.3.6 Rear Embedded Data”<ul style="list-style-type: none">- Added the descriptions of the time when the information is transmitted to the Rear Embedded Data.• “6.9.3.6.6 Frame CRC Information”<ul style="list-style-type: none">- Added the detailed descriptions of the Frame CRC Information.• “6.10.3.2 The Method for Writing a Value to the OTP ROM”
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		<ul style="list-style-type: none">- Updated the OTP write procedure.• "7.2.3.2 Setting the Light Metering Window Overlay Function"<ul style="list-style-type: none">- Added the description of the display width setting of the light metering window.• "4.3.1 Power-on Sequence"• "5.9.3.2 Setting the Center of the Lens Shading Compensation Function"• "5.9.4 Conditions"• "6.9.3.5.9 Temperature Information"<ul style="list-style-type: none">- Deleted TBDs. <p>Corrected misprints, layouts, fonts and inconsistent spellings.</p>
January 28, 2022	1.0.1	<p>Official Release</p> <ul style="list-style-type: none">• "1.2 The Sensor's Signal Process Flow"<ul style="list-style-type: none">- Added the description of the Output Mask function.• "2.1.5.1 Setting the Master Clock Frequency"<ul style="list-style-type: none">- Added notes for setting the INCK frequency via I²C communication.• "2.2.2 Regional Allocation of Serial NOR Flash Device"• "2.2.5 ECC Checking by the Serial NOR Flash Device"<ul style="list-style-type: none">- Added the descriptions of ECC checking by the Serial NOR Flash device.• "3.1.1 Register Categories"<ul style="list-style-type: none">- Added the FW_MODE_SENS category.- Deleted the security category.• "3.1.2 Remap Mode"<ul style="list-style-type: none">- Added the descriptions of the Remap Mode.• "4.3.1 Power-on Sequence"<ul style="list-style-type: none">- Updated the time after cancelling the XCLR pin until the sensor begins to output an image depending on whether ECC checking is enabled or disabled.• "4.8 The Registers That Can Be Changed While the Sensor Is in Streaming State"<ul style="list-style-type: none">- Deleted the security category.• "5.2.3.7.2 Full ME"<ul style="list-style-type: none">- Added the descriptions of the methods for calculating the exposure time.• "6.9.3.6 Rear Embedded Data"<ul style="list-style-type: none">- Added the descriptions of the light metering information.- Deleted the descriptions of the security functions.• "6.10.2 Functional Overview"<ul style="list-style-type: none">- Deleted the descriptions of the security functions. <p>Corrected misprints, layouts, fonts and inconsistent spellings.</p>

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Introduction

This document describes how to use the functions of IMX623-AA** in the following three parts, in order for application developers to design and develop automotive camera units.

■ Part 1: Overview

This part describes the functions of IMX623-AA** (hereinafter referred to as "the sensor") and potential system configurations.

"[Chapter 1 Overview](#)"

■ Part 2: Camera System Design

This part describes the information necessary to start up the sensor and to build interfaces with the sensor for communication and image output.

"[Chapter 2 System Structure](#)"

"[Chapter 3 Setting Registers via Serial Communication](#)"

"[Chapter 4 Startup Control](#)"

■ Part 3: Details of Functions

This part describes behaviors and usage of the functions of the sensor.

"[Chapter 5 Basic Functions](#)"

"[Chapter 6 Extension Functions](#)"

"[Chapter 7 Test Function](#)"

Please refer to the following documents provided separately by Sony Semiconductor Solutions Corporation (hereinafter referred to as "SSS").

- The IMX623-AA** "Data Sheet" for electrical, imaging or other characteristics
- The IMX623-AA** "Image Tuning Manual" for the methods to determine the sensor's register values
- The IMX623-AA** "Register Configuration File" for the sensor's register values
- The IMX623-AA** "Register Map" for details regarding the descriptions of the sensor's registers
- The IMX623-AA** "Safety Application Note" for details regarding the self-diagnostic functions of the sensor

Glossary of Terms

The terms used in this document are described in the following table.

Table 1-1 List of the Terms

Terms	Abbreviation	Description
Active Area	-	Active Area is the effective pixel area.
Active Area (Analog Crop)	-	Active Area (Analog Crop) is the pixel area cropped corresponding to the drive mode when the Active Area is exposed to exposure light.
Active Area (Output)	-	Active Area (Output) is the pixel area in output format.
Active Pixels		Active Pixels are the physical effective pixels.
Built-in Self-Test	BIST	Built-in Self-Test (BIST) is a function to detect failures by the built-in Self-Diagnostic function of the sensor.
High Dynamic Range	HDR	High Dynamic Range (HDR) enables the sensor to output an image with contrasts of a wide-range of illuminance from low to high by combining four images with different sensitivity.
Host	-	Host is a block communicating with the sensor to control it in a system.
Optical Black	OB	Optical Black (OB) is areas in a CMOS image sensor where light does not enter. The pixel level of the OB Area is the reference level (black level).
Optical Detector	OPD	Optical Detector integrates the pixel values of the input image to calculate information such as brightness and color information used for the AE and the AWB.
One Time Programmable ROM	OTP	One Time Programmable (OTP) Area is a ROM area that can be written only once.
Pattern Generator	PG	Pattern Generator (PG) is a function that generates images for testing.
Sub-pixel1	SP1	Sub-pixel1 (SP1) is an output of high-sensitivity pixels. The SP1 has two output lines.
Sub-pixel1 High Conversion Gain	SP1_HCG, SP1H	Sub-pixel1 High Conversion Gain (SP1_HCG, SP1H) transmits high sensitivity pixel values with high conversion efficiency.
Sub-pixel1 Low Conversion Gain	SP1_LCG, SP1L	Sub-pixel1 Low Conversion Gain (SP1_LCG, SP1L) transmits high-sensitivity pixels with low conversion efficiency.
Sub-pixel2	SP2	Sub-pixel2 (SP2) is an output of low-sensitivity pixels. The SP2 has two output lines.
Sub-pixel2 High Conversion Gain	SP2_HCG, SP2H	Sub-pixel2 High Conversion Gain (SP2_HCG, SP2H) is an output of low-sensitivity pixels converted with a priority to SNR.
Sub-pixel2 Low Conversion Gain	SP2_LCG, SP2L	Sub-pixel2 Low Conversion Gain (SP2_LCG, SP2L) is an output of low-sensitivity pixels converted with increasing saturated luminance.
Unit	-	Unit denotes the precision of a register configuration value with referred to as U8.0 (no sign, 8-digit integer part and no fractional part) or S1.7 (with sign, 1-digit integer part and 7-digit fractional part), for example.
V _{DDM}	-	V_{DDM} is the power supply voltage for I/O.
Drive Mode	-	Drive Mode is the sensor's operating mode determined by an output image size, a frame rate, an output interface (MIPI CSI-2), or the precision of an A/D converter (10 bits or 12 bits), and so forth.

Chapter 1 Overview

This chapter describes an overview of the sensor as follows:

- Examples of the connections for configuring a camera system using the sensor
- The functions embedded in the sensor

1.1. Example of a System Configuration

"Figure 1-1" illustrates an example of a system configuration using the sensor.

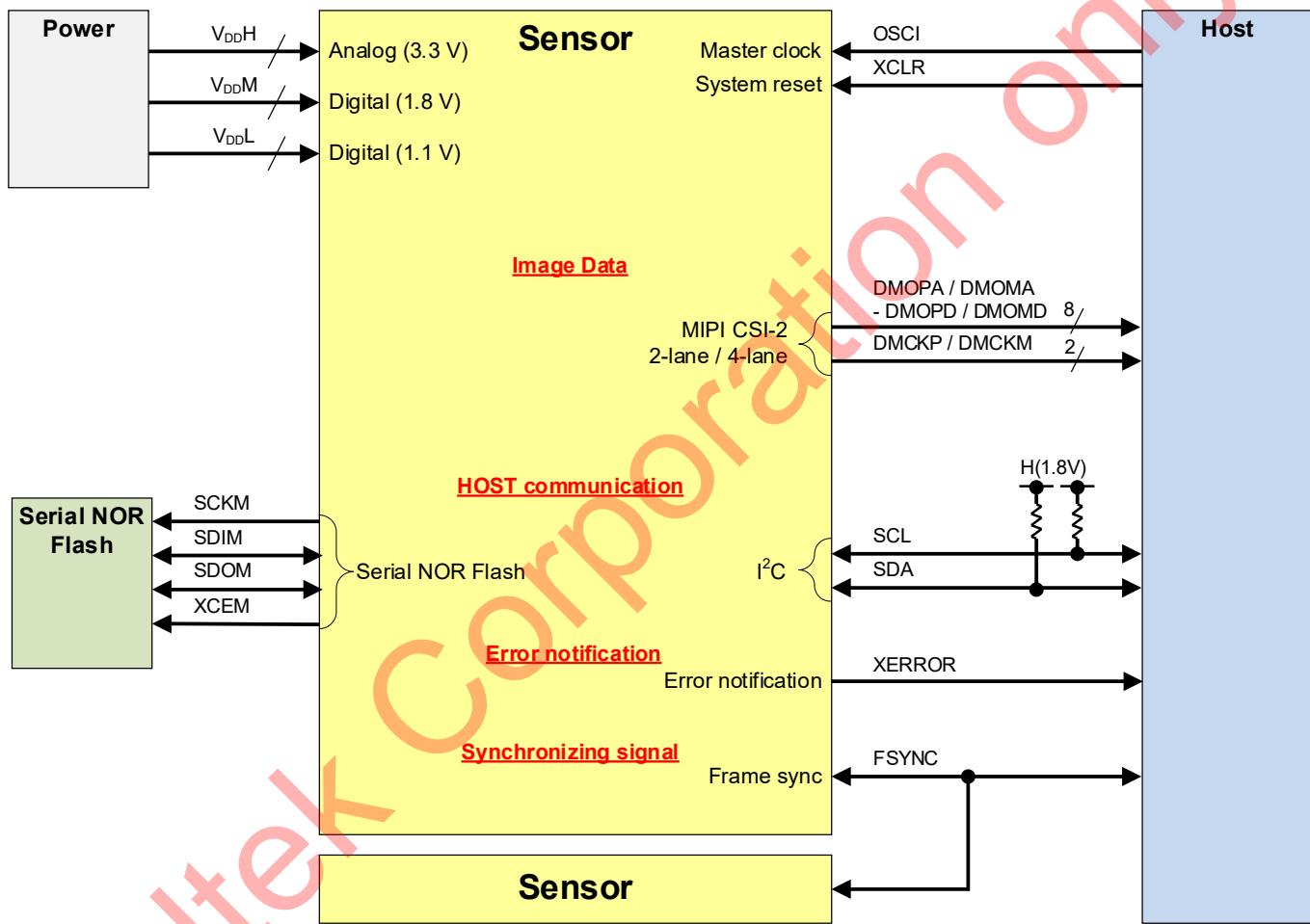


Figure 1-1 System Structure

◇ **Memo**

- Refer to the peripheral circuit diagrams in the IMX623-AA** "Data Sheet" regarding the connection diagrams of the power supply and GND pins.
- The sensor uses the MIPI CSI-2 interface for image output. The output format will vary depending on the drive mode of the sensor. For details regarding the format of output images, refer to "**2.3 Drive Modes.**"
- The sensor can be controlled via I²C communication. For details regarding the communication specifications and protocols, refer to "**Chapter 3 Setting Registers via Serial Communication**" and the IMX623-AA** "Register Map" provided separately by SSS.
- The sensor is equipped with an error notification function. For details regarding error notification, refer to "**2.1.3 XERROR Pin.**"
- It is possible to synchronize the operations of output images by connecting the sensor with other devices using an external sync signal. The external sync signal has two functions:
 1. The sensor generates the external sync signal to synchronize other devices.
 2. The sensor is synchronized by the external sync signal generated by other devices.For details regarding the Sync function, refer to "**6.1 Sync Function.**"

1.2. The Sensor's Signal Process Flow

"Figure 1-2" illustrates the sensor's signal process flow. The sensor performs image processing on each pixel in the RAW signal processing block to transmit image data via the MIPI CSI-2 interface.

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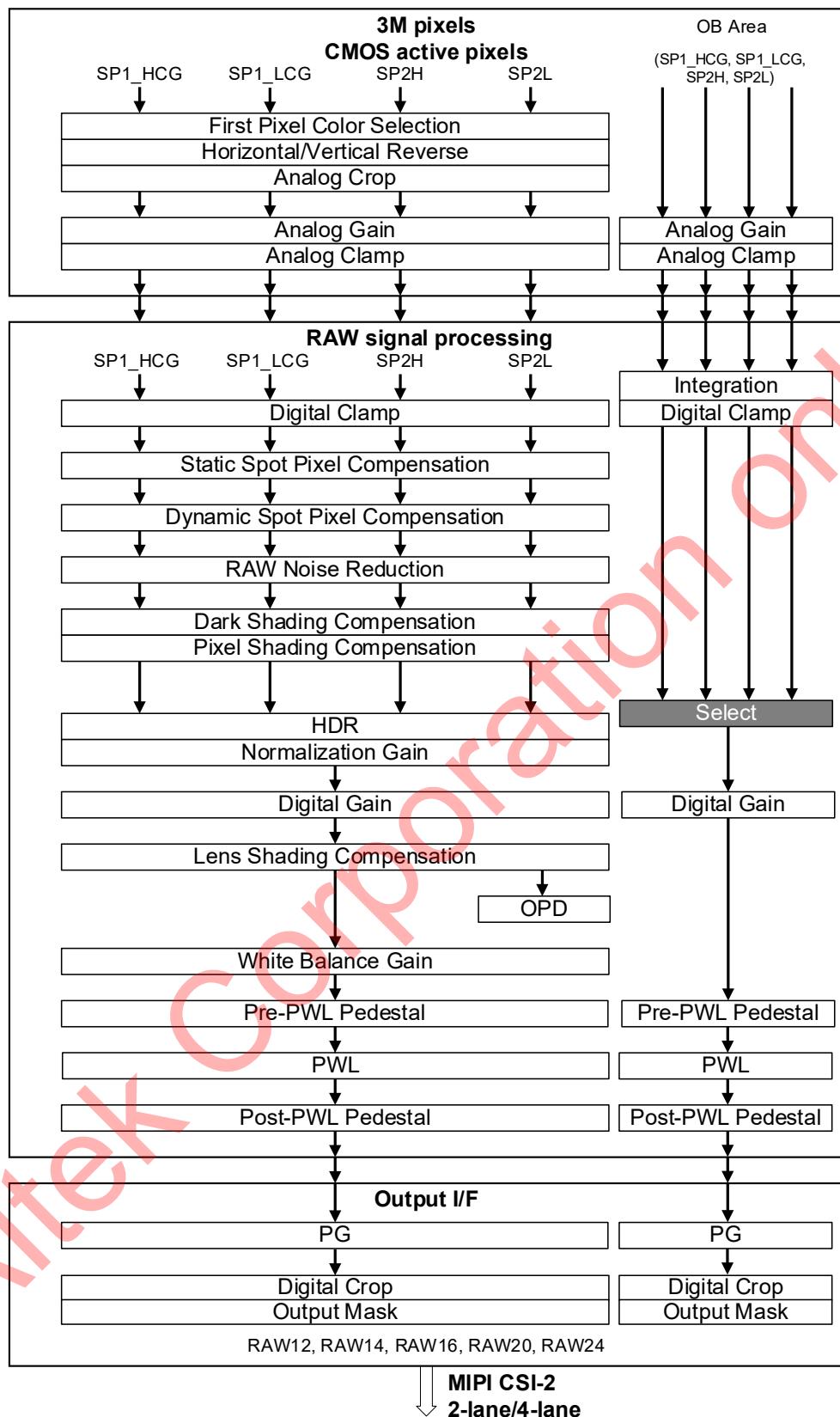


Figure 1-2 Signal Process Flow

◇ **Memo**

The sensor performs HDR imaging by using signals from the four lines with different sensitivity. Due to the negative effects of the optical system, the user can adjust the sensitivity ratio or the level of shading adjustment for signals of each line prior to HDR imaging.

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1.3. Color Filters

As illustrated in “**Table 1-1**,” the sensor’s color filter (CF) consists of a color array of 2x2 pixel units.

Table 1-1 Color Filter Type and Pixel Array

Filter Type	Pixel Array
RGGB (RGrGbB)	

As shown in “**Table 1-2**,” in this document, each pixel is denoted as CF0, CF1, CF2 and CF3 so that they can be described by using common names regardless of the color filter types.

Table 1-2 Terms for Each Pixel in This Document

Filter Type	Pixel Array
Notations in this document	

For example, CF1 indicates Gr of the color filter of RGGB type. The register name is described based on the filter type of RGGB. Identify the pixel array of the user’s system in the same way. For example, the FULLMWBGAIN_GR register is for the adjustment of CF1.

Chapter 2 System Structure

This chapter describes the following contents necessary for configuring a camera system using the sensor:

- The roles of input and output pins of the sensor
- Required settings of each input and output pin
- The sensor's drive modes (e.g., pixel size, frame rate, output format)
- Output format of an image data from the sensor

2.1. Input and Output Pins

2.1.1. List of Pins

"Table 2-1" lists the sensor's pins. Refer to the IMX623-AA** "Data Sheet" regarding the pins not listed in this table such as the power supply pins, GND pins, reference pins, and N.C. pins as well as the electrical characteristics of these pins.

Table 2-1 List of Pins

Pin Number	I/O	Pin Name	Description	Settings/Output
Clock/Reset				
M5	I	OSCI	Input pin for the master clock (INCK)	-
M6	O	OSCO	Output pin for the master clock	
K9	I	XCLR	System reset pin	High: Normal Low: Reset
Serial Communication I/F				
A6	I/O	SCL	Input pin for the I ² C clock signal	Refer to " 3.2 I²C Communication. "
B5	I/O	SDA	Input/output pin for I ² C data	
SPI Master (Serial NOR Flash I/F)				
K12	O	SCKM	SCK, Serial NOR Flash I/F pin	Refer to " 2.2 Serial NOR Flash Device. "
L11	I/O	SDIM	SDI, Serial NOR Flash I/F pin	
L12	I/O	SDOM	SDO, Serial NOR Flash I/F pin	
K11	O	XCEM	XCE, Serial NOR Flash I/F pin	
Error Notification				
B8	O	XERROR	Output pin for error notification	Refer to " 2.1.3 XERROR Pin. "
Sync				
B1	I/O	FSYNC	Input/output pin for external sync	Refer to " 2.1.4 FSYNC Pin. "
Reset Configuration				
E3	I/O	INCKSEL0	INCK frequency selection pin	Refer to " 2.1.5 Reset Configuration. "
A5	I/O	INCKSEL1	INCK frequency selection pin	
B1	I/O	FSYNC	Slave address selection pin	
K12	O	SCKM	Selection of readout of the Serial NOR Flash device	
MIPI CSI-2 I/F				
E1	O	DMOPA	MIPI CSI-2 output pin (Lane 1)	Refer to " 2.4 MIPI CSI-2 Transmitter. "
E2	O	DMOMA		
G1	O	DMOPB		

Pin Number	I/O	Pin Name	Description	Settings/Output
G2	O	DMOMB		
D1	O	DMOPC		
D2	O	DMOMC	MIPI CSI-2 output pin (Lane 3)	
H1	O	DMOPD	MIPI CSI-2 output pin (Lane 4)	
H2	O	DMOMD		
F1	O	DMCKP		
F2	O	DMCKM	MIPI CSI-2 output pin (Clock)	

2.1.2. Configuring the Settings for Pins' Input/Output and Driveability

Set the I/O and driveability of each output pin using the registers described in “[Table 2-2](#).“ Hi-Z indicates the sensor is in a state of high impedance. Select Hi-Z to start the signal input or to stop the signal output through each pin.

◆ Note

- Set register values while the sensor is in Start-up State.

For details, refer to “[4.1 The States of the Sensor](#).“

Table 2-2 Registers Used to Set the Output Pins' Input/Output and Driveability

[IO_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8AFF	1	3:2	FSYNC_DRVABTY	R/W	U2.0	This register is used to set the FSYNC pin's input/output and driveability. 0: 4.0 [mA] 1: 2.0 [mA] 2: 1.0 [mA] 3: Hi-Z (input setting or output disabled)

◇ Memo

To start up the sensor with the changed value(s) applied, write these values to the Serial NOR Flash device in accordance with the procedure as described in **"4.9.2 When Writing the Current Register Value(s) to the Serial NOR Flash Device."**

2.1.3. XERROR Pin

The sensor can notify the host of its error state following sensor startup via the XERROR pin.

- No error(s) have occurred if the XERROR pin is in a state of logic-high after sensor startup.
- Error(s) have occurred if the XERROR pin is in a state of logic-low after sensor startup.

For details regarding the errors that can be notified via the XERROR pin, refer to the IMX623-AA** "Safety Application Note."

2.1.4. FSYNC Pin

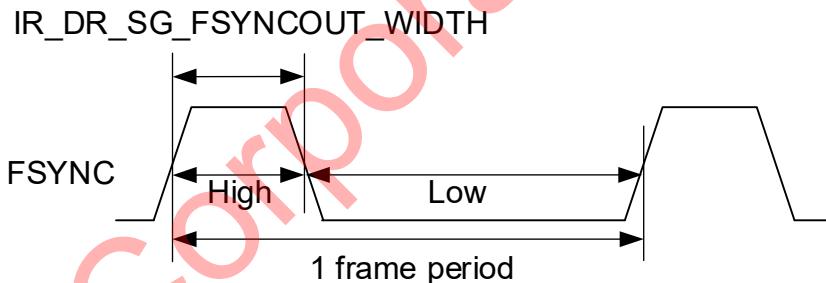
For details regarding the FSYNC pin's input/output and driveability settings, refer to "[2.1.2 Configuring the Settings for Pins' Input/Output and Driveability](#)." When not using the FSYNC pin, write 0x1 to the sensor's address 0x8AFE[3:2]. Regarding the AC characteristics of the external sync signal for the FSYNC pin, refer to the IMX623-AA** "Data Sheet." For details regarding the External Sync function, refer to "[6.1 Sync Function](#)."

2.1.4.1. External Sync Signal

The FSYNC pin can be used for the input or output of the external sync signal for the External Sync function.

"[Figure 2-1](#)" illustrates the specifications of the external sync signal input/output via the FSYNC pin. The polarity of the external sync signal can be selected from active high or active low.

(a) Active High mode



(b) Active Low mode

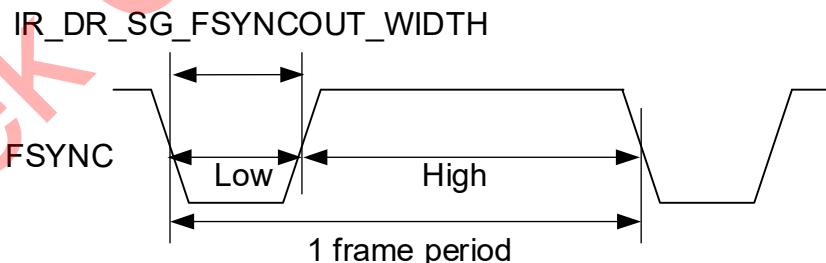


Figure 2-1 Specifications of the External Sync Signal

The polarity of the external sync signal can be set for input and output using the registers as described in "[Table 2-3](#)."

- For active high, set the register to 0.
- For active low, set the register to 1.

Table 2-3 Setting the Polarity of the External Sync Signal

Register Name	Description
IR_DR_SG_FSYNCOUT_SEL	This register is used to set the polarity of the external sync signal that the sensor transmits.
IR_DR_SG_FSYNCIN_SEL	This register is used to set the polarity of the FSYNC signal that the sensor receives.

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The output width of the external sync signal can be set using the IR_DR_SG_FSYNCOUT_WIDTH register under the following conditions:

- Configure the settings in units of the base clock.
- The base clock varies depending on the drive mode. For details, refer to “**2.3 Drive Modes**.”
- Set the output width to 500 ns or longer.

■ FSYNC pin (output settings)

In order for the sensor to transmit the external sync signal via the FSYNC pin, configure the following settings while the sensor is in Start-up State:

1. Set the address 0x8AFE[3:2] to 0.
2. Set the FSYNC_DRVABTY register to 0x0, 0x1 or 0x2.
3. Set the IR_CD_SG_FSYNCOUT_SEL register corresponding to the polarity of the signal that the sensor transmits via the FSYNC pin.
4. Set the width of the signal that the sensor transmits via the FSYNC pin, using the IR_DR_SG_FSYNCOUT_WIDTH register.

■ FSYNC pin (input settings)

To use the FSYNC pin for the input of the external sync signal, configure the following settings while the sensor is in Start-up State:

1. Set the address 0x8AFE[3:2] to 0.
2. Set the FSYNC_DRVABTY register to 0x3.
3. Set the polarity of the signal that the sensor receives via the FSYNC pin, using the IR_CD_SG_FSYNCIN_SEL register.

◇ Memo

- Regarding the AC characteristics of the external sync signal for the FSYNC pin, refer to the IMX623-AA** “Data Sheet.”
- For details regarding the FSYNC pin’s input/output and driveability settings, refer to “**2.1.2 Configuring the Settings for Pins’ Input/Output and Driveability**.”
- Input/output signals cannot be switched while the sensor is in Streaming State. Reset the sensor by performing one of the following:
 - * Change the corresponding register’s value while the sensor is in Start-up State.
 - * Update the Serial NOR Flash device after changing the corresponding register’s value.

Table 2-4 FSYNC Pin-Related Registers

[CONST1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x0153	1	0	IR_DR_SG_FSYNCIN_SEL	R/W	U1.0	This register is used to set the polarity of the external sync signal that the sensor receives. 0: Active high 1: Active low
0x0156	1	0	IR_DR_SG_FSYNCOUT_SEL	R/W	U1.0	This register is used to set the polarity of the external sync signal that the sensor transmits. 0: Active high 1: Active low

[MODE1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x0002	2	14:0	IR_DR_SG_FSYNCOUT_WIDTH	R/W	U15.0	This register is used to set the FSYNC's pulse width. <ul style="list-style-type: none">Set the width in units of the base clock determined by the drive mode.

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2.1.5. Reset Configuration

Reset Configuration is a function that controls the following by using the XCLR pin's state when the state changes from low to high:

- * The slave address for I²C communication
- * The connection settings of the Serial NOR Flash device
- * The INCK frequency

“Table 2-5” shows the pins used for the Reset Configuration function and the settings corresponding to these pins.

Table 2-5 Reset Configuration

Pin Name	Description	Settings	Remark
SCKM	Selection whether the Serial NOR Flash device is used at sensor startup	Low: The sensor does not load the Serial NOR Flash device at startup High: The sensor loads the Serial NOR Flash device at startup	“2.2 Serial NOR Flash Device”
FSYNC	Selection of a slave address	Low: 0x1A High: Set an address using the Serial NOR Flash device.* ¹	“3.3 Slave Address”
INCKSEL0	Selection of an INCK frequency	Both in low: A desired INCK frequency can be selected. 18 MHz when only INCKSEL0 is high 24 MHz when only INCKSEL1 is high 30 MHz when both are high	“2.1.5.1 Setting the Master Clock Frequency”
INCKSEL1			

* 1: When Using a Serial NOR Flash device, the user can set a desired value.

Set the Reset Configuration function before driving the XCLR pin high.

◆ **Note**

Do not change the settings during the period of 10 µs after driving the XCLR pin high. The settings, which are configured by using the Reset Configuration function, are not applied to the sensor's operations until the sensor is reset.

2.1.5.1. Setting the Master Clock Frequency

As illustrated in “**Figure 2-2**,” the host can set the sensor’s master clock frequency using the Reset Configuration function. In “**Figure 2-2**,” the red and blue names represent pins and registers respectively.

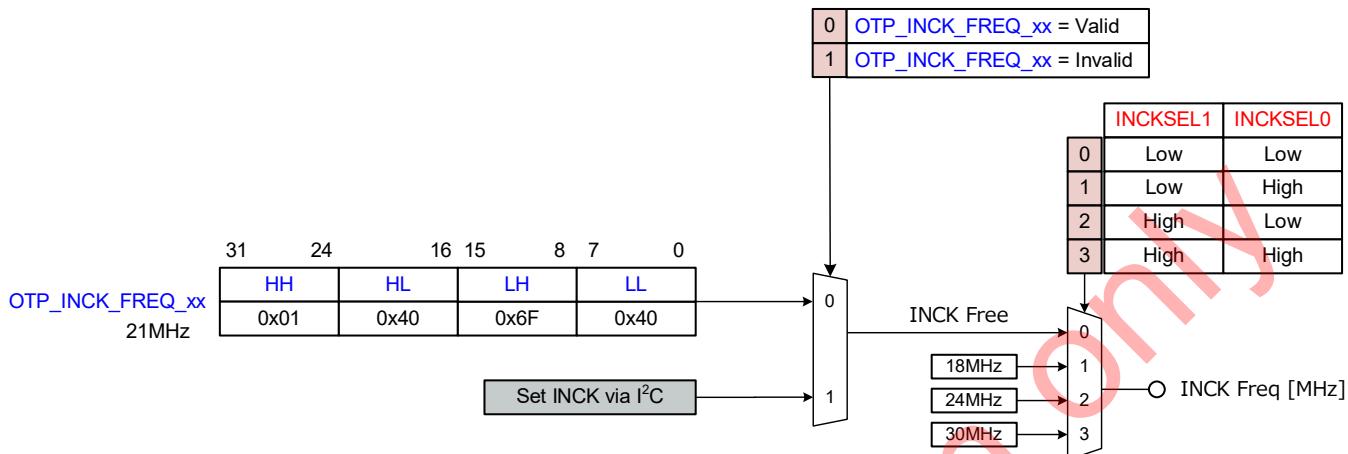


Figure 2-2 How to Set the Master Clock Frequency

“**Figure 2-2**” illustrates an example of setting the OTP_INCK_FREQ_xx (xx = HH, HL, LH, LL) registers to 21 MHz. Set the OTP_INCK_FREQ_xx (xx = HH, HL, LH, LL) register to a frequency in an 8-digit hexadecimal value, separated by 2 digits. In the example illustrated in “**Figure 2-2**,” set the four registers to the following values:

- OTP_INCK_FREQ_HH = 0x01
- OTP_INCK_FREQ_HL = 0x40
- OTP_INCK_FREQ_LH = 0x6F
- OTP_INCK_FREQ_LL = 0x40

The INCK frequency can be set ranging from 18 MHz (18000000 (0x112A880)) to 30 MHz (30000000 (0x1C9C380)). When the value of this register is set outside the available range, this value is invalid. In this case, it is necessary to set a valid frequency value via I²C communication.

◆ **Note**

The sensor loads values from the Serial NOR Flash device or the OTP ROM at startup and then sets these values to the OTP_INCK_FREQ_xx (xx = HH, HL, LH, LL) register. If valid values are stored in both, the values in the Serial NOR Flash device have priority.

◆ **Memo**

For details, refer to “**6.10 OTP Function**.”

“Figure 2-3” illustrates the process flow from when the user selects the mode for setting a desired INCK frequency using the Reset Configuration function until the INCK frequency is set.

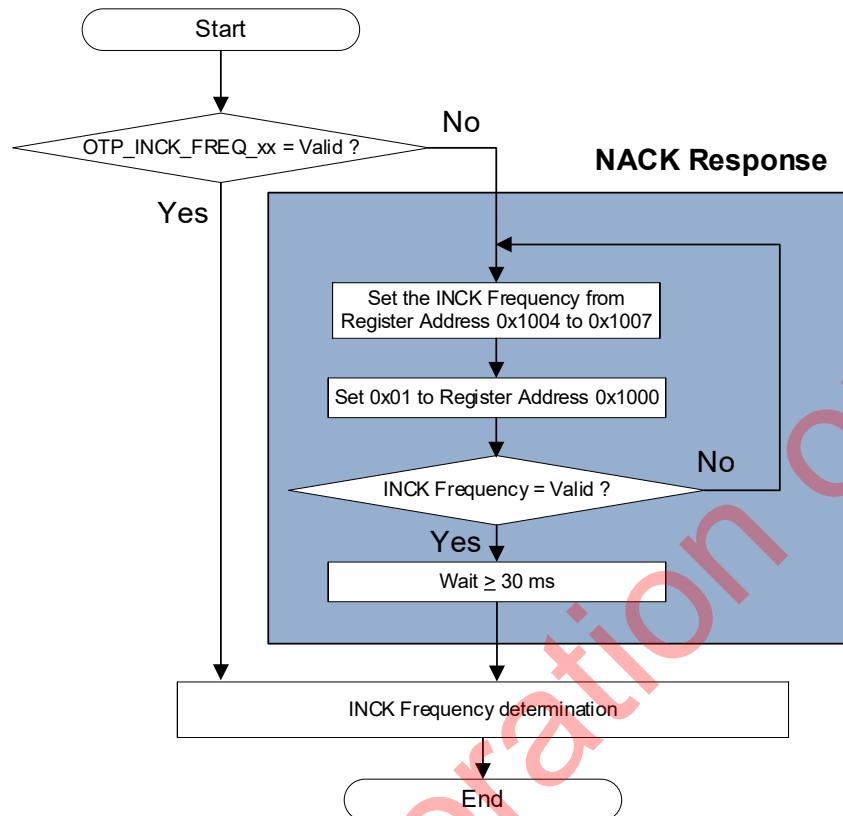


Figure 2-3 INCK Frequency Process Flow

When setting the INCK frequency via I²C communication (i.e., “Set INCK via I²C” in **“Figure 2-2”**), set the 4 bytes of register addresses ranging from 0x1004 to 0x1007 to a desired frequency as illustrated in **“Figure 2-3.”** Set the desired frequency in an 8-digit hexadecimal value for every 2 digits in ascending order, starting from the lowest 2 digits. For example, when setting the INCK frequency to 21 MHz, set the register addresses as follows:

- Set the register address 0x1004 to 0x40.
- Set the register address 0x1005 to 0x6F.
- Set the register address 0x1006 to 0x40.
- Set the register address 0x1007 to 0x01.

Note

- When the user selects the mode for setting a desired INCK frequency, in order for the sensor to begin transmitting each signal, it is necessary to cancel the XCLR pin and then set a valid frequency during the Power-On sequence.
For details, refer to **“4.3.1 Power-on Sequence.”**
- After the register address 0x1000 has been set to 0x01, the sensor enters and remains in a busy state for approximately 30 ms.

Table 2-6 Registers for Setting the Master Clock Frequency

[OTP]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBFD1	1	7:0	OTP_INCK_FREQ_LL	R/W	U8.0	This register is used to set the master clock frequency in Hz and to bits [7:0]. Available range for setting: 18 MHz to 30 MHz
0xBFD2	1	7:0	OTP_INCK_FREQ_LH	R/W	U8.0	This register is used to set the master clock frequency in Hz and to bits [15:8]. Available range for setting: 18 MHz to 30 MHz
0xBFD3	1	7:0	OTP_INCK_FREQ_HL	R/W	U8.0	This register is used to set the master clock frequency in Hz and to bits [23:16]. Available range for setting: 18 MHz to 30 MHz
0xBFD4	1	7:0	OTP_INCK_FREQ_HH	R/W	U8.0	This register is used to set the master clock frequency in Hz and to bits [31:24]. Available range for setting: 18 MHz to 30 MHz

2.2. Serial NOR Flash Device

The sensor has a dedicated SPI interface for its connection with a Serial NOR Flash device.

“Figure 2-4” illustrates a connection diagram between the sensor and the Serial NOR Flash device. “Table 2-7” shows the descriptions of the pins used for the Serial NOR Flash device connection.

The sensor saves the drive mode that is loaded at power-on and the data that is used for some functions to the Serial NOR Flash device. For details, refer to “**2.2.2 Regional Allocation of Serial NOR Flash Device.**”

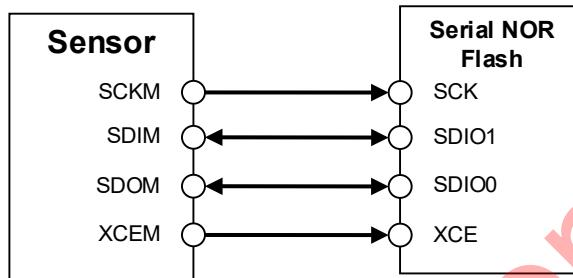


Figure 2-4 Example of Connection between the Sensor and the Serial NOR Flash Device

Table 2-7 List of SPI Master Pins (Dedicated to the Serial NOR Flash Device I/F)

Pin Number	Pin Name	Description
K12	SCKM	Serial clock
L11	SDIM	Serial data input When using Fast Read Dual I/O: Serial data input/output 1
L12	SDOM	Serial data output When using the Fast Read Dual I/O: Serial data input/output 0
K11	XCEM	Chip selection output

“Table 2-8” shows the main specifications of the Serial NOR Flash device.

Table 2-8 The Main Specifications of the Serial NOR Flash Device

Specifications	
Clock Frequency	60 MHz (Maximum)
Transfer Direction Bit	MSB first
XCEM Polarity	Active low
Power Supply Voltage	V _{DDM} (1.8 V)
Required Capacity	4 Mbits or greater
Sector Size	4096 bytes

Table 2-9 Recommended Serial NOR Flash Products

I/F	Manufacturers	Product Names	Specifications
Serial NOR Flash Device	Winbond	W25Q40EW	1.8V 4-Mbit Serial Flash Memory
		W25Q80EW	1.8V 8-Mbit Serial Flash Memory
		W25Q16FW	1.8V 16-Mbit Serial Flash Memory
		W25Q32JW	1.8V 32-Mbit Serial Flash Memory
	Macronix ^{*1}	MX25R4035F	1.8V 4-Mbit Serial Flash Memory
		MX25R8035F	1.8V 8-Mbit Serial Flash Memory
		MX25R1635F	1.8V 16-Mbit Serial Flash Memory
		MX25R3235F	1.8V 32-Mbit Serial Flash Memory

* 1: Only products with the High-Performance Mode enabled by default are available.

◆ Note

If an alternative product is being considered other than the products in “**Table 2-9**,” confirm the product specifications, perform operational verification, and ensure that there are no problems. Also check the direct current characteristics and input/output characteristics of the Serial NOR Flash device’s interface as described in the IMX623-AA** “Data Sheet.”

“**Table 2-10**” lists the set of the SPI instructions regarding the Serial NOR Flash device which is used by the sensor.

Table 2-10 The Set of the SPI Instructions Used by the Sensor

Instruction	Code
Write Enable	0x06
Write Disable	0x04
Fast Read Dual I/O	0xBB
Page Program (Write Data)	0x02
Sector Erase (4 KB)	0x20
Read Status Register	0x05
Write Status Register	0x01

“**Table 2-11**” shows the Serial NOR Flash device’s status register, which is checked and updated by the sensor.

Table 2-11 The Status Registers Which the Sensor Checks

Status Register	Bit	Description
Status Register	S0	Busy state or write in progress
	S1	Write Enable Latch Status
	S2	Block Protect Bits
	S3	
	S4	
	S7	Status Register Protect

2.2.1. Updating Function for the Serial NOR Flash Device's Status Register

The sensor can update and confirm the value of the Serial NOR Flash device's Status register using the registers in "**Table 2-12**." This function is available while the sensor is in Start-up or Streaming State. For details, refer to "**4.1 The States of the Sensor**." Regarding the structure of the Status register, see "**Table 2-11**."

■ To update the Serial NOR Flash device's Status register;

1. Set the **FLASH_STS_SET** register to the desired value in order to write it to the Status register.
2. Set the **FLASH_STS_SET_F** register to 1.
Following Step 2, the sensor will write the value set in the **FLASH_STS_SET** register to the Status register.

■ To check the value of the Serial NOR Flash device's Status register;

1. Set the **FLASH_STS_GET_F** register to 1.
Following Step 1, the sensor will read the value of the Status register and transmit the value to the **FLASH_STS_GET** register.
2. Check the **FLASH_STS_GET** register's value.

■ Example of configuring the settings of registers

To write-protect the Serial NOR Flash device, set the Status register's Block Protect bit to 1.

Table 2-12 Registers Used to Update the Serial NOR Flash Device's Status Register

[CMD_TRG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A12	1	3	FLASH_STS_SET_F	R/W	U1.0	<p>When the host sets this register to 1, the sensor issues a command to write the FLASH_STS_SET register's value to the Serial NOR Flash device's Status register.</p> <ul style="list-style-type: none"> Once the sensor issues a write command, the register's value will automatically revert to 0.
		4	FLASH_STS_GET_F	R/W	U1.0	<p>When the host sets this register to 1, the sensor issues a command to read the Serial NOR Flash device's Status register.</p> <p>The sensor transmits the readout value to the FLASH_STS_GET register.</p> <ul style="list-style-type: none"> Once the sensor issues a write command, the register's value will automatically revert to 0.

[SYS_CTRL]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8AC1	1	7:0	FLASH_STS_SET	R/W	U8.0	The value to be written to the Serial NOR Flash device's Status register

[SYS_SOUT]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x60D9	1	7:0	FLASH_STS_GET	R	U8.0	The value read from the Serial NOR Flash device's Status register

2.2.2. Regional Allocation of Serial NOR Flash Device

"Table 2-13" shows the regional allocation of the Serial NOR Flash device for the sensor.

Table 2-13 Regional Allocation of the Serial NOR Flash Device

Start Address	End Address	Description
0x00000	0x7EFFF	Reserved
0x7F000	0x7F003	Refer to "2.2.5 ECC Checking by the Serial NOR Flash Device."
0x7F004	0x7FBFF	Reserved
0x7FD00	0x7FD00	Refer to "2.2.5 ECC Checking by the Serial NOR Flash Device."
0x7FD01	0x7FFFF	Reserved
0x80000	The end address of the Serial NOR Flash device to be used	User Free Area (Available for 8 Mbits or greater only)

◆ **Note**

- Set the FLASH_SIZE register to the capacity of the Serial NOR Flash device to be used. For example, to use a 32-Mbit Serial NOR Flash device, set the register to 0x400000. For details regarding the FLASH_SIZE register, refer to "4.10.1 Input Registers."
- When not using a Serial NOR Flash device, setting this register is unnecessary.

◇ **Memo**

- The reserved region contains the drive mode necessary for the sensor's operations and data such as the registers' settings.
- When saving any files other than the Register Configuration File to the Serial NOR Flash device, SSS recommends that a Serial NOR Flash device with a capacity of 8 Mbits or greater be used.

2.2.3. Pin Assignment When No Serial NOR Flash Device Is Used

The sensor can start up without a Serial NOR Flash device. For details, refer to “[2.1.5 Reset Configuration](#).” “[Table 2-14](#)” and “[Figure 2-5](#)” show examples of pin assignment when no Serial NOR Flash device is used.

Table 2-14 Example of Pin Assignment When No Serial NOR Flash Device Is Used

Pin Name	Recommended Pin Assignment
SCKM	Pull-down resistor
SDIM	Open
SDOM	Open
XCEM	Open

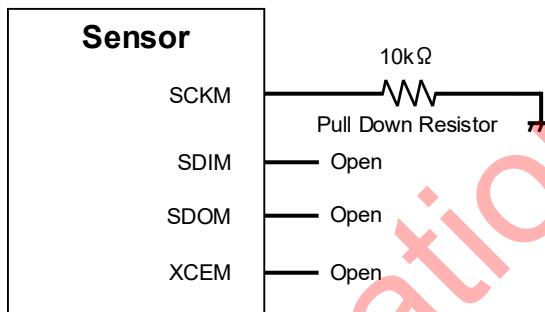


Figure 2-5 Example of Pin Assignment When No Serial NOR Flash Device Is Used

◆ **Note**

When a Serial NOR Flash device is not used, connect a pull-down resistor to the SCKM pin.

2.2.4. The State of the Serial NOR Flash Device

The Serial NOR Flash device's state can be read out from the following three registers:

- FL_CONNECT_STS register
This register indicates the connection state of the Serial NOR Flash device.
- LOAD_PARAM_SEL register
This register is used to select whether the Serial NOR Flash device is loaded at sensor startup.
- NV_STATUS register
This register indicates the state of the connected Serial NOR Flash device.

“Table 2-15” shows the state which each register indicates.

Table 2-15 The State of the Serial NOR Flash Device

FL_CONNECT_STS	Register Value	State
NOT_CONNECT	0	No Serial NOR Flash device is connected.* ¹
CONNECT	1	A Serial NOR Flash device is connected.
ACCESS_ERROR	2	Connection error of the Serial NOR Flash device

LOAD_PARAM_SEL	Register Value	State
ROM_DATA	0	The sensor does not load the Serial NOR Flash device at sensor startup.
FLASH_DATA	1	The sensor loads the Serial NOR Flash device at sensor startup.

NV_STATUS	Register Value	State
FLASH_INVALID	0	The Serial NOR Flash device is invalid or unused.
FLASH_USE	1	A load operation of the Serial NOR Flash device has successfully been completed.

* 1: This includes the case that the sensor cannot access the Serial NOR Flash device at sensor startup.

The sensor shows the Serial NOR Flash device's state in combination with the state which these registers indicate. “Table 2-16” shows relationships of the state between each register and the Serial NOR Flash device.

Table 2-16 Combinations of the State of the Serial NOR Flash Device

FL_CONNECT_STS	LOAD_PARAM_SEL	NV_STATUS	The State of the Serial NOR Flash Device
NOT_CONNECTED	ROM_DATA	FLASH_INVALID	No Serial NOR Flash device is connected.
		FLASH_USE	N/A
	FLASH_DATA	FLASH_INVALID	N/A
		FLASH_USE	N/A
CONNECT	ROM_DATA	FLASH_INVALID	Indicates one of the following: * The sensor does not load the Serial NOR Flash device at sensor startup. * The data in the Serial NOR Flash device is corrupted.
		FLASH_USE	N/A
	FLASH_DATA	FLASH_INVALID	N/A
		FLASH_USE	The data in the Serial NOR Flash device is correct.
ACCESS_ERROR	ROM_DATA	FLASH_INVALID	Error state such as the disconnection of the Serial NOR Flash device
		FLASH_USE	N/A
	FLASH_DATA	FLASH_INVALID	N/A
		FLASH_USE	N/A

When writing data to the Serial NOR Flash device, check the Serial NOR Flash device's state to confirm the data has been written correctly.

◆ **Note**

When checking the state of the Serial NOR Flash device connected to the sensor, check the fault notification by the Flash Check Safety Mechanism in addition to the NV_STATUS register. Flash Check is a safety mechanism that performs diagnostics within the sensor. For details regarding the Flash Check Safety Mechanism, refer to the IMX623-AA** "Safety Application Note."

Table 2-17 The Status Registers of the Serial NOR Flash Device

[SYS_SOUT]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x608B	1	7:0	FL_CONNECT_STS	R	U8.0	Connection state of the Serial NOR Flash device 0: No Serial NOR Flash device is connected. 1: A Serial NOR Flash device is connected. 2: Serial NOR Flash device connection error
0x608C	1	7:0	LOAD_PARAM_SEL	R	U8.0	This register is used to select whether the Serial NOR Flash device is loaded at sensor startup. 0: The sensor does not load the Serial NOR Flash device at sensor startup. 1: The sensor loads the Serial NOR Flash device at sensor startup.
0x608D	1	7:0	NV_STATUS	R	U8.0	This register indicates the state of the connected Serial NOR Flash device. 0: The Serial NOR Flash device is invalid or unused. 1: A load operation of the Serial NOR Flash device has successfully been completed.

2.2.5. ECC Checking by the Serial NOR Flash Device

The Serial NOR Flash device detects and corrects data errors using ECCs during data readout. ECC checking by the Serial NOR Flash device can be enabled or disabled using the addresses in “Table 2-18.”

Table 2-18 ECC Checking by the Serial NOR Flash Device

Start Address	End Address	Description
0x7F000	0x7F003	ECC checking by the Serial NOR Flash device can be enabled or disabled. 0x00000000: Disabled 0x00000001: Enabled
0x7FD00	0x7FD00	The ECC value to be written by the host depending on whether ECC checking by the Serial NOR Flash device is enabled or disabled. 0x00: The ECC value when ECC checking is disabled. 0x70: The ECC value when ECC checking is enabled.

The setting of ECC checking by the Serial NOR Flash device can be checked using the register in “Table 2-19.”

Table 2-19 The Register Used to Check the Setting of ECC Checking by the Serial NOR Flash Device

[SYS_COM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x6042	1	0	FLASH_ECC_EN	R	U1.0	This register is used to enable or disable ECC checking by the Serial NOR Flash device. 0: Disabled 1: Enabled

◇ **Memo**

The result of 1-bit data errors detected by the Serial NOR Flash device can be checked using the fault notification by the Flash Check Safety Mechanism. For details regarding the Flash Check Safety Mechanism, refer to the IMX623-AA** “Safety Application Note.”

2.3. Drive Modes

2.3.1. List of Drive Modes

The sensor has two drive modes: Normal and HDR. “Table 2-20” lists the sensor’s drive modes.

- In Normal mode, the sensor sends out one of the captured images of the SP1_HCG, SP1_LCG, SP2H, or SP2L lines.
- The HDR mode consists of the following three types:
 - HDR (Line/Line) mode: The sensor sequentially transmits captured images via the aforementioned two or four lines without combining the images.
 - HDR (UC) mode: The sensor transmits captured images after performing HDR imaging.
 - HDR (PWL) mode: The sensor compresses captured images after performing HDR imaging and transmits them.

For details regarding PWL compression, refer to “[5.10 PWL Function \(Gradation Compression Function\)](#).”

Table 2-20 List of the Drive Modes

Drive Mode	Compression	Frame Rate [Frames/s]	Base Clock [MHz]	A/D [Bits]	Raw Data Format	Output Frame	Active Area			
							Width [Pixel]	Height [Line]		
Normal (SP1_HCG)	Uncompressed	30	105	12	RAW24 RAW20 RAW16 RAW14 RAW12	SP1_HCG	1936	1552		
Normal (SP1_LCG)		60	120	10		SP1_LCG				
Normal (SP2H)		30	105	12		SP2H				
Normal (SP2L)		60	120	10		SP2L				
HDR (UC)		30	105	12		Combining four images				
		60	120	10	RAW24 RAW20					
HDR (PWL)	PWL Compression	30	105	12	RAW24 RAW20					
					RAW16 RAW14 RAW12					
		60	120	10						
HDR (Line/Line)	Uncompressed	30	105	12	RAW12 x 2	Line/Line	3104	6208		
		60	120	10						
		30	105	12	RAW12 x 4					

When checking the drive mode settings, refer to the information as shown in “Table 2-21.”

Table 2-21 The Relationship between the Drive Mode Settings and the Registers

Drive Mode Settings	Register
A/D [Bits]	ADBIT
Output Format	RAWOUTMODE_ OUTMODE_

The RAWOUTMODE_ and OUTMODE_ registers are compatible with the Application Lock function. For details, refer to “[3.1.5 Application Lock Function](#).”

The image output mode is determined by the frame rate and RAW data format of the sensor's drive mode. "**Table 2-22**" lists the output formats.

- The Active Area column shows the size of the effective areas, which is transmitted via the MIPI CSI-2 interface.
- The Total Pixel Area column shows the size of the entire frame including the blanking period and the Embedded Data.

Table 2-22 List of the Output Formats

• 4-Lane

Output Format	MIPI CSI-2 Data Format	Frame Rate [Frames/s]	Data Rate MIPI CSI-2 [Mbps/Lane]	Active Area		Total Pixel Area	
				Width [Pixel]	Height [Line]	Width [Pixel]	Height [Line]
RAW24	RAW12	30	693	1936	1552	2200	1750
		60	1296			2214	1626
RAW20	RAW20	30	630	1936	1552	2400	1750
		60	1080			2214	1626
RAW16	RAW16	30	462	1936	1552	2200	1750
		60	864			2214	1626
RAW14	RAW14	30	441	1936	1552	2400	1750
		60	756			2214	1626
RAW12	RAW12	30	378	1936	1552	2400	1750
		60	648			2214	1626
RAW12 x 2	RAW12	30	693	1936	1552	2200	3500
		60	1440			2460	3252
RAW12 x 4	RAW12	30	1470	6208	2200	7000	

• 2-Lane

Output Format	MIPI CSI-2 Data Format	Frame Rate [Frames/s]	Data Rate MIPI CSI-2 [Mbps/Lane]	Active Area		Total Pixel Area	
				Width [Pixel]	Height [Line]	Width [Pixel]	Height [Line]
RAW24	RAW12	30	1386	1936	1552	2200	1750
RAW20	RAW20	30	1260			2400	1750
RAW16	RAW16	30	924	1936	1552	2200	1750
RAW14	RAW14	30	882			2400	1750
		60	1428	1936	1552	2091	1626
RAW12	RAW12	30	756			2400	1750
		60	1296	1936	1552	2214	1626
RAW12 x 2	RAW12	30	1386			3104	2200
							3500

Table 2-23 Drive Mode-Related Registers

[CMN]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A7A	1	0	ADBIT	R/W	U1.0	This register indicates the A/D conversion precision. 0: 10 bits 1: 12 bits
0x8A7C	1	1:0	OUTMODE_	R/W	U2.0	Indicates the type of RAW output. 0: Output of one RAW image 1: Output of Line/Line (RAW12x2) 3: Output of Line/Line (RAW12x4)
0x8A84	1	2:0	RAWOUTMODE_	R/W	U3.0	Indicates the RAW output format. 0: RAW12 1: RAW14 2: RAW16 3: RAW20 4: RAW24 Any other settings are prohibited.

[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBF03	1	1:0	OUTMODE_APL	R/W	U2.0	This register is used to be compared with the OUTMODE_ register for the Application Lock function.
0xBF65	1	2:0	RAWOUTMODE_AP_L	R/W	U3.0	This register is used to be compared with the RAWOUTMODE_ register for the Application Lock function.

2.3.2. Mode Transition Between the Drive Modes

The sensor can switch the HDR (UC, PWL) and the Normal modes while the sensor is in Streaming State by setting the HDRON_ and OUTSEL_1 registers. The HDRON_ and OUTSEL_1 registers are compatible with the Application Lock function.

For details, refer to “**3.1.5 Application Lock Function**.” Regarding the relationship between the output modes and the registers used to switch the modes, refer to “**Table 2-24**” and “**Table 2-26**.” For details, refer to “**4.1 The States of the Sensor**.”

Table 2-24 Register Settings in the Case of a Mode Transition Between Drive Modes

Drive Modes	HDRON_	OUTSEL_1
Normal (SP1_HCG)	0	0
Normal (SP1_LCG)	0	1
Normal (SP2H)	0	2
Normal (SP2L)	0	3
HDR (UC), HDR (PWL)	1	0

A mode transition between drive modes is possible when the output format (Frame rate, A/D, RAW Data Format) is the same between the modes from and to the transition. Therefore, it is not possible to change the output format or change the mode to the HDR (Line/Line) in Streaming State.

When changing the output format (Frame rate, A/D, RAW Output Format) or when changing the mode to HDR (Line/Line), first transition the sensor to Start-up State and then configure the settings using the IMX623-AA** “Register Configuration File” provided by SSS for each drive mode.

2.3.3. Switching the Output Lines in HDR (Line/Line)

In HDR (Line/Line) mode, the output line can be changed by setting the OUTSEL_x (x = 1 to 4) registers. These settings can be changed even in Streaming State. However, the sensor cannot transmit signals from the same signal line. Nor can the sensor transmit any HDR images. “**Table 2-25**” shows an example of output settings for the RAW12x4 output in HDR (Line/Line) mode.

Table 2-25 Example of the Register Settings for the RAW12x4 Output

Line No.	Register	User-Set Value
1st Line: SP1_HCG	OUTSEL_1_	0
2nd Line: SP1_LCG	OUTSEL_2_	1
3rd Line: SP2H	OUTSEL_3_	2
4th Line: SP2L	OUTSEL_4_	3

The OUTSEL_x_ (x = 1 to 4) registers are compatible with the Application Lock function. For details, refer to “**3.1.5 Application Lock Function**.”

Table 2-26 Registers for a Mode Transition and Switching the Output Lines

[CMN]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A7B	1	0	HDRON_	R/W	U1.0	This register is used to select the output of HDR imaging results. Available when the drive mode is Normal, HDR (UC) or HDR (PWL) only. 0: Output of the line selected by the OUTSEL_1 register 1: Output of HDR imaging
0x8A80	1	1:0	OUTSEL_1_	R/W	U2.0	This register is used to select the signal line for the 1st line of the output image. 0: SP1_HCG 1: SP1_LCG 2: SP2H 3: SP2L
0x8A81	1	1:0	OUTSEL_2_	R/W	U2.0	This register is used to select the signal line for the 2nd line of the output image. Valid only when the drive mode is HDR (Line/Line). 0: SP1_HCG 1: SP1_LCG 2: SP2H 3: SP2L
0x8A82	1	1:0	OUTSEL_3_	R/W	U2.0	This register is used to select the signal line for the 3rd line of the output image. Valid only when the drive mode is HDR (Line/Line) and the output format is RAW12x4. 0: SP1_HCG 1: SP1_LCG 2: SP2H
0x8A83	1	1:0	OUTSEL_4_	R/W	U2.0	This register is used to select the signal line for the 4th line of the output image. Valid only when the drive mode is HDR (Line/Line) and the output format is RAW12x4. 0: SP1_HCG 1: SP1_LCG 2: SP2H 3: SP2L

[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBF02	1	0	HDRON_APL	R/W	U1.0	This register is used to be compared with the HDRON_ register for the Application Lock function.
0xBF61	1	1:0	OUTSEL_1_APL	R/W	U2.0	This register is used to be compared with the OUTSEL_1_ register for the Application Lock function.
0xBF62	1	1:0	OUTSEL_2_APL	R/W	U2.0	This register is used to be compared with the OUTSEL_2_ register for the Application Lock function.
0xBF63	1	1:0	OUTSEL_3_APL	R/W	U2.0	This register is used to be compared with the OUTSEL_3_ register for the Application Lock function.
0xBF64	1	1:0	OUTSEL_4_APL	R/W	U2.0	This register is used to be compared with the OUTSEL_4_ register for the Application Lock function.

2.4. MIPI CSI-2 Transmitter

2.4.1. MIPI CSI-2 Pins and Supported Specifications

This section explains the output pins of the MIPI CSI-2 interface (DMOPA to DMOPD, DMOMA to DMOMD, DMCKP and DMCKM). “Figure 2-6” illustrates the relationship between pin names and MIPI CSI-2 output lanes. The maximum bit rate for each lane is 1.5 Gbps.

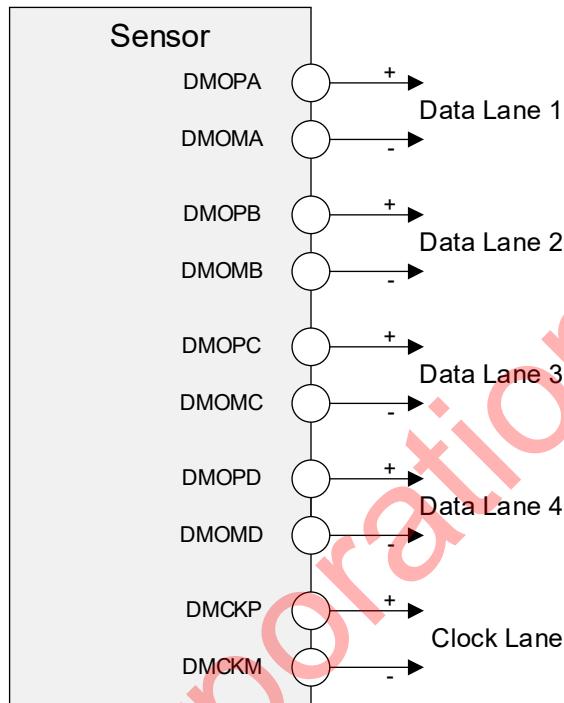


Figure 2-6 The Relationship Between the Pin Names and the MIPI CSI-2 Output Lanes

The sensor transmits images via the CSI-2 high-speed serial interface. Regarding the MIPI CSI-2 standard, refer to the following specifications:

- MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2) Version 1.2
- MIPI Alliance Specification for D-PHY Version 1.2

The RAW16, RAW20 and RAW24 formats are not described in the aforementioned specifications defined in the MIPI CSI-2 standard. For details, refer to the following:

- * “2.4.2 Setting MIPI CSI-2 Serial Data Output”
- * “2.4.3.1 Data Type”
- * “2.4.6 MIPI CSI-2 Frame Structure”
- * The IMX623-AA** “Data Sheet”

◇ Memo

The sensor does not support any output of 1.5 Gbps/lane or faster. For this reason, it does not support Skew Calibration.

2.4.2. Setting MIPI CSI-2 Serial Data Output

The sensor supports 2-lane and 4-lane of the MIPI CSI-2 serial data output. The sensor transmits the clock signal and the data signals of Lanes 1, 2, 3 and 4 via the following pins:

- Lane 1 data signal via the DMOPA and DMOMA pins
- Lane 2 data signal via the DMOPB and DMOMB pins
- Lane 3 data signal via the DMOPC and DMOMC pins
- Lane 4 data signal via the DMOPD and DMOMD pins
- Clock signal via the DMCKP and DMCKM pins

In addition, the number of lanes used to transmit data changes as follows, corresponding to the drive mode:

- In the case of 2-lane output drive: From Lanes 1 and 2
- In the case of 4-lane output drive: From Lanes 1, 2, 3 and 4

The user can select either the continuous or non-continuous operation for the clock signal operation using the IR_DR_I2I_MIPI_FRAME_VBLANKSTOP_CL register.

- Continuous Clock operation:
The clock signal continues to operate in high-speed mode during the frame blanking period.
- Non-Continuous Clock operation:
The clock signal operation changes to the LP-11 mode during the frame blanking period.
* However, the sensor continues to operate in high-speed mode during the line blanking period.

◆ Note

Change the corresponding register value while the sensor is in Start-up State. For details, refer to “[4.1 The States of the Sensor](#).”

◇ Memo

To start up the sensor with the changed value(s) applied, write these values to the Serial NOR Flash device in accordance with the procedure as described in “[4.9.2 When Writing the Current Register Value\(s\) to the Serial NOR Flash Device](#).”

Table 2-27 The MIPI CSI-2-Related Register

[CONST1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x015D	1	0	IR_DR_I2I_MIPI_FRAME_VBLANKSTOP_CL	R/W	U1.0	This register is used to select either the Continuous Clock or Non-Continuous Clock operation. 0: Clock signals operate in high-speed mode even during frame blanking period (Continuous Clock operation) 1: Clock signals transition to the LP-11 mode during frame blanking period (Non-Continuous Clock operation)

2.4.3. Data Identifier

The Data Identifier is part of the MIPI CSI-2 packet header and is transmitted with the data structure as illustrated in “**Figure 2-7**.” The Data Identifier contains the Virtual Channel and Data Type information.

For details regarding the Data Type and Virtual Channel transmitted by the sensor, refer to “**2.4.3.1 Data Type**” and “**2.4.3.2 Virtual Channel**.” For details regarding the packet header and packet footer, refer to the MIPI CSI-2 Standard.

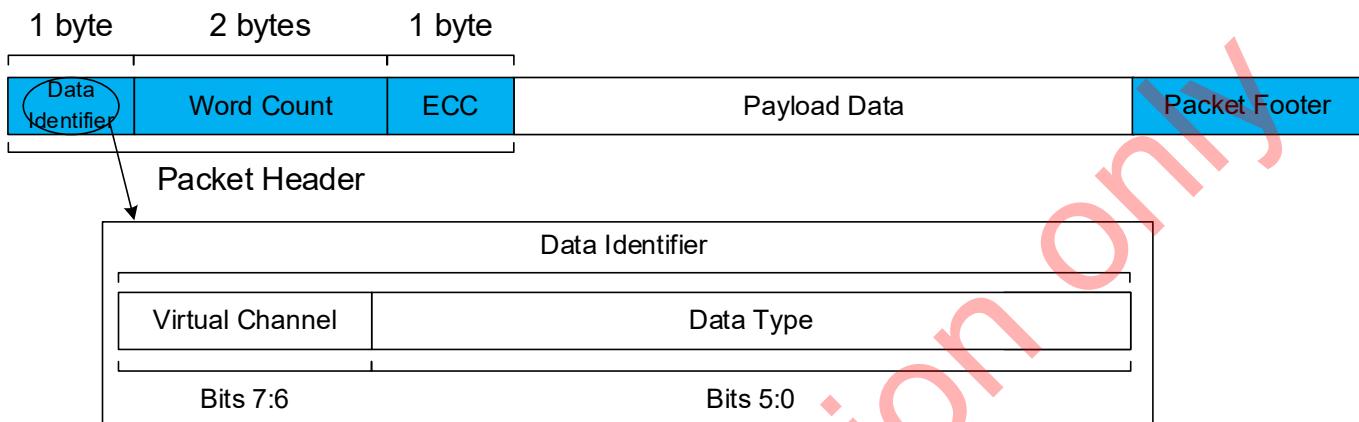


Figure 2-7 Example of How the Data Type and Virtual Channel are Transmitted

2.4.3.1. Data Type

“**Table 2-28**” lists the Data Type values used in the sensor.

Table 2-28 List of MIPI CSI-2 Data Type Values

Data Type (Header [5:0])	Name	Description
0x00	Frame Start Code	FS line output
0x01	Frame End Code	FE line output
0x12	Front Embedded Data	Front Embedded Data output
0x2C	RAW12	RAW12 output
0x2D	RAW14	RAW14 output
0x2E	RAW16	RAW16 output
0x2F	RAW20	RAW20 output
0x27	RAW24	RAW24 output
0x35	Rear Embedded Data	Rear Embedded Data output
0x37	OB	Optical Black data output
0x3F	Data Type Change	The Active Area (Output) output that is being processed by the Output Mask function. For details, refer to “ 6.8 Output Mask Function .”

The Data Type, part of the frame structure transmitted by the sensor, can be changed to a desired value using the corresponding register in the Data Type Value column in “**Table 2-29**.” To enable the value of the register in the column, set the corresponding register in the “Register for Enabling a Different Value” column to 1.

For example, to change the Data Type value of the Front Embedded Data to a desired value, first set the IFD_DATATYPE_FEBD_SEL register to 1, and then set the IFD_DATATYPE_FEBD register to the desired value.

Table 2-29 List of the Elements in the Frame Structure to Be Transmitted by the Sensor, the Data Type of Which Can Be Changed

Name	Register for Setting the Data Type		Data Type for Invalid Images	
	Register for Switching Values	Data Type Value	Register for Switching Values	Data Type Value
Front Embedded Data	IFD_DATATYPE_FEBD_SEL	IFD_DATATYPE_FEBD	-	-
Active Area (Output)	IFD_DATATYPE_VISIBLE_CTRLSEL	IFD_DATATYPE_VISIBLE	IFD_DATATYPE_VISIBLE_INVALID_CTRLSEL	IFD_DATATYPE_VISIBLE_INVALID
Rear Embedded Data	IFD_DATATYPE_REBD_SEL	IFD_DATATYPE_REBD	-	-
OB	IFD_DATATYPE_OB_SEL	IFD_DATATYPE_OB	-	-

The host can identify an invalid image output, for example immediately after sensor startup, by the sensor replacing the Data Type value of the Active Area (Output) of the invalid image with the value specified using the IFD_DATATYPE_VISIBLE_INVALID register. For details, refer to “**6.8 Output Mask Function**.”

◆ Note

Change the value of each register shown in “**Table 2-29**” while the sensor is in Start-up State.

Table 2-30 Data Type-Related Registers

[VIF]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBDF8	1	0	IFD_DATATYPE_FEBD_SEL	R/W	U1.0	This register is used to select the Data Type value of the Front Embedded Data. 0: The initial value corresponding to the drive mode 1: The value of the IFD_DATATYPE_FEBD register
0xBDF9	1	0	IFD_DATATYPE_REBD_SEL	R/W	U1.0	This register is used to select the Data Type value of the Rear Embedded Data. 0: The initial value corresponding to the drive mode 1: The value of the IFD_DATATYPE_REBD_SEL register
		1	IFD_DATATYPE_OB_SEL	R/W	U1.0	This register is used to select the Data Type value of the OB Area. 0: The initial value corresponding to the drive mode 1: The value of the IFD_DATATYPE_OB register
		2	IFD_DATATYPE_VISIBLE_CTRLSEL	R/W	U1.0	This register is used to select the Data Type value of the Active Area (Output). 0: The initial value corresponding to the drive mode 1: The value of the IFD_DATATYPE_VISIBLE register

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
		3	IFD_DATATYPE_VISI BLE_INVALID_CTRLSEL	R/W	U1.0	This register is used to select the value when changing the Data Type within the MIPI CSI-2 Packet Header by using the Output Mask function. 0: The initial value corresponding to the drive mode 1: The value of the IFD_DATATYPE_VISIBLE_INVALID register
0xBDFB	1	5:0	IFD_DATATYPE_FEBD	R/W	U6.0	This register is used to specify the Data Type value of the Front Embedded Data. Default: 0x12 Available range: 0x10 to 0x3F • This register is enabled when the value of the IFD_DATATYPE_FEBD_SEL register is 1.
0xBDFFC	1	5:0	IFD_DATATYPE_REBD	R/W	U6.0	This register is used to specify the Data Type value of the Rear Embedded Data. Default: 0x35 Available range: 0x10 to 0x3F • This register is enabled when the value of the IFD_DATATYPE_REBD_SEL register is 1.
0xBDFD	1	5:0	IFD_DATATYPE_OB	R/W	U6.0	This register is used to specify the Data Type value of the OB. Default value: 0x37 Available range: 0x10 to 0x3F • This register is enabled when the value of the IFD_DATATYPE_OB_SEL register is 1.
0xBDFFE	1	5:0	IFD_DATATYPE_VISIBLE	R/W	U6.0	This register is used to specify the Data Type value of the Active Area (Output). By default: RAW12: 0x2C RAW14: 0x2D RAW16: 0x2E RAW20: 0x2F RAW24: 0x27 Available range: 0x10 to 0x3F • This register is enabled when the value of the IFD_DATATYPE_VISIBLE_CTRLSEL register is 1.
0xBDFFF	1	5:0	IFD_DATATYPE_VISIBLE_INVALID	R/W	U6.0	This register is used to set the Data Type value when changing the Data Type within the MIPI CSI-2 Packet Header by using the Output Mask function. Default: 0x3F Available range: 0x10 to 0x3F • This register is enabled when the value of the IFD_DATATYPE_VISIBLE_INVALID_CTRLSEL register is 1.

2.4.3.2. Virtual Channel

It is possible to set the value that is being transmitted to the upper 2 bits of the Data Identifier (hereinafter referred to as "Virtual Channel ID") using the IFD_VCIDx ($x = 0$ to 3) registers. To enable each value of the IFD_VCIDx ($x = 0$ to 3) registers, set the IFD_VCIDx_CTRLSEL ($x = 0$ to 3) registers to 1.

In the drive mode of HDR (Line/Line), the following operations are available:

- The host can set an individual Virtual Channel ID for each output line.
- The sensor can transmit the FS and the FE for each output line. For details, see "**Figure 2-9.**"

The host can select the number of IDs to be set as Virtual Channel IDs using the IFD_VCID_NUM_SEL register. To enable the value of the IFD_VCID_NUM_SEL register, set the IFD_VCID_NUM_SEL_CTRLSEL register to 1. The available number of IDs for selection varies depending on the drive mode shown in "**Table 2-31.**"

Table 2-31 Setting the Virtual Channel IDs

Drive Modes	IFD_VCID_NUM_SEL	The Number of Virtual Channel IDs	The Register for Selecting the Signal Line for Each Horizontal Image Line	Virtual Channel ID Register
Normal HDR (UC) HDR (PWL)	0	1	OUTSEL_1_	IFD_VCID0
HDR (Line/Line) RAW 12 x 2	0	1	OUTSEL_1_	IFD_VCID0
			OUTSEL_2_	
HDR (Line/Line) RAW 12 x 4	1	2	OUTSEL_1_	IFD_VCID0
			OUTSEL_2_	
HDR (Line/Line) RAW 12 x 4	0	1	OUTSEL_1_	IFD_VCID0
			OUTSEL_2_	
			OUTSEL_3_	
			OUTSEL_4_	
	3	4	OUTSEL_1_	IFD_VCID0
			OUTSEL_2_	IFD_VCID1
			OUTSEL_3_	IFD_VCID2
			OUTSEL_4_	IFD_VCID3

◆ **Note**

Change register values for Virtual Channels while the sensor is in Start-up State.

Table 2-32 Virtual Channel-Related Registers

[VIF]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBDFA	1	0	IFD_VCID_NUM_SEL_CTRLSEL	R/W	U1.0	This register is used to select the number of IDs as Virtual Channel IDs. 0: The initial value corresponding to the drive mode 1: The value of the IFD_VCID_NUM_SEL register

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
		1	IFD_VCID0_CTRLSEL	R/W	U1.0	This register is used to select the value to be set to the Virtual Channel ID0. 0: The initial value corresponding to the drive mode 1: The value of the IFD_VCID0 register
		2	IFD_VCID1_CTRLSEL	R/W	U1.0	This register is used to select the value to be set to the Virtual Channel ID1. 0: The initial value corresponding to the drive mode 1: The value of the IFD_VCID1 register
		3	IFD_VCID2_CTRLSEL	R/W	U1.0	This register is used to select the value to be set to the Virtual Channel ID2. 0: The initial value corresponding to the drive mode 1: The value of the IFD_VCID2 register
		4	IFD_VCID3_CTRLSEL	R/W	U1.0	This register is used to select the value to be set to the Virtual Channel ID3. 0: The initial value corresponding to the drive mode 1: The value of the IFD_VCID3 register
0xBE00	1	2:0	IFD_VCID_NUM_SEL	R/W	U3.0	This register is used to set the number of Virtual Channel IDs to be used. 0: One ID 1: Two IDs 2: Setting prohibited 3: Four IDs Any other settings are prohibited. <ul style="list-style-type: none">• This register is enabled when the value of the IFD_VCID_NUM_SEL_CTRLSEL register is 1.
0xBE01	1	1:0	IFD_VCID0	R/W	U2.0	This register is used to set the 1st line's Virtual Channel ID. <ul style="list-style-type: none">• This register is enabled when the value of the IFD_VCID0_CTRLSEL register is 1.
0xBE02	1	1:0	IFD_VCID1	R/W	U2.0	This register is used to set the 2nd line's Virtual Channel ID when the Virtual Channel ID is 2 or 4. <ul style="list-style-type: none">• This register is enabled when the value of the IFD_VCID1_CTRLSEL register is 1.
0xBE03	1	1:0	IFD_VCID2	R/W	U2.0	This register is used to set the 3rd line's Virtual Channel ID when the Virtual Channel ID is 4. <ul style="list-style-type: none">• This register is enabled when the value of the IFD_VCID2_CTRLSEL register is 1.
0xBE04	1	1:0	IFD_VCID3	R/W	U2.0	This register is used to set the 4th line's Virtual Channel ID when the Virtual Channel ID is 4. <ul style="list-style-type: none">• This register is enabled when the value of the IFD_VCID3_CTRLSEL register is 1.

2.4.4. Frame Number

The Frame Number is a count value stored in the FS/FE packet of MIPI CSI-2 and is different from the Frame Count in the Embedded Data. The Frame Number operates as follows:

- The Frame Number counts up to the maximum value set in the IR_DR_I2I_MIPI_FRMNUM_MAX register.
- Frame Number 1 is defined as the first output frame after the sensor has transitioned to Streaming State. The Frame Number is incremented with every FS packet output.
- When the Frame Number reaches the value of the IR_DR_I2I_MIPI_FRMNUM_MAX register, it reverts to 1 in the subsequent frame.
- When the value of the IR_DR_I2I_MIPI_FRMNUM_MAX register is changed in Streaming State, the Frame Number is reset to 1. To reset the Frame Number at a desired time without changing the maximum value, set the WO_DR_I2I_MIPI_FRMNUM_CLR register to 1.
- When not using the Frame Number, set the IR_DR_I2I_MIPI_FRMNUM_MAX register to 0. With this setting, the sensor always transmits 0.

“Table 2-33” shows the registers for the Frame Number of the MIPI CSI-2 interface. For details, refer to “4.1 The States of the Sensor.”

◇ Memo

To start up the sensor with the changed value(s) applied, write these values to the Serial NOR Flash device in accordance with the procedure as described in “4.9.2 When Writing the Current Register Value(s) to the Serial NOR Flash Device.”

Table 2-33 Frame Number-Related Registers

[CTRL1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1AE0	2	15:0	IR_DR_I2I_MIPI_FRMNUM_MAX	R/W	U16.0	This register is used to set the maximum value of the Frame Number in the MIPI CSI-2 Packet Header. 0: The Frame Number is fixed at 0x00. Other than 0: The Frame Number is set to the maximum value.
0x1AE4	1	0	WO_DR_I2I_MIPI_FRMNUM_CLR	W	U1.0	This register is used to select whether to reset the Frame Number in the MIPI CSI-2 Packet Header to 1. 0: Reset disabled 1: Reset enabled

2.4.5. Line Information

As illustrated in “**Figure 2-9**,” in HDR (Line/Line) drive mode, the Line Information can be appended to the head of each line.

The Line Information consists of four pixels. Checking the value of the Line Information enables the host to identify the SP1_HCG, SP1_LCG, SP2H and SP2L lines. “**Table 2-34**” shows the Line Information.

- The register names in the table are those with their prefixes omitted. (x = IR_DR_I2I, y = IR_DR_EBD)
- To enable the Line Information of the Active Area (Output), the OB Area and the Mask Data, set the IR_DR_I2I_LINFO_VIS_EN register to 1 while the sensor is in Start-up State.
- To enable the Line Information of the Front Embedded Data and the Rear Embedded Data, set the IR_DR_I2I_LINFO_EBD_EN register to 1 while the sensor is in Start-up State.

Table 2-34 List of Line Information

Data Type	Line	Pixel 1		Pixel 2		Pixel 3		Pixel 4	
		Register	Default	Register	Default	Register	Default	Register	Default
Active Area (Output), OB, Mask Data	1st	x_LINFO_1ST	0xFFFF	x_LINFO_2ND	0x000	x_LINFO_3RD	0x000	x_LINFO_4T_H_1	0x810
	2nd							x_LINFO_4T_H_2	0x820
	3rd							x_LINFO_4T_H_3	0x830
	4th							x_LINFO_4T_H_4	0x840
Front Embedded Data	1st	y_LINFO_EBD_1S	0xFF	y_LINFO_EBD_2ND	0x00	y_LINFO_EBD_3RD	0x00	y_LINFO_FE_BD_4TH_1	0x91
	2nd							y_LINFO_FE_BD_4TH_2	0x92
	3rd							y_LINFO_FE_BD_4TH_3	0x93
	4th							y_LINFO_FE_BD_4TH_4	0x94
Rear Embedded Data	1st	y_LINFO_EBD_1S	0xFF	y_LINFO_EBD_2ND	0x00	y_LINFO_EBD_3RD	0x00	y_LINFO_RE_BD_4TH_1	0xA1
	2nd							y_LINFO_RE_BD_4TH_2	0xA2
	3rd							y_LINFO_RE_BD_4TH_3	0xA3
	4th							y_LINFO_RE_BD_4TH_4	0xA4

Table 2-35 List of Line Information-Related Registers

[CONST1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x017B	1	0	IR_DR_I2I_LINFO_VIS_EN	R/W	U1.0	This register is used to select whether or not the Line Information Pixel Data is appended to the head of each

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
						line (Active Area (Output), Optical Black and Mask Data) in HDR (Line/Line) mode. 0: Line Information Pixel Data not appended 1: Line Information Pixel Data appended
0x017C	1	0	IR_DR_I2I_LINFO_EBD_EN	R/W	U1.0	This register is used to select whether or not the Line Information Pixel Data is appended to the head of each line (Front Embedded Data and Rear Embedded Data) in HDR (Line/Line) mode. 0: Line Information Pixel Data not appended 1: Line Information Pixel Data appended
0x017E	2	11:0	IR_DR_I2I_LINFO_1ST	R/W	U12.0	This register indicates the Line Information value that contains the Active Area (Output), Optical Black and Mask Data. (1st pixel)
0x0180	2	11:0	IR_DR_I2I_LINFO_2ND	R/W	U12.0	This register indicates the Line Information value that contains the Active Area (Output), Optical Black and Mask Data. (2nd pixel)
0x0182	2	11:0	IR_DR_I2I_LINFO_3RD	R/W	U12.0	This register indicates the Line Information value that contains the Active Area (Output), Optical Black and Mask Data. (3rd pixel)
0x0184	2	11:0	IR_DR_I2I_LINFO_4TH_1	R/W	U12.0	This register indicates the Line Information value that contains the 1st line's Active Area (Output), Optical Black and Mask Data. (4th pixel)
0x0186	2	11:0	IR_DR_I2I_LINFO_4TH_2	R/W	U12.0	This register indicates the Line Information value that contains the 2nd line's Active Area (Output), Optical Black and Mask Data. (4th pixel)
0x0188	2	11:0	IR_DR_I2I_LINFO_4TH_3	R/W	U12.0	This register indicates the Line Information value that contains the 3rd line's Active Area (Output), Optical Black and Mask Data. (4th pixel)
0x018A	2	11:0	IR_DR_I2I_LINFO_4TH_4	R/W	U12.0	This register indicates the Line Information value that contains the 4th line's Active Area (Output), Optical Black and Mask Data. (4th pixel)
0x018C	1	7:0	IR_DR_EBD_LINFO_EBD_1ST	R/W	U8.0	This register indicates the Line Information value that contains the Front Embedded Data and Rear Embedded Data. (1st pixel)
0x018D	1	7:0	IR_DR_EBD_LINFO_EBD_2ND	R/W	U8.0	This register indicates the Line Information value that contains the Front Embedded Data and Rear Embedded Data. (2nd pixel)
0x018E	1	7:0	IR_DR_EBD_LINFO_EBD_3RD	R/W	U8.0	This register indicates the Line Information value that contains the Front Embedded Data and Rear Embedded Data. (3rd pixel)
0x018F	1	7:0	IR_DR_EBD_LINFO_FEBD_4TH_1	R/W	U8.0	This register indicates the Line Information value that contains the 1st line's Front Embedded Data. (4th pixel)

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x0190	1	7:0	IR_DR_EBD_LINFO_FEBD_4TH_2	R/W	U8.0	This register indicates the Line Information value that contains the 2nd line's Front Embedded Data. (4th pixel)
0x0191	1	7:0	IR_DR_EBD_LINFO_FEBD_4TH_3	R/W	U8.0	This register indicates the Line Information value that contains the 3rd line's Front Embedded Data. (4th pixel)
0x0192	1	7:0	IR_DR_EBD_LINFO_FEBD_4TH_4	R/W	U8.0	This register indicates the Line Information value that contains the 4th line's Front Embedded Data. (4th pixel)
0x0193	1	7:0	IR_DR_EBD_LINFO_REBD_4TH_1	R/W	U8.0	This register indicates the Line Information value that contains the 1st line's Rear Embedded Data. (4th pixel)
0x0194	1	7:0	IR_DR_EBD_LINFO_REBD_4TH_2	R/W	U8.0	This register indicates the Line Information value that contains the 2nd line's Rear Embedded Data. (4th pixel)
0x0195	1	7:0	IR_DR_EBD_LINFO_REBD_4TH_3	R/W	U8.0	This register indicates the Line Information value that contains the 3rd line's Rear Embedded Data. (4th pixel)
0x0196	1	7:0	IR_DR_EBD_LINFO_REBD_4TH_4	R/W	U8.0	This register indicates the Line Information value that contains the 4th line's Rear Embedded Data. (4th pixel)

2.4.6. MIPI CSI-2 Frame Structure

The frame structure consists of the following two types corresponding to the drive mode:

- “**Figure 2-8**” illustrates the frame structure in Normal, HDR (UC) or HDR (PWL) mode.
- “**Figure 2-9**” illustrates the frame structure in HDR (Line/Line) mode.

“**Table 2-37**” shows the sensor’s output format and image size in the case of MIPI CSI-2 output.

“**Table 2-36**” lists the frame structure data transmitted by the sensor.

Table 2-36 List of Frame Structure Data

Name	Description
Front Embedded Data	The Front Embedded Data is used to store various internal information regarding the output images. For details regarding the Front Embedded Data, refer to “ 6.9 Information Output Function .” The user can enable or disable the output of the Front Embedded Data. For details, refer to “ 6.9.3.1 Enabling or Disabling the Output of the Embedded Data .”
OB	The OB stores the pixel data in the OB Area. “ Table 2-38 ” shows the signal lines, from which each signal is transmitted to the OB Area. When the drive mode is HDR (UC) or HDR (PWL), the OB Area that is transmitted can be changed using the IR_IS_ALP_OB_SEL register.
Active Area (Output)	The Active Area (Output) is used to store the pixel data of the Active Area (Output). The image output size of the Active Area (Output) varies as shown in “ Table 2-37 ,” corresponding to the drive mode.
Rear Embedded Data	The Rear Embedded Data is used to store various internal information regarding the output images. For details regarding the Rear Embedded Data, refer to “ 6.9 Information Output Function .” The user can enable or disable the output of the Rear Embedded Data. For details, refer to “ 6.9.3.1 Enabling or Disabling the Output of the Embedded Data .”

Table 2-37 The Image Size of the Frame Structure in MIPI CSI-2 Output

Output Format	Active Area (Output)	
	Width [Pixel]	Height [Line]
RAW	1936	1552

Table 2-38 Signal Lines, From Which Each Signal Is Transmitted to the OB Area

Drive Modes	IR_IS_ALP_OB_SEL	Signal Line, From Which the Signal Is Transmitted to the OB Area
HDR (UC), HDR (PWL)	0	SP1_HCG
	1	SP1_LCG
	2	SP2H
	3	SP2L
Normal, HDR (Line/Line)	-	The signal line, from which its signal is transmitted as the Active Area (Output).

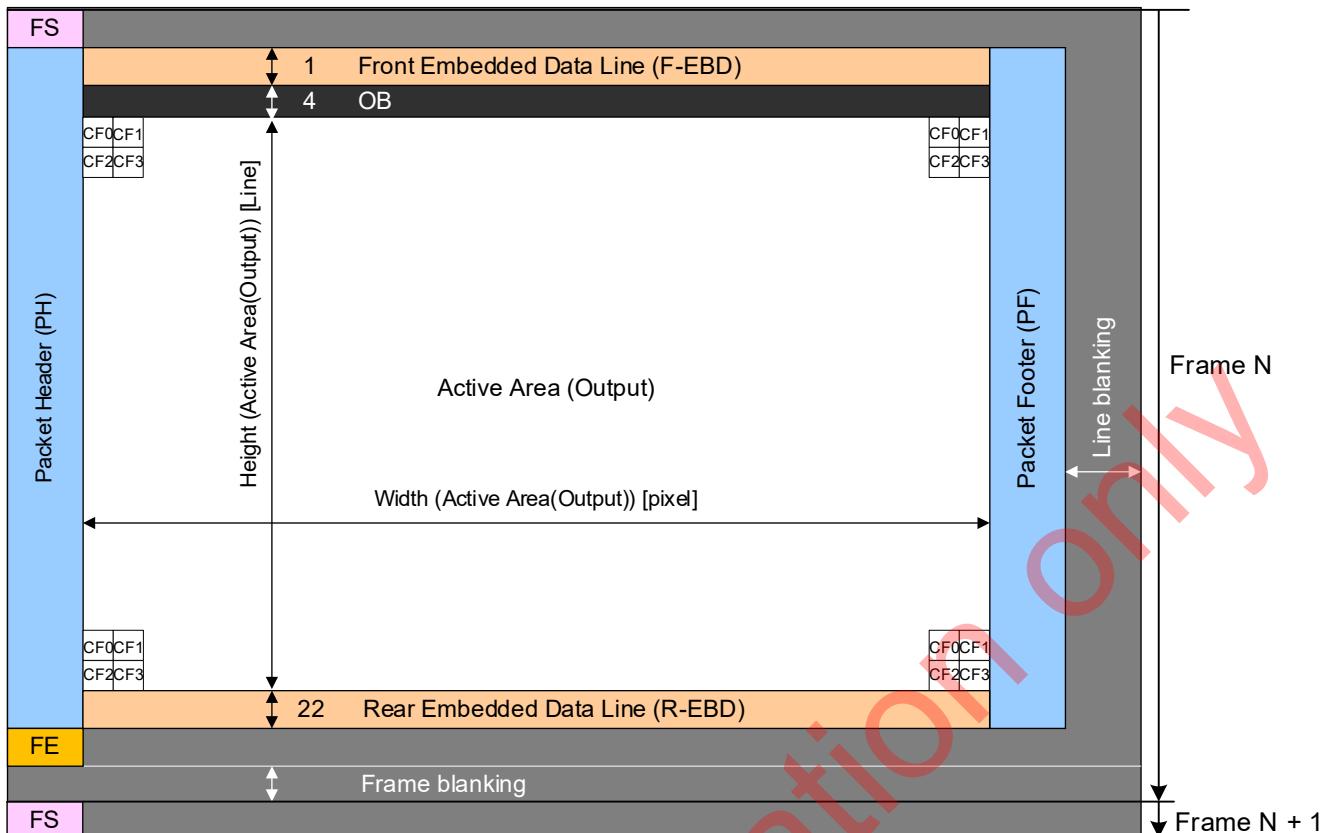


Figure 2-8 Frame Structure in Normal, HDR (UC) or HDR (PWL) Mode

In HDR (Line/Line) output mode, the sensor alternately transmits data from each line corresponding to the output settings. In addition, the sensor alternately transmits the Front Embedded Data, Rear Embedded Data and Optical Black data in areas other than the Active Area. Regarding the Front Embedded Data and Rear Embedded Data in HDR (Line/Line) output mode, the sensor transmits the same data to all four lines.

Both the Virtual Channel and the Line Information can be appended to identify the output line in HDR (Line/Line) output mode.

■ Virtual Channel Output

The left figure in “[Figure 2-9](#)” illustrates an example of output using one Virtual Channel ID (i.e., IFD_VCID_NUM_SEL = 0).

The right figure in “[Figure 2-9](#)” illustrates an example of output using four Virtual Channel IDs (i.e., IFD_VCID_NUM_SEL = 3).

When setting the IFD_VCID_NUM_SEL register to 1 or 3, the sensor sends out FS/FE packets corresponding to the number of output lines.

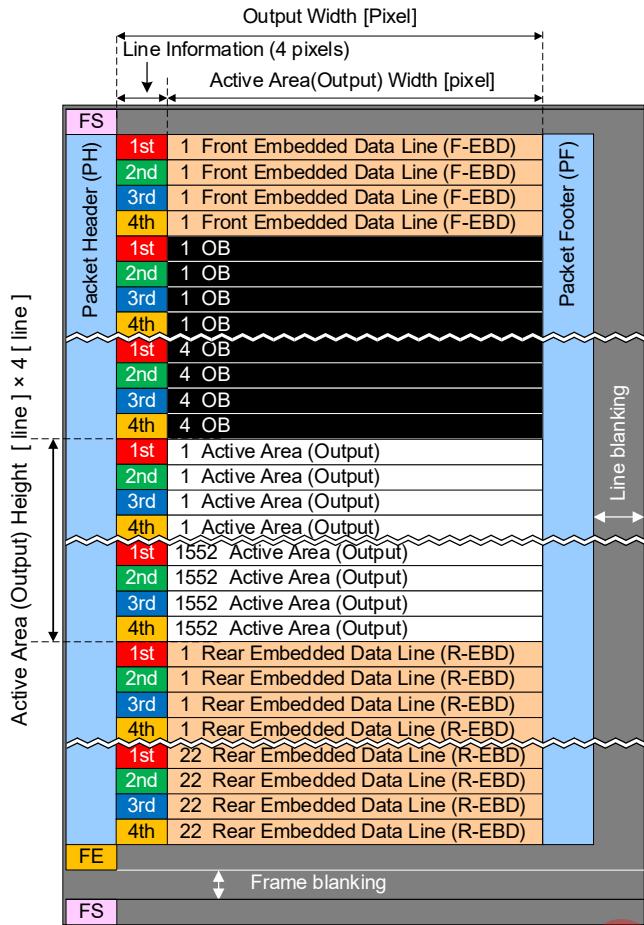
For details, refer to “[2.4.3.2 Virtual Channel](#).”

■ When the Line Information output is enabled;

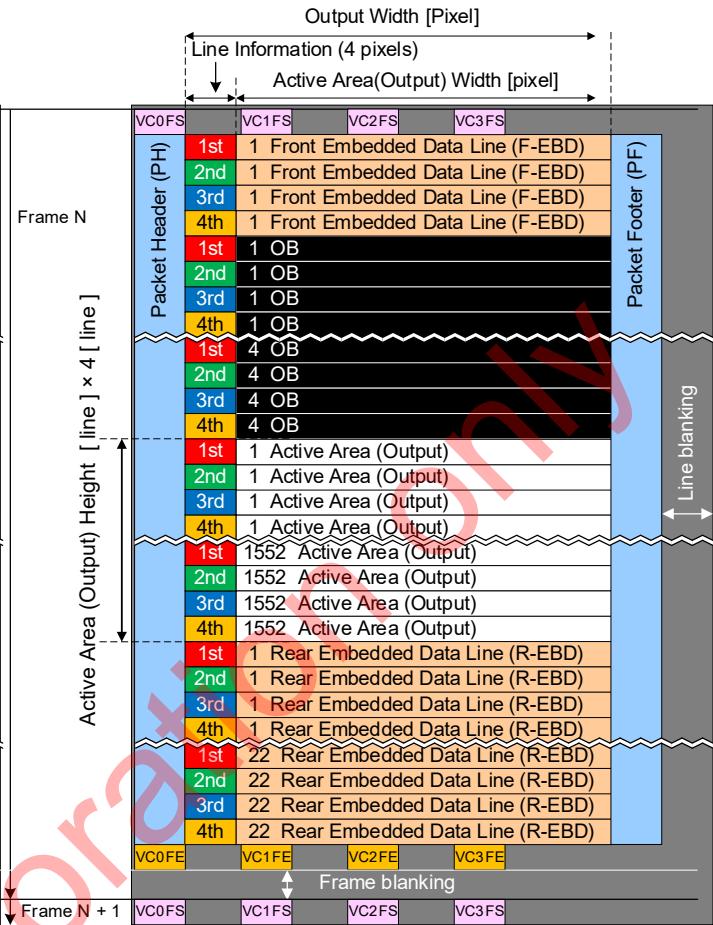
When the Line Information is enabled (i.e., IR_DR_I2I_LINFO_VIS_EN = 1 and IR_DR_I2I_LINFO_EBD_EN = 1), four pixels of Line Information are appended immediately after the packet header. For details, see “[Figure 2-9](#).”

Regarding the Line Information, refer to “[2.4.5 Line Information](#).”

In the case of IFD_VCID_NUM_SEL = 0



In the case of IFD_VCID_NUM_SEL = 3



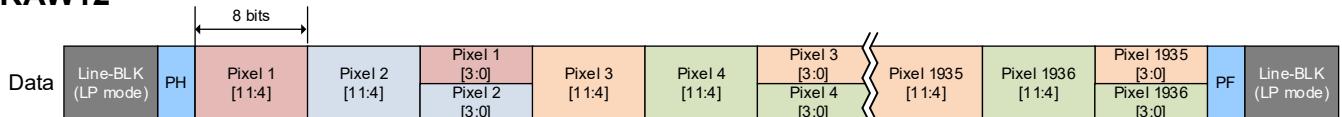
Output Width [Pixel] : Line Information Enabled → Line Information [pixel] + Active Area (Output) Width [pixel]
 Line Information Disabled → Active Area (Output) Width [pixel]

Figure 2-9 Frame Structure (RAW12x4 Output) in HDR (Line/Line) Mode

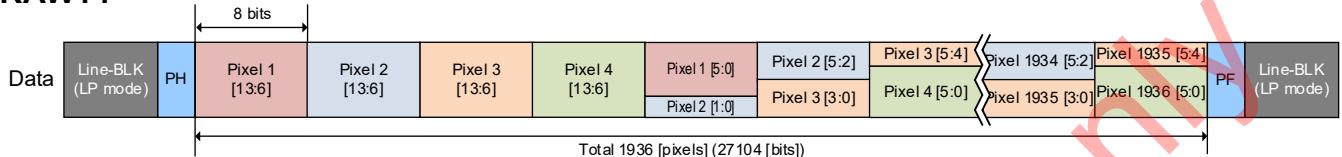
The output order of each line in HDR (Line/Line) mode can be changed using the method described in “[2.3.3 Switching the Output Lines in HDR \(Line/Line\)](#).”

"Figure 2-10" illustrates the output format of each line. Regarding the formats of RAW12, RAW14, RAW16, RAW20 and RAW24, the sensor sends out one line of data in the Active Area sequentially.

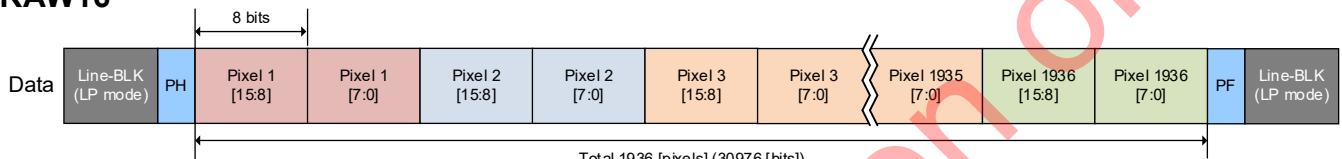
RAW12



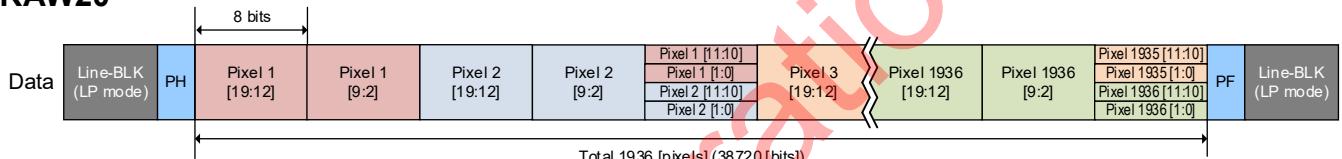
RAW14



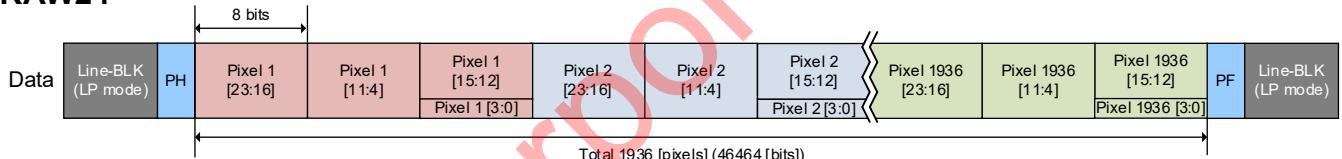
RAW16



RAW20



RAW24



RAW12x4

RAW12x2

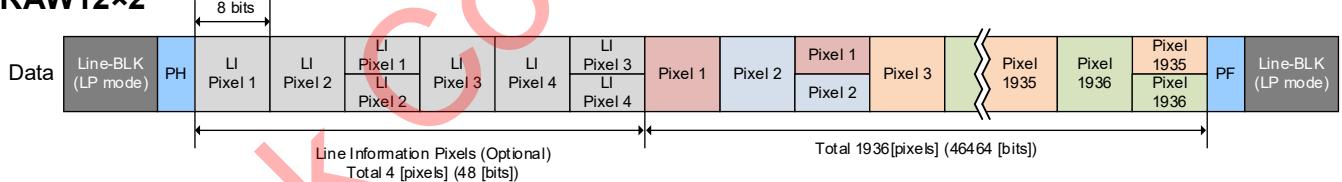


Figure 2-10 MIPI CSI-2 Output Format (RAW)

"Figure 2-11" illustrates the bit assignment of the formats of RAW12, RAW14, RAW16, RAW20 and RAW24.

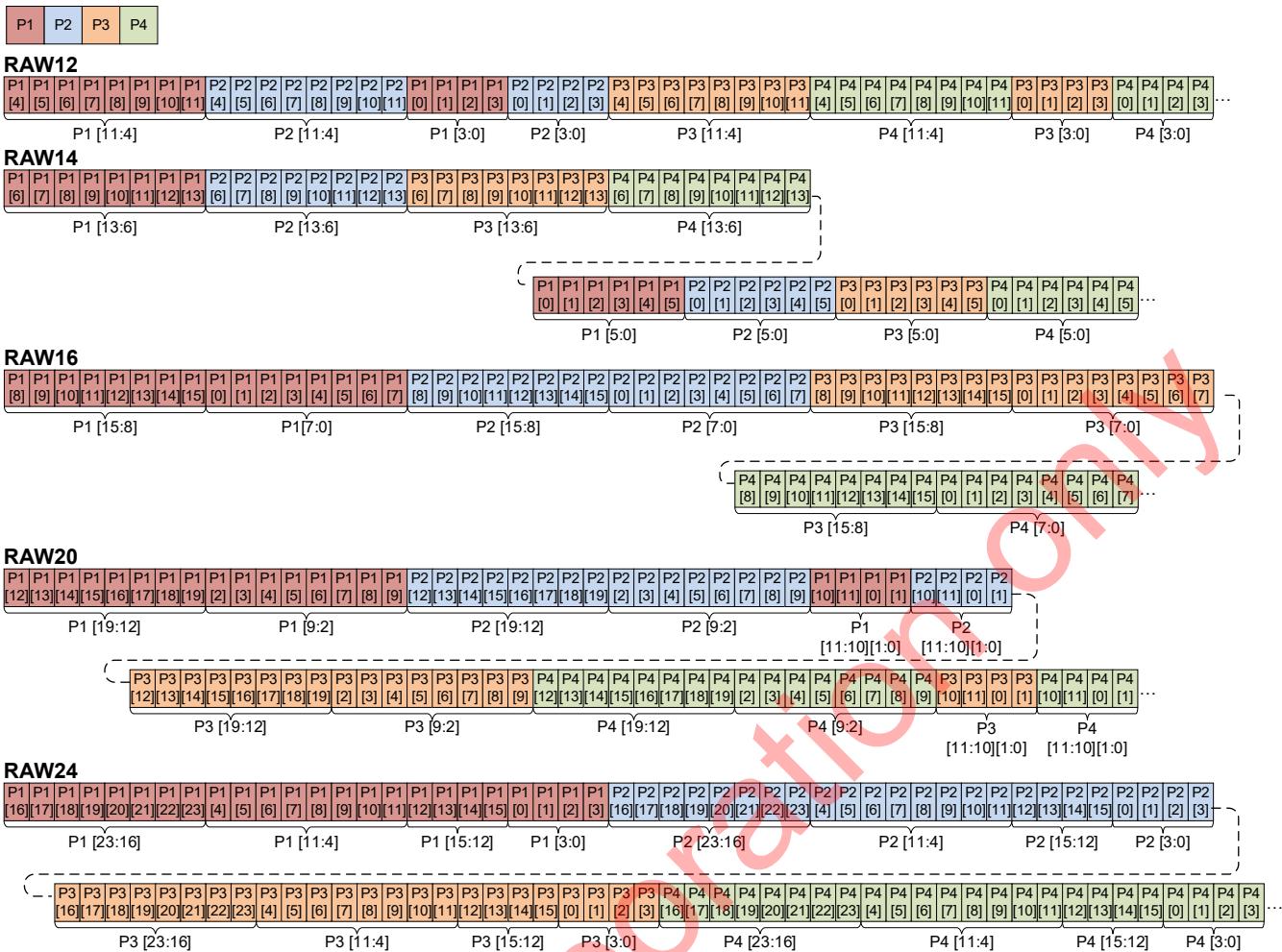


Figure 2-11 Bit Assignment in MIPI CSI-2 Output (RAW)

Table 2-39 Frame Structure-Related Register

[CONST1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x01F0	1	1:0	IR_IS_ALP_OB_SEL	R/W	U2.0	<p>This register is used to select one of the four signal lines that is transmitted as sensor's OB Area.</p> <p>This register is enabled only in HDR (UC) mode or HDR (PWL) mode.</p> <p>0: SP1_HCG 1: SP1_LCG 2: SP2H 3: SP2L</p>

Chapter 3 Setting Registers via Serial Communication

This chapter explains how to change the sensor's settings by the host.

- An overview of the sensor's registers for configuring the settings
- A method for reading from or writing to the sensor's registers and the Serial NOR Flash device (I²C communication method)
- Points to note regarding communication timings

3.1. Register Structure

3.1.1. Register Categories

The sensor's registers are classified into categories for each function. In addition, refer to the IMX623-AA** "Register Map" since this document contains a list of registers for each category.

◆ Note

For details regarding the register addresses in the case of I²C communication, refer to ["3.2.1 Register Address in the Case of I²C Communication."](#)

Regarding the addresses as described in the IMX623-AA** "Register Map" under the following conditions, be sure to exactly configure the settings in accordance with the IMX623-AA** "Register Configuration File" provided separately by SSS.

- An address which is indicated as RESERVED in the IMX623-AA** "Register Map"
- An address which is not specified in the IMX623-AA** "Register Map"

Some of the aforementioned registers include the registers, the value of which changes corresponding to the settings of the IMX623-AA** "Register Configuration File" or other registers.

◆ Memo

The region of the category name **USER** contains 1,024 bytes where the host can store desired values.

Table 3-1 List of Register Categories

Category Name	R/W
CONST1	R/W
CTRL1	R/W
MODE1	R/W
SM_CONST	R/W
SM_STATE	R
STATE	R
VERSION	R
SYS_COM	R
SYS_SOUT	R
AE_COM	R
AE_HDR_COM	R
HDR_COM	R
AWB_COM	R

Category Name	R/W
PICT_STC OTP_COM	R
VIF_COM	R
OTP_COM	R
SM	R
SETUP	R/W
CMD_TRG	R/W
CONFIG	R/W
CMN	R/W
SYS_CTRL	R/W
SG_CTRL	R/W
IO_CFG	R/W
SCENE_CFG	R/W
SCENE_DATA	R/W

Category Name	R/W
AE	R/W
AE_DGRM	R/W
AE_FLC	R/W
AE_FRM	R/W
AE_OPD	R/W
AE_HDR	R/W
HDR	R/W
PWL	R/W
AWB	R/W
AWB_FRM	R/W
AWB_OPD	R/W
AWB_ADJ	R/W
PICT_CTRL	R/W
PICT_INTERLOCKTYPE	R/W
PICT_OB	R/W

Category Name	R/W
PICT_STC	R/W
PICT_STC_PIX	R/W
PICT_DYC	R/W
PICT_RAWNR	R/W
PICT_SPSHD	R/W
PICT_SHD	R/W
VIF	R/W
SM_CFG	R/W
OTP	R/W
USER	R/W
FW_MODE_SENS	R/W
FW_MODE_POST	R/W
OTP_WRITE	R/W
PICT_SPSHD_GAIN OTP	R/W

3.1.2. Remap Mode

The sensor's registers and addresses are linked with each Remap Mode ID number. The accessible registers can be changed by changing the Remap Mode ID number.

"Figure 3-1" illustrates an overview of the Remap Mode.

Remap Mode A		Remap Mode B		Remap Mode C	
0x0000	Register A	0x0000	Register A	0x0000	Register A
0x0001	Register B	0x0001	Register B	0x0001	Register B
0x0002	Register C	0x0002	Register C	0x0002	Register C
0x0003	Register D	0x0003	–	0x0003	–
0x0004	Register E	0x0004	–	0x0004	Register X
0x0005	Register F	0x0005	–	0x0005	Register Y
0x0006	Register G	0x0006	Register G	0x0006	Register Z

Figure 3-1 An Overview of the Remap Mode

Set the Remap Mode ID number in order for the host to communicate with the sensor or to use the functions of the sensor. "Table 3-2" lists the Remap Mode ID numbers.

Table 3-2 List of the Remap Mode ID Numbers

Remap Mode ID Number	Overview
0x00	This is the mode ID number, by which the host accesses the registers, which can be set while the sensor is in Start-up State. When this ID number is set, these registers are automatically set after the sensor has transitioned to Start-up State.
0x01	This is the mode ID number, by which the host accesses the registers, which can be set while the sensor is in Start-up State. Use this ID number to access certain registers for the Pixel Shading Compensation function.
0x02	This is the mode ID number, by which the host accesses the registers, which can be set while the sensor is in Start-up State. When this ID number is set, certain registers that can be accessed in the mode ID number 0x00 are restricted. For normal use, no settings are required.
0x04	This is the mode ID number, by which the host accesses the registers, which can be set while the sensor is in Streaming State.
0x05	This is the mode ID number, by which the host accesses the registers, which can be set while the sensor is in Streaming State. Use this ID number to access certain registers for the Pixel Shading Compensation function. This ID number is automatically set after the sensor has transitioned to Streaming State.
0x06	This is the mode ID number, by which the host accesses the registers, which can be set while the sensor is in Streaming State. When this ID number is set, certain registers that can be accessed in the mode ID number 0x05 are restricted. For normal use, no settings are required.
0x20	This is the mode ID number, by which the host accesses the registers, which can be set while the sensor is in Sleep State. This ID number is automatically set when the sensor has transitioned to Sleep State.
0x30 to 0x36	Use these ID numbers to access HW registers for certain functions of the sensor.

For details regarding the Remap Mode ID numbers that are used to access the registers of the sensor, refer to the IMX623-AA** Register Map.

3.1.3. Access to Registers

Access to the registers of the sensor is available via the I²C interface. For details regarding the I²C interface, refer to “**3.2 I²C Communication.**”

The register addresses of the sensor which are specified by the host in the case of I²C communication varies corresponding to the selection of the Remap Mode. For details, refer to “**3.2.1 Register Address in the Case of I²C Communication.**”

To communicate with the sensor, set the address and value of a register. For example, when the host sets the registers in “**Figure 3-2**” to the following values:

REG_1 = 0x4

(Address: 0x0120 [3:0] = 0x4)

REG_2 = 0x23

(Address: 0x0121 [3:0] = 0x2, Address: 0x0120 [7:4] = 0x3)

REG_3 = 0x1

(Address: 0x0121 [7:4] = 0x1)

and when setting these values via I²C communication, set each value in bytes as follows:

0x0120 = 0x34

0x0121 = 0x12

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address 0x0120		REG_3			REG_2				REG_1						

Figure 3-2 Example of Setting a Register

3.1.4. Precision of Register Values

Depending on the use of signs (signed or unsigned) or the resolution of the user-set value, the precision of a register value is represented as follows:

U4.3: Unsigned

U4.3 represents the 4-digit integer part and 3-digit fractional part in 7 bits.

One LSB is 0.125, representing a number from 0 to 15.875.

S4.3: Signed

S4.3 represents the signed 1-digit part, 4-digit integer part and 3-digit fractional part in 8 bits in two's complement.

One LSB is 0.125, representing a number from -16 to 15.875.

Examples are as follows:

- When setting 1.5 to U4.3, set 0xC because 1.5 is 0001.100 in binary.
- When setting 1.5 to S4.3, set 0xC in the same way as U4.3.
- When setting -1.5 to S4.3, set 0xF4 because -1.5 is 11110.100 in binary.

3.1.5. Application Lock Function

Regarding the registers that may significantly affect output images in the case of incorrect settings by the host, they are duplicated for redundancy to prevent malfunctions. The Application Lock function consists of the following two methods:

- Duplicate Register method
While the sensor is in Streaming State, this function compares the value of each duplicate register. A user-set value is applied only when these values are the same. To change the value of any register controlled by the Application Lock function, set the same value to the register to be compared.
- Lock Key method
A user-set value will be applied only when the Lock/Unlock register is set to the unlock code while the sensor is in Start-up or Streaming State. To change the value of a register controlled by the Application Lock function, set this register to the unlock code.

“Table 3-3” shows the registers controlled by the Application Lock function.

Table 3-3 Registers Controlled by the Application Lock Function

Duplicate Register method

Function	Register Controlled by the Application Lock Function	Register to Be Compared
“2.3.1 List of Drive Modes”	OUTMODE_ RAWOUTMODE_	OUTMODE_APL RAWOUTMODE_APL
“2.3.2 Mode Transition Between the Drive Modes”	HDRON_	HDRON_APL
“2.3.3 Switching the Output Lines in HDR (Line/Line)”	OUTSEL_1_ OUTSEL_2_ OUTSEL_3_ OUTSEL_4_	OUTSEL_1_APL OUTSEL_2_APL OUTSEL_3_APL OUTSEL_4_APL
“6.1 Sync Function”	SG_MODE_	SG_MODE_APL
“6.2 Optical Center Compensation Function”	WND_SHIFT_H_ WND_SHIFT_V_	WND_SHIFT_H_APL WND_SHIFT_V_APL
“6.3 Horizontal/Vertical Flip Function”	H_REVERSE_ V_REVERSE_	H_REVERSE_APL V_REVERSE_APL
“6.4 Crop Function”	DCROP_ON_ DCROP_HOFFSET_ DCROP_HSIZE_ DCROP_VOFFSET_ DCROP_VSIZE_	DCROP_ON_APL DCROP_HOFFSET_APL DCROP_HSIZE_APL DCROP_VOFFSET_APL DCROP_VSIZE_APL
“6.5 First Pixel Color Selection Function”	LID_ BID_ OBBID_	LID_APL BID_APL OBBID_APL
“6.8 Output Mask Function”	INIT_MASK_CNT_ MUTE_CNT_ VID_DATA_MASK_EN_ VID_VALID_MASK_EN_ INIT_MUTE_DATA_MASK_EN_ INIT_MUTE_VALID_MASK_EN_	INIT_MASK_CNT_APL MUTE_CNT_APL VID_DATA_MASK_EN_APL VID_VALID_MASK_EN_APL INIT_MUTE_DATA_MASK_EN_APL INIT_MUTE_VALID_MASK_EN_APL
“7.1 PG Image Output Function”	DIF_PG_EN_	DIF_PG_EN_APL
“7.2 Light Metering Window Overlay Function”	OPO_BYPASS_	OPO_BYPASS_APL

Lock Key method

Section	Register Controlled by the Application Lock Function	Lock/Unlock Register	Unlock Code
"4.2 Setting the Drive Mode"	MODE_SET_F	MODE_SET_F_LOCK	0x53
"4.1 The States of the Sensor"	BIST_ENTRY	BIST_LOCK	0xA3
	SLEEP_REQ	SLEEP_REQ_LOCK	0xC3
	TEMP_CALC_REQ	TEMP_CALC_REQ_LOCK	0x3C

For details, refer to the chapters shown in the "Function" column of "**Table 3-3.**"

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3.2. I²C Communication

"Figure 3-3" illustrates the connection diagram in the case of I²C communication. In addition, "Table 3-4" describes the pins used for I²C communication. The sensor's I²C communication supports Standard mode, Fast mode and Fast mode Plus. For details, refer to the following specifications:

- UM10204, I²C-bus specification and user manual, Revision 6

◆ Note

The sensor does not support a multi-master system.

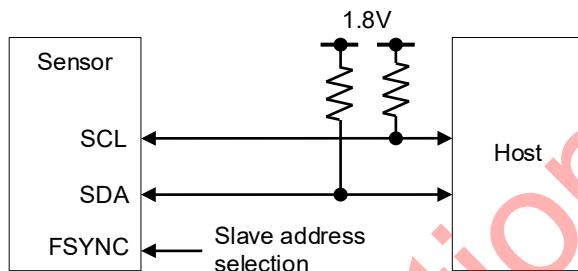


Figure 3-3 I²C Connection

Table 3-4 I²C Communication Pins

Pin Name	Description
SCL	Clock input/output for I ² C communication
SDA	Data input/output for I ² C communication
FSYNC	Selection of a slave address

The FSYNC pin is used to select a slave address by the Reset Configuration function. For details, refer to "3.3 Slave Address."

"Table 3-5" describes the communication specifications of the sensor.

Table 3-5 I²C Communication Specifications

Specifications	
Slave Address	7-bit address (Refer to "3.3 Slave Address.")
SCL Clock	100 kHz (Standard mode)
	400 kHz (Fast mode)
	1000 kHz (Fast-mode Plus)

3.2.1. Register Address in the Case of I²C Communication

Set the following to access a register of the sensor via I²C communication.

- The regional allocation of a register (Remap Mode)
- A register address

The regional allocation of the sensor's register varies corresponding to the value specified by the host in Remap Mode.

For details regarding the I²C address of each register corresponding to the Remap Mode, refer to the IMX623-AA** "Register Map."

◇ **Memo**

For details regarding the communication protocol to access the register and the request format for the sensor, refer to "**3.5 Communication Protocols**."

3.3. Slave Address

The sensor communicates using a 7-bit slave address. The user can set the slave address using the pins and registers shown in “[Figure 3-4](#).”

In “[Figure 3-4](#),” the red and blue names represent pins and registers respectively. The initial value of the register is shown in the brackets following each register name.

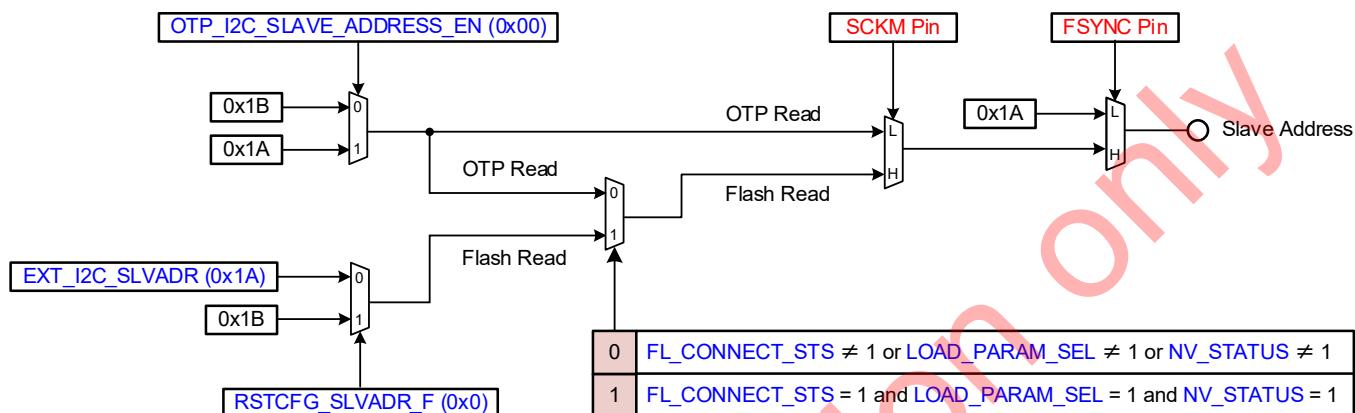


Figure 3-4 How to Set a Slave Address

The sensor’s slave address is selected by the Reset Configuration function. Therefore, it cannot be changed after the sensor’s startup.

To set the slave address to a desired value, change the relevant register values, update the Serial NOR Flash device and then reset the sensor.

◆ **Note**

- When setting the slave address of the sensor to 0x1A regardless of the state of the FSYNC pin by using the Reset Configuration function, be sure to use either of the aforementioned methods.

For details, refer to “[2.1.5 Reset Configuration](#).”

Table 3-6 Slave Address-Related Registers

[CONFIG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A54	1	6:0	EXT_I2C_SLVADR	R/W	U7.0	This register is used to set the slave address and is valid when the value of the RSTCFG_SLVADR_F register is 0.
		7	RSTCFG_SLVADR_F	R/W	U1.0	This register is used to enable or disable the value of the EXT_I2C_SLVADR register. 0: Enabled 1: Disabled

[OTP]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBFD0	1	7:0	OTP_I2C_SLAVE_ADDRESS_EN	R/W	U8.0	This register is used to enable or disable the value of the OTP_I2C_SLAVE_ADDRESS register. 0: Disabled 1: Enabled

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3.4. Communication Responses

In the case of I²C communication, the sensor generates an Acknowledge or Negative Acknowledge as a response. “Table 3-7” shows the conditions under which the sensor generates a Negative Acknowledge. For the conditions under which the sensor transitions to a busy state, refer to “Table 3-8.”

The sensor can execute clock stretching under the conditions represented by ✓ in the Clock Stretch column, instead of generating a Negative Acknowledge. For details, refer to “3.4.1 Clock Stretching.” The host can change the sensor to generate an Acknowledge under the conditions represented by ✓ in the Response Mode column. For details, refer to “3.4.2 Response Mode.” Regarding the position of an Acknowledge or Negative Acknowledge, also see “Figure 3-5.”

Table 3-7 The Sensor’s Negative Acknowledge Generating Conditions

Negative Acknowledge-Generating Conditions	Clock Stretching	Response Mode	Negative Acknowledge Position
Slave addresses are different.	-	-	Indicated in the red circle in “Figure 3-5” (A).
The sensor is in a busy state.	✓	-	Indicated in the red circle in “Figure 3-5” (A).
The host has specified a non-existent address.	-	-	Indicated in the red circle in “Figure 3-5” (B).
The host has specified the address of a read-only register. • Even when the sensor generates a Negative Acknowledge, the sensor can read an existing register’s value.	-	✓	Indicated in the red circle in “Figure 3-5” (B).
The sensor has written to an existing address and there is no subsequent address. • Even when the sensor generates a Negative Acknowledge, the sensor has successfully written data to the specified address.	-	✓	Indicated in the red circle in “Figure 3-5” (C).
The subsequent address after an existing address is the address for a Read Only register. • Even when the sensor generates a Negative Acknowledge, the sensor can read an existing register’s value.	-	✓	Indicated in the red circle in “Figure 3-5” (C).
Setting the INCK frequency via I ² C communication is in progress.	-	-	Indicated in the red circle in “Figure 3-5” (C).
The host communicates with the sensor by specifying a command.	-	✓	Indicated in the red circle in “Figure 3-5” (D).
The host receives the Message Counter information.	-	✓	Indicated in the red circle in “Figure 3-5” (E).

Table 3-8 Conditions for the Sensor Transitioning to a Busy State

Conditions	Remarks
The MODE_SET_F register is set.	“4.1 The States of the Sensor”
Transition to “Safe State Mode” State	“4.1 The States of the Sensor” Refer to the IMX623-AA** “Safety Application Note.”
The OTP_WRITE_START register is set.	Refer to “6.10.3.2 The Method for Writing a Value to the OTP ROM.”
The ECM_UPDATE_FLAG register is set.	Refer to the IMX623-AA** “Safety Application Note.”
The BIST_x (x = ENTRY, STANDBY, ACTIVATE_ERROR) registers are set.	“4.1 The States of the Sensor” Refer to the IMX623-AA** “Safety Application Note.”
The FLASH_STS_x (x = SET_F, GET_F) registers are set.	Refer to “2.2.1 Updating Function for the Serial NOR Flash Device’s Status Register.”

Conditions	Remarks
The SLEEP_REQ register is set.	Refer to "4.6 Sleep Sequence."
The TEMP_CALC_REQ register is set.	Refer to "4.5.1 STBY-TMPR Sequence."
The CHNG_TRANS_MODE register is set.	Refer to the IMX623-AA** "Safety Application Note."
The INCK frequency is set via I ² C communication.	"2.1.5.1 Setting the Master Clock Frequency"
The Serial NOR Flash Write subcommand is executed.	Refer to "3.5.1.3.3 Serial NOR Flash Write Subcommand."
The Serial NOR Flash Read subcommand is executed.	Refer to "3.5.1.3.4 Serial NOR Flash Read Subcommand."
The Serial NOR Flash Sector Erase subcommand is executed.	Refer to "3.5.1.3.2 Serial NOR Flash Sector Erase Subcommand."

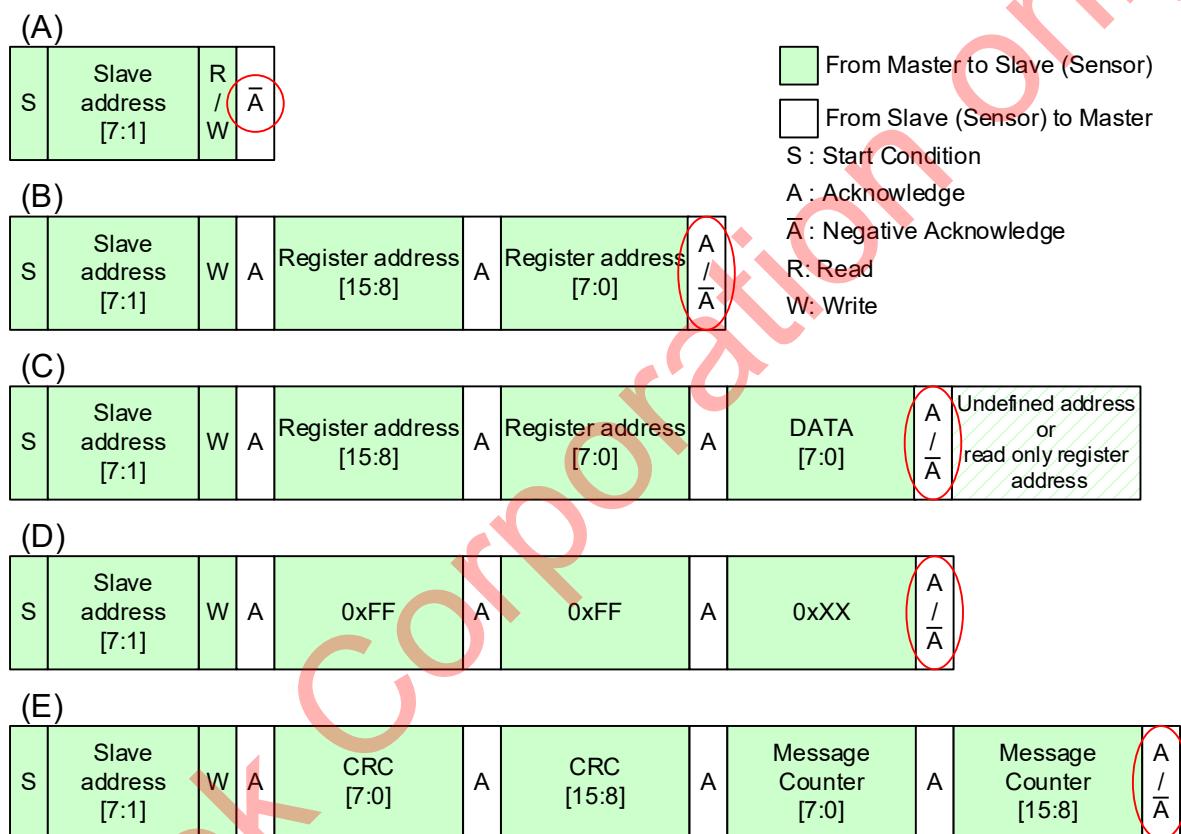


Figure 3-5 The Position Where a Negative Acknowledge Is Generated by the Sensor

◆ Memo

- For details regarding communication with specified commands, refer to "3.5.1 List of Commands and Subcommands."
- For details regarding the Message Counter, refer to the IMX623-AA** "Safety Application Note."

3.4.1. Clock Stretching

As illustrated in “**Figure 3-6**,” the host can select whether to enable or disable the sensor’s clock stretching. In “**Figure 3-6**,” the blue and red names represent register names and the state of the Reset Configuration pins, respectively. The value in the brackets following each register name is the initial value of each register.

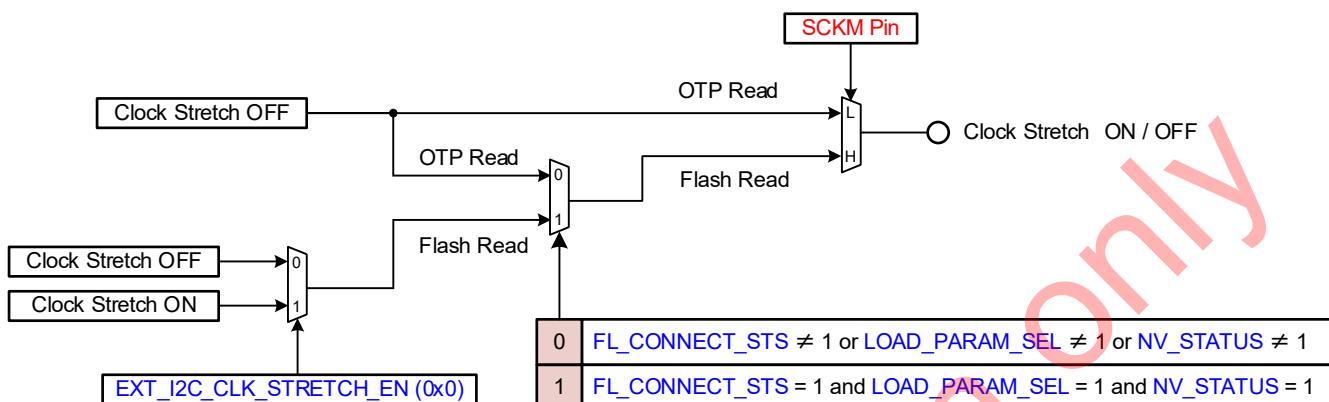


Figure 3-6 Setting Clock Stretching

◆ **Note**

When a Serial NOR Flash device is not used, clock stretching cannot be enabled.

When clock stretching is enabled, the sensor executes clock stretching under the conditions shown in “**Table 3-9**,” instead of generating a Negative Acknowledge.

Table 3-9 Conditions Under Which the Sensor Executes Clock Stretching

Conditions
The sensor is in a busy state.

“**Figure 3-7**” illustrates an example when the sensor executes clock stretching.

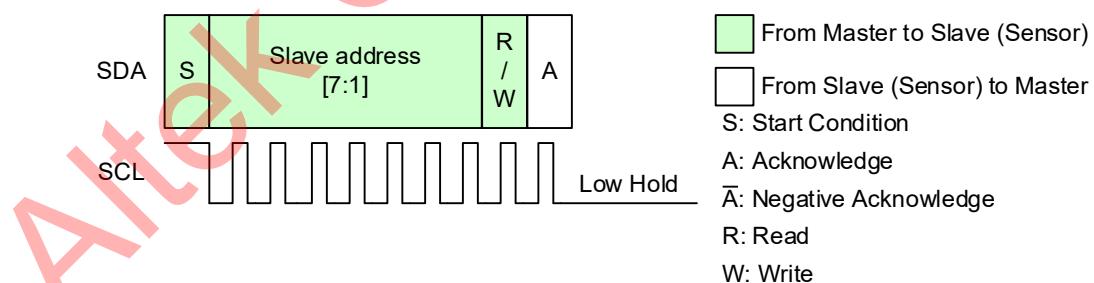


Figure 3-7 Example of Clock Stretching

Table 3-10 The Register Used to Set Clock Stretching

[CONFIG]

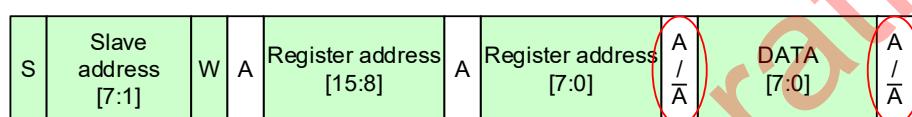
Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A55	1	1	EXT_I2C_CLK_STRETCH_EN	R/W	U1.0	This register is used to enable or disable clock stretching. 0: Disabled 1: Enabled

3.4.2. Response Mode

The sensor generates either a Negative Acknowledge or Acknowledge corresponding to the sensor's response mode under the conditions in “**Table 3-11.**” Regarding the position that can be changed corresponding to the response mode, see “**Figure 3-8.**”

Table 3-11 The Sensor's Response Corresponding to the Response Mode

Conditions	The Sensor's Response Mode	
	NACK Response Mode	ACK Response Mode
The host has specified the address of a read-only register.	Generates a Negative Acknowledge.	Generates an Acknowledge.
The sensor has written to an existing address and there is no subsequent address.		
The subsequent address after an existing address is the address for a Read Only register.		
The host communicates with the sensor by specifying a command.		
The host receives the Message Counter information.		



- From Master to Slave (Sensor)
- From Slave (Sensor) to Master
- S: Start Condition
- A: Acknowledge
- \bar{A} : Negative Acknowledge
- R: Read
- W: Write

Figure 3-8 Acknowledge/Negative Acknowledge Generating Positions That Can Be Changed Corresponding to the Response Mode

“**Figure 3-9**” illustrates how the response mode is selected. In “**Figure 3-9**,” the red and blue names represent pins and registers respectively. The initial value of the register is shown in the brackets following each register name.

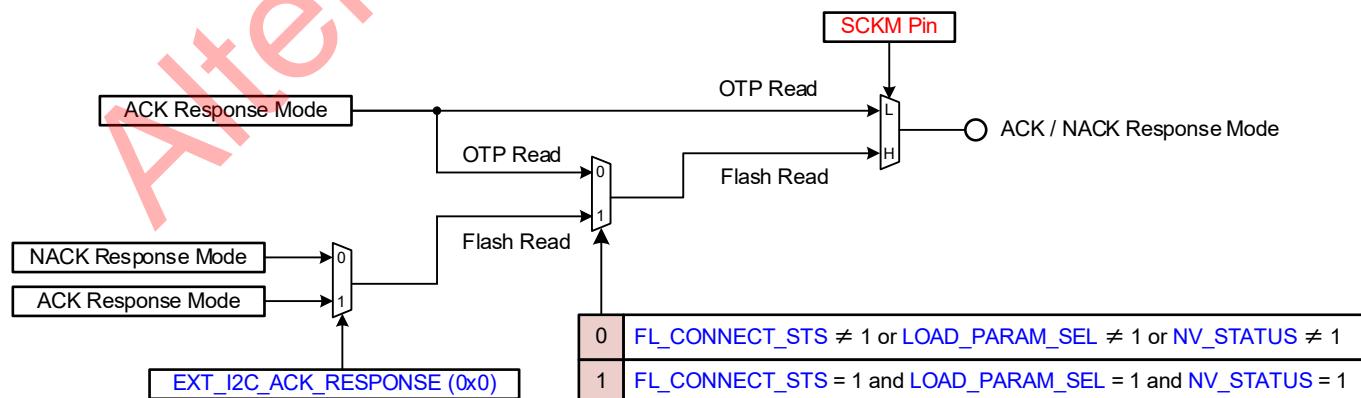


Figure 3-9 The Selection of the Sensor's Response Mode

◆ Note

When a Serial NOR Flash device is not used, any response mode cannot be selected.

Table 3-12 Response Mode-Related Registers

[CONFIG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A55	1	2	EXT_I2C_ACK_RESP ONSE	R/W	U1.0	This register is used to set the sensor's response mode. 0: NACK Response Mode 1: ACK Response Mode

3.4.3. The Sensor's Undefined Regions

The regions, where the sensor's registers do not exist (undefined regions), vary corresponding to the Remap Mode. “**Table 3-13**” shows these undefined regions corresponding to the Remap Mode. The register addresses not listed in the “Undefined Region” column are the regions, where registers are defined.

Table 3-13 The Sensor's Undefined Regions

Register Address	Remap Mode	Undefined Region	
		Start Address	End Address
0x0000 to 0x5FFF	0x00, 0x01, 0x02, 0x20	0x0030	0x003F
		0x0128	0x013F
		0x0228	0x023F
		0x1AB0	0x1ABF
		0x1DF4	0x1DFF
		0x1E2C	0x1E3F
		0x1E6C	0x1E7F
		0x1F04	0x1F3F
		0x2234	0x223F
		0x2714	0x273F
	0x04, 0x05, 0x06	0x28EC	0x5FFF
		0x0000	0x1ABF
		0x1DF4	0x1E3F
		0x1E6C	0x1E7F
0x6000 to 0xCBFF	0x00, 0x01, 0x02, 0x04, 0x05, 0x06 0x20	0x1F04	0x1F3F
		0x2234	0x273F
		0x28EC	0x5FFF
		0x88A0	0x89FF
		0x8A04	0x8A0F
	0x20	0x8A20	0x8A3F
		0xC4A8	0xCBFF
		0x6088	0x89FF
		0x8A04	0x8A0F
		0x8A20	0x8A3F
0xCC00 to 0xFFFF	0x00, 0x04	0xC4A8	0xCBFF
		0xD590	0xD7FF
	0x01, 0x05	0xD910	0xFFFFE
		0xD590	0xD7FF
	0x02, 0x06	0xF6F0	0xFFFFE
		0xD5F4	0xD5FF
		0xFE2C	0xFFFFE
	0x20	0xCC00	0xFFFFE

As shown in “**Table 3-7**,” if the sensor writes to an address where a register exists and if the subsequent address does not exist, the sensor generates a Negative Acknowledge.

3.5. Communication Protocols

The host can communicate with the sensor using relevant commands to enable or disable access to the Serial NOR Flash device or switch the access target. The host can also use subcommands to read, write, or erase data at an address.

3.5.1. List of Commands and Subcommands

“Table 3-14” lists the commands available for the sensor. **“Table 3-15”** and **“Table 3-16”** list the subcommands available after switching the sensor’s communication targets using the commands.

Table 3-14 List of Commands

Command	Description
Serial NOR Flash Access Lock Command	This command enables or disables access to the Serial NOR Flash device. When the access lock is enabled, the sensor cannot perform a read, write, or Sector-Erase operation.
Serial NOR Flash All Write Command	This command writes register's data to the Serial NOR Flash device.
Serial NOR Flash Access Command	This command switches the sensor's communication target to the Serial NOR Flash device.
Register Access Command	This command switches the sensor's communication target to the register or switches the Remap Mode ID numbers. For details regarding the Remap Mode, refer to “3.2.1 Register Address in the Case of I²C Communication” and the IMX623-AA** “Register Map.”

Table 3-15 List of Executable Subcommands When the Sensor's Communication Target Is the Serial NOR Flash Device

Subcommand	Description
Serial NOR Flash Sector Erase Subcommand	This subcommand erases data in the sector including the specified address of the Serial NOR Flash device.
Serial NOR Flash Write Subcommand	This subcommand writes data to the specified address of the Serial NOR Flash device.
Serial NOR Flash Read Subcommand	This subcommand reads out data from the specified address of the Serial NOR Flash device.

Table 3-16 List of Executable Subcommands When the Sensor's Communication Target Is the Sensor's Registers

Subcommand	Description
Register Write Subcommand	This subcommand writes data to the specified register's address.
Register Read Subcommand	This subcommand reads out data from the specified register's address.

◆ Memo

When access to the Serial NOR Flash device is disabled, the sensor does not perform any processing even if the following commands and subcommands are issued to the sensor:

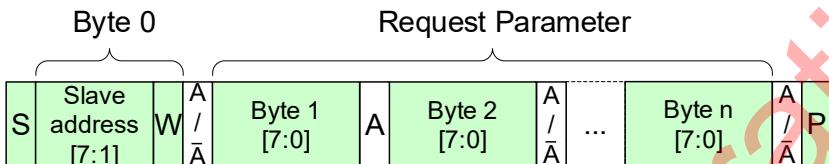
- Serial NOR Flash All Write Command
- Serial NOR Flash Access Command
- Serial NOR Flash Sector Erase Subcommand
- Serial NOR Flash Write Subcommand
- Serial NOR Flash Read Subcommand

◆ Note

Execute each subcommand after switching the sensor's communication targets.

For example, to write data to the Serial NOR Flash device, execute the Serial NOR Flash Access command before executing the Serial NOR Flash Write subcommand.

"Figure 3-10" illustrates an example of the I²C communication protocols to communicate with the sensor.

Request (Host -> Sensor)

From Master to Slave (Sensor)

From Slave (Sensor) to Master

S: Start Condition

P: Stop Condition

A: Acknowledge

Ā: Negative Acknowledge

R: Read Access Bit

W: Write Access Bit

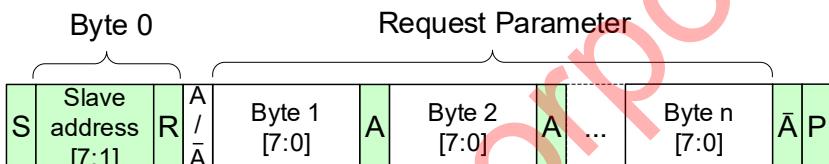
Response (Sensor -> Host)

Figure 3-10 Example of Command Data Communication

1. Start communication with the sensor by issuing a Start Condition.
2. Issue a slave address and either the Read Access Bit or Write Access Bit.
In the case of the Write Access Bit, send the value as shown in **"Table 3-17"** corresponding to the command or subcommand to be executed.
In the case of the Read Access Bit, send an Acknowledge or a Negative Acknowledge corresponding to the amount of data which the host receives.
3. To finish communication with the sensor, issue a Stop Condition.

Table 3-17 Simplified Communication Packet Table

* Command

Command	Byte 0	Byte 1	Byte 2	Byte 3
Serial NOR Flash Access Lock Command (Enable)	SL (W)	0xFF	0xFF	0xF5
Serial NOR Flash Access Lock Command (Disable)	SL (W)	0xFF	0xFF	0xF4
Serial NOR Flash All Write Command	SL (W)	0xFF	0xFF	0xFF
Serial NOR Flash Access Command	SL (W)	0xFF	0xFF	0xF7
Register Access Command	SL (W)	0xFF	0xFF	Remap Mode

* List of executable subcommands when the sensor's communication target is the Serial NOR Flash device

Subcommand	Byte 0	Byte 1	Byte 2	Byte 3
Serial NOR Flash Sector Erase Subcommand ^{*1}	SL (W)	0x80	0x00	0x03
Serial NOR Flash Write Subcommand ^{*1}	SL (W)	0x80	0x00	0x02
Serial NOR Flash Read Subcommand ^{*1}	SL (W)	0x80	0x00	0x01

* 1: Setting the subcommand is required before executing it.
For details, refer to "**3.5.1.3.1 Setting a Subcommand**".

* List of executable subcommands when the sensor's communication target is the sensor's registers

Subcommand	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	...
Register Write Subcommand	SL (W)	ADDRESS [15:8]	ADDRESS [7:0]	WR [0] - WR [n]		
Register Read Subcommand (Request)	SL (W)	ADDRESS [15:8]	ADDRESS [7:0]		-	
Register Read Subcommand (Response)	SL (R)			RD [0] - RD [n]		

SL (W) = a 7-bit slave address + a Write Access Bit

SL (R) = a 7-bit slave address + a Read Access Bit

WR [0] - WR [n]: Data to write (n ≤ 255)

RD [0] - RD [n]: The data to be read (n ≤ 255)

The accessible register can be changed by setting the value of the Remap Mode. Refer to the IMX623-AA** "Register Map" to check accessible registers to the host corresponding to the value of the Remap Mode.

3.5.1.1. Serial NOR Flash Access Lock Command

The user can disable access to the Serial NOR Flash device to prevent any data corruption due to unauthorized access to the device. “Figure 3-11” and “Figure 3-12” illustrate the request formats.

Serial NOR Flash access lock request (Host -> Sensor)

S	Slave address [7:1]	W	A / \bar{A}	0xFF	A	0xFF	A / \bar{A}	0xF5	A / \bar{A}	P
---	------------------------	---	---------------	------	---	------	---------------	------	---------------	---

Figure 3-11 The Request Format for the Serial NOR Flash Access Lock (Enable) Command

Serial NOR Flash access unlock request (Host -> Sensor)

S	Slave address [7:1]	W	A / \bar{A}	0xFF	A	0xFF	A / \bar{A}	0xF4	A / \bar{A}	P
---	------------------------	---	---------------	------	---	------	---------------	------	---------------	---

Figure 3-12 The Request Format for the Serial NOR Flash Access Lock (Disable) Command

◆ Note

The Serial NOR Flash Access Lock mechanism is designed to prevent the sensor from inadvertently accessing the Serial NOR Flash device. This mechanism cannot be used to prevent other devices from accessing the Serial NOR Flash device.

◇ Memo

- When the access lock is enabled, the sensor cannot perform a read, write or erase operation on the Serial NOR Flash device. To access the Serial NOR Flash device, enable access to the Serial NOR Flash device using this command.
- Use the FL_ACCESS_SEL register to check whether access to the Serial NOR Flash device is disabled.

3.5.1.2. Serial NOR Flash All Write Command

When changing a register's value and to save this value to the Serial NOR Flash device, use the Serial NOR Flash All Write command. “Figure 3-13” illustrates the request format for the Serial NOR Flash Access command.

Serial NOR Flash all write request (Host -> Sensor)

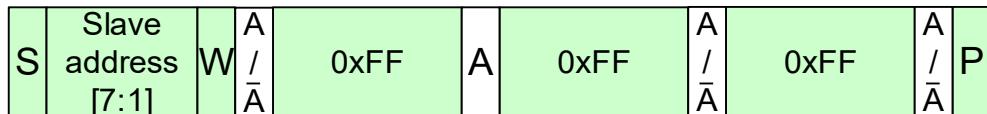


Figure 3-13 The Request Format for the Serial NOR Flash All Write Command

◇ Memo

- The Serial NOR Flash All Write command rewrites the data in the 4-Mbit region used by the sensor. When rewriting the data in other regions, refer to “[3.5.1.3.3 Serial NOR Flash Write Subcommand](#).”
- To execute this command, first enable access to the Serial NOR Flash device.

3.5.1.3. Serial NOR Flash Access Command

This command switches the sensor's communication target to the Serial NOR Flash device. “Figure 3-14” illustrates the request format.

Serial NOR Flash access request (Host -> Sensor)

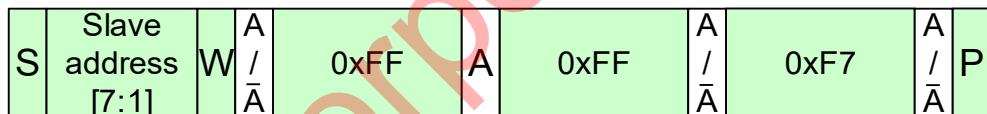


Figure 3-14 The Request Format for the Serial NOR Flash Access Command

◇ Memo

- To execute this command, first enable access to the Serial NOR Flash device.

3.5.1.3.1. Setting a Subcommand

The subcommands can be set after switching the sensor's communication target to the Serial NOR Flash device. To set a subcommand, set data in the addresses ranging from 0x8000 to 0x8005. “Figure 3-15” illustrates the data format to set a subcommand. “Table 3-18” lists the data to be transferred.

“Subcommand setting” request (Host -> Sensor)

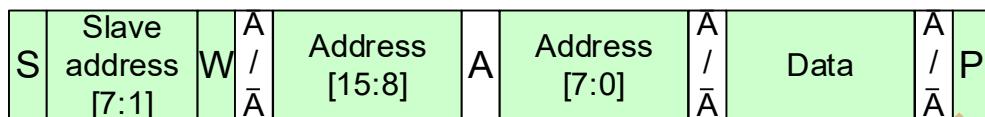


Figure 3-15 The Request Format for Setting a Subcommand

Table 3-18 List of the Data Used to Set a Subcommand

Settings	Address [15:8]	Address [7:0]	Data
Selection of a subcommand	0x80	0x00	0x01: Serial NOR Flash Read 0x02: Serial NOR Flash Write 0x03: Serial NOR Flash Sector Erase
Address setting of the Serial NOR Flash device [31:24]	0x80	0x01	ADDRESS [31:24]
Address settings of the Serial NOR Flash device [23:16]	0x80	0x02	ADDRESS [23:16]
Address settings of the Serial NOR Flash device [15:8]	0x80	0x03	ADDRESS [15:8]
Address settings of the Serial NOR Flash device [7:0]	0x80	0x04	ADDRESS [7:0]
Execution of a subcommand	0x80	0x05	0x5A

◆ Note

To execute a subcommand, select a subcommand and then set the Serial NOR Flash device's address.

In the case of the Serial NOR Flash Read and Write operations, the sensor uses its buffer for a data transaction with the Serial NOR Flash device. The buffer's region is allocated in the addresses ranging from 0x0000 to 0x00FF with the size of 256 bytes.

“Figure 3-16” and “Figure 3-17” illustrate the data format to read from or write to the buffer. To access the buffer, set the Buffer Address to the start address. “Figure 3-17” illustrates two patterns of request formats to issue a Stop Condition (P) and a Repeat Start Condition (Sr).

Buffer write request (Host -> Sensor)

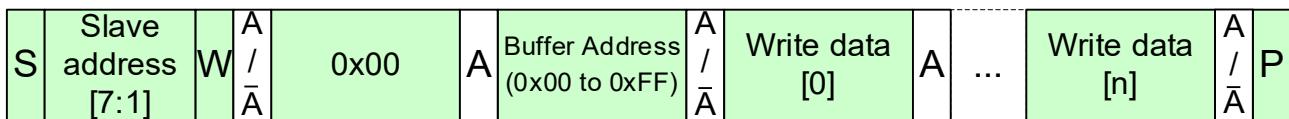
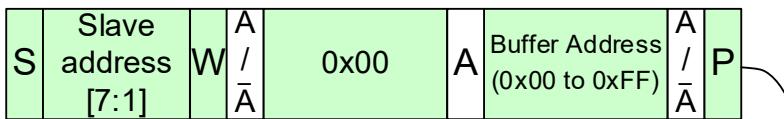


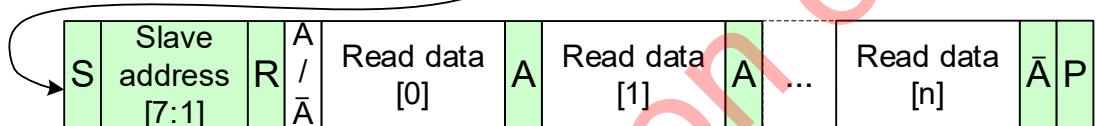
Figure 3-16 Request Format for Writing Data to the Buffer

Buffer read request (Host -> Sensor)

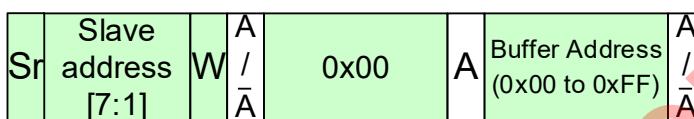
Sr: Repeated Start Condition



Serial NOR Flash read response (Sensor -> Host)



Buffer read request (Host -> Sensor)



Serial NOR Flash read response (Sensor -> Host)

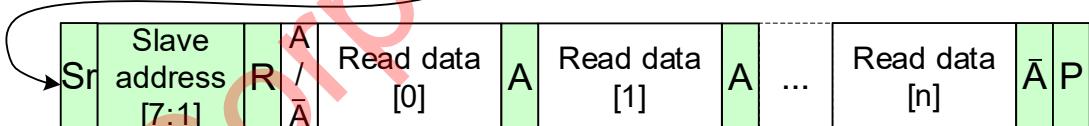


Figure 3-17 Request Format for Reading Data from the Buffer

◆ Note

When accessing the buffer outside the buffer region (addresses from 0x0000 to 0x00FF), the sensor returns a Negative Acknowledge.

◆ Memo

For details regarding the Serial NOR Flash Read and Write subcommands, refer to “3.5.1.3.3 Serial NOR Flash Write Subcommand” and “3.5.1.3.4 Serial NOR Flash Read Subcommand.”

3.5.1.3.2. Serial NOR Flash Sector Erase Subcommand

This subcommand erases data in the sector that contains the specified address of the Serial NOR Flash device.

To execute the Serial NOR Flash Sector Erase subcommand, switch the sensor's communication target to the Serial NOR Flash device and then set the subcommand as shown in "**Table 3-19.**"

Table 3-19 List of the Transferred Data to Execute the Serial NOR Flash Sector Erase Subcommand

Address [15:8]	Address [7:0]	Data	Overview of the Settings
0x80	0x00	0x03	Selection of a subcommand Serial NOR Flash Sector Erase Subcommand
0x80	0x01	ADDRESS [31:24]	Address settings of the Serial NOR Flash device [31:24]
0x80	0x02	ADDRESS [23:16]	Address settings of the Serial NOR Flash device [23:16]
0x80	0x03	ADDRESS [15:8]	Address settings of the Serial NOR Flash device [15:8]
0x80	0x04	ADDRESS [7:0]	Address settings of the Serial NOR Flash device [7:0]
0x80	0x05	0x5A	Execution of a subcommand

◇ **Memo**

For details regarding the method for setting a subcommand, refer to "**3.5.1.3.1 Setting a Subcommand.**"

3.5.1.3.3. Serial NOR Flash Write Subcommand

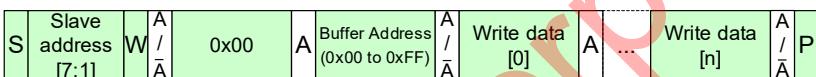
This subcommand writes data to the Serial NOR Flash device in units of 256 bytes. Before executing this subcommand, set data to be written to the sensor's buffer. To execute the Serial NOR Flash Write subcommand, set the buffer and then set the subcommand as shown in “**Table 3-20**”.

Table 3-20 List of the Transferred Data to Execute the Serial NOR Flash Write Subcommand

Address [15:8]	Address [7:0]	Data	Overview of the Settings
0x80	0x00	0x02	Selection of a subcommand (Serial NOR Flash Write Subcommand)
0x80	0x01	ADDRESS [31:24]	Address settings of the Serial NOR Flash device [31:24]
0x80	0x02	ADDRESS [23:16]	Address settings of the Serial NOR Flash device [23:16]
0x80	0x03	ADDRESS [15:8]	Address settings of the Serial NOR Flash device [15:8]
0x80	0x04	ADDRESS [7:0]	Address settings of the Serial NOR Flash device [7:0]
0x80	0x05	0x5A	Execution of a subcommand

“**Figure 3-18**” illustrates the request format starting with setting the data to be written to the Serial NOR Flash device in the buffer until executing the Serial NOR Flash Write subcommand.

Buffer write request (Host -> Sensor)



Serial NOR Flash write request (Host -> Sensor)

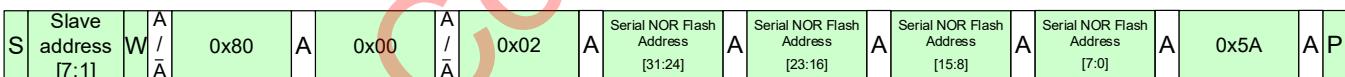


Figure 3-18 Request Format for Writing Data to the Serial NOR Flash Device

◆ **Note**

The sensor's buffer size is 256 bytes (Buffer Address: 0x00 to 0xFF). In the case of writing data to the region greater than the buffer size, the sensor returns a Negative Acknowledge.

◇ **Memo**

For details regarding the method for setting a subcommand, refer to “**3.5.1.3.1 Setting a Subcommand**.”

3.5.1.3.4. Serial NOR Flash Read Subcommand

This subcommand reads out 256 bytes of data from the Serial NOR Flash device.

To execute the Serial NOR Flash Read subcommand, switch the sensor's communication target to the Serial NOR Flash device and then set the subcommand as shown in "**Table 3-21.**"

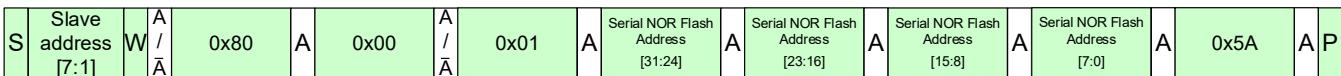
Table 3-21 List of the Transferred Data to Execute the Serial NOR Flash Read Subcommand

Address [15:8]	Address [7:0]	Data	Overview of the Settings
0x80	0x00	0x01	Selection of a subcommand (Serial NOR Flash Read Subcommand)
0x80	0x01	ADDRESS [31:24]	Address settings of the Serial NOR Flash device [31:24]
0x80	0x02	ADDRESS [23:16]	Address settings of the Serial NOR Flash device [23:16]
0x80	0x03	ADDRESS [15:8]	Address settings of the Serial NOR Flash device [15:8]
0x80	0x04	ADDRESS [7:0]	Address settings of the Serial NOR Flash device [7:0]
0x80	0x05	0x5A	Execution of a subcommand

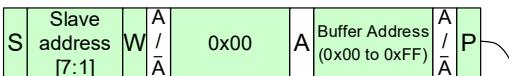
The data read out from the Serial NOR Flash device is saved to the sensor's buffer. "**Figure 3-19**" illustrates the request format starting with executing the Serial NOR Flash Read subcommand until reading out the data set in the buffer.

Bus-free communication

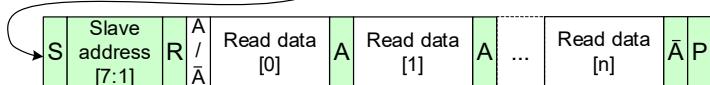
Serial NOR Flash read request (Host -> Sensor)



Buffer read request (Host -> Sensor)

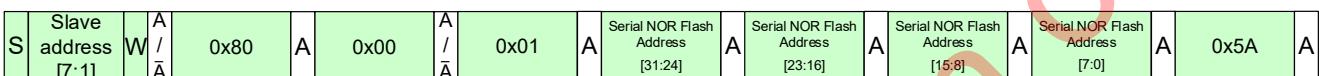


Serial NOR Flash read response (Sensor -> Host)

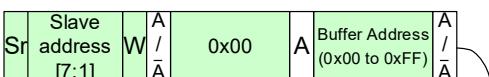


Bus-hold communication

Serial NOR Flash read request (Host -> Sensor)



Buffer read request (Host -> Sensor)



Serial NOR Flash read response (Sensor -> Host)

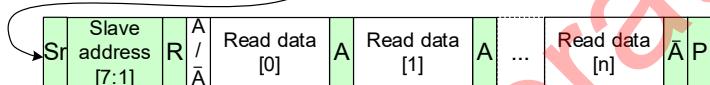


Figure 3-19 Request Format for Reading Out Data from the Serial NOR Flash Device

“Figure 3-19” illustrates two formats: Bus-Free and Bus-Hold.

Regarding the Bus-Free method, the sensor issues a Stop Condition (P) at the end of each processing and frees up the bus. Regarding the Bus-Hold method, the sensor continues to hold the bus and issues a Repeat Start Condition (Sr) to perform each processing.

◆ **Note**

The sensor's buffer size is 256 bytes (Buffer Address: 0x00 to 0xFF). In the case of reading out data from the region greater than the buffer size, the sensor returns a Negative Acknowledge.

◆ **Memo**

For details regarding the method for setting a subcommand, refer to “**3.5.1.3.1 Setting a Subcommand**.”

3.5.1.4. Register Access Command

This command switches the sensor's communication target to a register. This command also switches the mode ID number of the Remap Mode. **"Figure 3-20"** illustrates the request format.

Register access request (Host -> Sensor)

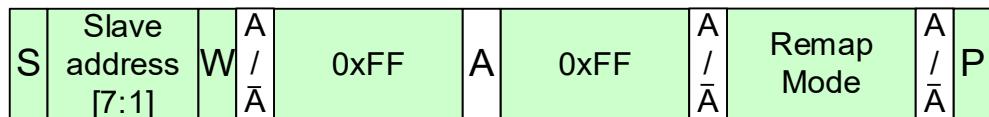


Figure 3-20 Request Format for the Register Access Command

The accessible register can be changed corresponding to the value of the Remap Mode shown in **"Figure 3-20."** Refer to the IMX623-AA** "Register Map" to check which registers are accessible to the host corresponding to the value of the Remap Mode.

3.5.1.4.1. Register Write Subcommand

To write data to the registers (illustrated in “**Figure 3-21**”) in bytes, switch the access target to these registers and then transmit data in accordance with the request format (also illustrated in “**Figure 3-21**”).

Register write request (Host -> Sensor)



Figure 3-21 Request Format for the Register Write Subcommand

3.5.1.4.2. Register Read Subcommand

To read data from the registers (illustrated in “**Figure 3-22**”) in bytes, switch the access target to these registers and then transmit data in accordance with the request format (also illustrated in “**Figure 3-22**”).

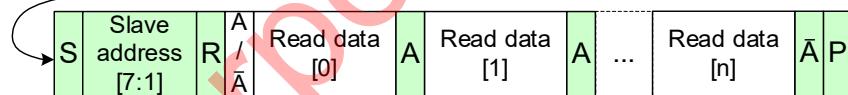
Bus-free communication

Sr: Repeated Start Condition

Register read request (Host -> Sensor)



Register read response (Sensor -> Host)



Bus-hold communication

Register read request (Host -> Sensor) & response (Sensor -> Host)

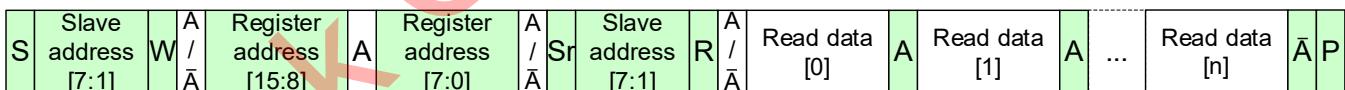


Figure 3-22 Request Format for the Register Read Subcommand

“**Figure 3-22**” illustrates two formats: Bus-Free and Bus-Hold.

Regarding the Bus-Free method, the sensor issues a Stop Condition (P) at the end of each processing and frees up the bus. Regarding the Bus-Hold method, the sensor continues to hold the bus and issues a Repeat Start Condition (Sr) to perform each processing.

3.5.2. Examples of Command and Subcommand Usage

This section describes examples of the usage of the sensor's commands and subcommands. In this example, it is assumed that the sensor's slave address is set to 0x1A.

"Figure 3-23" to "Figure 3-26" illustrate simplified read and write operations by omitting the following elements from the figures used in "3.5.1 List of Commands and Subcommands:"

- Start Condition
- Stop Condition
- Acknowledge
- Negative Acknowledge
- Read Access Bit
- Write Access Bit

3.5.2.1. Writing the Sensor's Register Value(s) to the Serial NOR Flash Device

"Figure 3-23" illustrates an example of communication when the sensor writes a register's value to the Serial NOR Flash device.

(a)	0x1A	0xFF	0xFF	0xF4	Serial NOR Flash access unlock
(b)	0x1A	0xFF	0xFF	0xFF	Serial NOR Flash all write
(c)	0x1A	0xFF	0xFF	0xF5	Serial NOR Flash access lock

Figure 3-23 Example of Communication When the Sensor Writes a Register Value to the Serial NOR Flash Device

Communicate with the sensor in the order: Command Data (a), (b) and (c) as illustrated in "Figure 3-23." The details of Command Data (a), (b) and (c) are as follows:

- Command Data (a)
In this command, the host enables access to the Serial NOR Flash device. For details, refer to "**3.5.1.1 Serial NOR Flash Access Lock Command**." This setting is required when access to the Serial NOR Flash device is disabled.
- Command Data (b)
Write the sensor's register value(s) to the Serial NOR Flash device as described in "**3.5.1.2 Serial NOR Flash All Write Command**." When writing to a register using this command, it is not necessary to erase the sector(s) to be written in advance.
- Command Data (c)
In this command, the host disables access to the Serial NOR Flash device. For details, refer to "**3.5.1.1 Serial NOR Flash Access Lock Command**."

3.5.2.2. When Writing Data to the Serial NOR Flash Device

"Figure 3-24" illustrates an example of communication when the sensor writes a value (e.g., 0x1122) to an address, which is 0x80000 or greater (i.e., User Free Area), of the Serial NOR Flash device.

- (a)

0x1A	0xFF	0xFF	0xF4
------	------	------	------

 Serial NOR Flash access unlock
- (b)

0x1A	0xFF	0xFF	0xF7
------	------	------	------

 Serial NOR Flash access
- (c)

0x1A	0x80	0x00	0x03	0x00	0x08	0x00	0x00	0x5A
------	------	------	------	------	------	------	------	------

 Serial NOR Flash sector erase
- (d)

0x1A	0x00	0x00	0x11	0x22
------	------	------	------	------

 Buffer write
- (e)

0x1A	0x80	0x00	0x02	0x00	0x08	0x00	0x00	0x5A
------	------	------	------	------	------	------	------	------

 Serial NOR Flash write
- (f)

0x1A	0xFF	0xFF	0xF5
------	------	------	------

 Serial NOR Flash access lock

Figure 3-24 Example of Communication When the Sensor Writes a Value to the User Free Area of the Serial NOR Flash Device

Communicate with the sensor in the order: Command Data (a) to (f) as illustrated in "Figure 3-24." The details of Command Data (a) to (f) are as follows:

- Command Data (a)
In this command, the host enables access to the Serial NOR Flash device. For details, refer to "**3.5.1.1 Serial NOR Flash Access Lock Command**." This setting is required when access to the Serial NOR Flash device is disabled.
- Command Data (b)
In this command, the host switches access to the Serial NOR Flash device. For details, refer to "**3.5.1.3 Serial NOR Flash Access Command**." This setting is required in order for the host to set the "Serial NOR Flash Sector Erase", "Serial NOR Flash Read" or "Serial NOR Flash Write" subcommand.
- Command Data (c)
In this command, the host erases the sectors of the User Free Area (start address: 0x00080000). For details, refer to "**3.5.1.3.2 Serial NOR Flash Sector Erase Subcommand**."
- Command Data (d)
In this command, the host writes 0x1122 to the buffer. For details, refer to "**3.5.1.3.1 Setting a Subcommand**." The sensor writes data to the Serial NOR Flash device in units of 256 bytes. When writing another value, write this value in succession after 0x1122.
- Command Data (e)
The sensor writes the value stored in its buffer to the address 0x00080000 in the User Free Area. For details, refer to "**3.5.1.3.3 Serial NOR Flash Write Subcommand**."
- Command Data (f)
In this command, the host disables access to the Serial NOR Flash device. For details, refer to "**3.5.1.1 Serial NOR Flash Access Lock Command**."

3.5.2.3. When Reading Out Data from the Serial NOR Flash Device

"Figure 3-25" illustrates an example of communication when the sensor reads out a value from an address, which is 0x80000 or greater (i.e., User Free Area), of the Serial NOR Flash device.

- (a)

0x1A	0xFF	0xFF	0xF4
------	------	------	------

 Serial NOR Flash access unlock
- (b)

0x1A	0xFF	0xFF	0xF7
------	------	------	------

 Serial NOR Flash access
- (c)

0x1A	0x80	0x00	0x01	0x00	0x08	0x00	0x00	0x5A
------	------	------	------	------	------	------	------	------

 Serial NOR Flash read
- (d)

0x1A	0x00	0x00
------	------	------

 Buffer read
 - | | | |
|------|------|------|
| 0x1A | 0x11 | 0x22 |
|------|------|------|

 Read response
- (e)

0x1A	0xFF	0xFF	0xF5
------	------	------	------

 Serial NOR Flash access lock

Figure 3-25 Example of Communication When the Sensor Reads Out Data from the Serial NOR Flash Device

Communicate with the sensor in the order: Command Data (a) to (e) as illustrated in "Figure 3-25." The details of Command Data (a) to (e) are as follows:

- Command Data (a)
In this command, the host enables access to the Serial NOR Flash device. For details, refer to "**3.5.1.1 Serial NOR Flash Access Lock Command**." This setting is required when access to the Serial NOR Flash device is disabled.
- Command Data (b)
In this command, the host switches access to the Serial NOR Flash device. For details, refer to "**3.5.1.3 Serial NOR Flash Access Command**." This setting is required in order for the host to set the "Serial NOR Flash Sector Erase", "Serial NOR Flash Read" or "Serial NOR Flash Write" subcommand.
- Command Data (c)
The sensor writes the value of the address 0x00080000 in the User Free Area of the Serial NOR Flash device to its buffer. For details, refer to "**3.5.1.3.4 Serial NOR Flash Read Subcommand**." The data read out in units of 256 bytes from the Serial NOR Flash device is saved to the sensor's buffer.
- Command Data (d)
In this command, the host requests a buffer read to receive data. For details, refer to "**3.5.1.3.1 Setting a Subcommand**." "Figure 3-25" shows only two bytes of the value 0x1122 that is used in the example of "**3.5.2.2 When Writing Data to the Serial NOR Flash Device**." However, actually, data in increments of 256 bytes is written to the buffer of the sensor.
- Command Data (e)
In this command, the host disables access to the Serial NOR Flash device. For details, refer to "**3.5.1.1 Serial NOR Flash Access Lock Command**."

3.5.2.4. When Reading and Writing a Register Value

"Figure 3-26" illustrates an example of communication when the sensor reads and writes a value to the USER_255 register (Register Address 0xC438) and the Remap Mode is 0x00.

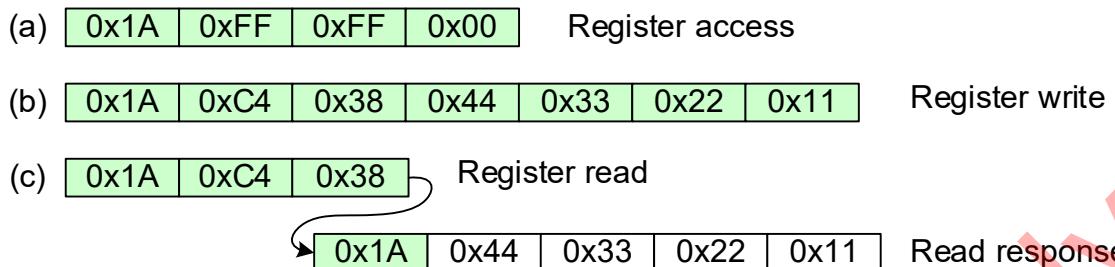


Figure 3-26 Example of Communication When the Sensor Reads and Writes a Register Value Using the USER_255 Register

Communicate with the sensor in the order: Command Data (a), (b) and (c) as illustrated in "Figure 3-26." The details of Command Data (a), (b) and (c) are as follows:

- Command Data (a)
Set the sensor's Remap Mode to 0x00. For details, refer to "[3.5.1.4 Register Access Command](#)."
- Command Data (b)
In this command, the sensor writes a user-set value (e.g., 0x11223344) to the USER_255 register (Address: 0xC438). For details, refer to "[3.5.1.4.1 Register Write Subcommand](#)."
- Command Data (c)
In this command, the host requests a buffer read of the USER_255 register (Address: 0xC438) to receive the data. For details, refer to "[3.5.1.4.2 Register Read Subcommand](#)."

3.6. Communication Timing

The sensor can communicate via I²C communication while the sensor is in the following states:

- Start-up State
- Sleep State
- Streaming State
- BIST Standby State
- "Safe State Mode" State

If the sensor is not available for I²C communication, it generates a Negative Acknowledge using the value of the EXT_I2C_CLK_STRETCH_EN register or holds the SCL pin's output low. Refer to "**Chapter 4 Startup Control**" for the sensor's states and the timing of I²C communication in relation to the transition of the sensor's states.

■ Communication Time Frames in Streaming State

As illustrated in "**Figure 3-27**," communicate with the sensor after the output of the FS line until the end of the T_{CMACT} period while the sensor is in Streaming State.

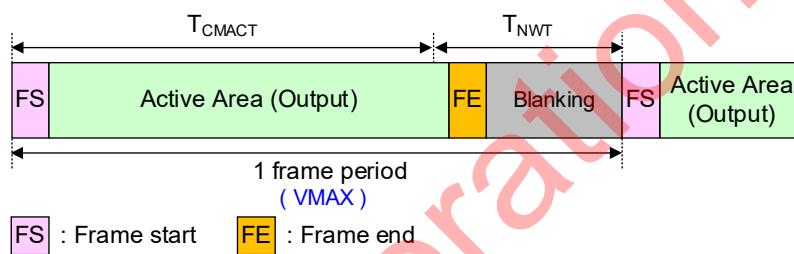


Figure 3-27 The Communication Timing While the Sensor Is in Streaming State

T_{NWT} in "**Figure 3-27**" is the period of time, during which the application of any changes in settings for the sensor via I²C communication is not guaranteed. As shown in "**Table 3-22**," the T_{NWT} period varies corresponding to the drive mode.

Table 3-22 Definition of the T_{NWT} Period

Drive Modes	T _{NWT} Period
Normal	
HDR (UC)	41 [H] + 3.5 [ms]
HDR (PWL)	
HDR (Line/Line)	(41 [H] x N) + 3.5 [ms]*

* N in the expression represents the output format of RAW. Calculate the T_{NWT} period using the following values and the value of the OUTMODE_ register.

OUTMODE_ = 1:2

OUTMODE_ = 3:4

The T_{CMACT} period is obtained by subtracting the T_{NWT} period from the VMAX (i.e., the maximum number of lines of the vertical sync signal) of the sensor.

H in the expression is the unit of time for the sensor's output of one line of data. One H can be calculated from the following equation using the frame rate of the drive mode in use:

$$1 \text{ HTIME[ms]} = \frac{1000}{\text{Frame Rate} \times \text{VMAX}}$$

If the host does not complete communication with the sensor within the T_{CMACT} period, it is not guaranteed whether the sensor processes this communication within the same frame or the subsequent frame. Specifically, in the case of multibyte registers, the communication time frame of the upper and lower bytes can be delayed, thereby negatively affecting the image quality and the sensor's operations.

◇ **Memo**

- For details regarding the VMAX and frame rates, refer to "**5.2.3.2.1 Units of Exposure Time.**"

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Chapter 4 Startup Control

This chapter explains the following information in order for the host to start up the sensor and for the sensor to output an image:

- The types of the sensor's operating states
- Transition between the sensor's states and the power-on sequence
- How to update the Serial NOR Flash device

4.1. The States of the Sensor

The sensor has multiple operating states as described in “**Table 4-1.**” The sensor can communicate with the host while the sensor is in the following states:

- Start-up State
- Sleep State
- Streaming State
- BIST Standby State
- “Safe State Mode” State

Check the state using the DEVSTS register.

In a state in which communication with the sensor is available, the host can check the current state using the DEVSTS register. In the state in which communication with the sensor is not available, the value of the DEVSTS register cannot be read out. Therefore, it is shown as “N/A” in “**Table 4-1.**”

◇ **Memo**

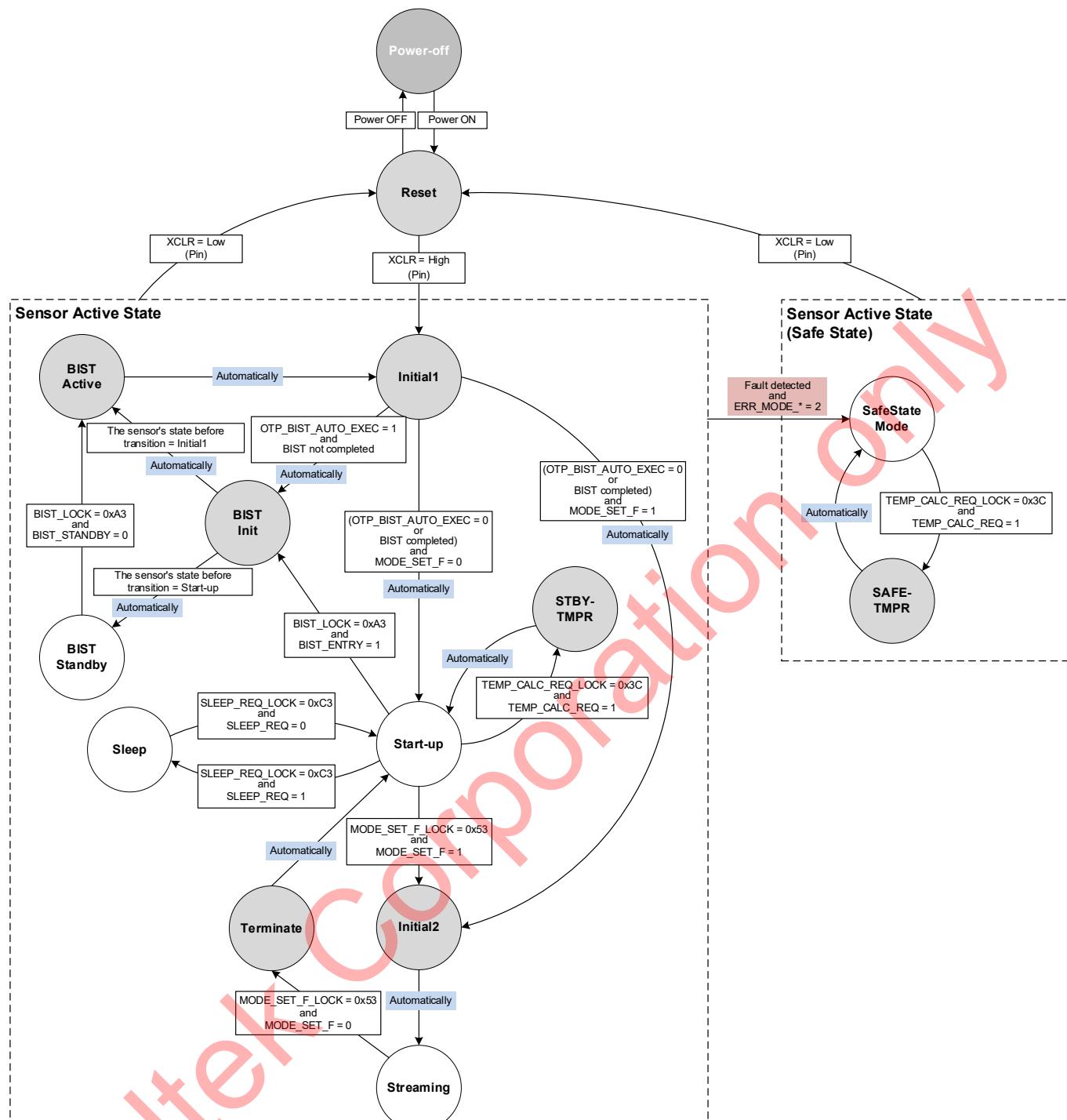
- For details regarding the transition conditions to Logic BIST State, Memory BIST State and “Safe State Mode” State, refer to the IMX623-AA** “Safety Application Note.”

Table 4-1 The States of the Sensor

Sensor State	DEVSTS	Availability of I ² C Communication	Description	Conditions for Transition
Power-off	N/A	Not available	The power voltages (1.1 V, 1.8 V and 3.3 V) are not supplied to the sensor. In this state, all functions and interfaces do not operate.	When all power voltages (1.1 V, 1.8 V and 3.3 V) are supplied, the sensor transitions to Reset State.
Reset	N/A	Not available	All power voltages (1.1 V, 1.8 V and 3.3 V) are supplied to the sensor. In Reset State, all functions and interfaces do not operate.	When the XCLR pin is driven high, the sensor transitions to Initial1 State.
Initial1	N/A	Not available	The sensor applies the stored settings in the OTP ROM or Serial NOR Flash device, and performs startup processing. After the sensor's startup	When the drive mode setting has been stored in the Serial NOR Flash device (i.e., MODE_SET_F = 1), the sensor transitions to Initial2 State.

Sensor State	DEVSTS	Availability of I ² C Communication	Description	Conditions for Transition
			processing is complete, the sensor transitions to another state corresponding to the conditions in the "Conditions for Transition" column.	When the automatic execution settings of Logic BIST and Memory BIST are stored in the Serial NOR Flash device, the sensor transitions to BIST Init State. The sensor transitions to Start-up State in the following case: <ul style="list-style-type: none"> • When no Serial NOR Flash device is connected When the sensor does not read the Serial NOR Flash device at startup (The SCKM pin is in a state of logic-low.) • When the drive mode has not been stored in the Serial NOR Flash device (i.e., MODE_SET_F = 0) When the sensor's Self-Diagnostic function detects a fault, the sensor transitions to "Safe State Mode" State.
Start-up	1 or 2	Available	The host can configure various settings including the sensor's drive mode.	When the host sets the drive mode, the sensor transitions to Initial2 State. When the host issues a Sleep State transition request, the sensor transitions to Sleep State. When the host sets the manual execution settings of Logic BIST and Memory BIST, the sensor transitions to BIST Init State. When the host issues a temperature measurement request, the sensor transitions to STBY-TMPR State.
Sleep	8	Available	The state in which the sensor reduces the power consumption. <ul style="list-style-type: none"> • The host can configure various settings including the sensor's drive mode. • The host cannot access the Serial NOR Flash device. 	When the host issues a Sleep State cancellation request, the sensor transitions to Start-up State.
STBY-TMPR	N/A	Not available	The sensor measures temperature using its on-chip temperature sensors. For details regarding the temperature information of the sensor, refer to " 6.9.3.5.9 Temperature Information ".	When the temperature measurement is complete, the sensor transitions to Start-up State.
Initial2	N/A	Not available	The sensor performs startup processing corresponding to the settings stored in the Serial NOR Flash device and the settings configured in Start-up State.	When startup processing is complete while the sensor is in Initial2 State, the sensor transitions to Streaming State. When the sensor's Self-Diagnostic function detects a fault, the sensor transitions to "Safe State Mode" State.

Sensor State	DEVSTS	Availability of I ² C Communication	Description	Conditions for Transition
Streaming	5	Available	<p>The sensor transmits images corresponding to the settings stored in the Serial NOR Flash device or the settings configured by the host.</p> <p>The sensor also measures temperature using its on-chip temperature sensors.</p>	When the host transitions the sensor to Start-up State while the sensor is in Streaming State, the sensor transitions to Terminate State.
				When the sensor's Self-Diagnostic function detects a fault, the sensor transitions to "Safe State Mode" State.
Terminate	N/A	Not available	The sensor performs processing such as stopping clocks to transition to Start-up State.	When the sensor completes processing while the sensor is in Terminate State, the sensor transitions to Start-up State.
Safe State Mode	13	Available	<p>This state indicates that the sensor's Self-Diagnostic function has detected a fault.</p> <ul style="list-style-type: none"> The sensor does not transition by any other methods except a sensor reset or power-off. 	When the host issues a temperature measurement request, the sensor transitions to SAFE-TMPR State.
SAFE-TMPR	N/A	Not available	<p>The sensor measures temperature using its on-chip temperature sensors.</p> <p>For details regarding the temperature information of the sensor, refer to "6.9.3.5.9 Temperature Information".</p>	When the temperature measurement is complete, the sensor transitions to "Safe State Mode" State.
BIST Init	N/A	Not available	<p>The sensor configures the required settings to execute Logic BIST and Memory BIST. After the settings have been configured, the sensor transitions to another state corresponding to the conditions in the "Conditions for Transition" column.</p>	When the sensor transitions from Initial1 State to BIST Init State, it automatically transitions to BIST Active State.
				When the sensor transitions from Start-up State to BIST Init State, it automatically transitions to BIST Standby State.
BIST Standby	17	Available	This state indicates that the sensor is on standby for the Logic BIST and Memory BIST execution settings from the host.	When the host configures the execution settings of Logic BIST and Memory BIST, the sensor transitions to BIST Active State.
BIST Active	N/A	Not available	The sensor executes Logic BIST and Memory BIST.	When both Logic BIST and Memory BIST are complete, the sensor resets its internal state and transitions to Initial1 State.



* For details regarding the transition conditions to "Safe State Mode" State, refer to the IMX623-AA** "Safety Application Note."

Figure 4-1 State Transition

4.2. Setting the Drive Mode

The method for setting the sensor's drive mode varies corresponding to whether the Serial NOR Flash device is used. Set the drive mode for each case as follows:

4.2.1. When Using the Serial NOR Flash Device

To set the drive mode, it is necessary to write the IMX623-AA** "Register Configuration File" provided by SSS to the Serial NOR Flash device in advance. If the IMX623-AA** "Register Configuration File" provided by SSS has not been written to the Serial NOR Flash device, perform the procedure described in "[4.9.1 Writing the Register Configuration File to the Serial NOR Flash Device.](#)"

The sensor's drive mode is determined via communication with the host while the sensor is in Start-up State. Set the drive mode in accordance with the following procedure:

1. Set the MODE_SEL register to the index number corresponding to the drive mode. "Table 4-2" shows the index number corresponding to the drive mode.
2. In addition to the drive mode-based settings, if configuring any other settings, configure these at this time.
3. After setting all registers, set the MODE_SET_F register to 1. The MODE_SET_F register is compatible with the Application Lock function. For details, refer to "3.1.5 Application Lock Function." The sensor applies the register settings, completes necessary initializations, and then transitions to Streaming State.
4. After the sensor transitions to Streaming State, configure the settings for the registers that require a dynamic change as necessary.

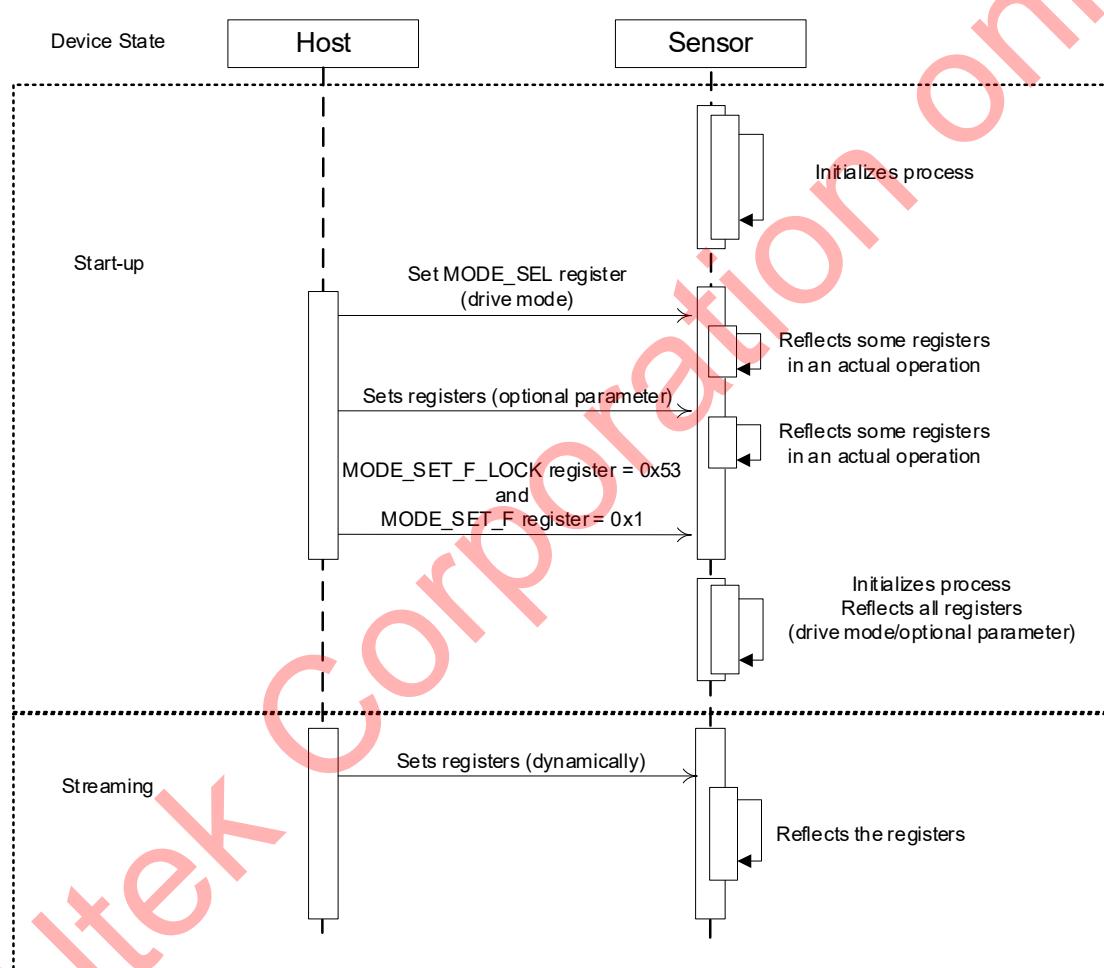


Figure 4-2 Flow of Configuring the Settings for the Drive Mode When Using the Serial NOR Flash Device

Table 4-2 List of Drive Mode Index Numbers

Index Number	Image Size	Frame Rate [Frames/s]	Interface	Output Format
4	1936 x 1552	60	MIPI CSI-2 4-Lane	RAW12
5	1936 x 1552	60	MIPI CSI-2 2-Lane	RAW12
6	1936 x 1552	60	MIPI CSI-2 4-Lane	RAW14
7	1936 x 1552	60	MIPI CSI-2 2-Lane	RAW14
8	1936 x 1552	60	MIPI CSI-2 4-Lane	RAW16
9	1936 x 1552	60	MIPI CSI-2 4-Lane	RAW20
10	1936 x 1552	60	MIPI CSI-2 4-Lane	RAW24
11	1936 x 3104	60	MIPI CSI-2 4-Lane	RAW12 x 2
29	1936 x 1552	30	MIPI CSI-2 4-Lane	RAW12
30	1936 x 1552	30	MIPI CSI-2 2-Lane	RAW12
31	1936 x 1552	30	MIPI CSI-2 4-Lane	RAW14
32	1936 x 1552	30	MIPI CSI-2 2-Lane	RAW14
33	1936 x 1552	30	MIPI CSI-2 4-Lane	RAW16
34	1936 x 1552	30	MIPI CSI-2 2-Lane	RAW16
35	1936 x 1552	30	MIPI CSI-2 4-Lane	RAW20
36	1936 x 1552	30	MIPI CSI-2 2-Lane	RAW20
37	1936 x 1552	30	MIPI CSI-2 4-Lane	RAW24
38	1936 x 1552	30	MIPI CSI-2 2-Lane	RAW24
39	1936 x 6208	30	MIPI CSI-2 4-Lane	RAW12 x 4
40	1936 x 3104	30	MIPI CSI-2 4-Lane	RAW12 x 2
41	1936 x 3104	30	MIPI CSI-2 2-Lane	RAW12 x 2

◇ Memo

To transition the sensor to Streaming State without going through Start-up State, perform the following procedure:

1. Set the MODE_SEL register to the drive mode index number to select the drive mode when the sensor starts up.
2. Set the MODE_SET_F register to 1.
3. Update the Serial NOR Flash device.

4.2.2. When Not Using a Serial NOR Flash Device

The sensor's drive mode is determined via communication with the host while the sensor is in Start-up State. Set the drive mode in accordance with the following procedure:

1. Configure register settings in accordance with the IMX623-AA** "Register Configuration File" provided separately by SSS.
2. In addition to the settings in accordance with the IMX623-AA** "Register Configuration File", if configuring any other settings, configure them at this time.
3. After setting all registers, set the MODE_SET_F register to 1. The MODE_SET_F register is compatible with the Application Lock function. For details, refer to "**3.1.5 Application Lock Function.**" The sensor applies the register settings, completes necessary initializations, and then transitions to Streaming State.
4. After the sensor transitions to Streaming State, configure the settings for the registers that require a dynamic change as necessary.

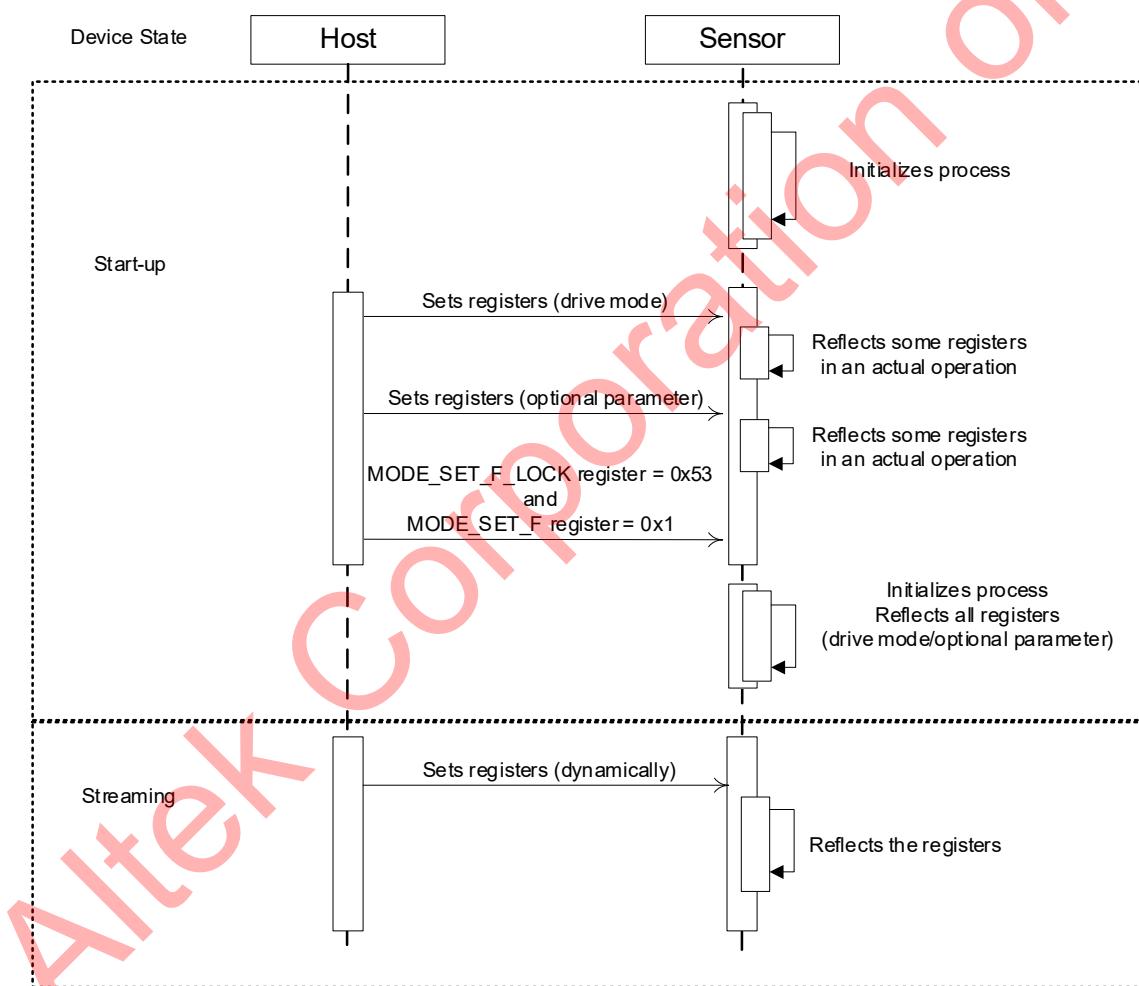


Figure 4-3 Drive Mode Setting Flow When Not Using the Serial NOR Flash Device

4.3. Power ON

4.3.1. Power-on Sequence

“Figure 4-4” illustrates a sequence in which the sensor transitions to Steaming State after the sensor is powered on, using the Serial NOR Flash device’s data which has been saved with the drive mode selected.

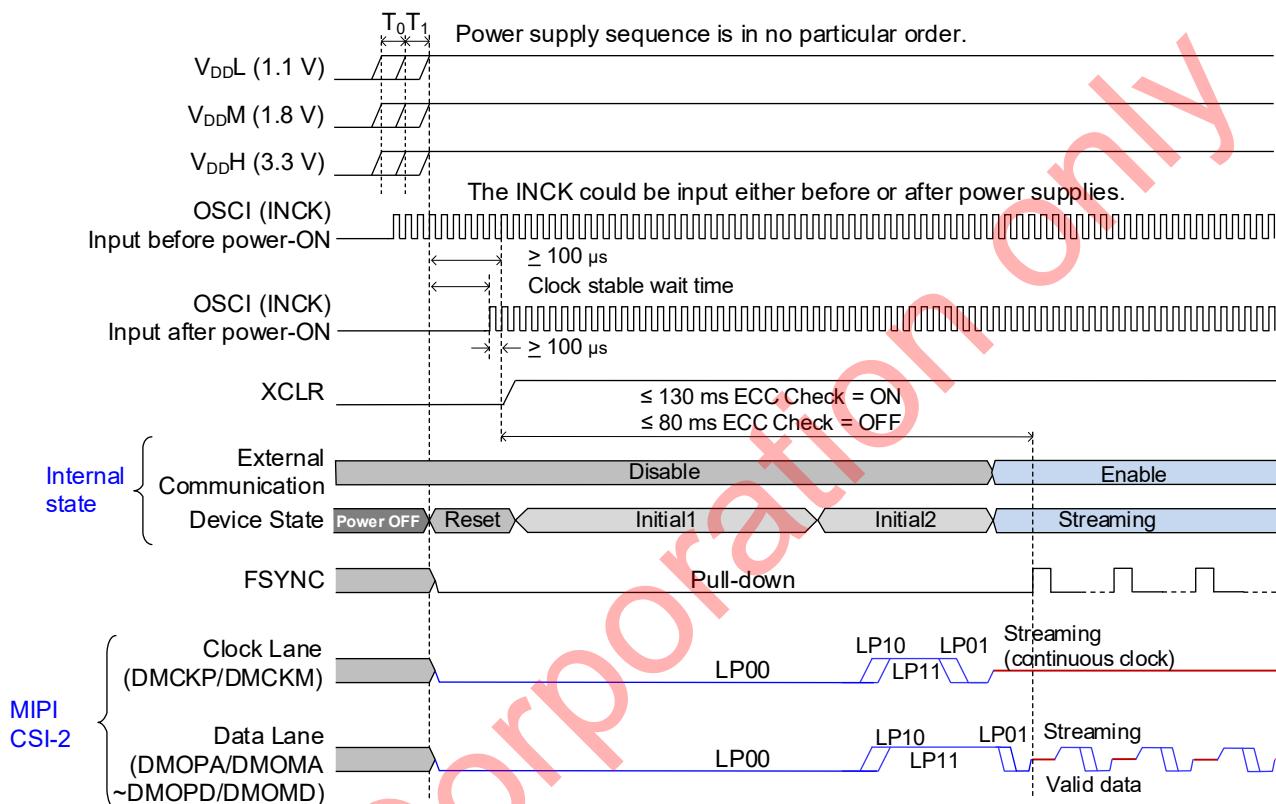


Figure 4-4 Power-on Sequence

1. The startup order of the power supply voltages (1.1 V, 1.8 V and 3.3 V) is at the user's discretion ($T_0, T_1 \geq 0$ ns). For details regarding power voltages, refer to the IMX623-AA** Data Sheet.
2. The start of the INCK input via the OSCI pin can be either before or after the power supply voltages ramp up to a stable state. When using any oscillator, be sure not to drive the sensor's XCLR pin high until the oscillator output stabilizes.
3. Hold the XCLR pin low while all power supply voltages start up and the INCK input clock is stabilized, and then for a further 100 μ s. For details regarding the power supply, refer to the IMX623-AA** "Data Sheet."
4. After cancelling the XCLR pin (i.e., driving the pin high), the sensor transitions to Initial1 State and starts initialization processing. Communication with the sensor is prohibited until the sensor transitions to Streaming State. The sensor accesses the Serial NOR Flash device's data during power-on. Therefore, enable the sensor to read data from and write data to the Serial NOR Flash device before driving the XCLR pin high.
5. The sensor transitions to Initial2 State under the following conditions:
 - When the processing of Initial1 State is complete
 - When a Serial NOR Flash device is connected
 - When the drive mode is set
6. In Initial2 State, the sensor performs initialization corresponding to the drive mode.
7. After Initial2 State processing is complete and the sensor transitions to Streaming State, the sensor begins output of each signal.

◆ Note

- The sensor performs reset configuration after cancelling the XCLR pin. Set the state of pins which are used for the Reset Configuration function before cancelling the XCLR pin (i.e., driving the pin high). For details, refer to "**2.1.5 Reset Configuration**".
- When the user selects the mode for setting a desired Reset Configuration frequency, in order for the sensor to begin initialization processing, cancel the XCLR pin (i.e., drive the pin high) and then set a valid INCK frequency. For details, refer to "**2.1.5.1 Setting the Master Clock Frequency**".

"Figure 4-4" is an example of the power-on sequence when the settings shown in "Table 4-3" have been written to the Serial NOR Flash device. For details regarding these settings, refer to the corresponding section.

Table 4-3 Assumed Values for the Power-on Sequence

Settings	User-Set Value	Remark
MIPI CSI-2	IR_DR_I2I_MIPI_FRAME_VBLANKSTOP_CL = 0	" 2.5.2 Setting MIPI CSI-2 Serial Data Output "
FSYNC	FSYNC_DRVABTY = 0	" 2.1.2 Configuring the Settings for Pins' Input/Output and Driveability "
INCK	Valid INCK frequency	" 2.1.8.1 Setting the Master Clock Frequency "
This register is used to enable or disable an automatic execution of Logic BIST and Memory BIST.	OTP_BIST_AUTO_EXEC = 0	" 4.1 The States of the Sensor "
Output Mask	INIT_MASK_CNT_ = 0	" 7.12 Output Mask Function "

Settings	User-Set Value	Remark
	MUTE_CNT_ = 0	
Sync Control	SG_MODE_ = 0	"7.1 Sync Function"
	SG_MODE_APL = 0	
Drive Mode	MODE_SEL ≠ 0	"4.2 Setting the Drive Mode"
	MODE_SET_F_LOCK = 0x53	
	MODE_SET_F = 1	
ECC Checking	ECC checking can be enabled or disabled.	"2.2.5 ECC Checking by the Serial NOR Flash Device."

◆ Note

When setting the registers shown in "**Table 4-3**" while the sensor is in Start-up State, set the drive mode at the end of these settings.

4.3.1.1. When the Sensor Transitions to Start-up State after Sensor Power-On

In the following cases, the sensor stops in Start-up State after the sensor is powered on:

- A Serial NOR Flash device is not used
- No data has been written to the Serial NOR Flash device
- The drive mode has not been selected (`MODE_SET_F` = 0)
- The sensor does not read out the Serial NOR Flash device at sensor startup due to the settings in the Reset Configuration.

“Figure 4-5” illustrates a sequence in which the sensor transitions to Start-up State after the sensor is powered on. This is an example, in which a Serial NOR Flash device is not used and the host configures the same settings as those of the power-on sequence shown in “**Table 4-3**” after the sensor has transitioned to Start-up State.

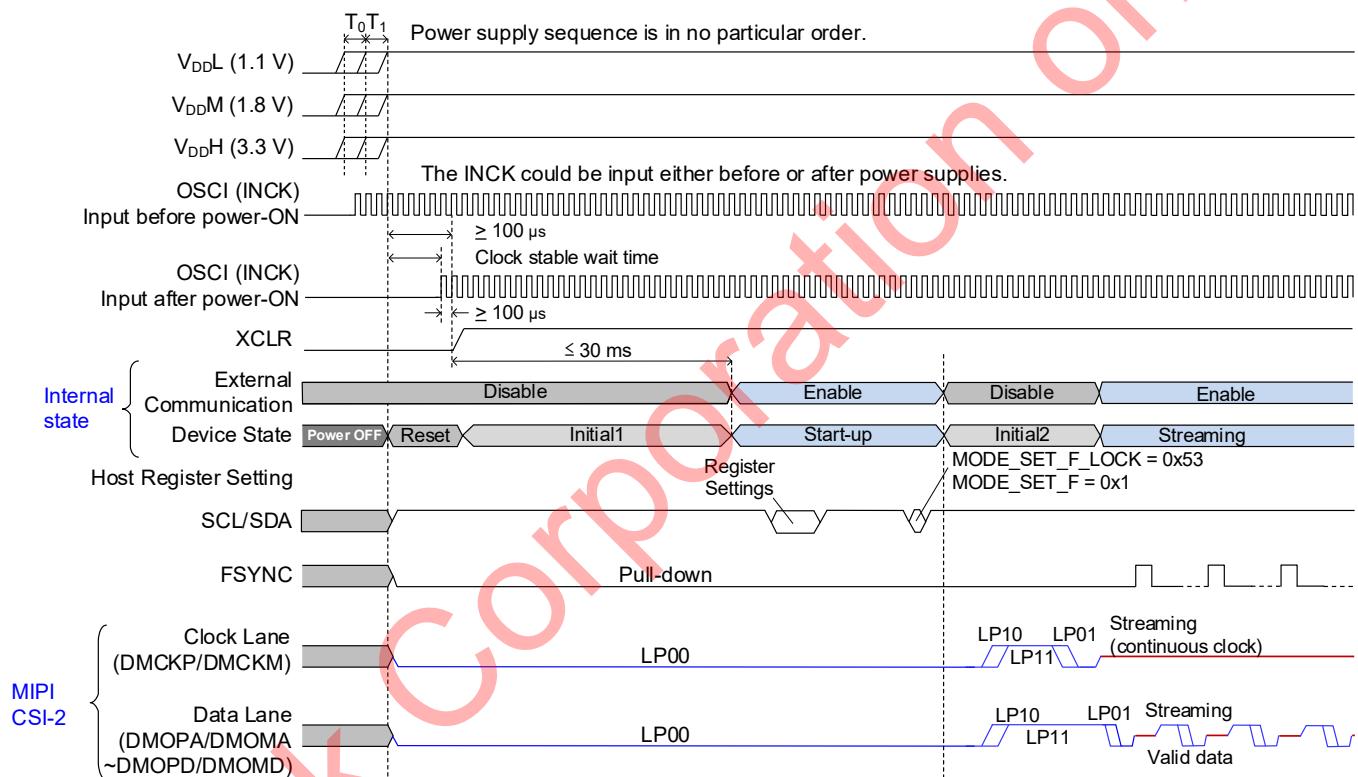


Figure 4-5 Transition to Start-up State During Power on (Without a Serial NOR Flash Device)

4.3.1.1.1. When Transitioning the Sensor to Start-up State After Sensor Power-On

To transition the sensor to Start-up State after sensor power-on, for example, when writing to the OTP ROM or switching drive modes, perform the following operations:

- * Select the drive mode using the MODE_SEL register.
- * Set the MODE_SET_F register to 0x0.
- * Execute the Serial NOR Flash All Write command.

◇ **Memo**

To perform an operation such as switching drive modes after the sensor has transitioned to Streaming State, transition the sensor to Start-up State by performing the procedure described in “[4.4 When Transitioning the Sensor from Streaming State to Start-up State](#).”

4.3.2. Power-on Sequence in External Pulse-Based Sync

To start up the sensor in external pulse-based sync, configure the settings shown in “[Table 4-4](#).”

Table 4-4 List of the Settings Required for External Pulse-Based Sync

Name	User-Set Value	Remark
FSYNC	FSYNC_DRVABTY = 3	“2.1.2 Configuring the Settings for Pins’ Input/Output and Driveability”
Sync Control	SG_MODE_ = 1	“6.1 Sync Function”
	SG_MODE_APL = 1	

“[Figure 4-6](#)” illustrates the sequence in which the sensor is switched on while the drive mode has not been set in the Serial NOR Flash device and then the drive mode is selected in Start-up State. This figure is an example of when the host changes the value of each register shown in “[Table 4-4](#)” for the registers shown in “[Table 4-3](#)” after the sensor transitions to Start-up State.

◇ **Memo**

See “[Figure 4-5](#)” in “[4.3.1.1 When the Sensor Transitions to Start-up State after Sensor Power-On](#),” for the behavior of the sensor until the sensor transitions to Start-up State.

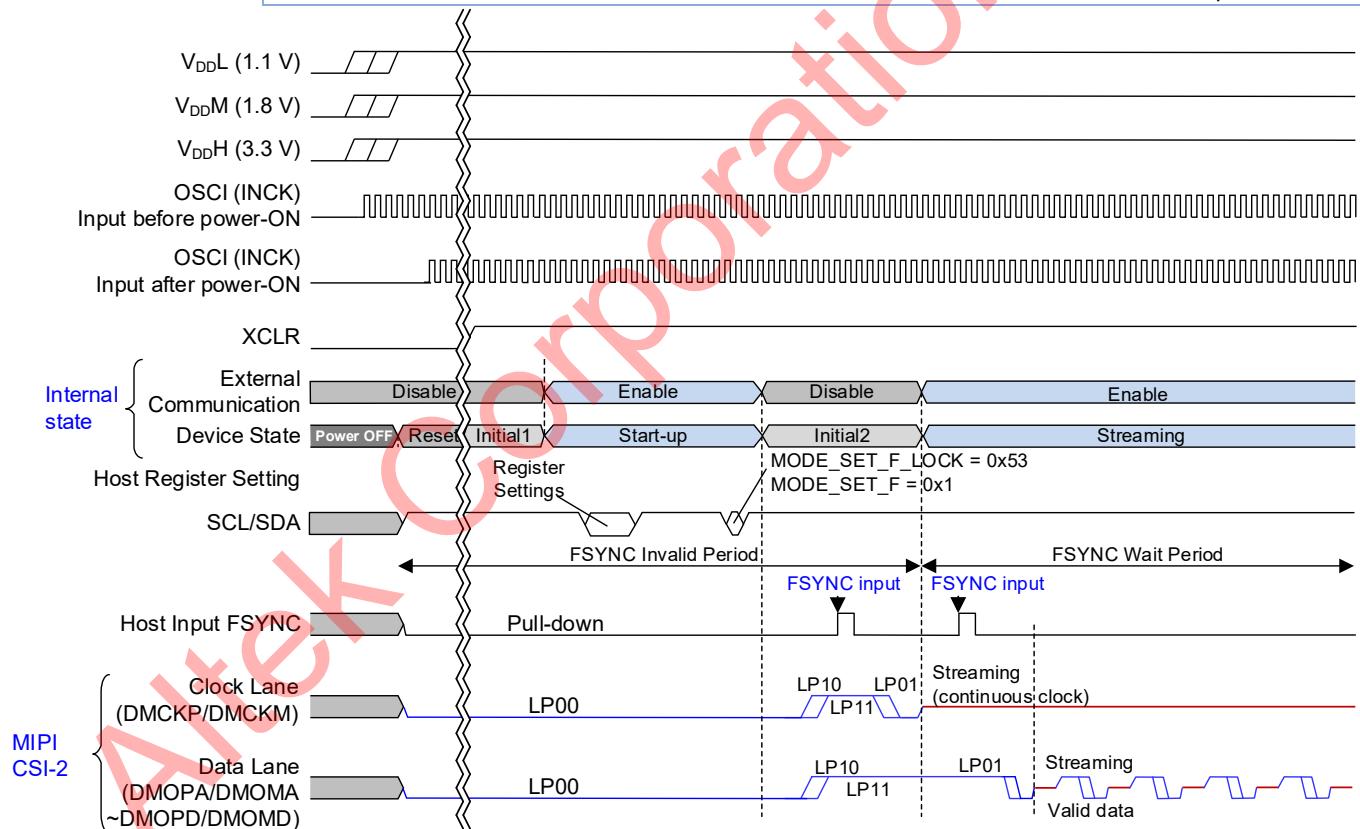


Figure 4-6 Power-On Sequence (External Pulse-Based Sync)

◆ Note

- When the external pulse-based sync settings are enabled, the sensor begins transmitting an image when the sensor receives the external sync signal from the host after the sensor has transitioned to Streaming State.
- If the sensor has not transitioned to Streaming State, the sensor does not perform synchronization with the external sync signal that the sensor receives from the host.
- After the sensor has transitioned to Streaming State and the sensor has received the external sync signal, the sensor begins operating autonomously in sync with its own internal clock. For details, refer to “[6.1 Sync Function](#).”

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4.3.3. Power-on Sequence in Shutter Trigger-Based Sync

To start up the sensor in shutter trigger-based sync, configure the settings as described in “[Table 4-5](#).”

Table 4-5 List of the Settings Required for Shutter Trigger-Based Sync

Name	User-Set Value	Remark
FSYNC	FSYNC_DRVABTY = 3	“ 2.1.2 Configuring the Settings for Pins' Input/Output and Driveability ”
Sync Control	SG_MODE_ = 2 SG_MODE_APL = 2	“ 6.1 Sync Function ”

“[Figure 4-7](#)” illustrates the sequence in which the sensor is switched on while the drive mode has not been set in the Serial NOR Flash device and then the drive mode is selected in Start-up State. This figure is an example of when the host sends the user-set values shown in “[Table 4-5](#)” from the list of the settings shown in “[Table 4-3](#)” to the sensor after the sensor transitions to Start-up State.

◇ **Memo**

See “[Figure 4-5](#)” in “[4.3.1.1 When the Sensor Transitions to Start-up State after Sensor Power-On](#),” for the behavior of the sensor until the sensor transitions to Start-up State.

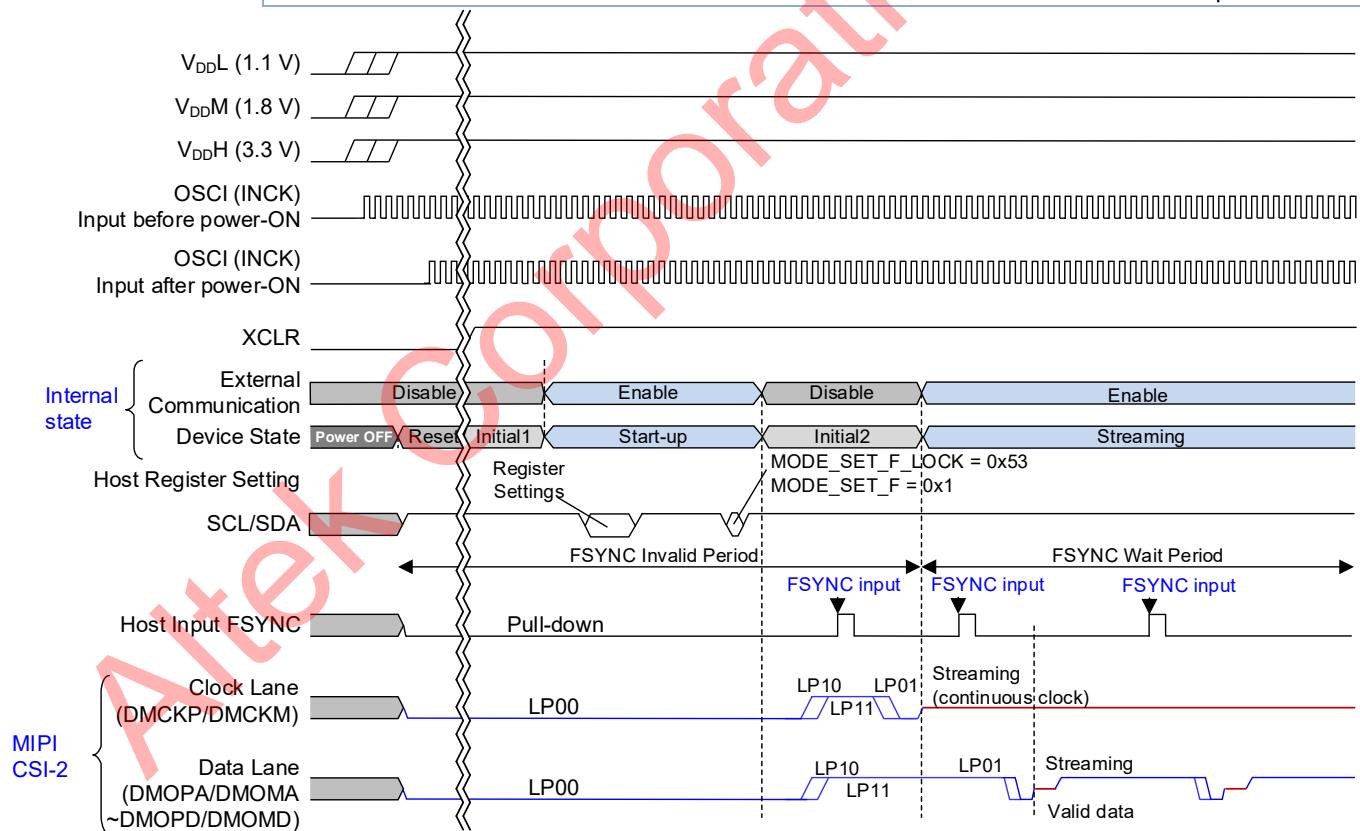


Figure 4-7 Power-On Sequence in Shutter Trigger-Based Sync

◆ Note

- The sensor begins exposure under the following conditions:
 - When the shutter trigger-based sync settings are enabled
 - After the sensor has transitioned to Streaming State and after the sensor has received the external sync signal from the host
 - If the sensor has not transitioned to Streaming State, the sensor does not perform synchronization with the external sync signal that the sensor receives from the host.
 - Unlike the external pulse-based sync, the sensor does not operate autonomously after having received the external sync signal. To operate the sensor autonomously in shutter trigger-based sync, configure the settings for the autonomous operating mode.
Regarding the autonomous operating mode, refer to "**6.1.3.3 Shutter Trigger-Based Synchronization.**"
-

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4.4. When Transitioning the Sensor from Streaming State to Start-up State

4.4.1. Sequence from Streaming State to Start-up State

To change the drive mode or registers' values in Streaming State, the sensor is required to be transitioned from Streaming State to Start-up State. To transition the sensor to Start-up State, follow the procedure below:

■ The settings to transition the sensor from Streaming State to Start-up State

To transition the sensor to Start-up State, set the MODE_SET_F register to 0x0.

“Figure 4-8” illustrates the sequence in which the sensor transitions from Streaming State to Start-up State. This figure is an example in which the settings shown in “**Table 4-3**,” which are the same settings as the power-on sequence, are applied.

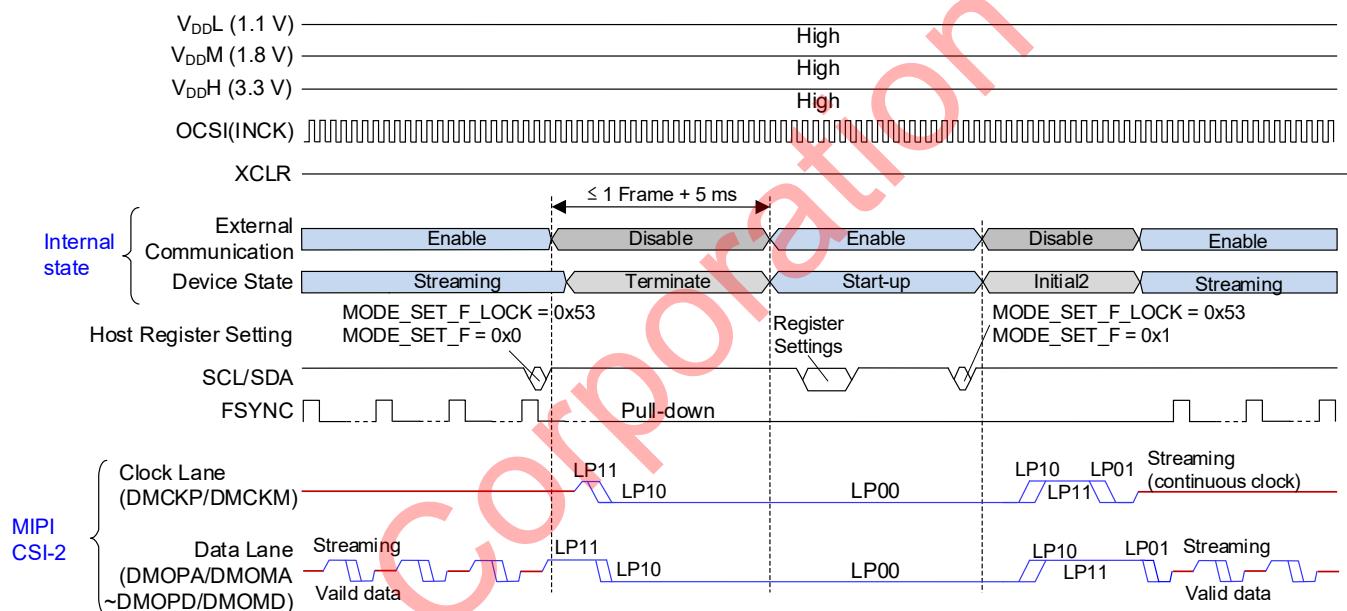


Figure 4-8 Start-up Sequence

To transition the sensor back to Streaming State after the sensor has transitioned to Start-up State, set the MODE_SET_F register to 0x1. The process in which the sensor transitions from Startup State to Streaming State is the same as described in “**4.3.1 Power-on Sequence**.”

4.5. Temperature Measurement

In Streaming State, the sensor continues to measure temperature and update the information. The host can confirm the temperature information using the RO_CD_DU_TEMP_SEN0_OUT and RO_CD_DU_TEMP_SEN1_OUT registers or the Front Embedded Data.

◇ Memo

- For details regarding the Front Embedded Data, refer to “[6.9.3.5.9 Temperature Information](#).”
- For details regarding how to measure temperature in Low-Power State, refer to “[4.5.1 STBY-TMPR Sequence](#).”

4.5.1. STBY-TMPR Sequence

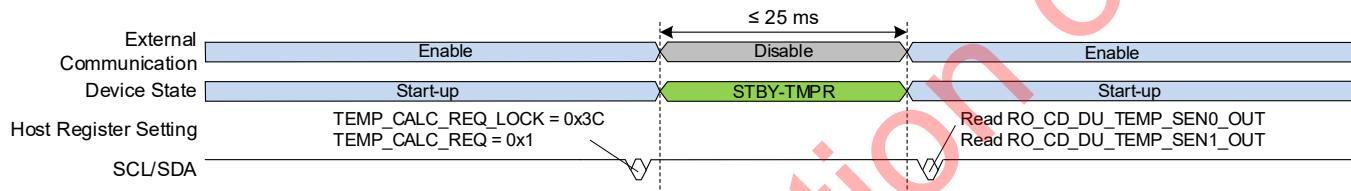


Figure 4-9 STBY-TMPR Sequence

To obtain the sensor's temperature while the sensor is in Start-up State, perform the procedure as follows:

- Set the TEMP_CALC_REQ register to 0x1.**
When the sensor starts temperature measurement, it cannot perform I²C communication. The TEMP_CALC_REQ register is compatible with the Application Lock function. For details, refer to “[3.1.5 Application Lock Function](#).”
- Set the TEMP_CALC_REQ register to 0x1 and wait until the DEVSTS register changes to 0x2 (Start-up State).**
After setting the TEMP_CALC_REQ register to 0x1, the sensor completes the temperature measurement within 25 ms and returns to Start-up State. When the temperature measurement is complete, the sensor applies the measured value to the RO_CD_DU_TEMP_SEN0_OUT and RO_CD_DU_TEMP_SEN1_OUT registers.
- Obtain the temperature information from the RO_CD_DU_TEMP_SEN0_OUT and RO_CD_DU_TEMP_SEN1_OUT registers.**

◇ Memo

- The same procedure applies to the case of temperature measurement in “Safe State Mode” State.
- The host can check the measurement value using the Front Embedded Data. For details, refer to “[6.9.3.5.9 Temperature Information](#).”

4.6. Sleep Sequence

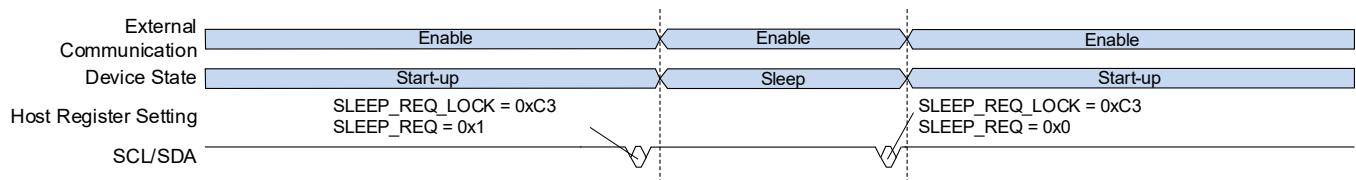


Figure 4-10 Sleep Sequence

To transition the sensor to Sleep State, perform the following procedure:

- 1. Set the SLEEP_REQ register to 0x1.**
The SLEEP_REQ register is compatible with the Application Lock function. For details, refer to “[3.1.5 Application Lock Function](#).”
- 2. Set the SLEEP_REQ register to 0x1 and wait until the DEVSTS register changes to 0x8 (Sleep State).**
The host can configure various settings including the sensor’s drive mode while the sensor is in Sleep State. The host cannot access the Serial NOR Flash device.
- 3. To transition the sensor back to Start-up State after it has transitioned to Sleep State, set the SLEEP_REQ register to 0x1.**

4.7. When Transitioning the Sensor to “Safe State Mode” State

4.7.1. “Safe State Mode” State Sequence

The sensor may transition to “Safe State Mode” State when any safety mechanism of the sensor detects a fault. For details regarding how these functions detect a fault, refer to the IMX623-AA** “Safety Application Note.”

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4.8. The Registers That Can Be Changed While the Sensor Is in Streaming State

"**Table 4-6**" shows the registers that can be changed while the sensor is in Streaming State. Any registers in categories not listed in "**Table 4-6**" must be set while the sensor is in Start-up State. Categories described as "With exceptions" in the "Remarks" column of "**Table 4-6**" indicate that they include the registers, the settings of which cannot be changed while the sensor is in Streaming State. For details, refer to "**Table 4-7**." Set the registers in "**Table 4-7**" while the sensor is in Start-up State.

Table 4-6 The Category of the Registers, the Settings of Which Can Be Changed While the Sensor Is in Streaming State

Category Name	Remarks
CTRL1	Available
CMD_TRG	With exceptions
CONFIG	With exceptions
CMN	With exceptions
SYS_CTRL	With exceptions
SCENE_CFG	With exceptions
SCENE_DATA	Available
AE	With exceptions
AE_DGRM	Available
AE_FLC	Available
AE_FRM	Available
AE_OPD	Available
AE_HDR	Available
HDR	Available
PWL	Available
AWB	With

Category Name	Remarks
	exceptions
AWB_FRM	Available
AWB_OPD	With exceptions
AWB_ADJ	With exceptions
PICT_CTRL	Available
PICT_INTERLOCKTYPE	Available
PICT_OB	Available
PICT_STC	Available
PICT_DYC	Available
PICT_RAWNR	Available
PICT_SPSHD	Available
PICT_SHD	Available
VIF	With exceptions
SM_CFG	With exceptions
USER	Available
FW_MODE_POST	Available
PICT_SPSHD_GAIN_OTP	Available

Table 4-7 The Registers, the Settings of Which Cannot Be Changed While the Sensor Is in Streaming State

Category Name	Register Name	Category Name	Register Name
CMD_TRG	OTP_WRITE_START BIST_ENTRY BIST_STANDBY BIST_ACTIVATE_ERROR SLEEP_REQ TEMP_CALC_REQ CHNG_TRANS_MODE	VIF	NORMB PRER PREB IFD_DATATYPE_FEBD_SEL IFD_DATATYPE_REBD_SEL IFD_DATATYPE_OB_SEL IFD_DATATYPE_VISIBLE_CTRLSEL IFD_DATATYPE_VISIBLE_INVALID_CTRLSEL IFD_VCID_NUM_SEL_CTRLSEL IFD_VCID0_CTRLSEL IFD_VCID1_CTRLSEL IFD_VCID2_CTRLSEL IFD_VCID3_CTRLSEL IFD_DATATYPE_FEBD IFD_DATATYPE_REBD IFD_DATATYPE_OB
CONFIG	EXT_I2C_SLVADR RSTCFG_SLVADR_F EXT_I2C_TRANS_MODE EXT_I2C_CLK_STRETCH_EN EXT_I2C_ACK_RESPONSE FLASH_SIZE INIT_MASK_CNT_ MUTE_CNT_ REBD_STC_INFO_DISABLE	VIF	IFD_DATATYPE_VISIBLE_INVALID IFD_VCID_NUM_SEL IFD_VCID0 IFD_VCID1 IFD_VCID2 IFD_VCID3
CMN	H_REVERSE_ V_REVERSE_ LID_ BID_ OBVID_ VMAX ADBIT RAWOUTMODE_	SM_CFG	IFD_DATATYPE_VISIBLE_INVALID IFD_VCID_NUM_SEL IFD_VCID0 IFD_VCID1 IFD_VCID2 IFD_VCID3 MODE_SET_F_LOCK SLEEP_REQ_LOCK TEMP_CALC_REQ_LOCK BIST_LOCK ECM_LOCK H_REVERSE_APL V_REVERSE_APL LID_APL BID_APL OBVID_APL SG_MODE_APL INIT_MASK_CNT_APL MUTE_CNT_APL CHNG_TRANS_MODE_APL
SYS_CTRL	DCROP_DATA_SEL		
SCENE_CFG	SCN_NFRAME_AUTO_CNT_EN SCN_NFRAME_MAX		
AE	AEMODE		
AWB	WS_INIT INITMOVE_GIVEUP_CNT ATW_INITMASK INIT_CONT_WSO_R INIT_CONT_WSO_B INIT_CONT_WS1_R INIT_CONT_WS1_B		
AWB_OPD	RAWTHR_MODE		
AWB_ADJ	NORMR		

4.9. Updating the Serial NOR Flash Device

To update the Serial NOR Flash device via the sensor, use the method described in “[Chapter 3 Setting Registers via Serial Communication](#).” This section explains the following two cases:

- Write the data provided by SSS to the Serial NOR Flash device.
- Change the value of the desired register to overwrite this value to the Serial NOR Flash device.

4.9.1. Writing the Register Configuration File to the Serial NOR Flash Device

When using the Serial NOR Flash device for the first time, be sure to first follow this procedure because these settings are necessary to be written for image output. “[Figure 4-11](#)” illustrates the procedure for writing the Register Configuration File provided by SSS to the Serial NOR Flash device.

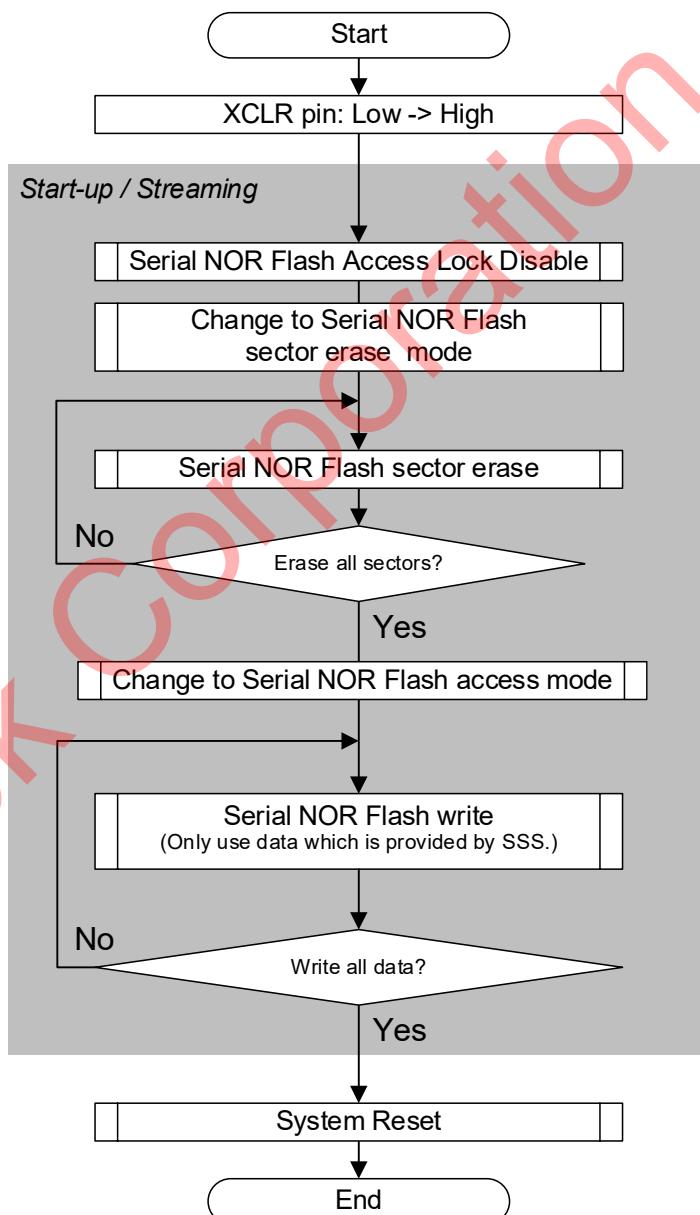


Figure 4-11 The Flow of Writing the Register Configuration File Provided by SSS to the Serial NOR Flash Device

- The SSS-provided Register Configuration File is generated on the assumption that the settings are written to a 4-Mbit reserved region. For this reason, sector-erase a 4-Mbit region of the Serial NOR Flash device and then write these settings to the region.
- To check if the settings have been correctly written to the Serial NOR Flash device, first reset the sensor and then check the Serial NOR Flash device's state. For details, refer to “[2.2.4 The State of the Serial NOR Flash Device](#).”

4.9.2. When Writing the Current Register Value(s) to the Serial NOR Flash Device

This section describes how to change a register's value and how to write the value to the Serial NOR Flash device.

◆ **Note**

When using the Serial NOR Flash device for the first time, first follow the procedure described in “[4.9.1 Writing the Register Configuration File to the Serial NOR Flash Device](#).”

■ Flow of Saving and Restoring Register Values

To change the SSS-provided register value(s) and start up the sensor, change the sensor's value(s) and then write the value(s) to the Serial NOR Flash device.

“[Figure 4-12](#)” illustrates the flow of writing changed values to the Serial NOR Flash device. The saved register value(s) are restored from the Serial NOR Flash device by the sensor while the sensor is in Initial1 State from the next startup onward.

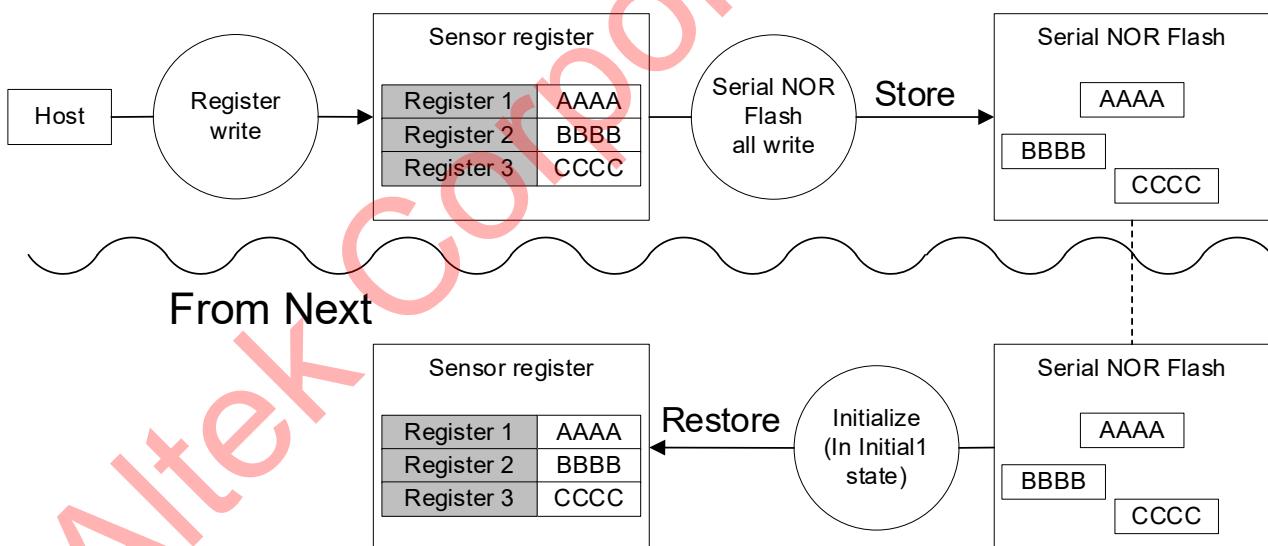


Figure 4-12 The Flow of Storing and Restoring Changed Register Values to and from the Serial NOR Flash Device

■ Procedure for Writing Register Value(s) to the Serial NOR Flash Device

“Figure 4-13” illustrates the procedure for writing the current register value(s) to the Serial NOR Flash device. To write data to the Serial NOR Flash device when updating register value(s), use the Serial NOR Flash All Write command.

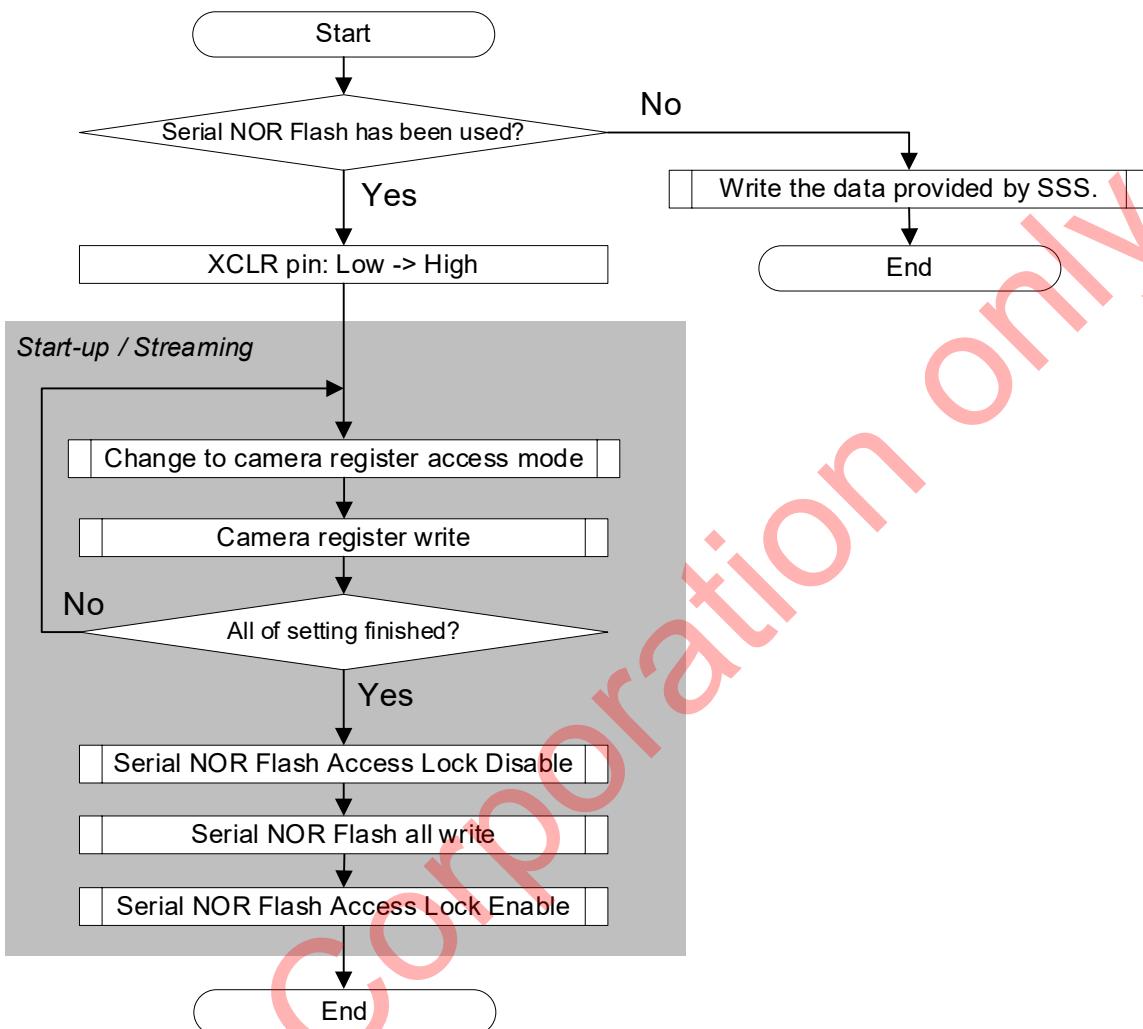


Figure 4-13 The Flow of Writing the Current Register Value(s) to the Serial NOR Flash Device

❖ Memo

- For details regarding the method for communicating with the sensor using the Serial NOR Flash All Write command, refer to “**3.5.1.2 Serial NOR Flash All Write Command**.”
- After writing to the Serial NOR Flash device, to check if the settings have been correctly written, first reset the sensor and then check the Serial NOR Flash device’s state. For details, refer to “**2.2.4 The State of the Serial NOR Flash Device**.”

4.9.3. Points to Note When Writing the User's Data to the Serial NOR Flash Device

When using a Serial NOR Flash device of 8 Mbits or greater, the desired data can be written to the addresses which are 0x0008_0000 or greater.

- The area of the addresses which are less than or equal to 0x0007_FFFF can be updated using the Serial NOR Flash All Write command.
- When writing data to the area of the addresses which are 0x0008_0000 or greater, refer to “[3.5.1.3.3 Serial NOR Flash Write Subcommand](#).”

◆ Note

- When accessing the area of the addresses which are 0x0008_0000 or greater, set the FLASH_SIZE register to the capacity of the corresponding Serial NOR Flash device.
- After changing the value of the FLASH_SIZE register, update the Serial NOR Flash device and reset the sensor.

4.10. Interface

4.10.1. Input Registers

Table 4-8 Startup Control-Related Input Registers

[SETUP]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A00	2	14:0	MODE_SEL	R/W	U15.0	This register is used to set the drive mode index number.
		15	MODE_SET_F	R/W	U1.0	This register is used to set the state transition. 0: Transition to Start-up State 1: Transition to Streaming State * Enabled only when the MODE_SET_LOCK register is 0x53.

[CMD_TRG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A12	1	0	BIST_ENTRY	R/W	U1.0	This register is used to transition the sensor to BIST Standby. <ul style="list-style-type: none">When the host sets this register to 0x1 while the sensor is in Start-up State, the sensor transitions to BIST Standby via BIST Init. * Enabled only when the BIST_LOCK register is 0xA3.
		1	BIST_STANDBY			This register is used to set an execution of Logic BIST and Memory BIST. <ul style="list-style-type: none">When the host sets this register to 0x0 while the sensor is in BIST Standby State, the sensor executes Logic BIST and then Memory BIST. After the sensor executes Memory BIST, the sensor transitions to Reset State. * Enabled only when the BIST_LOCK register is 0xA3.
0x8A18	1	0	SLEEP_REQ	R/W	U1.0	This register is used to set the transition to Sleep State. 0: Transition to Start-up State 1: Transition to Sleep State * Enabled only when the SLEEP_REQ_LOCK register is 0xC3.
0x8A1C	1	0	TEMP_CALC_REQ	R/W	U1.0	This register is used to issue a temperature measurement request. <ul style="list-style-type: none">When the host sets this register to 0x1 while the sensor is in Start-up State, the sensor transitions to STBY-TMPR State and starts temperature measurement.When the host sets this register to 0x1 while the

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
						<p>sensor is in "Safe State Mode" State, the sensor transitions to SAFE-TMPR State and starts temperature measurement.</p> <ul style="list-style-type: none">• Upon receiving a request, this register automatically reverts to 0x0.• This register is enabled only when the TEMP_CALC_REQ_LOCK register is 0x3C.

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[CONFIG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A58	4	31:0	FLASH_SIZE	R/W	U32.0	<p>This register is used to set the capacity of the Serial NOR Flash device.</p> <p>4 Mbits: 0x080000 8 Mbits: 0x100000 16 Mbits: 0x200000 32 Mbits: 0x400000</p> <p>* When not using a Serial NOR Flash device, setting this register is unnecessary.</p>

[SG_CTRL]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8AF0	1	1:0	SG_MODE_	R/W	U2.0	<p>This register is used to select the sync method.</p> <p>0: Internal sync 1: External pulse-based sync 2: Shutter trigger-based sync 3: Setting prohibited</p>

[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBEFO	1	7:0	MODE_SET_F_LOCK	R/W	U8.0	<p>This register is used to enable the MODE_SET_F register for the Application Lock function.</p> <p>0x53: Enabled</p>
0xBEF2	1	7:0	SLEEP_REQ_LOCK	R/W	U8.0	<p>This register is used to enable the sensor to transition from Start-up State to Sleep State or vice versa.</p> <p>0xC3: Enabled</p>
0xBEF3	1	7:0	TEMP_CALC_REQ_LOCK	R/W	U8.0	<p>This register is used to enable the sensor to transition either from Start-up State to STBY-TMPR State or from "Safe State Mode" State to SAFE-TMPR State.</p> <p>0x3C: Enabled</p>
0xBEF5	1	7:0	BIST_LOCK	R/W	U8.0	<p>This register is used to enable the sensor to transition either from Start-up State to BIST Init State or from BIST Standby State to BIST Active State.</p> <p>0xA3: Enabled</p>
0xBF14	1	1:0	SG_MODE_APL	R/W	U2.0	<p>This register is used to be compared with the SG_MODE_ register for the Application Lock function.</p>

[OTP]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBFC6	1	7:0	OTP_BIST_AUTO_EXEC	R/W	U8.0	<p>This register is used to enable or disable an automatic execution of Logic BIST and Memory BIST.</p> <p>0: Automatic execution disabled 1: Automatic execution enabled</p> <p>Any other settings are prohibited.</p> <ul style="list-style-type: none"> To enable the automatic execution of Logic BIST and Memory BIST at sensor startup, set this register to 1 and then update the Serial NOR Flash device.

4.10.2. Output Registers

Table 4-9 Startup Control-Related Output Registers

[SYS_COM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x6005	1	7:0	DEVSTS	R	U8.0	This register indicates the sensor's state. 1: Start-up (Available only immediately after powering on the sensor) 2: Start-up 5: Streaming 8: Sleep 13: Safe State Mode 17: BIST Standby

[SM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x838C	1	0	BIST_COMP	R	U1.0	This register indicates the "Logic BIST and Memory BIST completion" flag. 0x0: In progress 0x1: Complete

[STATE]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1F40	2	11:0	RO_CD_DU_TEMP_SEN_0_OUT	R	U8.4	This register indicates the temperature information of Temperature Sensor 1. The sensor's temperature [°C] = the sensor's temperature information / 16 – 50
0x1F42	2	11:0	RO_CD_DU_TEMP_SEN_1_OUT	R	U8.4	This register indicates the temperature information of Temperature Sensor 2. The sensor's temperature [°C] = the sensor's temperature information / 16 – 50

Chapter 5 Basic Functions

This chapter describes the following functions required to transmit images using the sensor.

Table 5-1 Basic Functions

Function Name	Applications
HDR Function	Controls HDR imaging
Exposure Control Function	Adjusts image brightness.
White Balance Function	Adjusts color.
Clamp Function	Compensates for the characteristics of the sensor and the optical system.
RAW Noise Reduction Function	Enhances output image quality.
Spot Pixel Compensation Function	Compensates for the characteristics of the sensor and the optical system.
Dark Shading Compensation Function	
Pixel Shading Compensation Function	
Lens Shading Compensation Function	Compresses gradation after HDR imaging.
PWL Function (Gradation Compression Function)	

5.1. HDR Function

5.1.1. Functional Purpose

The HDR function combines multiple images with different sensitivities, enabling the sensor to transmit images without blown-out highlights or blocked-up shadows when shooting a subject with a wide dynamic range from low to high illuminance.

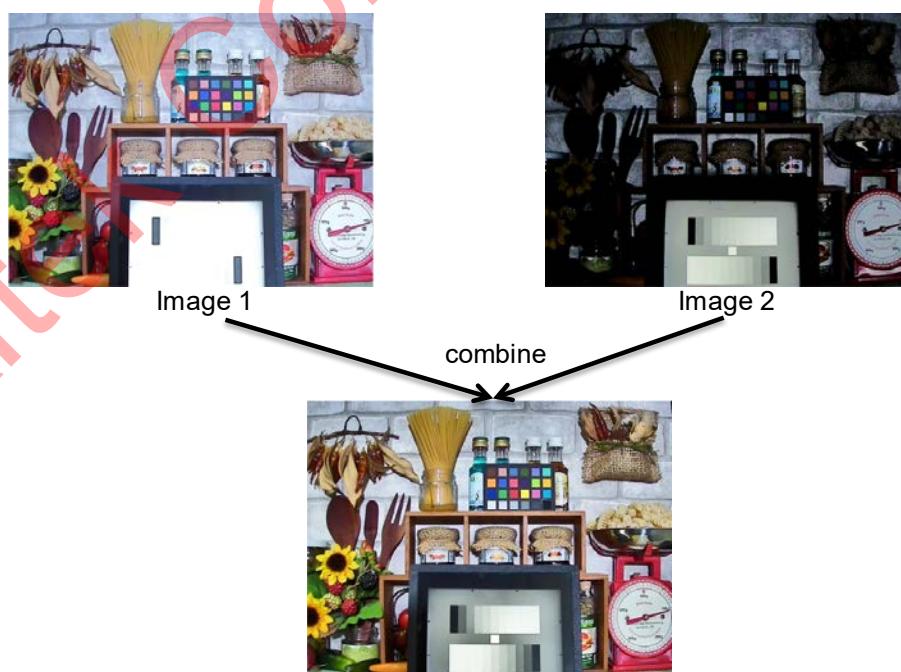


Figure 5-1 HDR Imaging

5.1.2. Functional Overview

The sensor generates images with a wide dynamic range using signals of four lines (SP1_HCG, SP1_LCG, SP2H and SP2L) which vary in sensitivities. “**Figure 5-2**” illustrates an example of HDR imaging using signals from the four lines. The figure illustrates switching lines from SP1_HCG to SP1_LCG, from SP1_LCG to SP2H and from SP2H to SP2L based on SP1_HCG that has the highest sensitivity among the four lines.

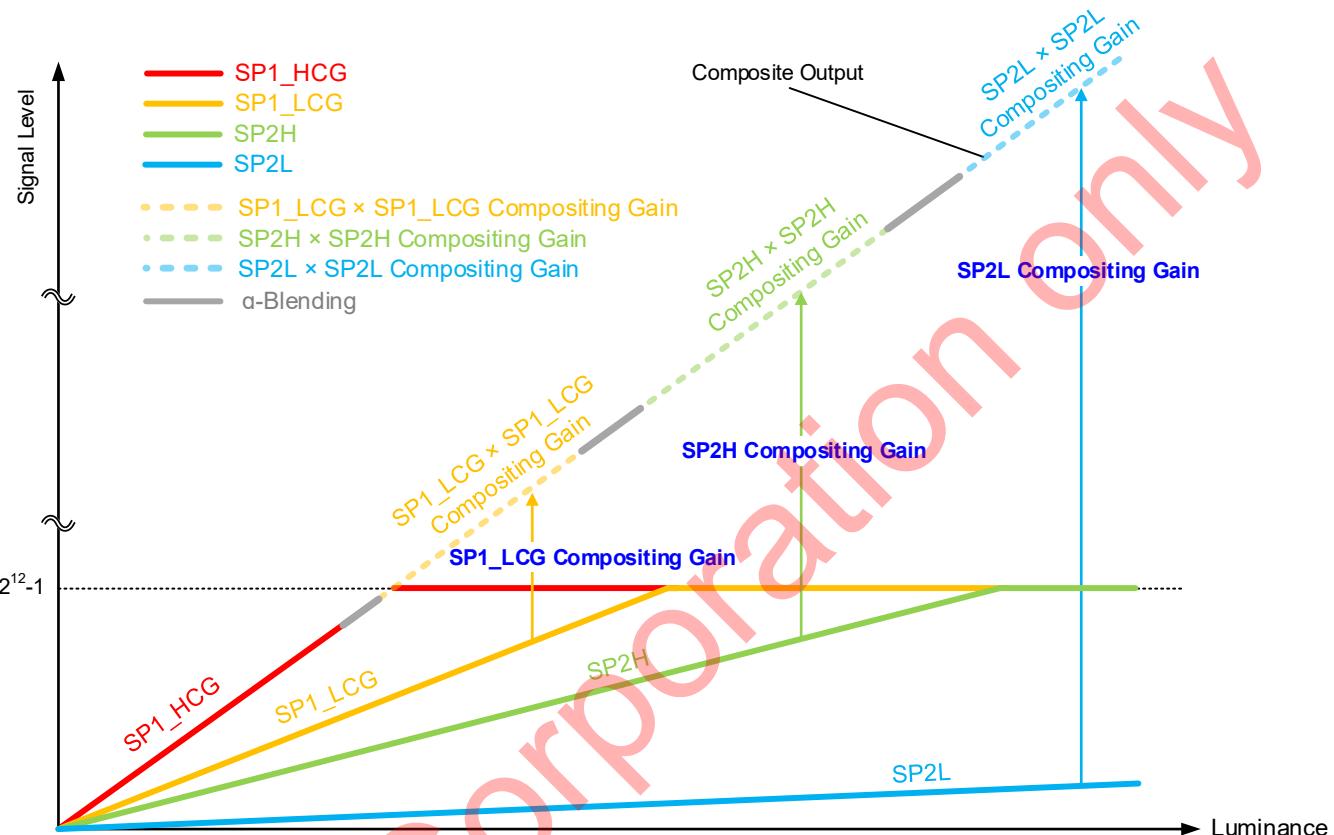


Figure 5-2 Depiction of HDR Imaging by Combining Signals from the Four Lines

Before HDR imaging, each line's signal level varies due to exposure times or sensitivity ratios of pixels. To adjust each signal level to the signal from SP1_HCG, which is the reference, the HDR function adjusts each signal level by applying compositing gains.

In this chapter, each compositing gain is named as follows:

- Between SP1_HCG and SP1_LCG: SP1_LCG Compositing Gain
- Between SP2H and SP2L: SP2L Compositing Gain
- Between SP1 and SP2: SP2 Compositing Gain

To reduce coloring caused by HDR processing errors in each line, the HDR function performs alpha-blending on signals in the proximity of a composite region, thereby smoothing signal transition.

5.1.3. Functional Specifications

5.1.3.1. HDR Imaging

"Figure 5-3" illustrates the signal processing, in which the sensor sequentially combines the signals from each line.

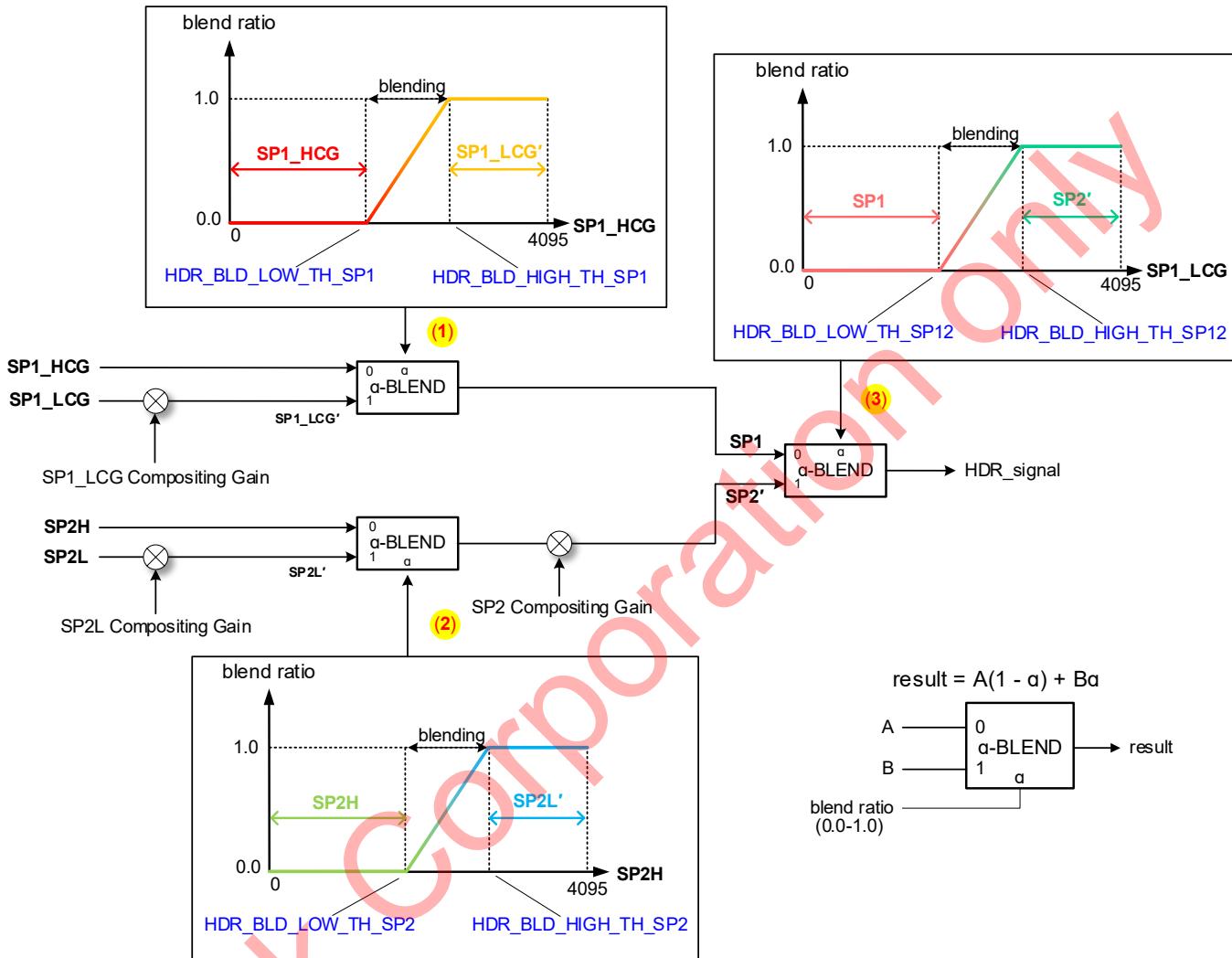


Figure 5-3 HDR Imaging Signal Process Flow

The sensor's HDR imaging consists of three processes: (1), (2) and (3). In Process (1), the sensor combines the signals from the **SP1_HCG** and **SP1_LCG'** lines, the latter of which is obtained by multiplying the signal from **SP1_LCG** by the **SP1_LCG** compositing gain. The result is represented as **SP1**. In Process (2), the sensor combines **SP2H** and **SP2L'**, the latter of which is obtained by multiplying **SP2L** by the **SP2L** compositing gain. The result is represented as **SP2**. In Process (3), the sensor combines **SP1** and **SP2'**, the latter of which is obtained by multiplying **SP2** by the **SP2** compositing gain. The sensor combines four signal lines by utilizing these three processes.

5.1.3.2. Alpha-Blending and Compositing Thresholds

This section explains the details of HDR imaging in order, (1), (2) and (3), as illustrated in "Figure 5-3." HDR imaging consists of two processes: "Blend Ratio Calculation" and "Alpha-Blending."

"Figure 5-4" illustrates how to calculate the blend ratio. The horizontal axis represents the reference signal (cmp_sig) and the vertical axis represents the blend ratio. The sensor calculates the blend ratio, ranging from 0.0 to 1.0, based on the relationship between the reference signal (cmp_sig), lower compositing threshold (th_low) and upper compositing threshold (th_high).

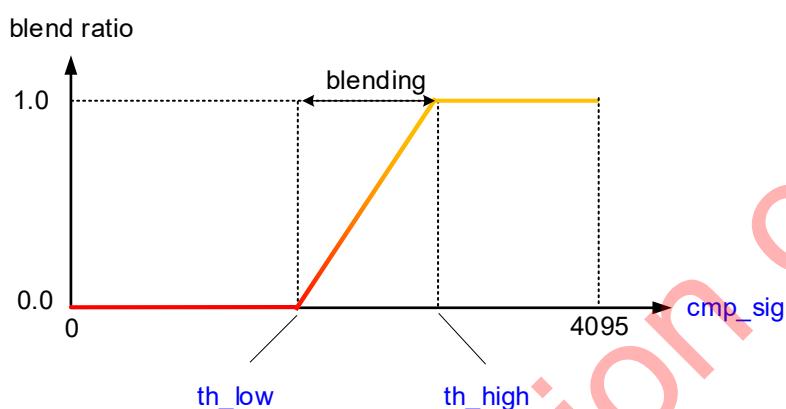


Figure 5-4 Blend Ratio Calculation

If the reference signal (cmp_sig) level is less than the th_low, the blend ratio is 0.0. If the level is higher than the th_high, the blend ratio is 1.0. If the level is between th_low and th_high, the sensor calculates the blend ratio from the reference signal (cmp_sig), th_low, and th_high.

The equations for calculating the blend ratio are shown as follows:

- Case 1: Less than or equal to the lower compositing threshold value ($\text{cmp_sig} \leq \text{th_low}$)
 $\text{blend_ratio} = 0.0$
- Case 2: Blend region ($\text{th_low} < \text{reference signal (cmp_sig)} < \text{th_high}$)
 $\text{blend_ratio} = (\text{cmp_sig} - \text{th_low}) / (\text{th_high} - \text{th_low})$
- Case 3: Greater than or equal to the upper compositing threshold value ($\text{cmp_sig} \geq \text{th_high}$)
 $\text{blend_ratio} = 1.0$

"Figure 5-5" is a signal processing diagram, in which the sensor alpha-blends two signals (Signals A and B) using the aforementioned blend ratio. The sensor transmits Signal A or Signal B when the blend ratio is 0.0 or 1.0, respectively. As the blend ratio gradually changes from 0.0 to 1.0, the output signal gradually changes from Signal A to Signal B.

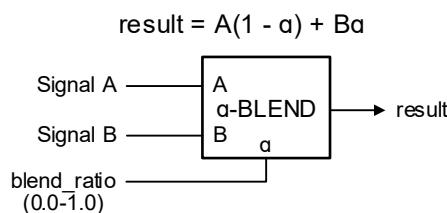


Figure 5-5 Alpha Blending

"**Table 5-2**" shows the relationships between the following:

- cmp_sig, th_low, th_high, Signal A and Signal B in "**Figure 5-4**" and "**Figure 5-5**"
- The signal and register names in HDR imaging processes (1) to (3) in "**Figure 5-3**"

Table 5-2 The Relationship Between the Signals and Compositing Thresholds

No.	Alpha Blending		cmp_sig	th_low	th_high
	Signal A	Signal B			
(1)	SP1_HCG	SP1_LCG'	SP1_HCG	HDR_BLD_LOW_TH_SP1	HDR_BLD_HIGH_TH_SP1
(2)	SP2H	SP2L'	SP2H	HDR_BLD_LOW_TH_SP2	HDR_BLD_HIGH_TH_SP2
(3)	SP1	SP2'	SP1_LCG	HDR_BLD_LOW_TH_SP12	HDR_BLD_HIGH_TH_SP12

Set a compositing threshold to satisfy the following conditions:

- $\text{th_low} \leq \text{th_high}$
- $\text{th_high} \leq 4095$

5.1.3.2.1. Selecting the Signal Switching Method

Regarding HDR signal switching, there are two methods: Pixel Value Switching and Luminance Switching.

- Pixel Value Switching Method:
The HDR algorithm individually measures the signal level for each pixel to switch signals.
- Luminance Switching Method:
The HDR algorithm measures signal levels in 9 pixels, consisting of 3 rows and 3 columns of pixels, including other color filters, to switch signals.

For details regarding the features, the benefits and negative effects of each method, refer to the IMX623-AA** "Image Tuning Manual."

This section explains how to select the signal switching method. Select the signal switching method using the following registers:

- IR_IS_ALP_BLD_BASE_SEL_SP1 register for the method between SP1_HCG and SP1_LCG
- IR_IS_ALP_BLD_BASE_SEL_SP2 register for the method between SP2H and SP2L
- IR_IS_ALP_BLD_BASE_SEL_SP12 register for the method between SP1 and SP2

When using the Pixel Value Switching Method, set the aforementioned registers to 0.

Alternatively, when using the Maximum Pixel Value Switching Method, set the aforementioned registers to 1. The user can individually select these methods at the three positions in HDR processing as illustrated in "**Figure 5-3.**"

◇ **Memo**

When changing the signal switching methods, be sure to adjust each compositing threshold corresponding to the pixel values or luminance.

5.1.3.3. Compositing Gain

This section explains how the sensor calculates compositing gain.

The sensor calculates compositing gains for each color filter and can be calculated by using the following equations:

- SP1_LCG Compositing Gain

$$\text{HDR_SGAIN_SP1_y_OUT} = \frac{\text{SENS_AGAIN0}}{\text{SENS_AGAIN1}} \times \text{sp1_sens_ratio} \times \text{HDR_SGAIN_ADJ_SP1_y}$$

- SP2L Compositing Gain

$$\text{HDR_SGAIN_SP2_y_OUT} = \frac{\text{SENS_AGAIN2}}{\text{SENS_AGAIN3}} \times \text{sp2_sens_ratio} \times \text{HDR_SGAIN_ADJ_SP2_y}$$

- SP2 Compositing Gain

$$\text{HDR_SGAIN_SP2_y_OUT} = \frac{\text{SHT_TIME_SP1}}{\text{SHT_TIME_SP2}} \times \frac{\text{SENS_AGAIN0}}{\text{SENS_AGAIN2}} \times \text{sp1_sp2_sens_ratio} \times \text{HDR_SGAIN_ADJ_SP12_y}$$

* The symbol **y** denotes R, GR, GB or B, depending on the color filter, for which the compositing gain is calculated.

◆ Note

- The results may differ from the values of the relevant registers due to the bit precision during calculation processes.
- Each value of the SENS_AGAINx (x = 0, 1, 2, 3) registers is in dB. When calculating the compositing gain using the following equations, convert a value in dB into a magnification factor.

■ Sensitivity ratio

The sensitivity ratios (sp1_sens_ratio and sp1_sp2_sens_ratio) are the ratios of the sensitivity between sub-pixels. Since the sensitivity ratio varies from sensor to sensor, the sensitivity ratios are saved to the OTP area at the SSS factory. The user can adjust sensitivity ratios, which change due to the characteristics of the optical system, by using the "compositing gain adjustment" parameters (the values of the HDR_SGAIN_ADJ_SP1_y (y = R, GR, GB, B) and HDR_SGAIN_ADJ_SP2_y (y = R, GR, GB, B) registers).

Regarding the sensitivity ratio, the user can select either SSS's factory-default values or the values specified by the host using the AE_SENSRATIO_SEL register. For details, refer to "Table 5-3."

Table 5-3 Sensitivity Ratio Used to Calculate Compositing Gain

AE_SENSRATIO_SEL	The Values To Be Used			Description
	sp1_sens_ratio	sp2_sens_ratio	sp1_sp2_sens_ratio	
0	AE_SENSRATIO_SP1_y	AE_SENSRATIO_SP2_y	AE_SENSRATIO_SP12_y	Sensitivity ratio specified by the host
1	OTP_SENS_RATIO_z_S P1_H OTP_SENS_RATIO_z_S P1_L	OTP_SENS_RATIO_z_S P2_H OTP_SENS_RATIO_z_S P2_L	OTP_SENS_RATIO_z_S P12_H OTP_SENS_RATIO_z_S P12_M OTP_SENS_RATIO_z_S P12_L	Factory-default value

* The symbol **y** denotes R, GR, GB or B whereas the symbol **z** denotes CF0, CF1, CF2 or CF3, depending on the color filter, for

which the compositing gain is calculated.

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5.1.3.4. Artifact Compensation

When setting different exposure times to the SP1 and SP2 lines during HDR imaging, artifacts such as false colors may occur in the regions where moving subjects are present. See “[Figure 5-6](#)” for details. The Artifact Compensation function can reduce these artifacts.

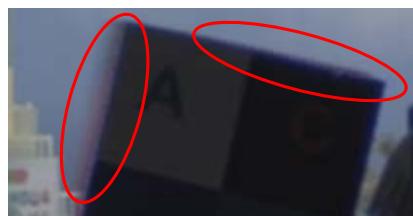


Figure 5-6 Example of Artifacts in the Regions Where Moving Subjects Are Present

5.1.3.4.1. Enabling or Disabling Motion Artifact Compensation

Motion Artifact Compensation is a function that reduces artifacts which occur during HDR imaging. The function determines whether a moving subject is present from the signal differentials between the SP1_LCG and SP2H lines. When detecting any moving subjects, the function replaces the detected region with the output of the line selected using the IR_IS_ALP_MDET_MODE register.

“[Table 5-4](#)” describes the processing of motion artifact compensation corresponding to the value of the IR_IS_ALP_MDET_MODE register. When not performing motion artifact compensation, set the IR_IS_ALP_MDET_MODE register to 0.

Table 5-4 Method for Setting Motion Artifact Compensation

IR_IS_ALP_MDET_MODE	Description
0	Motion artifact compensation is disabled.
1	The function replaces the regions where moving objects have been detected with SP1's signal (i.e., the combined signal between SP1_HCG and SP1_LCG).
2	The function replaces the regions where moving objects have been detected with SP2's signal (i.e., the combined signal between SP2H and SP2L).
3	The function replaces the regions with the signals of either SP1 or SP2 whichever has the maximum value.

5.1.3.4.2. Enabling or Disabling False Color Correction

False colors may occur when certain colors are saturated in high-luminance regions. In particular, there may be certain false colors around moving subjects.

False Color Correction performs the following processing:

- Identifies regions where false colors have occurred due to saturation.
- Compensates for the entire region or the regions where moving subjects have been detected.

To enable or disable the Motion Artifact Compensation function, set the IR_IS_ALP_SUP_ON register to 1 or 0 respectively.

5.1.4. Interface

5.1.4.1. Input Registers

Table 5-5 Input Registers for the HDR Function

[AE_HDR]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xAE56	1	0	AE_SENSRATIO_SEL	R/W	U1.0	Selection of sensitivity ratio 0: The register's value 1: The OTP area's value
0xAE58	2	14:0	AE_SENSRATIO_SP1_R	R/W	U3.12	Setting of the sensitivity ratio for the CF0 pixels between SP1_HCG and SP1_LCG Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE5A	2	14:0	AE_SENSRATIO_SP1_GR	R/W	U3.12	Setting of the sensitivity ratio for the CF1 pixels between SP1_HCG and SP1_LCG Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE5C	2	14:0	AE_SENSRATIO_SP1_GB	R/W	U3.12	Setting of the sensitivity ratio for the CF2 pixels between SP1_HCG and SP1_LCG Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE5E	2	14:0	AE_SENSRATIO_SP1_B	R/W	U3.12	Setting of the sensitivity ratio for the CF3 pixels between SP1_HCG and SP1_LCG Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE60	2	14:0	AE_SENSRATIO_SP2_R	R/W	U3.12	Setting of the sensitivity ratio for the CF0 pixels between SP2H and SP2L Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE62	2	14:0	AE_SENSRATIO_SP2_GR	R/W	U3.12	Setting of the sensitivity ratio for the CF1 pixels between SP2H and SP2L Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE64	2	14:0	AE_SENSRATIO_SP2_GB	R/W	U3.12	Setting of the sensitivity ratio for the CF2 pixels between SP2H and SP2L Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE66	2	14:0	AE_SENSRATIO_SP2_B	R/W	U3.12	Setting of the sensitivity ratio for the CF3 pixels between SP2H and SP2L Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE68	3	21:0	AE_SENSRATIO_SP1_2_R	R/W	U10.12	Setting of the sensitivity ratio for the CF0 pixels between SP1 and SP2 Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE6C	3	21:0	AE_SENSRATIO_SP1_2_GR	R/W	U10.12	Setting of the sensitivity ratio for the CF1 pixels between SP1 and SP2 Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE70	3	21:0	AE_SENSRATIO_SP1_2_GB	R/W	U10.12	Setting of the sensitivity ratio for the CF2 pixels between SP1 and SP2 Enabled when the AE_SENSRATIO_SEL register is 0.
0xAE74	3	21:0	AE_SENSRATIO_SP1_2_B	R/W	U10.12	Setting of the sensitivity ratio for the CF3 pixels between SP1 and SP2 Enabled when the AE_SENSRATIO_SEL register is 0.
0x9C24	4	31:0	NORM_GAIN_Y1	R/W	U1.31	Setting of the Illuminance Interlocking Normalization Gain

[HDR]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xAFB4	2	11:0	HDR_BLD_HIGH_TH_SP1	R/W	U12.0	This register's value is the upper threshold used to calculate the blend ratio between SP1_HCG and SP1_LCG.
0xAFB6	2	11:0	HDR_BLD_LOW_TH_SP1	R/W	U12.0	This register's value is the lower threshold used to calculate the blend ratio between SP1_HCG and SP1_LCG.
0xAFB8	2	11:0	HDR_BLD_HIGH_TH_SP2	R/W	U12.0	This register's value is the upper threshold used to calculate the blend ratio between SP2H and SP2L.
0xAFBA	2	11:0	HDR_BLD_LOW_TH_SP2	R/W	U12.0	This register's value is the lower threshold used to calculate the blend ratio between SP2H and SP2L.
0xAFBC	2	11:0	HDR_BLD_HIGH_TH_SP12	R/W	U12.0	This register's value is the upper threshold used to calculate the blend ratio between SP1 and SP2.
0xAFBE	2	11:0	HDR_BLD_LOW_TH_SP12	R/W	U12.0	This register's value is the lower threshold used to calculate the blend ratio between SP1 and SP2.
0x9C38	2	14:0	HDR_SGAIN_ADJ_SP1_R	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF0 pixels between SP1_HCG and SP1_LCG
0x9C3A	2	14:0	HDR_SGAIN_ADJ_SP1_GR	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF1 pixels between SP1_HCG and SP1_LCG
0x9C3C	2	14:0	HDR_SGAIN_ADJ_SP1_GB	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF2 pixels between SP1_HCG and SP1_LCG
0x9C3E	2	14:0	HDR_SGAIN_ADJ_SP1_B	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF3 pixels between SP1_HCG and SP1_LCG
0x9C40	2	14:0	HDR_SGAIN_ADJ_SP2_R	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF0 pixels between SP2H and SP2L
0x9C42	2	14:0	HDR_SGAIN_ADJ_SP2_GR	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF1 pixels between SP2H and SP2L
0x9C44	2	14:0	HDR_SGAIN_ADJ_SP2_GB	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF2 pixels between SP2H and SP2L
0x9C46	2	14:0	HDR_SGAIN_ADJ_SP2_B	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF3 pixels between SP2H and SP2L
0x9C48	2	14:0	HDR_SGAIN_ADJ_SP12_R	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF0 pixels between SP1 and SP2
0x9C4A	2	14:0	HDR_SGAIN_ADJ_SP12_GR	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF1 pixels between SP1 and SP2
0x9C4C	2	14:0	HDR_SGAIN_ADJ_SP12_GB	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF2 pixels between SP1 and SP2
0x9C4E	2	14:0	HDR_SGAIN_ADJ_SP12_B	R/W	U3.12	Adjustment for the compositing gain calculated by the sensor for the CF3 pixels between SP1 and SP2

[CTRL1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x9C50	2	9:0	IR_IS_FBK_LMX_COEF_C00_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C00 element (SP2H).
0x9C52	2	9:0	IR_IS_FBK_LMX_COEF_C01_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C01 element (SP2H).

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x9C54	2	9:0	IR_IS_FBK_LMX_COEF_C_02_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C02 element (SP2H).
0x9C56	2	9:0	IR_IS_FBK_LMX_COEF_C_03_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C03 element (SP2H).
0x9C58	2	9:0	IR_IS_FBK_LMX_COEF_C_10_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C10 element (SP2H).
0x9C5A	2	9:0	IR_IS_FBK_LMX_COEF_C_11_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C11 element (SP2H).
0x9C5C	2	9:0	IR_IS_FBK_LMX_COEF_C_12_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C12 element (SP2H).
0x9C5E	2	9:0	IR_IS_FBK_LMX_COEF_C_13_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C13 element (SP2H).
0x9C60	2	9:0	IR_IS_FBK_LMX_COEF_C_20_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C20 element (SP2H).
0x9C62	2	9:0	IR_IS_FBK_LMX_COEF_C_21_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C21 element (SP2H).
0x9C64	2	9:0	IR_IS_FBK_LMX_COEF_C_22_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C22 element (SP2H).
0x9C66	2	9:0	IR_IS_FBK_LMX_COEF_C_23_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C23 element (SP2H).
0x9C68	2	9:0	IR_IS_FBK_LMX_COEF_C_30_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C30 element (SP2H).
0x9C6A	2	9:0	IR_IS_FBK_LMX_COEF_C_31_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C31 element (SP2H).
0x9C6C	2	9:0	IR_IS_FBK_LMX_COEF_C_32_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C32 element (SP2H).
0x9C6E	2	9:0	IR_IS_FBK_LMX_COEF_C_33_SP2H	R/W	S2.7	This register is used to set the linear matrix coefficient for the C33 element (SP2H).
0x9C70	2	9:0	IR_IS_FBK_LMX_COEF_C_00_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C00 element (SP2L).
0x9C72	2	9:0	IR_IS_FBK_LMX_COEF_C_01_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C01 element (SP2L).
0x9C74	2	9:0	IR_IS_FBK_LMX_COEF_C_02_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C02 element (SP2L).
0x9C76	2	9:0	IR_IS_FBK_LMX_COEF_C_03_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C03 element (SP2L).
0x9C78	2	9:0	IR_IS_FBK_LMX_COEF_C_10_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C10 element (SP2L).
0x9C7A	2	9:0	IR_IS_FBK_LMX_COEF_C_11_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C11 element (SP2L).
0x9C7C	2	9:0	IR_IS_FBK_LMX_COEF_C_12_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C12 element (SP2L).
0x9C7E	2	9:0	IR_IS_FBK_LMX_COEF_C_13_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C13 element (SP2L).

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x9C80	2	9:0	IR_IS_FBK_LMX_COEF_C20_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C20 element (SP2L).
0x9C82	2	9:0	IR_IS_FBK_LMX_COEF_C21_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C21 element (SP2L).
0x9C84	2	9:0	IR_IS_FBK_LMX_COEF_C22_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C22 element (SP2L).
0x9C86	2	9:0	IR_IS_FBK_LMX_COEF_C23_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C23 element (SP2L).
0x9C88	2	9:0	IR_IS_FBK_LMX_COEF_C30_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C30 element (SP2L).
0x9C8A	2	9:0	IR_IS_FBK_LMX_COEF_C31_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C31 element (SP2L).
0x9C8C	2	9:0	IR_IS_FBK_LMX_COEF_C32_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C32 element (SP2L).
0x9C8E	2	9:0	IR_IS_FBK_LMX_COEF_C33_SP2L	R/W	S2.7	This register is used to set the linear matrix coefficient for the C33 element (SP2L).
0x1B40	1	0	IR_IS_ALP_BLD_BASESEL_SP1	R/W	U1.0	This register is used to select the signal switching methods between SP1_HCG and SP1_LCG. 0: Pixel value switching method 1: Luminance switching method
0x1B41	1	0	IR_IS_ALP_BLD_BASESEL_SP2	R/W	U1.0	This register is used to select the signal switching methods between SP2H and SP2L. 0: Pixel value switching method 1: Luminance switching method
0x1B42	1	0	IR_IS_ALP_BLD_BASESEL_SP12	R/W	U1.0	This register is used to select the signal switching methods between SP1 and SP2. 0: Pixel value switching method 1: Luminance switching method
0x1B43	1	1:0	IR_IS_ALP_MDET_MODE	R/W	U2.0	This register is used to set the method for motion artifact compensation. 0: Motion artifact compensation disabled 1: Motion artifact compensation enabled (Signal replacement with SP1) 2: Motion artifact compensation enabled (Signal replacement with SP2) 3: Motion artifact compensation enabled (Signal replacement with the maximum value)
0x1B4D	1	0	IR_IS_ALP_SUP_ON	R/W	U1.0	This register is used to enable or disable the Motion Artifact Compensation function. 0: Motion artifact compensation disabled 1: Motion artifact compensation enabled
0x1B55	1	0	IR_IS_ALP_MED_WS_SP1H_ON	R/W	U1.0	This register is used to enable or disable white pixel compensation for signals which are used to calculate the blend ratio between SP1_HCG and SP1_LCG. 0: Disabled 1: Enabled • Valid only when pixel values are selected for these signals.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1B56	1	0	IR_IS_ALP_MED_BS_SP1_H_ON	R/W	U1.0	<p>This register is used to enable or disable black pixel compensation for signals which are used to calculate the blend ratio between SP1_HCG and SP1_LCG.</p> <p>0: Disabled 1: Enabled</p> <ul style="list-style-type: none"> Valid only when pixel values are selected for these signals.
0x1B62	1	0	IR_IS_ALP_MED_WS_SP2H_ON	R/W	U1.0	<p>This register is used to enable or disable white pixel compensation for signals which are used to calculate the blend ratio between SP2H and SP2L.</p> <p>0: Disabled 1: Enabled</p> <ul style="list-style-type: none"> Valid only when pixel values are selected for these signals.
0x1B63	1	0	IR_IS_ALP_MED_BS_SP2H_ON	R/W	U1.0	<p>This register is used to enable or disable black pixel compensation for signals which are used to calculate the blend ratio between SP2H and SP2L.</p> <p>0: Disabled 1: Enabled</p> <ul style="list-style-type: none"> Valid only when pixel values are selected for these signals.
0x1B6F	1	0	IR_IS_ALP_MED_WS_SP1L2L_ON	R/W	U1.0	<p>This register is used to enable or disable white pixel compensation for signals which are used to calculate the blend ratio between SP1 and SP2.</p> <p>0: Disabled 1: Enabled</p> <ul style="list-style-type: none"> Valid only when pixel values are selected for these signals.
0x1B70	1	0	IR_IS_ALP_MED_BS_SP1L2L_ON	R/W	U1.0	<p>This register is used to enable or disable black pixel compensation for signals which are used to calculate the blend ratio between SP1 and SP2.</p> <p>0: Disabled 1: Enabled</p> <ul style="list-style-type: none"> Valid only when pixel values are selected for these signals.

5.1.4.2. Output Registers

Table 5-6 Output Registers for the HDR Function

[OTP_COM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x81C0	1	7:0	OTP_SENS_RATIO_CFO_SP1_L	R	U8.0	<p>The sensitivity ratio stored in the OTP ROM for the CF0 pixels between SP1_HCG and SP1_LCG</p> <p>This register indicates [7:0] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.</p>
0x81C1	1	7:0	OTP_SENS_RATIO_CFO_SP1_H	R	U8.0	<p>The sensitivity ratio stored in the OTP ROM for the CF0 pixels between SP1_HCG and SP1_LCG</p> <p>This register indicates [14:8] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.</p>
0x81C2	1	7:0	OTP_SENS_RATIO_CFO_SP2_L	R	U8.0	<p>The sensitivity ratio stored in the OTP ROM for the CF0 pixels between SP2H and SP2L</p> <p>This register indicates [7:0] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.</p>

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x81C3	1	7:0	OTP_SENS_RATIO_C_F0_SP2_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF0 pixels between SP2H and SP2L This register indicates [14:8] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81C4	1	7:0	OTP_SENS_RATIO_C_F1_SP1_L	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF1 pixels between SP1_HCG and SP1_LCG This register indicates [7:0] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81C5	1	7:0	OTP_SENS_RATIO_C_F1_SP1_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF1 pixels between SP1_HCG and SP1_LCG This register indicates [14:8] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81C6	1	7:0	OTP_SENS_RATIO_C_F1_SP2_L	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF1 pixels between SP2H and SP2L This register indicates [7:0] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81C7	1	7:0	OTP_SENS_RATIO_C_F1_SP2_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF1 pixels between SP2H and SP2L This register indicates [14:8] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81C8	1	7:0	OTP_SENS_RATIO_C_F2_SP1_L	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF2 pixels between SP1_HCG and SP1_LCG This register indicates [7:0] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81C9	1	7:0	OTP_SENS_RATIO_C_F2_SP1_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF2 pixels between SP1_HCG and SP1_LCG This register indicates [14:8] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81CA	1	7:0	OTP_SENS_RATIO_C_F2_SP2_L	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF2 pixels between SP2H and SP2L This register indicates [7:0] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81CB	1	7:0	OTP_SENS_RATIO_C_F2_SP2_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF2 pixels between SP2H and SP2L This register indicates [14:8] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81CC	1	7:0	OTP_SENS_RATIO_C_F3_SP1_L	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF3 pixels between SP1_HCG and SP1_LCG This register indicates [7:0] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81CD	1	7:0	OTP_SENS_RATIO_C_F3_SP1_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF3 pixels between SP1_HCG and SP1_LCG This register indicates [14:8] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81CE	1	7:0	OTP_SENS_RATIO_C_F3_SP2_L	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF3 pixels between SP2H and SP2L This register indicates [7:0] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x81CF	1	7:0	OTP_SENS_RATIO_C_F3_SP2_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF3 pixels between SP2H and SP2L. This register indicates [14:8] of U3.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81D0	1	7:0	OTP_SENS_RATIO_C_F0_SP12_L	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF0 pixels between SP1 and SP2. This register indicates [7:0] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81D1	1	7:0	OTP_SENS_RATIO_C_F0_SP12_M	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF0 pixels between SP1 and SP2. This register indicates [15:8] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81D2	1	7:0	OTP_SENS_RATIO_C_F0_SP12_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF0 pixels between SP1 and SP2. This register indicates [21:16] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81D3	1	7:0	OTP_SENS_RATIO_C_F1_SP12_L	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF1 pixels between SP1 and SP2. This register indicates [7:0] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81D4	1	7:0	OTP_SENS_RATIO_C_F1_SP12_M	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF1 pixels between SP1 and SP2. This register indicates [15:8] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81D5	1	7:0	OTP_SENS_RATIO_C_F1_SP12_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF1 pixels between SP1 and SP2. This register indicates [21:16] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81D6	1	7:0	OTP_SENS_RATIO_C_F2_SP12_L	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF2 pixels between SP1 and SP2. This register indicates [7:0] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81D7	1	7:0	OTP_SENS_RATIO_C_F2_SP12_M	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF2 pixels between SP1 and SP2. This register indicates [15:8] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81D8	1	7:0	OTP_SENS_RATIO_C_F2_SP12_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF2 pixels between SP1 and SP2. This register indicates [21:16] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81D9	1	7:0	OTP_SENS_RATIO_C_F3_SP12_L	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF3 pixels between SP1 and SP2. This register indicates [7:0] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81DA	1	7:0	OTP_SENS_RATIO_C_F3_SP12_M	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF3 pixels between SP1 and SP2. This register indicates [15:8] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.
0x81DB	1	7:0	OTP_SENS_RATIO_C_F3_SP12_H	R	U8.0	The sensitivity ratio stored in the OTP ROM for the CF3 pixels between SP1 and SP2. This register indicates [21:16] of U10.12. Enabled when the AE_SENSRATIO_SEL register is 1.

[HDR_COM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x653C	3	21:0	HDR_SGAIN_SP1_R_OUT	R	U10.12	Compositing gain calculated by the sensor between SP1_HCG and SP1_LCG for the CF0 pixels
0x6540	3	21:0	HDR_SGAIN_SP1_G_R_OUT	R	U10.12	Compositing gain calculated by the sensor between SP1_HCG and SP1_LCG for the CF1 pixels
0x6544	3	21:0	HDR_SGAIN_SP1_G_B_OUT	R	U10.12	Compositing gain calculated by the sensor between SP1_HCG and SP1_LCG for the CF2 pixels
0x6548	3	21:0	HDR_SGAIN_SP1_B_OUT	R	U10.12	Compositing gain calculated by the sensor between SP1_HCG and SP1_LCG for the CF3 pixels
0x654C	3	19:0	HDR_SGAIN_SP2_R_OUT	R	U8.12	Compositing gain calculated by the sensor between SP2H and SP2L for the CF0 pixels
0x6550	3	19:0	HDR_SGAIN_SP2_G_R_OUT	R	U8.12	Compositing gain calculated by the sensor between SP2H and SP2L for the CF1 pixels
0x6554	3	19:0	HDR_SGAIN_SP2_G_B_OUT	R	U8.12	Compositing gain calculated by the sensor between SP2H and SP2L for the CF2 pixels
0x6558	3	19:0	HDR_SGAIN_SP2_B_OUT	R	U8.12	Compositing gain calculated by the sensor between SP2H and SP2L for the CF3 pixels
0x655C	3	23:0	HDR_SGAIN_SP12_R_OUT_H	R	U24.0	Compositing gain calculated by the sensor between SP1 and SP2 for the CF0 pixels Represents 24 bits of the integer part of the precision U24.12.
0x6560	2	11:0	HDR_SGAIN_SP12_R_OUT_L	R	U0.12	Compositing gain calculated by the sensor between SP1 and SP2 for the CF0 pixels Represents 12 bits of the fractional part of the precision U24.12.
0x6564	3	23:0	HDR_SGAIN_SP12_GR_OUT_H	R	U24.0	Compositing gain calculated by the sensor between SP1 and SP2 for the CF1 pixels Represents 24 bits of the integer part of the precision U24.12.
0x6568	2	11:0	HDR_SGAIN_SP12_GR_OUT_L	R	U0.12	Compositing gain calculated by the sensor between SP1 and SP2 for the CF1 pixels Represents 12 bits of the fractional part of the precision U24.12.
0x656C	3	23:0	HDR_SGAIN_SP12_GB_OUT_H	R	U24.0	Compositing gain calculated by the sensor between SP1 and SP2 for the CF2 pixels Represents 24 bits of the integer part of the precision U24.12.
0x6570	2	11:0	HDR_SGAIN_SP12_GB_OUT_L	R	U0.12	Compositing gain calculated by the sensor between SP1 and SP2 for the CF2 pixels Represents 12 bits of the fractional part of the precision U24.12.
0x6574	3	23:0	HDR_SGAIN_SP12_B_OUT_H	R	U24.0	Compositing gain calculated by the sensor between SP1 and SP2 for the CF3 pixels Represents 24 bits of the integer part of the precision U24.12.
0x6578	2	11:0	HDR_SGAIN_SP12_B_OUT_L	R	U0.12	Compositing gain calculated by the sensor between SP1 and SP2 for the CF3 pixels Represents 12 bits of the fractional part of the precision U24.12.

5.2. Exposure Control Function

5.2.1. Functional Purpose

The Exposure Control function adjusts the exposure time and gain so that the brightness of the captured image will be at the optimum level.

5.2.2. Functional Overview

"Figure 5-7" illustrates a block diagram regarding the flow of the sensor's exposure control. The thick arrows indicate the flow of image signals and thin arrows indicate the control applied. There are two types of gains: Analog gain that amplifies analog signals which have been photoelectrically converted, and digital gain that amplifies signals at the RAW signal processing block.

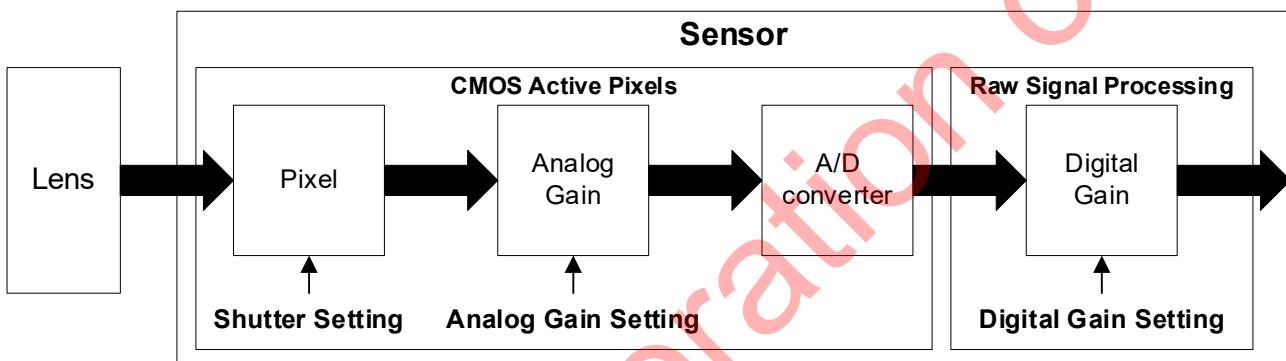


Figure 5-7 An Overview of Exposure Control

The Exposure Control function adjusts the exposure time and gain using an AE diagram so that the brightness of the captured image will be at the optimum level. As shown in "Figure 5-8," the AE diagram shows the relationship between controlled exposure time and gain, corresponding to the brightness.

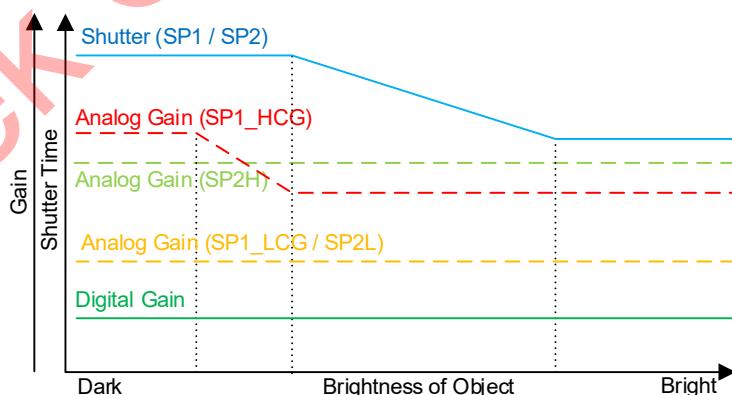


Figure 5-8 AE Diagram

◇ Memo

- The sensor can detect flashing cycles and adjust the exposure time to mitigate flickering (i.e., color rolling) caused by a fluorescent light.
- When controlling exposure without using the sensor's automatic exposure (AE) control, the host can control the exposure time and gain individually.

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5.2.3. Functional Specifications

5.2.3.1. Exposure Control Methods

The sensor's exposure control methods consist of auto exposure (AE) and manual exposure (ME). In the AE method, the sensor automatically controls exposure. Alternatively, in the ME method, the host controls exposure times and gain. “Table 5-7” describes how to set each exposure control method.

Table 5-7 List of the Exposure Control Modes

Name	AEMODE	Adjustment Method	Description	Remark
AE	0	AE (Auto)	The sensor controls exposure time and gain, corresponding to the brightness and using the AE diagram.	“5.2.3.5.1 AE (Auto)”
	1	AE (Hold)	When the host switches the method to AE (Hold) while AE (Auto) is in operation, the sensor retains the exposure control settings.	“5.2.3.5.2 AE (Hold)”
ME	2	Scale ME	The sensor controls exposure by converting a total gain specified by the host to the exposure time and gain using the AE diagram.	“5.2.3.7.1 Scale ME”
	3	Full ME	The sensor controls exposure using the exposure time and gain specified by the host.	“5.2.3.7.2 Full ME”

5.2.3.2. Exposure Control

The following explains the exposure time and gain used for exposure control.

5.2.3.2.1. Units of Exposure Time

“Table 5-8” describes the units of the sensor's exposure time.

Table 5-8 Units of Exposure Time

Unit	Description
Line	Line is the unit for setting the exposure time based on the sensor's vertical sync signal. The exposure time per line of the vertical sync signal can be obtained using the following equation: Exposure time [s] per line = $1 / (\text{Frame Rate}) / \text{VMAX}$, where the VMAX represents the maximum number of lines which vary corresponding to the drive mode, and the Frame Rate represents the number of output frames per second. Exposure time [s] per line = $1 / (\text{Frame Rate}) / \text{VMAX}$
μs	μs is the unit for setting the exposure time in microseconds. Since the sensor operates using the vertical sync signal as the reference, the sensor performs exposure by converting the value set in μs into the time per line of the vertical sync signal. Therefore, the exposure time may be shorter than the time in μs determined by the drive mode.
Frame	Frame is the unit for setting the exposure time using the sensor's one frame as the reference. The exposure time per frame of the sensor can be obtained using the following equation: Exposure time [s] per frame = $1 / (\text{Frame Rate})$, where Frame Rate indicates the number of frames transmitted per second.

"Table 5-9" shows the relationship between the drive modes, Frame Rates and VMAX values.

Table 5-9 VMAX Values

Frame Rate [Frames/s]	Output Format	VMAX
30	RAW24 RAW20 RAW16 RAW14 RAW12 RAW12 x 2	1750
30	RAW12 x 4	1750
60	RAW24 RAW20 RAW16 RAW14 RAW12 RAW12 x 2	1626

5.2.3.2.2. Gain Control

The sensor has analog and digital gains. The number of steps that can be set for analog and digital gains differs, depending on the range to be set. For details, refer to "5.2.4 Conditions."

5.2.3.2.3. Long Exposure

Long exposure refers to a condition, under which the exposure time is set greater than or equal to the time that can be set within one frame. By performing long exposure, the sensor can continue exposure over multiple frames even in a low-light environment and obtain a sufficient signal level.

The sensor can perform long exposure in the case of internal or external pulse-based synchronization. The conditions under which long exposure is performed in units of lines are shown as follows:

- In the case of internal sync
 $VMAX + VMAX_OFFSET - 8 < \text{Exposure Time}$
- In the case of external pulse-based sync
 $VMAX + VMAX_OFFSET - 18 < \text{Exposure Time}$

The sensor can extend the exposure time by up to eight frames (i.e., extension of an additional seven frames).

◆ Note

Long exposure cannot be set in the case of shutter trigger-based sync.

◇ Memo

For details on how to calculate the exposure time per line, refer to “[5.2.3.2.1 Units of Exposure Time](#).”

■ Extended Frame

When the sensor extends frames using long exposure, there will be frames wherein the sensor produces image output and other frames wherein the sensor does not produce any within one long exposure. Regarding the sensor, the latter frames are referred to as “extended frames.” The Output Mask function performs masking on these extended frames. For example, when the sensor extends frames to three, the sensor transmits one effective frame that contains the result of long exposure and produces output with the remaining two frames masked.

For details, refer to “[6.8.3.2 Masking Extended Frames](#).”

◇ Memo

The user can check whether the long exposure has been applied, using the Front Embedded Data. For details regarding the Front Embedded Data, refer to “[6.9.3.5.21 Extended Frame and Extended Line Information](#).”

5.2.3.3. Setting an AE Diagram

The sensor uses an AE diagram when the exposure control method has been set to AE (Auto) or Scale ME.

The sensor's AE diagram shows how the sensor controls exposure time and gain corresponding to the illuminance. Define the AE diagram by setting the exposure time and gain to their minimum values at high illuminance, through to their maximum values at low illuminance. A segment where the sensor switches user-set values is referred to as a control segment. In a control segment, the sensor performs linear interpolation to change user-set values gradually. This can prevent any sudden change to the brightness of images.

Regarding the sensor, these control segments are shared between the exposure time and gain, and can be set up to six. Each control segment can be assigned to either Invalid (i.e., a control segment which is not used in the AE diagram), Exposure Time, Gain or No Control (i.e., a no-control segment in which both the exposure time and gain do not change). The exposure time and gain can be assigned up to two and three, respectively. Assign the remaining control segments to either invalid (a control segment unused in the AE diagram) or no control (a control segment where both the exposure time and the gain do not change).

"Figure 5-9" illustrates an example of the sensor's AE diagram settings.

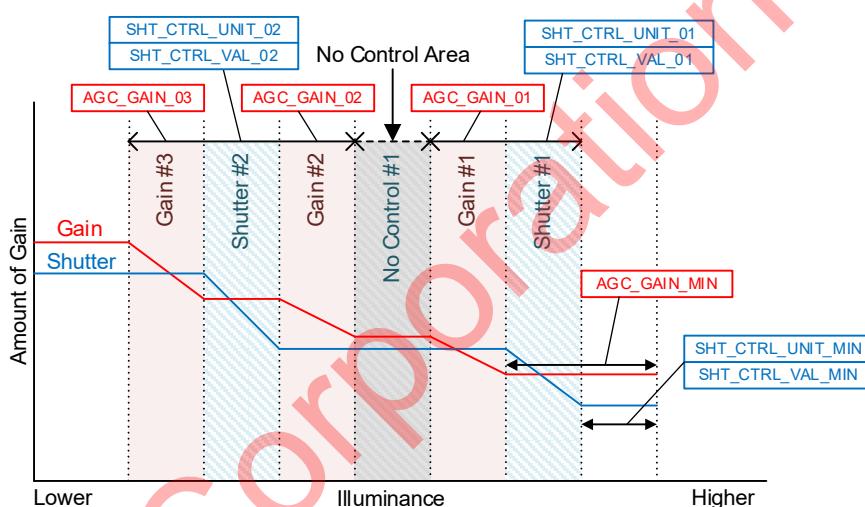


Figure 5-9 AE Diagram Settings

■ Minimum Exposure Time and Minimum Gain

When defining the AE diagram, first set the minimum exposure time and minimum gain at high illuminance which are the starting point of the AE diagram. Set the registers shown in **"Table 5-10"** to the minimum exposure time and minimum gain.

Table 5-10 Registers Used to Set the Minimum Exposure Time and Minimum Gain

Settings	Register Name	Unit for Settings
Minimum Exposure Time	SHT_CTRL_VAL_MIN	SHT_CTRL_UNIT_MIN
Minimum Analog Gain (SP1_HCG)	AGC_GAIN_MIN	0.1 [dB]
Minimum Analog Gain (SP1_LCG)	AGC_AGAIN_SP1L	0.1 [dB]
Minimum Analog Gain (SP2H)	AGC_GAIN_MIN_S	0.1 [dB]
Minimum Analog Gain (SP2L)	AGC_AGAIN_SP2L	0.1 [dB]

◆ Note

The number of steps that can be set for analog and digital gains differs, depending on the range to be set. For details, refer to “**5.2.4 Conditions.**”

In the sensor’s AE diagram, the sensor controls gain by using the adjustment of SP1_HCG’s minimum analog gain as the reference. When adjusting the gain, the sensor first uses SP1_HCG’s analog gain. If the sensor cannot adjust the gain by using SP1_HCG’s analog gain only, the sensor uses the digital gain to adjust the gain level that is insufficient with the analog gain.

■ Control Method for Control Segments

To select the control method, set the CTRL_AREA_TYPE_x (x = 01 to 06) registers as follows:

- The suffix **x** is required to be assigned so that the settings of a register with a smaller number are applied to higher illuminance and a register with a greater number are applied to lower illuminance.
- Select the control method from Invalid, Exposure Time, Gain and No Control.
- Regarding segment(s) in which the sensor does not control the exposure time and gain, select “No Control.”
- When setting the register to 0 (invalid), the segment will become invalid and the settings of the register with the subsequent number will be applied.
- When more than the available number of steps of the exposure time or gain is set, the sensor will operate in the same way as when a value of 0 is set, from the control segment in which the number of steps has exceeded the available quantity of steps.

■ Exposure Time and Gain for Each Control Segment

Set the registers in “**Table 5-11**” to the exposure time and gain, corresponding to the number of control methods assigned to each control segment.

Table 5-11 Registers Used to Set the Exposure Time and Gain for Each Control Segment

Settings	Register Name	Unit for Settings
Exposure Time	SHT_CTRL_VAL_x (x = 01 to 02)	SHT_CTRL_UNIT_x (x = 01 to 02)
Gain	AGC_GAIN_x (x = 01 to 03)	0.1 [dB]

Be sure to set each value of the registers considering the following:

- $SHT_CTRL_VAL_{02} \geq SHT_CTRL_VAL_{01}$
- $AGC_GAIN_{03} \geq AGC_GAIN_{02} \geq AGC_GAIN_{01}$
- Increase each value monotonically. Values vary depending on the unit of exposure time. Therefore, when using different units, set the unit carefully so that each value increases monotonically in real time.
- If a setting does not satisfy the aforementioned magnitude conditions, the sensor operates under the condition of the preceding segment. For example, in the case of $AGC_GAIN_{02} < AGC_GAIN_{01}$, the sensor operates under the condition of $AGC_GAIN_{02} = AGC_GAIN_{01}$.

■ No Control Segment

When selecting "No Control" for a control segment, the user can set the width of the "No Control" segment using the NCTRL_WIDTH_01 register. The sensor calculates the width of the "No Control" segment using the following equation and applies the value:

$$\text{Width} = \text{NCTRL_WIDTH_01 Register values} \times 6.02 \div 1024 [\text{dB}]$$

■ Example of Setting an AE Diagram

"Table 5-12" shows an example when generating the AE diagram using four control segments:

Table 5-12 Example When Setting the AE Diagram Using Four Control Segments

Settings	Register Values			
	Control Methods	Exposure Times	Gain	Width of No Control Segment
Minimum Exposure Time	-	SHT_CTRL_VAL_MIN = 1 SHT_CTRL_UNIT_MIN = 1	-	
Minimum Gain	-	-	AGC_GAIN_MIN = 1 AGC_AGAIN_SP1L = 1 AGC_GAIN_MIN_S = 1 AGC_AGAIN_SP2L = 1	
1st Control Segment (Exposure Time)	CTRL_AREA_TYPE_01 = 1	SHT_CTRL_VAL_01 = 200 SHT_CTRL_UNIT_01 = 1	-	
2nd Control Segment (Gain)	CTRL_AREA_TYPE_02 = 2	-	AGC_GAIN_01 = 80	
3rd Control Segment (No Control)	CTRL_AREA_TYPE_03 = 3	-	-	NCTRL_WIDTH_01 = 512
4th Control Segment (Exposure time)	CTRL_AREA_TYPE_04 = 1	SHT_CTRL_VAL_02 = 400 SHT_CTRL_UNIT_02 = 1	-	
5th Control Segment (Invalid)	CTRL_AREA_TYPE_05 = 0	-	-	
6th Control Segment (Invalid)	CTRL_AREA_TYPE_06 = 0	-	-	

5.2.3.4. Light Metering

Light metering is a function that meters the brightness of an image.

5.2.3.4.1. Selecting the Light Metering Method

The sensor enables the user to select three light metering methods as shown in “**Table 5-13**” using the AEWEIGHTMODE_HDR register.

Table 5-13 Light Metering Methods

Light Metering Method	AEWEIGHTMODE_HDR Register	Description
Mesh Light Metering	0	A method for weighting 63 cells.
Histogram Light Metering	1	A method of assigning a weight to each luminance region from a subject's luminance distribution.
Blend-Switching Light Metering	2	A method for blend-switching between mesh and histogram metering methods, corresponding to the subject's illuminance.

5.2.3.4.2. Mesh Light Metering

Mesh Light Metering is a method where the sensor calculates the average luminance of each of the 63 cells, consisting of 9 horizontal x 7 vertical cells, to assign a weight to each cell. The user can change the weight of each cell using MESH_WEIGHT_x (x = 00 to 62) registers. The register's suffix represents the cell's ID number as shown in “**Figure 5-10**.”

00	01	02	03	04	05	06	07	08
09	10	11	12	13	14	15	16	17
18	19	20	21	22	23	24	25	26
27	28	29	30	31	32	33	34	35
36	37	38	39	40	41	42	43	44
45	46	47	48	49	50	51	52	53
54	55	56	57	58	59	60	61	62

Figure 5-10 Cell ID Numbers for Light Metering

5.2.3.4.3. Histogram Light Metering

Histogram Light Metering is a method where the sensor divides the luminance level into 30 gradations and counts the pixels for each gradation to assign weights to each gradient. Set the HIST_WEIGHT_x ($x = 00$ to 29) registers to the weighting factor for the luminance gradation segments.

■ Dynamic and Static Modes

Histogram Light Metering consists of Static and Dynamic modes. In Histogram Metering mode, to select the Dynamic or Static mode, set the HISTTH_SEL register to 0 or 1, respectively.

Static Mode

In Static mode, the sensor calculates an AE evaluation value using a luminance level threshold which has been set using the MANUALHISTTHx ($x = 00$ to 29) registers. Set these registers so that the luminance level increases monotonically from the value of the MANUALHISTH00 register.

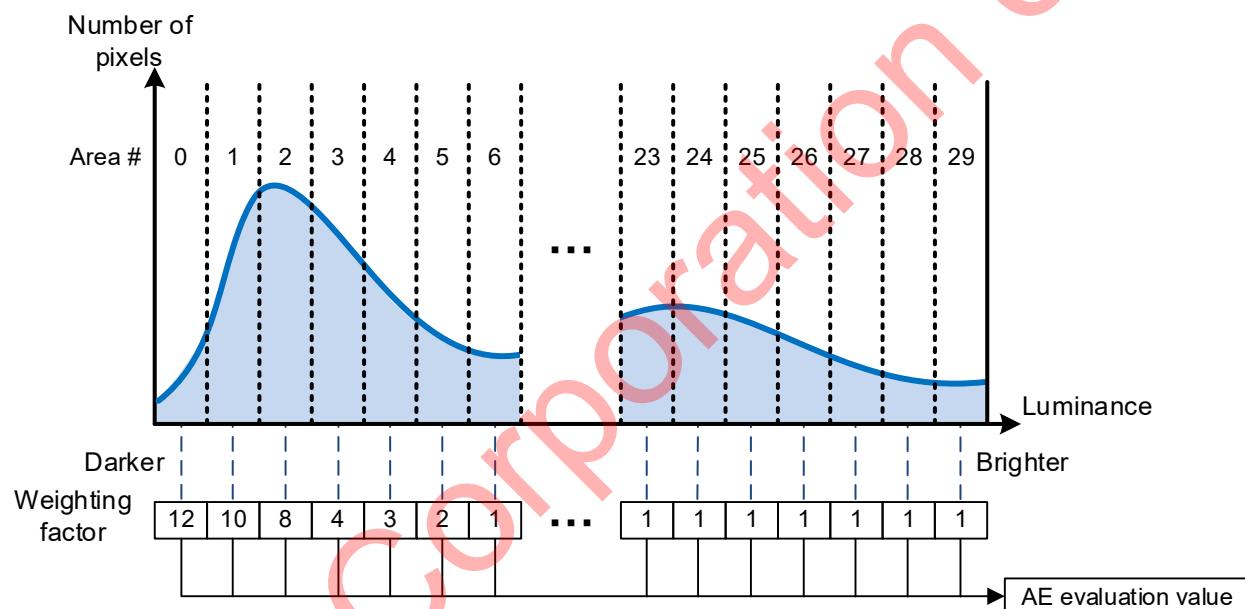


Figure 5-11 The Calculation of AE Evaluation Values Using the Pixel Count and the Weighting Factor in the Case of Static Histogram Light Metering

Dynamic Mode

In Dynamic mode, the sensor dynamically changes the segments based on the current average luminance to calculate an AE evaluation value. This enables the sensor to maintain the same histogram distribution to some extent even if the luminance level changes. The width of the gradation segment changes as the average value of luminance per pixel changes. The 29 segments from the lowest luminance (Segment #0 to #28) are determined by this width, and the distribution in the higher segments are the remaining part.

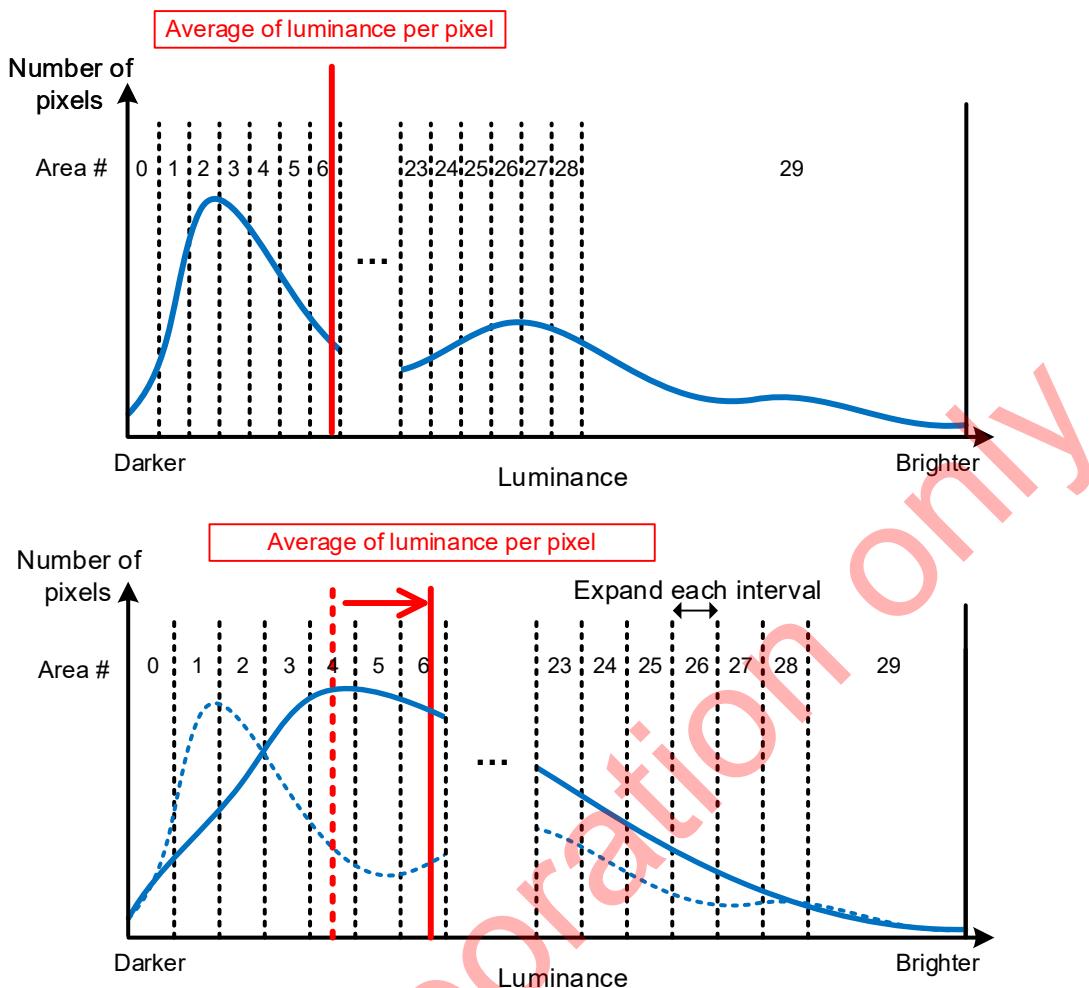


Figure 5-12 Dynamic Histogram Light Metering

5.2.3.4.4. Blend-Switching Light Metering

Blend-Switching Light Metering is a method of switching between mesh metering and histogram metering, corresponding to the illuminance. The sensor's Blend-Switching Light Metering uses mesh metering at low illuminance and histogram metering at high illuminance. The sensor switches light metering using the thresholds for illuminance in “**Table 5-14.**”

Table 5-14 Registers Used to Set the Threshold for Blend-Switching Light Metering

Register Name	Description
BLNDHIST_ILM_LOW	The threshold at which the sensor switches light metering from histogram to mesh.
BLNDHIST_ILM_HIGH	The threshold at which the sensor switches light metering from mesh to histogram.

For the illuminance between the BLNDHIST_ILM_LOW and BLNDHIST_ILM_HIGH registers, the sensor blends the evaluation values obtained from Mesh Metering and Histogram Metering. As shown in “**Figure 5-13,**” the blending of these evaluation values is performed so that these metering methods are switched smoothly, corresponding to the illuminance.

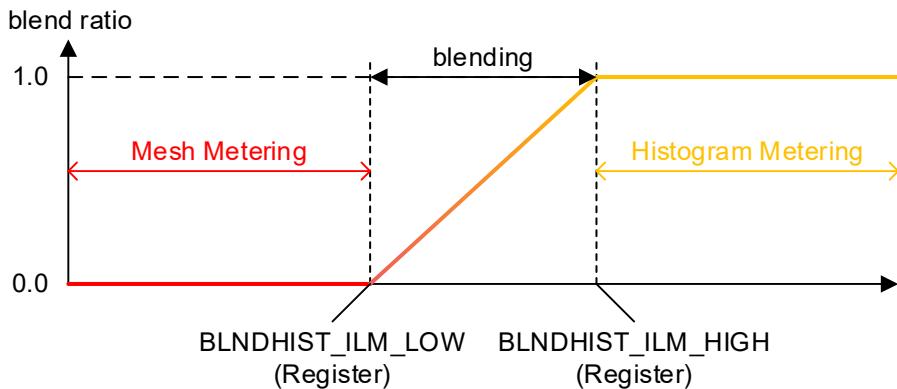


Figure 5-13 Switching between Mesh and Histogram Light Metering

5.2.3.4.5. Adjusting the Light Metering Window

The sensor performs light metering using 63 cells, consisting of 9 horizontal and 7 vertical cells. The host can adjust the size and position of the light metering window.

To adjust the size, use the AE_WND_MODE register. “**Table 5-15**” describes how to adjust the size.

Table 5-15 Methods for Setting the Light Metering Window’s Size

AE_WND_MODE	Description
0	<p>Specify the width and height for each of the 63 cells, which consist of 9 horizontal x 7 vertical cells, in multiples of 2.</p> <ul style="list-style-type: none"> • AE_WND_SIZE_H register: Set the width of one cell. (Unit: pixel) • AE_WND_SIZE_V register: Set the height of one cell. (Unit: pixel)
1	<p>Specify the width and height of the metering window, which consist of 9 horizontal x 7 vertical cells, using ratios with respect to the Active Area.</p> <ul style="list-style-type: none"> • AE_WND_SIZE_H register: Specify the width of the metering window using a ratio with respect to the width of the Active Area.¹ The width of one cell: The width of the Active Area x (AE_WND_SIZE_H / 256) / 9³ The width of the light metering window: The width of one cell x 9 • AE_WND_SIZE_V register: Specify the height of the metering window using a ratio with respect to the height of the Active Area.² The height of one cell: The height of the Active Area x (AE_WND_SIZE_V / 256) / 7³ The height of the light metering window: The height of one cell x 7
2	<p>Specify the width and height of the metering window, which consist of 9 horizontal x 7 vertical cells, using ratios with respect to the Active Area (Output).</p> <ul style="list-style-type: none"> • AE_WND_SIZE_H register: Specify the width of the metering window using a ratio with respect to the width of the Active Area (Output).¹ The width of one cell: The horizontal size of the Active Area (Output) x (AE_WND_SIZE_H / 256) / 9³ The width of the light metering window: The width of one cell x 9 • AE_WND_SIZE_V register: Specify the height of the metering window using a ratio with respect to the height of the Active Area (Output).² The height of one cell: The vertical size of the Active Area (Output) x (AE_WND_SIZE_V / 256) / 7³ The height of the light metering window: The height of one cell x 7

*¹ The value of the AE_WND_SIZE_H register is within the range of 16 (0x10) to 256 (0x100). Any other settings are prohibited.

*² The value of the AE_WND_SIZE_V register is within the range of 4 (0x04) to 256 (0x100). Any other settings are prohibited.

*³ Round the calculated value down to the nearest value that is a multiple of 2. For example, if the calculated value is 61.8, round it down to 60. Likewise, round the value 62.2 down to 62.

To adjust the position of the light metering window, set the AE_WND_OFFSET_H and AE_WND_OFFSET_V registers to the amount of offset. "Figure 5-14" illustrates the relationship between the offset direction and the value of each of the registers.

- Horizontal direction (AE_WND_OFFSET_H register): Positive to the right and negative to the left from the center of the Active Area or the output image.
- Vertical direction (AE_WND_OFFSET_V): Positive downward and negative upward from the center of the Active Area or the output image.

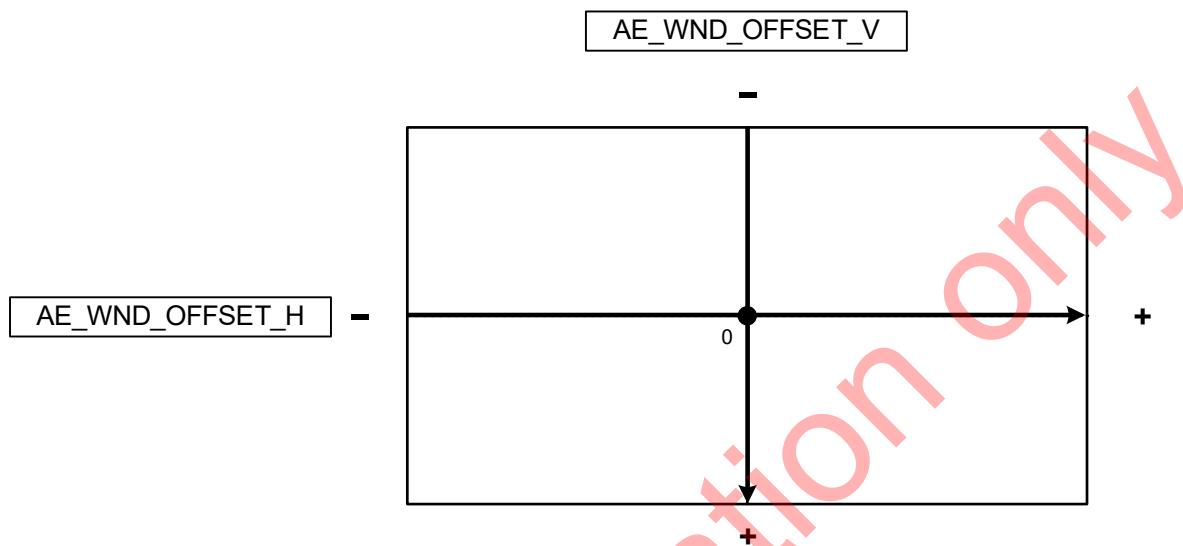


Figure 5-14 The Relationship Between the Offset Direction and the Value of Each of the Registers

◆ Note

- When using the Horizontal/Vertical Flip function with the AE_OPD_REVERSE_EN register set to 1, both of the aforementioned directions are reversed. For details regarding the AE_OPD_REVERSE_EN register, refer to "5.2.3.4.9 Interlocking with the Horizontal/Vertical Flip Function."
- When adjusting the position, set the light metering window after adjustment so that it does not exceed the effective pixel area.

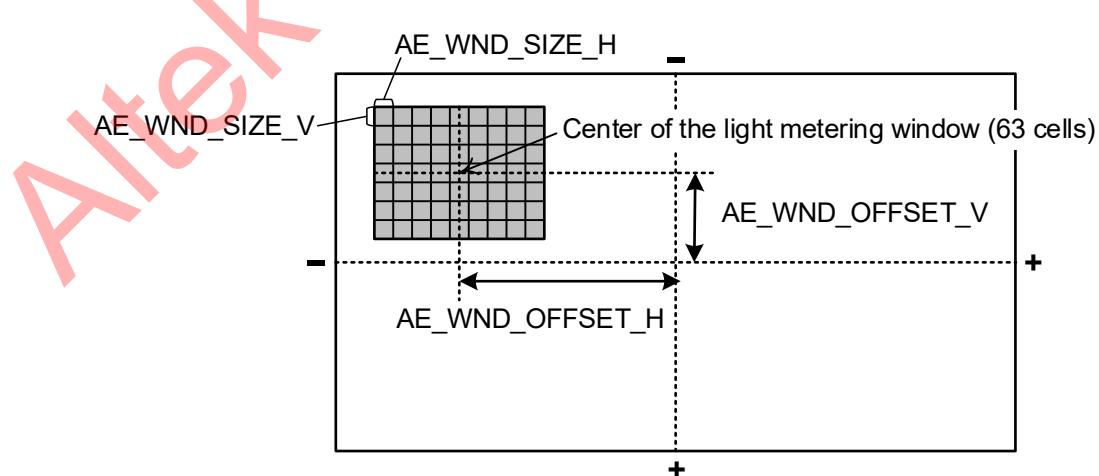


Figure 5-15 Adjustment of the Light Metering Window's Position (AE_WND_MODE = 0)

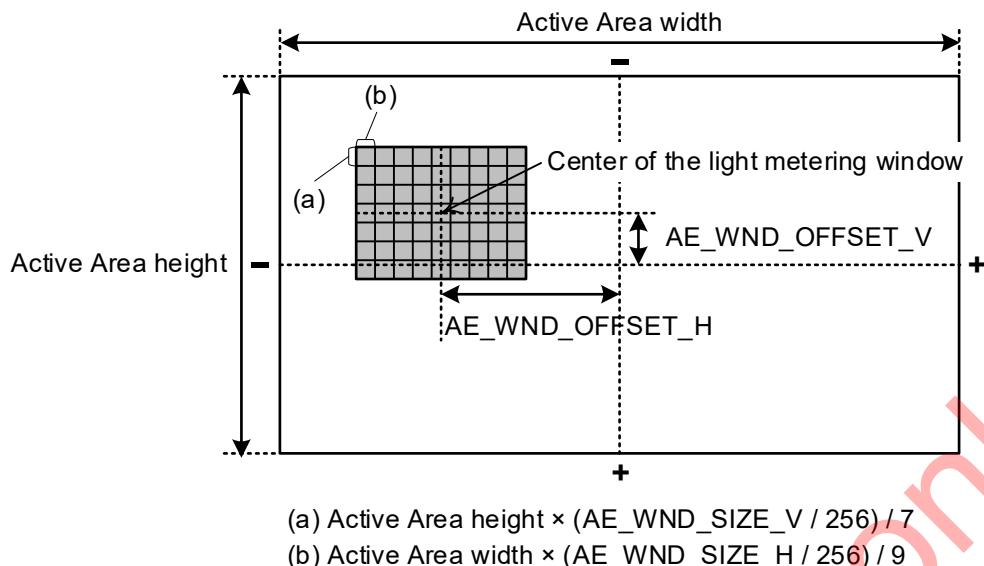


Figure 5-16 Adjustment of the Light Metering Window's Position (AE_WND_MODE = 1)

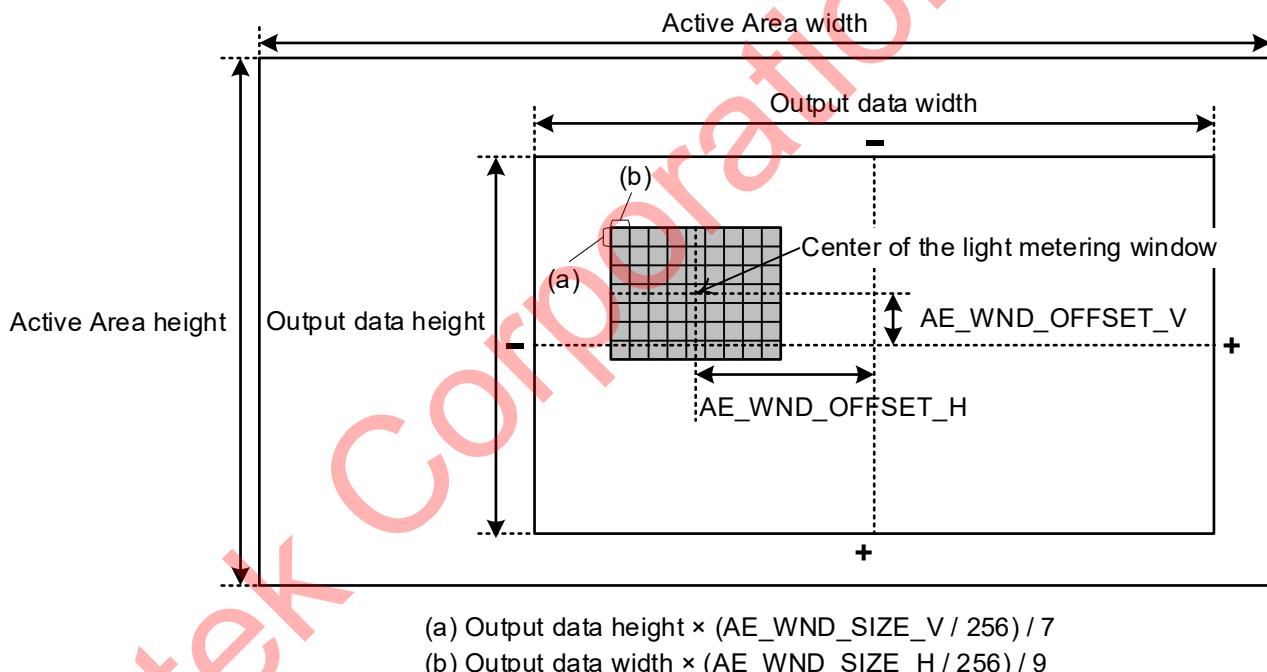


Figure 5-17 Adjustment of the Light Metering Window's Position (AE_WND_MODE = 2)

5.2.3.4.6. Light Metering Region Mask Function

The Light Metering Region Mask function excludes specific region(s) of the image from light metering. The user can set a maximum of eight rectangular regions or one elliptical region. The following describes how to mask rectangular or elliptical regions.

■ How to set the Light Metering Region Mask function

This function can be set using the IR_OP_OIF_AE_MSK_SEL register as follows:

- When the value is 0: The Light Metering Region Mask function is disabled.
- When the value is 1: Only elliptical region is masked.
- When the value is 2: Only rectangular region(s) are masked.

- When the value is 3: Both elliptical and rectangular regions are masked.

■ Rectangular Region

To enable or disable rectangular masking, configure the settings using the registers in “**Table 5-16**.” Set the position of each region as follows:

- * The xy coordinates are in multiples of two with the upper left corner of the Active Area defined as the origin (0,0).
 - * The start position's coordinates are less than the end position's coordinates.
- “**Figure 5-18**” illustrates an example of setting rectangular regions.

Table 5-16 Registers for Light Metering Window Mask Function (Rectangular Region)

Register Name	Description
OPD_MASK_EN_x (x = 00 to 07)	This register is used to enable or disable rectangular masking.
OPD_MASK_STAH_x (x = 00 to 07)	This register is used to set the horizontal starting point of Region x. • The left edge of the Active Area is defined as 0.
OPD_MASK_ENDH_x (x = 00 to 07)	This register is used to set the horizontal end point of Region x. • The left edge of the Active Area is defined as 0.
OPD_MASK_STAV_x (x = 00 to 07)	This register is used to set the vertical starting point of Region x. • The upper edge of the Active Area is defined as 0.
OPD_MASK_ENDV_x (x = 00 to 07)	This register is used to set the vertical end point of Region x. • The upper edge of the Active Area is defined as 0.

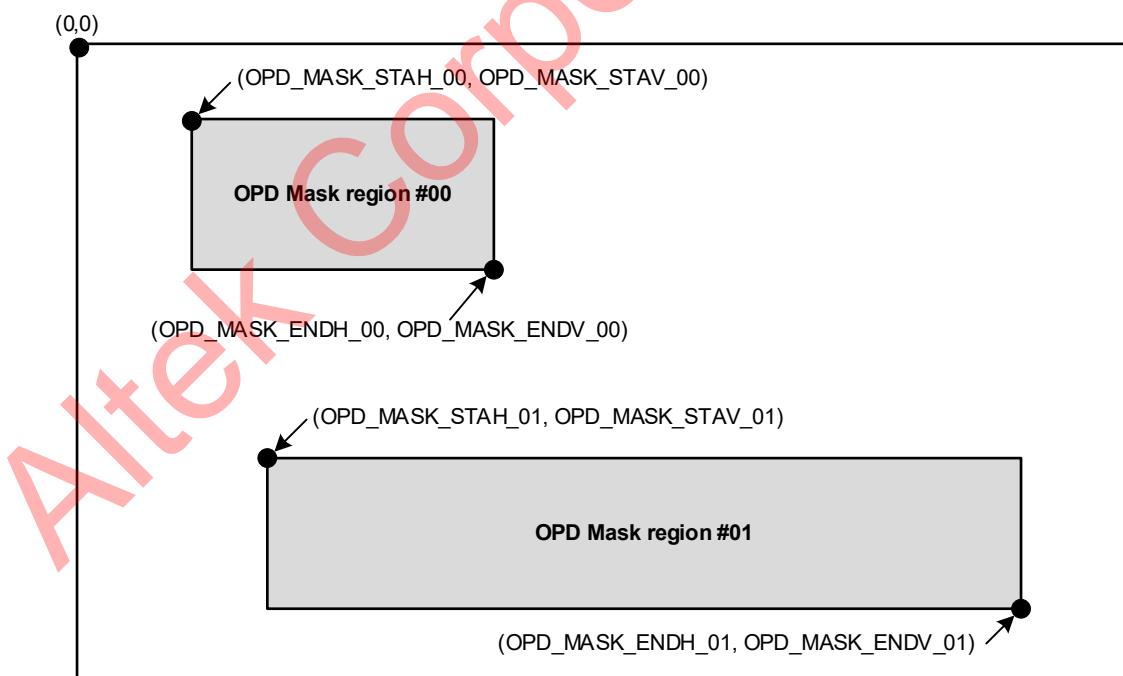


Figure 5-18 Rectangular Regions to Be Masked

■ Elliptical Region

To use the elliptical region, configure the settings using the registers in “**Table 5-17.**” Set the upper-left corner of the Active Area to the origin (0,0). Since these settings vary due to the Optical Center Compensation function, configure them before compensating for the optical center.

“**Figure 5-19**” illustrates an example of setting the elliptical region.

Table 5-17 Registers for Light Metering Window Mask Function (Elliptical Region)

Register Name	Description
OPD_MASK_EL_HCEN	This register is used to set the horizontal center position of the elliptical region. • The left edge of the Physical Active Pixel Area is defined as 0.
OPD_MASK_EL_VCEN	This register is used to set the vertical center position of the elliptical region. • The upper edge of the Physical Active Pixel Area is defined as 0.
OPD_MASK_EL_RADH	This register is used to set the elliptical region's horizontal size. • The center of the elliptical region is defined as 0.
OPD_MASK_EL_RADV	This register is used to set the elliptical region's vertical size. • The center of the elliptical region is defined as 0.

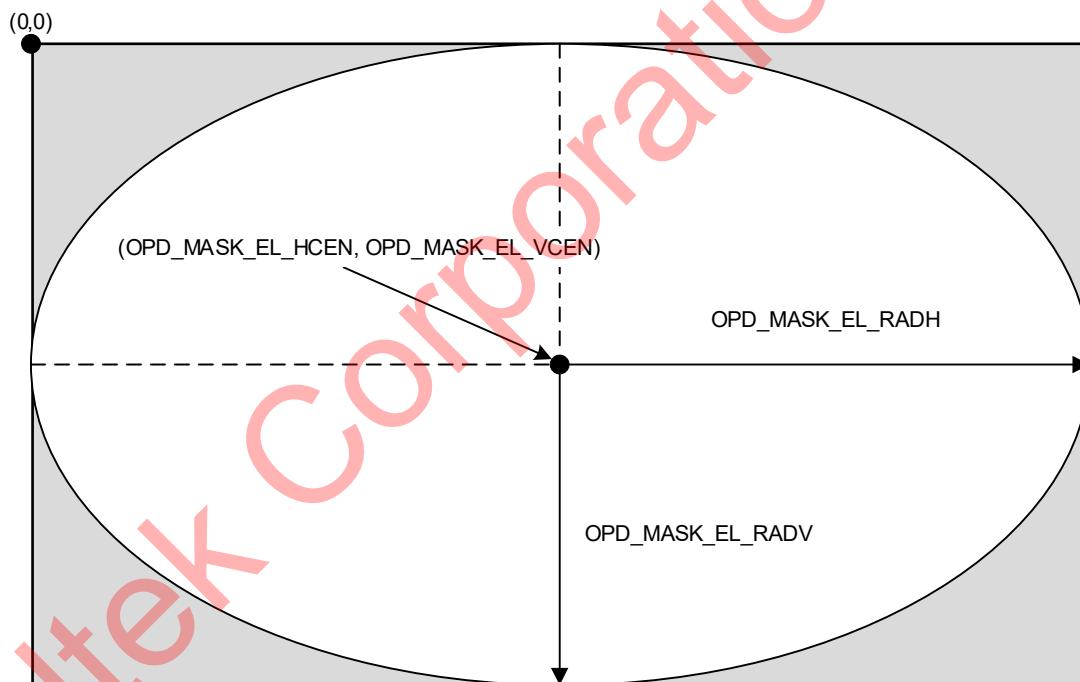


Figure 5-19 Light Metering Window Mask Function (Elliptical Region)

Of the light metering masking methods, the settings of the elliptical region are the same as those of the AWB light metering window.

5.2.3.4.7. AE Evaluation Value

The value that is obtained by performing various types of weighting on the results of light metering is referred to as an AE evaluation value. In AE mode, the sensor controls the AE evaluation value so that it approaches the convergence target value specified in the EVREF register.

5.2.3.4.8. AE Error

The differential between the AE evaluation value and the EVREF register's value is referred to as an AE error, which can be checked using the ERRSCL register.

5.2.3.4.9. Interlocking with the Horizontal/Vertical Flip Function

This section describes a function that weights the light metering window and adjusts the window position interlocking with the “[6.3 Horizontal/Vertical Flip Function](#).” “[Table 5-18](#)” shows the variables for positional adjustments and the registers used to configure the interlocking settings.

To enable or disable the interlocking of the light metering window with the Horizontal/Vertical Flip function, set the relevant register to 1 or 0 respectively.

◇ **Memo**

When interlocking the assignment of weights to the Mesh Light Metering window with the Horizontal/Vertical Flip function, set the SENS_REVERSE_CTRL register to 1.

Table 5-18 Variables and the Registers to Be Interlocked with the Horizontal/Vertical Flip Function

Settings	Register Name
Weights to the Mesh Light Metering window	SENS_REVERSE_CTRL
Position of the light metering window	AE_OPD_REVERSE_EN
Position of the rectangular region(s) to be masked from light metering	OPD_MASK_REVERSE_EN
Position of the elliptical region to be masked from light metering	OPD_MASK_EL_REVERSE_EN

◆ **Note**

Set register values while the sensor is in Start-up State.

"Figure 5-20" illustrates examples of interlocking between the Horizontal/Vertical Flip function and the light metering window when the SENS_REVERSE_CTRL and AE_OPD_REVERSE_EN registers are set to 1.

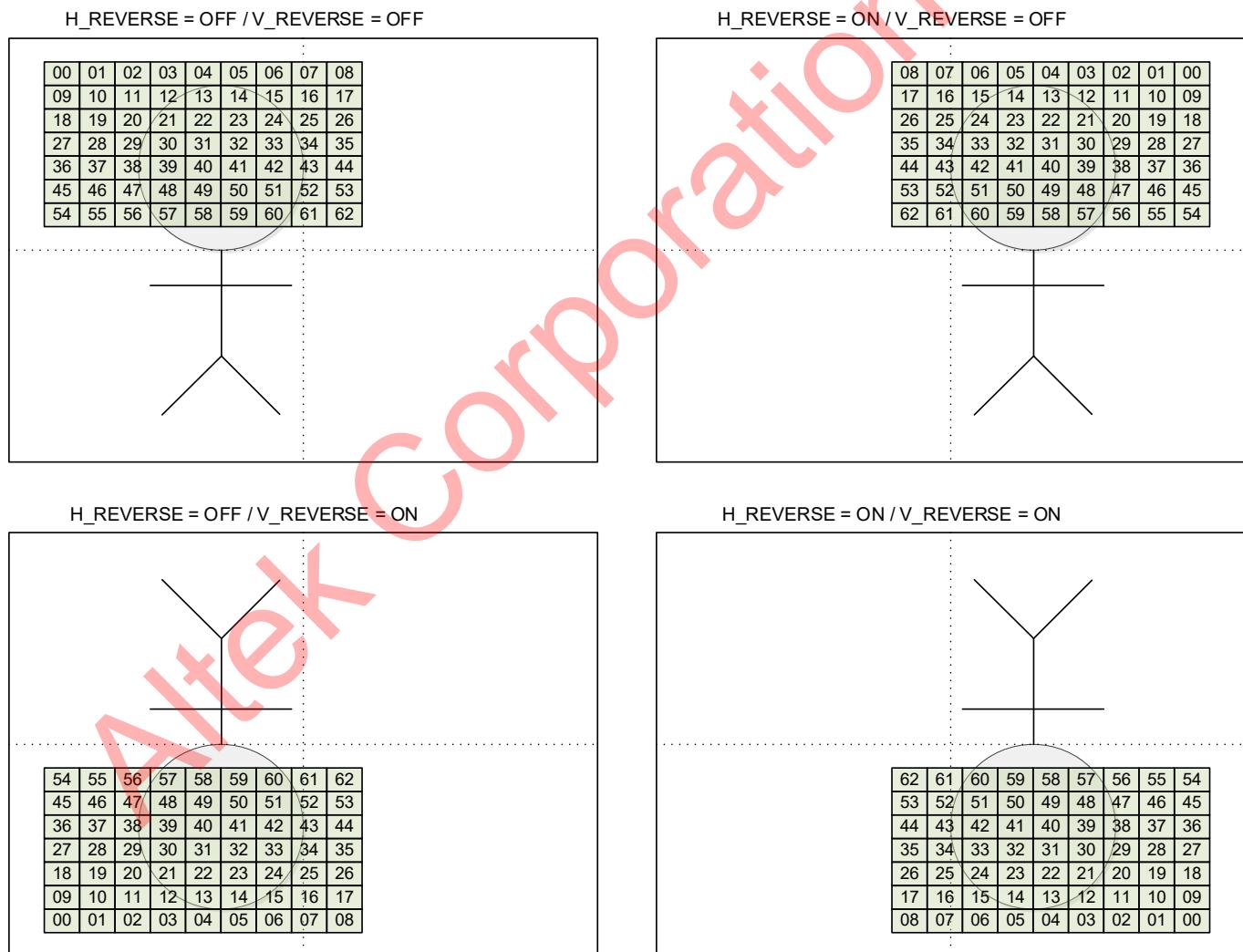


Figure 5-20 Interlocking between the Horizontal/Vertical Flip Function and the Light Metering Window

5.2.3.5. AE

5.2.3.5.1. AE (Auto)

AE (Auto) is a method in which the sensor controls exposure time and gain, corresponding to brightness and using the AE diagram. In this method, the sensor uses a light metering window to estimate the brightness of a captured image.

5.2.3.5.2. AE (Hold)

When the host sets the AEMODE register to 1 while the AE (Auto) method is in operation, the sensor switches the method to the AE (Hold) method. While the AE (Hold) method is in operation, the sensor retains the exposure time and gain which have been set using the AE (Auto) method. Therefore, the sensor does not adjust the exposure time and/or gain even if the brightness changes while the AE (Hold) method is in operation.

5.2.3.5.3. Exposure Control

The user can adjust the amount of exposure in increments of 0.1 dB using the EVREF_OFFSET register.

5.2.3.5.4. Convergence Speed

Adjust the speed at which auto exposure (AE) converges within the optimum exposure range using the AESPEED register. Increasing the value of the AESPEED register will increase the AE convergence speed.

5.2.3.5.5. Two-Tracking Speed Control

The tracking mode can be switched between low-speed and high-speed corresponding to the amount of AE error. “**Table 5-19**” shows the registers used to configure the settings for each mode. “**Figure 5-21**” illustrates an example of the two-tracking speed control.

The AEINDEADBAND and AEOUTDEADBAND registers are used to determine the state of the auto exposure (AE). Set these registers so that the following condition is satisfied:

$$AEINDEADBAND < AEOUTDEADBAND \times 16$$

While the auto exposure (AE) is in a state of tracking and when the following state continues for three frames, the sensor transitions to a state of convergence:

$$Amount\ of\ AE\ error < AEINDEADBAND$$

While the auto exposure (AE) is in a state of convergence and when the following state continues over multiple frames set in the AEMOVECNT or AEMOVECNT_SLOW register, the sensor transitions to a state of tracking:

$$Amount\ of\ AE\ error > AEOUTDEADBAND$$

Table 5-19 Registers Used to Configure the Settings Corresponding to the Tracking Mode

	Description	Register Name
Threshold for state transition User-set value $\times 16 \times 6.02 / 1024$ [dB]	This register is used to determine that auto exposure (AE) is in a state of high-speed tracking.	AEDEADBAND_FAST
	This register is used to determine that auto exposure (AE) is in a state of low-speed tracking.	AEDEADBAND_SLOW
Scale limit value	Tracking scale in high-speed tracking mode	ERRSCLLIMIT
	Tracking scale in low-speed tracking mode	ERRSCLLIMIT_SLOW
State transition frame	Transition from high- to low-speed tracking mode	TH_CNT_SPD_F2S

Description		Register Name
	Transition from low- to high-speed tracking mode	TH_CNT_SPD_S2F
Tracking start frame	High-speed tracking mode	AEMOVECNT
	Low-speed tracking mode	AEMOVECNT_SLOW

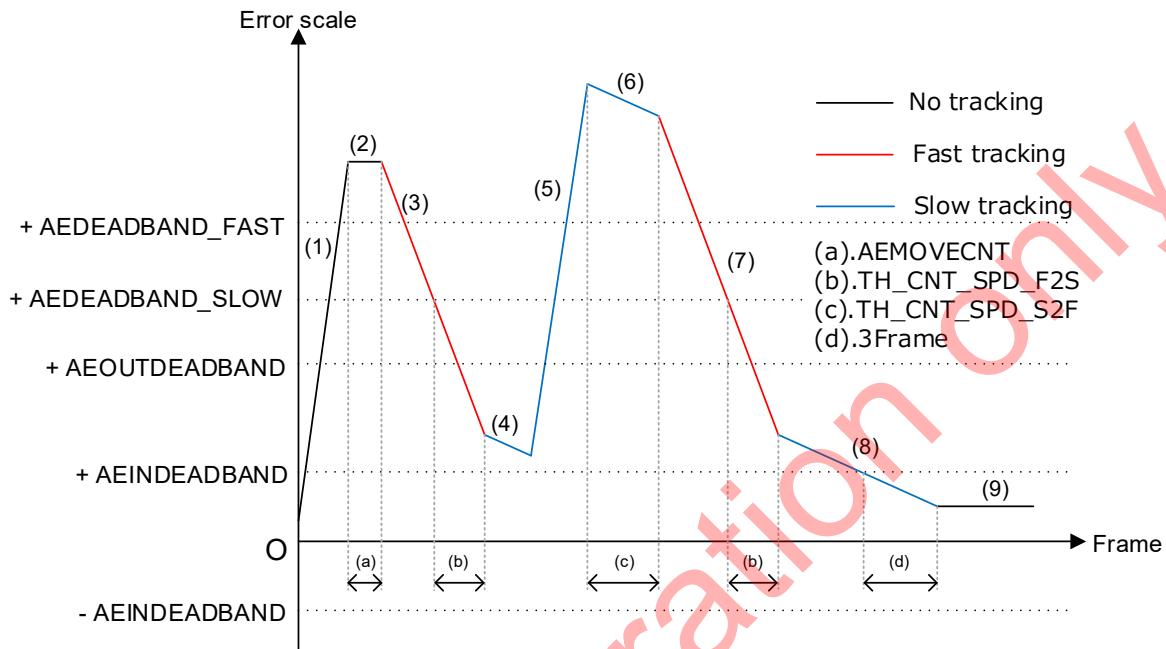


Figure 5-21 Example of Two-Tracking Speed Control Operations

- (1) The amount of AE error increases in a state of convergence.
- (2) The following state continues over multiple frames set in the AEMOVECNT register:
Amount of AE Error > High-speed Tracking Mode Threshold
- (3) The sensor transitions to the high-speed tracking mode and starts tracking.
The following state continues over multiple frames set in the TH_CNT_SPD_F2S register:
Amount of AE Error < Low-Speed Tracking Mode Threshold
- (4) The sensor transitions to the low-speed tracking mode and starts tracking.
- (5) The amount of AE error increases in a state of low-speed tracking.
- (6) In low-speed tracking mode, the following state continues over multiple frames set in the TH_CNT_SPD_S2F register:
Amount of AE Error > High-speed Tracking Mode Threshold
- (7) The sensor transitions to the high-speed tracking mode and starts tracking.
In high-speed tracking mode, the following state continues over multiple frames set in the TH_CNT_SPD_F2S register:
Amount of AE Error < Low-Speed Tracking Mode Threshold
- (8) The sensor transitions to the low-speed tracking mode and starts tracking.
When the following state continues for three consecutive frames, the sensor determines that the auto exposure has completed convergence:
Amount of AE Error < AEINDEADBAND Register Value x 6.02 / 1024
- (9) The auto exposure is in a state of convergence. Also, after transitioning from the tracking state to a state of convergence, the mode is changed to low-speed tracking mode.

5.2.3.5.6. Illuminance-Interlocking EVREF Control

The Illuminance-Interlocking EVREF control is a function that sets a maximum of 5 control points based on the subject's illuminance and the exposure compensation level for each point.

Regarding the method for setting the Illuminance-Interlocking function, refer to "[6.6 Interlocking Control Function](#)."

- To operate this function, set the EVREF_CTRL_SEL register to 1 in Normal AE mode.
- The 5 control points are named as Points A, B, C, D and E in ascending order from the lowest illuminance.
- Regarding the five control points, set the exposure compensation level and the luminance to the EVREF_GAIN_x ($x = A, B, C, D, E$) and EVREF_TH_x ($x = A, B, C, D, E$) registers.
- Illuminance can be confirmed using the ILMLEVEL register.
- A greater value of illuminance indicates a brighter condition.
- Be sure to set the registers to satisfy the following condition:
 $EVREF_TH_A \leq EVREF_TH_B \leq EVREF_TH_C \leq EVREF_TH_D \leq EVREF_TH_E$
- The sensor performs linear interpolation for values between the control points.

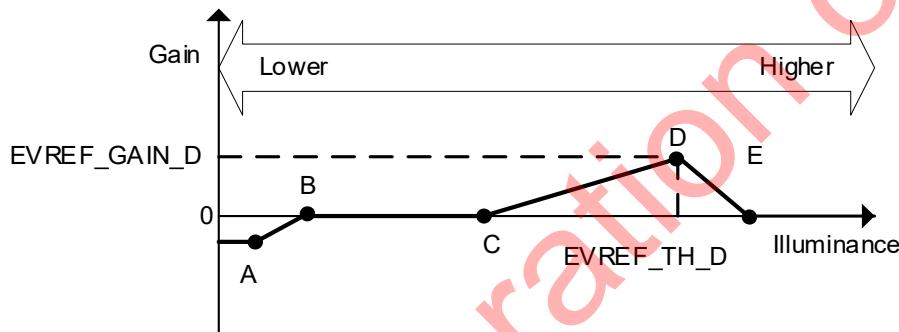


Figure 5-22 Setting the Parameters of Illuminance-Interlocking EVREF Control

5.2.3.6. Flickerless AE

When a light source, such as a fluorescent light, has a flickering frequency that is different from the exposure time, flickering (color rolling) may occur as shown in "Figure 5-23." Flickering can be mitigated by matching the frequency of flickering with the exposure time. This function is known as Flickerless AE.



Figure 5-23 Flicker (Color Rolling)

5.2.3.6.1. Detecting Flickering

This section describes how to enable or disable the automatic flicker detection and set the detection sensitivity. "Table 5-20" shows the registers used to configure the flicker settings.

Table 5-20 Registers for Flicker Detection

Register Name	Description
FLC_DTCT_100HZ_ON	This register is used to enable or disable the detection of 100-Hz flickering. 0x0: Disabled 0x1: Enabled
FLC_DTCT_120HZ_ON	This register is used to enable or disable the detection of 120-Hz flickering. 0x0: Disabled 0x1: Enabled
FLCCHTCNT_TH	This register is used to set the number of times when the result of flicker detection (i.e., the number of flicker detections) matches the number of samplings.
FLCCHTCNT_DENOMI	This register is used to set the number of samplings.

5.2.3.6.2. Flickerless AE Function's Operating Modes

Flickerless AE consists of two functions: a function that detects flickering at 50 Hz or 60 Hz, and another function that compensates for the flickering.

- The minimum exposure time for Flickerless AE is 1/100 second for 50 Hz and 1/120 second for 60 Hz. Set the FLSHT_50 and FLSHT_60 registers to the exposure time.
- The exposure time that can be set for Flickerless AE is only in multiples of the minimum exposure time. Exposure times in between these multiples are interpolated using gain.
- To set an exposure time shorter than the minimum exposure time, select the Normal AE mode.

“Figure 5-24” illustrates an example of the AE diagram in Flickerless AE mode.

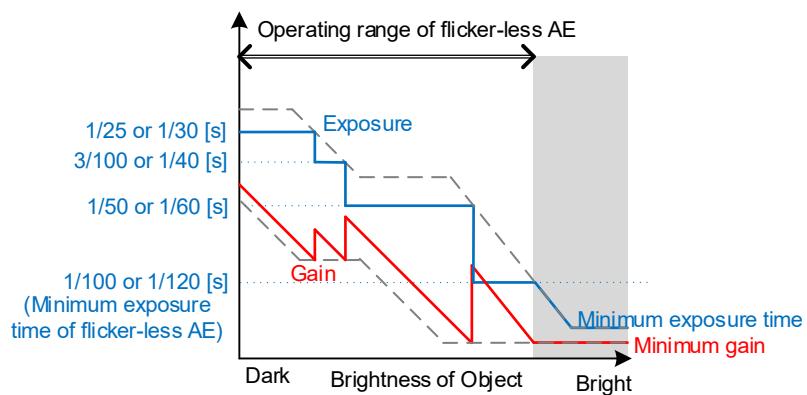


Figure 5-24 Adjusting the Exposure Time and Gain in Flickerless AE

Flickerless AE consists of multiple modes as described in **“Table 5-21.”** To activate Flickerless AE, set the AEMODE register to 0 and set the FLCMODE register to any value other than 7.

Table 5-21 List of Flickerless AE Modes

FLCMODE	Function Name	Flicker Mitigation Frequency	Initial Value	Description
0	Auto Flickerless		50 Hz, 60 Hz, No Mitigation	The sensor will mitigate flickering under the following conditions: <ul style="list-style-type: none">Either while the sensor starts up or when the settings have been configuredWhen the sensor detects the initial mitigation frequency When having detected any frequency that can be mitigated, the sensor will mitigate flickering corresponding to the flickering detected. If the sensor has not detected any mitigable frequency, the sensor will not mitigate flickering.
1	“50-Hz Flickerless At Startup” Function Flickerless	50 Hz 60 Hz	50 Hz	<ul style="list-style-type: none">To suspend flicker mitigation, use the sensor’s Flicker Mitigation Reset function.
2	“60-Hz Flickerless At Startup” Function Flickerless		60 Hz	
3	“Forced 50-Hz Flickerless” Function Flickerless	50 Hz	50 Hz	The sensor always mitigates flickering that is listed in the mitigable frequency. <ul style="list-style-type: none">Since these modes are not supported by the Flicker Mitigation Reset function, flicker mitigation will not be suspended even if the frequency is to be reset.
4	“Forced 60-Hz Flickerless” Function Flickerless	60 Hz	60 Hz	<ul style="list-style-type: none">When having detected any flickering that is listed in the mitigable frequency, the sensor will mitigate flickering. If the sensor has not detected any mitigable frequency, the sensor will not mitigate flickering.To suspend flicker mitigation, use the sensor’s Flicker Mitigation Reset function.
5	“Fixed 50-Hz” Function Flickerless	50 Hz	50 Hz	
6	“Fixed 60-Hz” Function Flickerless	60 Hz	60 Hz	
7	Flickerless Disabled	-	-	The sensor detects flickering, but does not mitigate any flickering.

5.2.3.6.3. Operating States in Flickerless AE Mode

"Table 5-22" describes the operating states in Flickerless AE mode.

Table 5-22 Operating States in Flickerless AE Mode

State	Description
No flicker mitigation	The sensor is in a state of not performing flicker mitigation.
50-Hz Flicker Mitigation	The sensor is in a state of performing 50-Hz flicker mitigation.
60-Hz Flicker Mitigation	The sensor is in a state of performing 60-Hz flicker mitigation.

■ FLCMODE = 0 to 2

Normal operations among Auto Flickerless, 50-Hz Flickerless at startup and 60-Hz Flickerless at startup are the same except for the operations when the sensor starts up or the operations of Flickerless AE, corresponding to the settings.

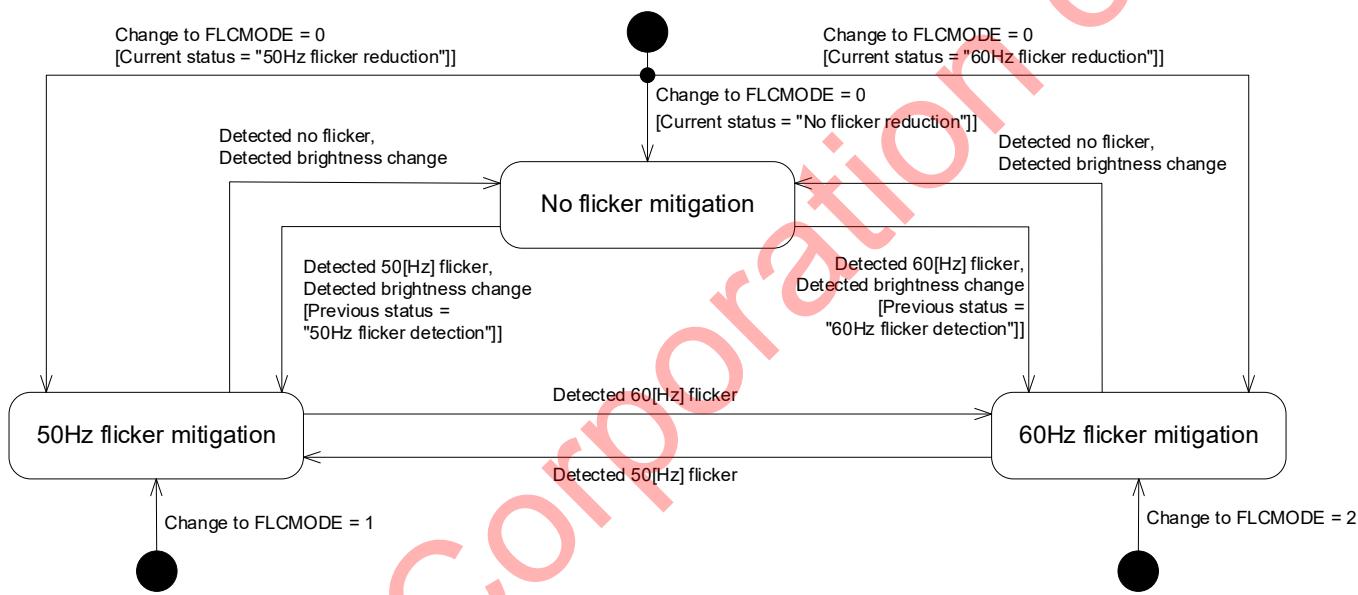


Figure 5-25 State Transitions of Flickerless AE (FLCMODE = 0, 1, 2)

■ FLCMODE = 3, 4, 7

In Forced 50-Hz or 60-Hz Flickerless states, the sensor operates while always mitigating flickering at 50 Hz or 60 Hz respectively. In the Flickerless Off state, the sensor does not mitigate flickering at all.

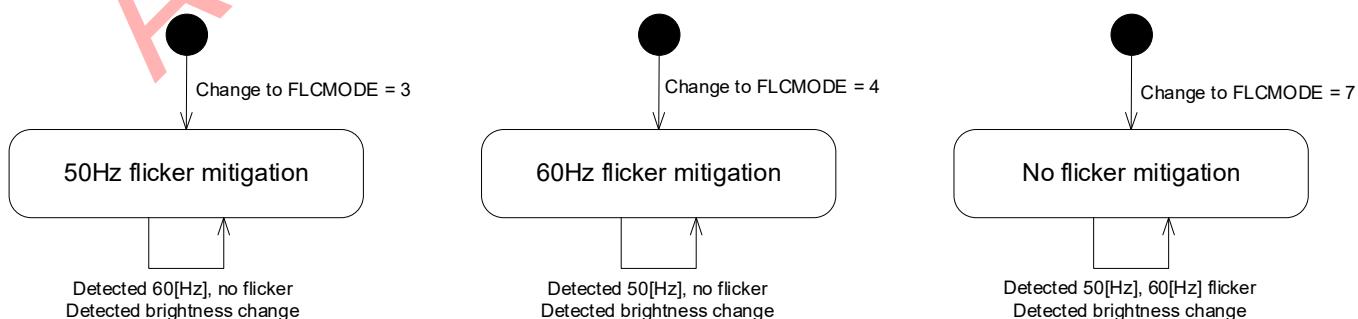


Figure 5-26 State Transitions of Flickerless AE (FLCMODE = 3, 4, 7)

■ FLCMODE = 5, 6

The Fixed 50-Hz Flickerless state transitions only to the No Flicker Mitigation or 50-Hz Flicker Mitigation states, not to the 60-Hz Flicker Mitigation state. In the same way, the Fixed 60-Hz Flickerless state transitions only to the No Flicker Mitigation or 60-Hz Flicker Mitigation states, and not to the 50-Hz Flicker Mitigation state.

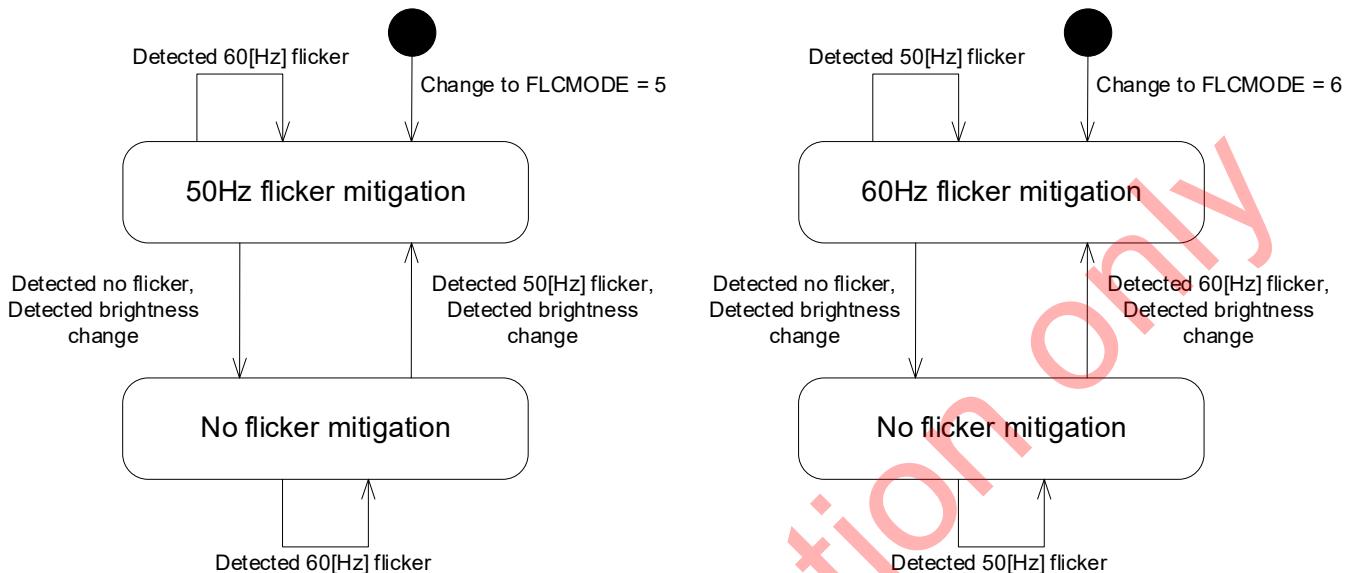


Figure 5-27 State Transitions of Flickerless AE (FLCMODE = 5, 6)

5.2.3.6.4. Flicker Mitigation Reset Function

The Flicker Mitigation Reset function resets the flicker mitigation when the brightness of the subject changes during flicker mitigation.

- This function resets the flicker mitigation when the absolute value of the amount of AE error continuously exceeds the FLC_RESET_DB register's threshold by the count that has been set in the FLC_RESET_CNT register.
- When the FLC_RESET_CNT register is set to 0, this function will not reset any flicker mitigation.
- Apply this function in Flickerless AE mode in which a flicker mitigation reset is enabled as illustrated in "Figure 5-28."

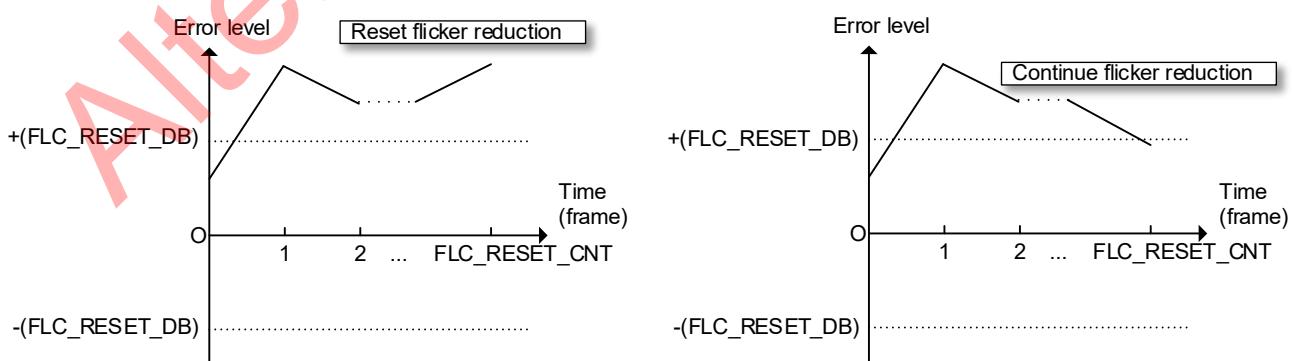


Figure 5-28 Flicker Mitigation Reset Function

5.2.3.6.5. High Luminance Flickerless AE Function

When the subject becomes brighter than the condition in which the flickerless minimum exposure time is 1/100 second or 1/120 second, the sensor switches to the normal exposure control. However, the user can prevent the transition to normal auto exposure by using the High Luminance Flickerless AE function.

- When the amount of error is less than or equal to the value set in the AEIN2OUT register, the sensor will continue Flickerless AE operations. Set the AEIN2OUT register to satisfy the following condition:

$$\text{AEIN2OUT} \times 0x10 \times 6.02 / 1024 \leq \text{FLC_RESET_DB} \times 0.3$$
- The threshold at which the control method returns from Normal AE to Flickerless AE can be adjusted by using the AEOUT2INGAP register. Refer to “**Figure 5-29**” regarding the relationship between this adjustment and the operational ranges of Normal AE and Flickerless AE.

◆ Note

In the range, in which the sensor performs adjustments using the AEIN2OUT register's value, flicker reduction takes precedence over exposure compensation. Regarding exposure compensation, refer to “**5.2.3.2 Exposure Control**.” Setting exposure compensation to a negative value disables exposure compensation.

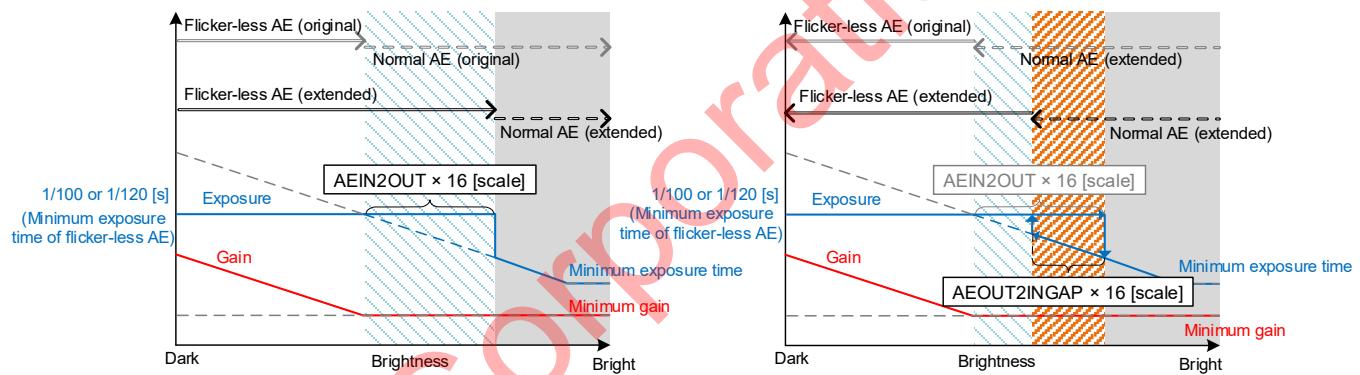


Figure 5-29 High Luminance Flickerless AE Function

5.2.3.6.6. Confirming the State of Flickerless Operations

The user can check whether the sensor mitigates flickering using the FLCLESS_STS register.

5.2.3.7. ME

5.2.3.7.1. Scale ME

In Scale ME mode, the sensor converts the exposure time and gain using the AE diagram from a specified output gain, and performs exposure control. To select the Scale ME mode, set the AEMODE register to 2.

In this mode, first set the desired position on the AE diagram using the SCALEME_SCL register. Increasing the register's value by 1024 will increase the gain by 6.02 dB. The value of the SCALEME_SCL register is defined as 0 when the illuminance is at the maximum value on the AE diagram.

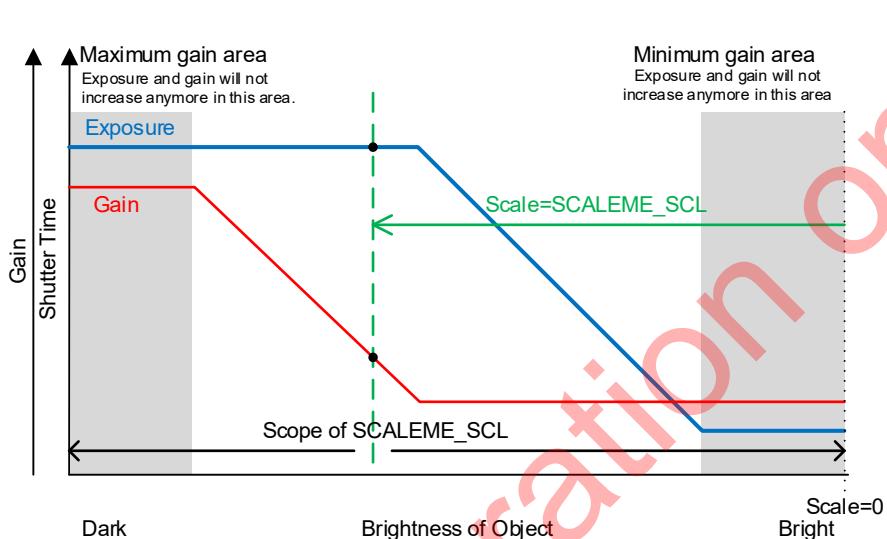


Figure 5-30 Output Gain in Scale ME Mode

5.2.3.7.2. Full ME

Full ME is a method in which the host directly controls exposure time and gain instead of the sensor's automatic exposure. “**Table 5-23**” describes registers used to configure the settings of the Full ME method.

Set exposure time using the exposure unit in the “Unit for Settings” column of “**Table 5-23**.”

Table 5-23 Registers Used to Configure the Settings of the Full ME Method

Variable for Settings	Target Line	Register Name	Unit for Settings	Description
Exposure Time	SP1	FME_SHTVAL	FME_SHTVAL_UNIT	SP1's exposure time* ¹
	SP2	FME_SHTVAL_S1	FME_SHTVAL_S1_UNIT	SP2's exposure time* ²
Analog Gain	SP1_HCG	FME_SENSAGAIN	0.1 [dB]	SP1_HCG line's analog gain
	SP1_LCG	FME_SENSAGAIN_S1	0.1 [dB]	SP1_LCG line's analog gain
	SP2H	FME_SENSAGAIN_S2	0.1 [dB]	SP2H line's analog gain
	SP2L	FME_SENSAGAIN_S3	0.1 [dB]	SP2L line's analog gain
Digital Gain (With HDR imaging)	-	FME_ISPGAIN	0.1 [dB]	This register indicates digital gain for HDR output.
Digital Gain (Without HDR imaging)	SP1_HCG	ISP_GAIN_RAW0	Magnification factor	Digital gain for the SP1_HCG line
	SP1_LCG	ISP_GAIN_RAW1	Magnification factor	Digital gain for the SP1_LCG line
	SP2H	ISP_GAIN_RAW2	Magnification factor	Digital gain for the SP2H line
	SP2L	ISP_GAIN_RAW3	Magnification factor	Digital gain for the SP2L line

* ¹ The unit of SP1's exposure time = FME_SHTVAL; The unit of exposure time varies corresponding to the value of the FME_SHTVAL_UNIT register (i.e., [line], [μs] or [frame])

* ² The unit of SP2's exposure time = FME_SHTVAL_S1; The unit of exposure time varies corresponding to the value of the FME_SHTVAL_S1_UNIT register (i.e., [line], [μs] or [frame])

◆ Note

The number of steps that can be set for analog and digital gains differs, depending on the range to be set. For details, refer to “**5.2.4 Conditions**.”

■ Calculating the Exposure Time

When the exposure time is set in units of lines by the Full ME method, it can be calculated using the following equations:

- 1 line period

$$T_{\text{line}} = \frac{1}{\text{Frame rate} \times \text{VMAX}}$$

- 1 pixel period

$$T_{\text{pixel}} = \frac{1}{\text{Frame rate} \times \text{VMAX} \times \text{FW_MODE_HMAX}}$$

- SP1_HCG exposure time

$$(\text{FME_SHTVAL} \times T_{\text{line}}) + (\text{FW_MODE_INTG_TIME_FINE_SP1} \times T_{\text{pixel}})$$

- SP1_LCG exposure time

$$\text{FME_SHTVAL} \times T_{\text{line}}$$

- SP2 exposure time

$$(\text{FME_SHTVAL_S1} \times T_{\text{line}}) + (\text{FW_MODE_INTG_TIME_FINE_SP2} \times T_{\text{pixel}})$$

◇ Memo

- The blue notations in the aforementioned equations are registers' names.
- For details regarding the VMAX and frame rates, refer to “[5.2.3.2.1 Units of Exposure Time](#).”

5.2.3.8. LED Flickering

LED flickering occurs due to the difference between an LED's light-emission period and the sensor's image-capturing period. For example, even when an LED traffic light is on, if the exposure time for image-capturing is shorter than the LED's light-emission period, the sensor cannot capture the LED's light-emission state and may produce an image with the LED traffic light off.

“[Figure 5-31](#)” illustrates an example of the sensor's output images when LED flickering occurs while a red LED traffic light is on.

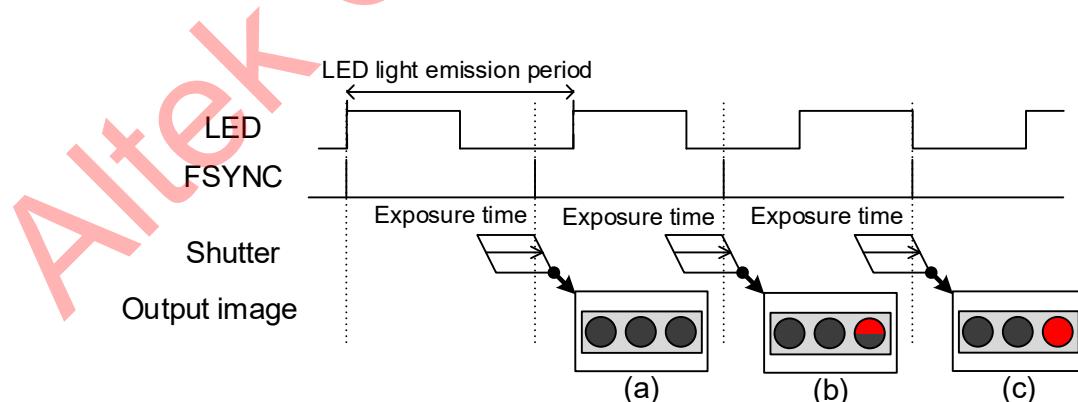


Figure 5-31 Example of Sensor's Output Images When LED Flickering Occurs While a Red LED Traffic Light Is On

It is under the condition that the sensor's image-capturing period is shorter than the LED's light-emission period. The details of each image are as follows:

(a)

In output image (a), all lights are Off because the image has been captured when all lights were Off during their light-emission cycles.

(b)

In output image (b), half the red light is Off because the image has been captured when the red light's state was in transition from On to Off.

(c)

In output image (c), the red light is On because the image has been captured when the red light was On.

LED flickering occurs when the sensor repeats the output sequence in which the sensor transmits images such as (a), (b) and (c) indicating the sensor has correctly or incorrectly captured the light-emission of an LED light source.

5.2.3.8.1. How to Mitigate LED Flickering

The sensor mitigates LED flickering (LFM) by setting the exposure time longer than an LED's light emission period so that the sensor can capture the LED's light emission state. "Figure 5-32" illustrates an example of capturing an image when setting the exposure time longer than an LED's light emission period. In this example, since the sensor captures an LED's light emission state during the sensor's exposure time, output images (a), (b) and (c) appear with LED flickering mitigated.

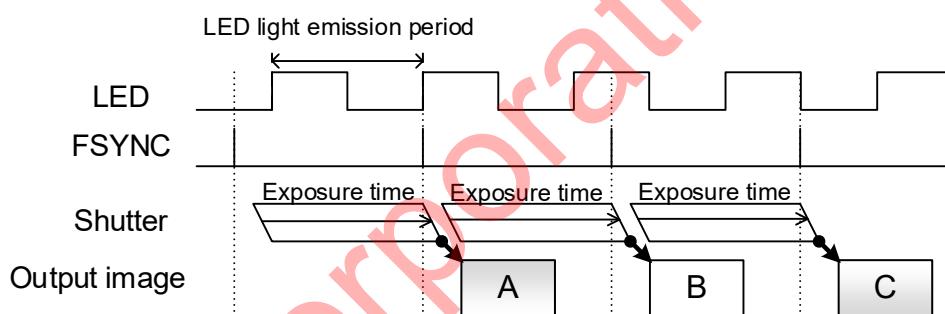


Figure 5-32 Image-Capturing Example of Mitigated LED Flickering

The sensor performs exposure using the rolling shutter method. Consequently, the luminance varies within the same image if the period, during which the light emission of an LED is captured line by line, differs. See output images (a) and (c) for example. In order to suppress the luminance variation, configure the settings so that the exposure time of an LED's light emission is uniform for each line.

❖ Memo

Note that increasing exposure time may cause saturation of pixels and blown-out highlights. Therefore, set the exposure time appropriately.

5.2.4. Conditions

5.2.4.1. Conditions on Analog and Digital Gains

Adjust analog and digital gains within the ranges as described in “**Table 5-24.**”

Table 5-24 Available Ranges and Steps for Analog and Digital Gains

Gain	Available Range	Unit for Settings
Analog Gain	0 to 24 dB	0.1 dB
	24 to 30 dB	0.3 dB
Digital Gain	0 to 48 dB	0.1 dB

5.2.4.2. Available Range for the Exposure Time

Set the exposure time corresponding to the sync mode within the following range:

- In the case of internal sync
 $4 \leq \text{Exposure Time} \leq (\text{VMAX} \times 8) - 8$
- In the case of external pulse-based sync
 $4 \leq \text{Exposure Time} \leq (\text{VMAX} \times 8) - 18$
- In the case of shutter trigger-based sync
 $4 \leq \text{Exposure Time} \leq \text{VMAX} - 18$

◇ **Memo**

- The aforementioned formulas are expressed in units of lines. For details on how to calculate the exposure time per line, refer to “**5.2.3.2.1 Units of Exposure Time.**”
- The user can check the number of extended frames applied, using the Front Embedded Data. For details regarding the Front Embedded Data, refer to “**6.9.3.5.21 Extended Frame and Extended Line Information.**”

5.2.5. Interface

5.2.5.1. Input Registers

Table 5-25 Input Registers for the Exposure Control Function

[AE]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xABCO	1	7:0	AEMODE	R/W	U8.0	AE Mode 0: AE (Auto) 1: AE (Hold) 2: Scale ME 3: Full ME Any other settings are prohibited.
0xABC2	2	15:0	SCALEME_SCL	R/W	U16.0	This register is used to set the output for exposure control in Scale ME mode. • This register is used to transmit the settings of gain and exposure time, which are equivalent to a value of "User-set value x 6.02 / 1024 [dB]" with the highest illuminance on the AE diagram.
0xABC4	4	31:0	EVREF	R/W	U32.0	This register is used to set the target value for AE convergence. • AE converges so that the light metering evaluation value equals this value.
0xABC8	1	7:0	EVREF_OFFSET	R/W	S7.0	This register is used to set the compensation level for the EVREF. [0.1 dB]
0xABC9	1	0	EVREF_CTRL_SEL	R/W	U1.0	This register is used to enable or disable the illuminance interlocking EVREF control. 0: Disabled 1: Enabled
0xABCA	1	7:0	EVREF_GAIN_A	R/W	S7.0	An amount of increase or decrease in illuminance interlocking EVREF control (Control point A: darkest point) • Set the amount of exposure compensation using the gain level in relation to the reference EVREF. User-set value x 0.3 [dB]
0xABCB	1	7:0	EVREF_GAIN_B	R/W	S7.0	An amount of increase or decrease in illuminance interlocking EVREF control (Control point B: dark point) • Set the amount of exposure compensation using the gain level in relation to the reference EVREF. User-set value x 0.3 [dB]
0xABCC	1	7:0	EVREF_GAIN_C	R/W	S7.0	An amount of increase or decrease in illuminance interlocking EVREF control (Control point C: middle point) • Set the amount of exposure compensation using the gain level in relation to the reference EVREF. User-set value x 0.3 [dB]
0xABCD	1	7:0	EVREF_GAIN_D	R/W	S7.0	An amount of increase or decrease in illuminance interlocking EVREF control (Control point D: bright point) • Set the amount of exposure compensation using the gain level in relation to the reference EVREF. User-set value x 0.3 [dB]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xABCE	1	7:0	EVREF_GAIN_E	R/W	S7.0	An amount of increase or decrease in illuminance interlocking EVREF control (Control point E: brightest point) • Set the amount of exposure compensation using the gain level in relation to the reference EVREF. User-set value x 0.3 [dB]
0xABCF	1	7:0	EVREF_TH_A	R/W	U8.0	The illuminance (ILMLEVEL) at Control Point A (darkest point) for illuminance interlocking EVREF control 0x00: Darkest - 0xFF: Brightest • Set the value to satisfy the following condition: $EVREF_TH_A \leq EVREF_TH_B$
0xABD0	1	7:0	EVREF_TH_B	R/W	U8.0	The illuminance (ILMLEVEL) at Control Point B (dark point) for illuminance interlocking EVREF control 0x00: Darkest - 0xFF: Brightest • Set the value to satisfy the following condition: $EVREF_TH_A \leq EVREF_TH_B$ and $EVREF_TH_B \leq EVREF_TH_C$
0xABD1	1	7:0	EVREF_TH_C	R/W	U8.0	The illuminance (ILMLEVEL) at Control Point C (middle point) for illuminance interlocking EVREF control 0x00: Darkest - 0xFF: Brightest • Set the value to satisfy the following condition: $EVREF_TH_B \leq EVREF_TH_C$ and $EVREF_TH_C \leq EVREF_TH_D$
0xABD2	1	7:0	EVREF_TH_D	R/W	U8.0	The illuminance (ILMLEVEL) at Control Point D (bright point) for illuminance interlocking EVREF control 0x00: Darkest - 0xFF: Brightest • Set the value to satisfy the following condition: $EVREF_TH_C \leq EVREF_TH_D$ and $EVREF_TH_D \leq EVREF_TH_E$
0xABD3	1	7:0	EVREF_TH_E	R/W	U8.0	The illuminance at Control Point E (brightest point) for illuminance interlocking EVREF control 0x00: Darkest - 0xFF: Brightest • Set the value to satisfy the following condition: $EVREF_TH_D \leq EVREF_TH_E$
0xABD4	1	7:0	AESPEED	R/W	U8.0	This register is used to set the AE convergence speed. • Increasing the value will increase the AE convergence speed.
0xABD6	2	15:0	ERRSCLLIMIT	R/W	U16.0	This register is used to set the upper and lower limits in an absolute value for the amount of predicted error. • The positive value of this register is applied as the upper limit. • The negative value of this register is applied as the lower limit. • Setting any value greater than 0x7FFF is prohibited.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xABDB	1	7:0	AEMOVECNT	R/W	U8.0	<p>This register is used to set the number of frames to initiate tracking exposure under the following conditions:</p> <ul style="list-style-type: none"> • In a state where AE convergence has been completed. • The occurrence of an amount of AE error greater than or equal to the value set in the AEOUTDEADBAND register. <p>If this occurrence continues for the number of frames greater than or equal to the value of the AEMOVECNT register.</p>
0xABDC	1	7:0	AEINDEADBAND	R/W	U8.0	<p>This register is used to set the width of the dead zone, by which the sensor determines the completion of convergence. (User-set value x 6.02 / 1024 [dB])</p> <ul style="list-style-type: none"> • The sensor determines that the convergence is complete when the amount of AE error continues to be less than this register's value for three frames.
0xABDD	1	7:0	AEOUTDEADBAND	R/W	U8.0	<p>This register is used to set the width of the dead zone, by which the sensor determines the beginning of exposure tracking. (User-set value x 16 x 6.02 / 1024 [dB])</p> <ul style="list-style-type: none"> • Tracking begins when the amount of AE error exceeds this register's value and continues for the number of frames greater than or equal to the value set in the AEMOVECNT register.
0x9C08	4	31:0	FME_SHTVAL	R/W	U32.0	[For the Full ME mode] Exposure time for SP1 * Valid only when the AEMODE register is set to 3.
0x9C0C	1	7:0	FME_SHTVAL_UNIT	R/W	U8.0	[For the Full ME mode] This register is used to set the unit for FME_SHTVAL 1: In lines 3: In microseconds 4: In frames Any other settings are prohibited.
0x9C10	4	31:0	FME_SHTVAL_S1	R/W	U32.0	[For the Full ME mode] Exposure time for SP2 * Valid only when the AEMODE register is set to 3.
0x9C14	1	7:0	FME_SHTVAL_S1_UNIT	R/W	U8.0	[For the Full ME mode] This register is used to set the unit for FME_SHTVAL_S1. 1: In lines 3: In microseconds 4: In frames Any other settings are prohibited.
0x9C18	2	9:0	FME_SESAGAIN	R/W	U10.0	[For the Full ME mode] This register is used to set analog gain for SP1_HCG. User-set value x 0.1 [dB] * Valid only when the AEMODE register is set to 3.
0x9C1A	2	9:0	FME_SESAGAIN_S1	R/W	U10.0	[For the Full ME mode] This register is used to set analog gain for SP1_LCG. User-set value x 0.1 [dB] * Valid only when the AEMODE register is set to 3.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x9C1C	2	9:0	FME_SENSAGAIN_S2	R/W	U10.0	[For the Full ME mode] This register is used to set analog gain for SP2H. User-set value x 0.1 [dB] * Valid only when the AEMODE register is set to 3.
0x9C1E	2	9:0	FME_SENSAGAIN_S3	R/W	U10.0	[For the Full ME mode] This register is used to set analog gain for SP2L. User-set value x 0.1 [dB] * Valid only when the AEMODE register is set to 3.
0x9C20	2	9:0	FME_ISPGAIN	R/W	U10.0	[For the Full ME mode] This register is used to set digital gain. User-set value x 0.1 [dB] * Valid only when the AEMODE register is set to 3.
0xAC0F	1	7:0	AEMOVECNT_SLOW	R/W	U8.0	This register is used to set the threshold for the frame count which is used to determinate that AE is outside the dead zone. (For low-speed tracking) <ul style="list-style-type: none"> This register is used to set the number of frames to initiate tracking exposure under the following conditions: <ul style="list-style-type: none"> In the case of low-speed tracking The occurrence of the amount of AE error greater than or equal to the value set in the AEOUTDEADBAND register When this occurrence continues for the number of frames greater than or equal to the value of the AEMOVECNT_SLOW register
0xAC10	1	7:0	ERRSCLLIMIT_SLOW	R/W	U8.0	This register is used to set the upper and lower limits for the predicted amount of error. (For low-speed tracking) <ul style="list-style-type: none"> The positive value of this register is applied as the upper limit. The negative value of this register is applied as the lower limit.
0xAC11	1	7:0	TH_CNT_SPD_F2S	R/W	U8.0	This register is used to set the threshold for the frame count when the sensor switches the tracking speed from high to low.
0xAC12	1	7:0	TH_CNT_SPD_S2F	R/W	U8.0	This register is used to set the threshold for the frame count when the sensor switches the tracking speed from low to high.
0xAC13	1	7:0	AEDEADBAND_FAST	R/W	U8.0	This register is used to set the width of the dead zone (outside), by which the sensor checks whether the tracking speed is high or low. <ul style="list-style-type: none"> Dead zone width = Register value x $16 \times 6.02/1024$ [dB]
0xAC14	1	7:0	AEDEADBAND_SLOW	R/W	U8.0	This register is used to set the width of the dead zone (inside), by which the sensor checks whether the tracking speed is high or low. <ul style="list-style-type: none"> Dead zone width = Register value x $16 \times 6.02/1024$ [dB]
0xAC26	1	7:0	AGC_AGAIN_SP1L	R/W	U8.0	This register is used to set the minimum gain for SP1_LCG. User-set value x 0.1 [dB]

[AE_DGRM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xAC38	1	3:0	CTRL_AREA_TYPE_01	R/W	U4.0	Selection of the exposure control for the AE diagram (Region 01) 0: Disabled 1: Exposure time 2: Gain 3: No control
0xAC39	1	3:0	CTRL_AREA_TYPE_02	R/W	U4.0	Selection of the exposure control for the AE diagram (Region 02) 0: Disabled 1: Exposure time 2: Gain 3: No control
...		
0xAC3D	1	3:0	CTRL_AREA_TYPE_06	R/W	U4.0	Selection of the exposure control for the AE diagram (Region 06) 0: Disabled 1: Exposure time 2: Gain 3: No control
0xAC40	4	31:0	SHT_CTRL_VAL_MIN	R/W	U32.0	Setting of the shortest exposure time. • Specify the unit using the SHT_CTRL_UNIT_MIN register.
0xAC44	4	31:0	SHT_CTRL_VAL_01	R/W	U32.0	This register is used to set the exposure time when the user sets each value of the CTRL_AREA_TYPE_x (01 to 06) registers to 1. (1st exposure time setting) • Specify the unit using the SHT_CTRL_UNIT_01 register.
0xAC48	4	31:0	SHT_CTRL_VAL_02	R/W	U32.0	This register is used to set the exposure time when the user sets each value of the CTRL_AREA_TYPE_x (01 to 06) registers to 1. (2nd exposure time setting) • Specify the unit using the SHT_CTRL_UNIT_02 register.
0xAC4C	1	7:0	SHT_CTRL_UNIT_MIN	R/W	U8.0	This register is used to set the unit for the SHT_CTRL_VAL_MIN register. 1: In lines 3: in μ sec 4: In frames Any other settings are prohibited.
0xAC4D	1	3:0	SHT_CTRL_UNIT_01	R/W	U4.0	This register is used to set the unit for the SHT_CTRL_VAL_01 register. 1: In lines 3: in μ sec 4: In frames Any other settings are prohibited.
0xAC4E	1	3:0	SHT_CTRL_UNIT_02	R/W	U4.0	This register is used to set the unit for the SHT_CTRL_VAL_02 register. 1: In lines 3: in μ sec 4: In frames Any other settings are prohibited.
0xAC5A	2	10:0	AGC_GAIN_MIN	R/W	U11.0	This register is used to set the minimum gain. User-set value x 0.1 [dB]
0xAC5C	2	10:0	AGC_GAIN_01	R/W	U11.0	This register is used to set the gain when the user sets each value of the CTRL_AREA_TYPE_x (01 to 06) registers to 1. (1st gain setting) User-set value x 0.1 [dB]
0xAC5E	2	10:0	AGC_GAIN_02	R/W	U11.0	This register is used to set the gain when the user sets each value of the CTRL_AREA_TYPE_x (01 to 06) registers to 1. (2nd gain setting) User-set value x 0.1 [dB]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xAC60	2	10:0	AGC_GAIN_03	R/W	U11.0	This register is used to set the gain when the user sets each value of the CTRL_AREA_TYPE_x (01 to 06) registers to 1. (3rd gain setting) User-set value x 0.1 [dB]
0xAC74	2	15:0	NCTRL_WIDTH_01	R/W	U16.0	This register is used to set the width of the No Control segment when the user sets the CTRL_AREA_TYPE_x (01 to 06) registers to 3. User-set value x 6.02 / 1024 [dB]

[AE_FLC]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xAC78	1	2:0	FLCMODE	R/W	U3.0	This register is used to set the flickerless mode. 0: Auto Flickerless 1: 50-Hz Flickerless at Startup 2: 60-Hz Flickerless at Startup 3: Forced 50-Hz Flickerless 4: Forced 60-Hz Flickerless 5: Fixed 50-Hz Flickerless 6: Fixed 60-Hz Flickerless 7: Flickerless disabled mode
0xAC79	1	7:0	FLCCHTCNT_TH	R/W	U8.0	This register is used to set the number of times when the result of flicker detection (i.e., the number of flicker detections) matches the number of samplings. <ul style="list-style-type: none">Set the number of frames to eliminate chatter when flicker is detected.
0xAC7A	1	7:0	FLCCHTCNT_DENOMI	R/W	U8.0	This register is used to set the number of samplings. <ul style="list-style-type: none">Set the parameter of the number of frames to eliminate chatter when flicker is detected.
0xAC7C	1	7:0	AEIN2OUT	R/W	U8.0	This register is used to set the High Luminance Flickerless AE function <ul style="list-style-type: none">When the amount of error is less than or equal to "User-set value x 16 x 6.02 / 1024 [dB]," the sensor will not switch to normal AE.
0xAC7D	1	7:0	AEOUT2INGAP	R/W	U8.0	This register is used to set the High Luminance Flickerless AE function <ul style="list-style-type: none">The sensor adjusts the threshold for the normal AE operation to return to the Flickerless AE operation.
0xAC84	2	15:0	FLSHT_50	R/W	U16.0	This register is used to set the shutter time in 50-Hz flickerless mode. <ul style="list-style-type: none">Set a shutter time of 1/100 [s] in microseconds [μs].
0xAC86	2	15:0	FLSHT_60	R/W	U16.0	This register is used to set the shutter time in 60-Hz flickerless mode. <ul style="list-style-type: none">Set a shutter time of 1/120 [s] in microseconds [μs].
0xAC88	1	7:0	FLC_RESET_DB	R/W	U8.0	This register is used to set the error level for a flicker mitigation reset. User-set value x 0.3 [dB]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xAC89	1	7:0	FLC_RESET_CNT	R/W	U8.0	Setting of the frame count value for a flicker mitigation reset • When an AE error exceeds the error level set in the FLC_RESET_DB register for the consecutive number of frames set in the FLC_RESET_CNT register, the sensor performs the Flicker Mitigation Reset function. When this register is set to 0, the sensor does not perform the Flicker Mitigation Reset function.
0xACAB	1	0	FLC_DTCT_100HZ_ON	R/W	U1.0	This register is used to enable or disable the detection of 100-Hz flickering. 0x0: Disabled 0x1: Enabled
		1	FLC_DTCT_120HZ_ON	R/W	U1.0	This register is used to enable or disable the detection of 120-Hz flickering. 0x0: Disabled 0x1: Enabled

[AE_FRM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xACB2	1	0	SENS_REVERSE_CTRL	R/W	U1.0	This register is used to enable or disable the interlocking between the Horizontal/Vertical Flip function and the settings of light metering window's weights. 0: The settings of the light metering window's weights are not interlocked with the Horizontal/Vertical Flip function. 1: The settings of the light metering window's weights are interlocked with the Horizontal/Vertical Flip function.
0xACB6	1	7:0	MESH_WEIGHT_00	R/W	U8.0	Setting of the weight coefficient for the Mesh light metering (For Cell #00)
0xACB7	1	7:0	MESH_WEIGHT_01	R/W	U8.0	Setting of the weight coefficient for the Mesh light metering (For Cell #01)
...		
0xAF4	1	7:0	MESH_WEIGHT_62	R/W	U8.0	Setting of the weight coefficient for the Mesh light metering (For Cell #62)
0xAF6	2	9:0	HIST_WEIGHT_00	R/W	U10.0	Setting of the weight coefficient for the Histogram light metering (For Cell #00)
0xAF8	2	9:0	HIST_WEIGHT_01	R/W	U10.0	Setting of the weight coefficient for the Histogram light metering (For Cell #01)
...		
0xAD30	2	9:0	HIST_WEIGHT_29	R/W	U10.0	Setting of the weight coefficient for the Histogram light metering (For Cell #29)
0xAD36	1	0	HISTTH_SEL	R/W	U1.0	Setting of the Histogram Light Metering mode 0: Static histogram 1: Dynamic histogram
0xAD40	3	23:0	MANUALHISTTH00	R/W	U24.0	Setting of the threshold for Region #00 in static histogram Available range: 0 to 4095
0xAD44	3	23:0	MANUALHISTTH01	R/W	U24.0	Setting of the threshold for Region #01 in static histogram Available range: 0 to 4095
...		
0xADB4	3	23:0	MANUALHISTTH29	R/W	U24.0	Setting of the threshold for Region #29 in static histogram Available range: 0 to 4095
0xADBC	1	7:0	BLNDHIST_ILM_LOW	R/W	U8.0	Setting of the threshold for Blend-Switching Light Metering (Lower illuminance)

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xADBD	1	7:0	BLNDHIST_ILM_HIGH	R/W	U8.0	Setting of the threshold for Blend-Switching Light Metering (Higher illuminance)

[AE_OPD]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xADC0	1	1:0	AE_WND_MODE	R/W	U2.0	This register is used to select the mode for the AE light metering window. 0: Specify the window using the cell's width and height in pixels when dividing the light metering window into 9 horizontal x 7 vertical cells. 1: Specifies using a width-height ratio with respect to the Active Area. 2: Specifies using a width-height ratio with respect to the Active Area (Output). Any other settings are prohibited.
0xA010	2	15:0	AE_WND_OFFSET_H	R/W	S15.0	This register is used to set the horizontal offset from the center of the reference area to the center of the window to be set. The reference area is as follows: <ul style="list-style-type: none">When AE_WND_MODE = 0 or 1, the area is the Active Area.When AE_WND_MODE = 2, the area is the output image.
0xA012	2	15:0	AE_WND_OFFSET_V	R/W	S15.0	This register is used to set the vertical offset from the center of the reference area to the center of the window to be set. The reference area is as follows: <ul style="list-style-type: none">When AE_WND_MODE = 0 or 1, the area is the Active Area.When AE_WND_MODE = 2, the area is the output image.
0xA014	2	15:0	AE_WND_SIZE_H	R/W	U16.0	This register is used to set the width of the light metering window when adjusting its position. <ul style="list-style-type: none">When AE_WND_MODE = 0, set the width of the cell, 63 (9 horizontal x 7 vertical cells) of which constitute the light metering window, using a value that is a multiple of 2 pixels. (Unit: U16.0)When AE_WND_MODE = 1, set the width of the cell, 63 (9 horizontal x 7 vertical cells) of which constitute the light metering window, using a ratio with respect to the width of the Active Area. (Unit: U1.8) Available range: 16 (0x10) to 256 (0x100)When AE_WND_MODE = 2, set the width of the cell, 63 (9 horizontal x 7 vertical cells) of which constitute the light metering window, using a ratio with respect to the width of the output image. (Unit: U1.8) Available range: 16 (0x10) to 256 (0x100)

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xA016	2	15:0	AE_WND_SIZE_V	R/W	U16.0	<p>This register is used to set the height of the light metering window when adjusting its position.</p> <ul style="list-style-type: none"> When AE_WND_MODE = 0, set the height of the cell, 63 (9 horizontal x 7 vertical cells) of which constitute the light metering window, using a value that is a multiple of 2 pixels. (Unit: U16.0) When AE_WND_MODE = 1, set the height of the cell, 63 (9 horizontal x 7 vertical cells) of which constitute the light metering window, using a ratio with respect to the height of the Active Area. (Unit: U1.8) Available range: 4 (0x04) to 256 (0x100) When AE_WND_MODE = 2, set the height of the cell, 63 (9 horizontal x 7 vertical cells) of which constitute the light metering window, using a ratio with respect to the height of the output image. (Unit: U1.8) Available range: 4 (0x04) to 256 (0x100)
0xADD2	1	0	AE_OPD_REVERSE_EN	R/W	U1.0	<p>This register is used to enable or disable the tracking of the light metering window in horizontal and vertical directions</p> <p>0: Disabled 1: Enabled</p>
0xA018	1	0	OPD_MASK_EN_00	R/W	U1.0	<p>This register is used to enable or disable the display of the Rectangular Mask #0 for exposure control.</p> <p>0: Disabled 1: Enabled</p>
0xA019	1	0	OPD_MASK_EN_01	R/W	U1.0	<p>This register is used to enable or disable the display of the Rectangular Mask #1 for exposure control.</p> <p>0: Disabled 1: Enabled</p>
...		
0xA01F	1	0	OPD_MASK_EN_07	R/W	U1.0	<p>This register is used to enable or disable the display of the Rectangular Mask #7 for exposure control.</p> <p>0: Disabled 1: Enabled</p>
0xA020	2	11:0	OPD_MASK_STAH_00	R/W	U12.0	<p>This register is used to set the horizontal start position.</p> <p>For the light metering window masking of the Rectangular Region #00 to be used for exposure control</p>
0xA022	2	11:0	OPD_MASK_STAV_00	R/W	U12.0	<p>This register is used to set the vertical start position.</p> <p>For the light metering window masking of the Rectangular Region #00 to be used for exposure control</p>
0xA024	2	11:0	OPD_MASK_ENDH_00	R/W	U12.0	<p>This register is used to set the horizontal end position.</p> <p>For the light metering window masking of the Rectangular Region #00 to be used for exposure control</p>
0xA026	2	11:0	OPD_MASK_ENDV_00	R/W	U12.0	<p>This register is used to set the vertical end position.</p> <p>For the light metering window masking of the Rectangular Region #00 to be used for exposure control</p>

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xA028	2	11:0	OPD_MASK_STAH_01	R/W	U12.0	This register is used to set the horizontal start position. For the light metering window masking of the Rectangular Region #01 to be used for exposure control
0xA02A	2	11:0	OPD_MASK_STAV_01	R/W	U12.0	This register is used to set the vertical start position. For the light metering window masking of the Rectangular Region #01 to be used for exposure control
0xA02C	2	11:0	OPD_MASK_ENDH_01	R/W	U12.0	This register is used to set the horizontal end position. For the light metering window masking of the Rectangular Region #01 to be used for exposure control
0xA02E	2	11:0	OPD_MASK_ENDV_01	R/W	U12.0	This register is used to set the vertical end position. For the light metering window masking of the Rectangular Region #01 to be used for exposure control
...		
0xA058	2	11:0	OPD_MASK_STAH_07	R/W	U12.0	This register is used to set the horizontal start position. For the light metering window masking of the Rectangular Region #07 to be used for exposure control
0xA05A	2	11:0	OPD_MASK_STAV_07	R/W	U12.0	This register is used to set the vertical start position. For the light metering window masking of the Rectangular Region #07 to be used for exposure control
0xA05C	2	11:0	OPD_MASK_ENDH_07	R/W	U12.0	This register is used to set the horizontal end position. For the light metering window masking of the Rectangular Region #07 to be used for exposure control
0xA05E	2	11:0	OPD_MASK_ENDV_07	R/W	U12.0	This register is used to set the vertical end position. For the light metering window masking of the Rectangular Region #07 to be used for exposure control
0xAE28	1	0	OPD_MASK_REVERSE_EN	R/W	U1.0	Setting the tracking of the light metering window in horizontal and vertical directions For the light metering window masking of a rectangular region to be used for exposure control 0: Disabled 1: Enabled
0xAE2A	2	11:0	OPD_MASK_EL_HCEN	R/W	U12.0	Setting of the horizontal position of the elliptical region to be masked. <ul style="list-style-type: none">• The left edge of the Active Area is defined as 0.• Set a value that is a multiple of 2.
0xAE2C	2	11:0	OPD_MASK_EL_VCEN	R/W	U12.0	Setting of the vertical center position of the elliptical region to be masked <ul style="list-style-type: none">• The left edge of the Active Area is defined as 0.• Set a value that is a multiple of 2.
0xAE2E	2	11:0	OPD_MASK_EL_RADH	R/W	U12.0	Setting of the horizontal size of the elliptical region to be masked. <ul style="list-style-type: none">• The center of the elliptical region is defined as 0.• Set a value that is a multiple of 2.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xAE30	2	11:0	OPD_MASK_EL_RADV	R/W	U12.0	Setting of the vertical size of the elliptical region to be masked. • The center of the elliptical region is defined as 0. • Set a value that is a multiple of 2.
0xAE32	1	0	OPD_MASK_EL_REVERSE_EN	R/W	U1.0	Setting the tracking of the elliptical region to be masked in horizontal and vertical directions 0: Disabled 1: Enabled

[AE_HDR]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xAE39	1	1:0	AEWEIGHTMODE_HDR	R/W	U2.0	This register is used to set the light metering mode in HDR mode 0: Mesh light metering 1: Histogram light metering 2: Blend-switching light metering
0xAE46	2	9:0	AGC_GAIN_MIN_S	R/W	U10.0	This register is used to set the minimum gain for SP2_HCG. User-set value x 0.1 [dB]
0xAE84	3	16:0	ISP_GAIN_RAW0	R/W	U9.8	This register is used to set digital gain for SP1_HCG in a magnification factor when the sensor does not perform HDR imaging.
0xAE88	3	16:0	ISP_GAIN_RAW1	R/W	U9.8	This register is used to set digital gain for SP1_LCG in a magnification factor when the sensor does not perform HDR imaging.
0xAE8C	3	16:0	ISP_GAIN_RAW2	R/W	U9.8	This register is used to set digital gain for SP2H in a magnification factor when the sensor does not perform HDR imaging.
0xAE90	3	16:0	ISP_GAIN_RAW3	R/W	U9.8	This register is used to set digital gain for SP2L in a magnification factor when the sensor does not perform HDR imaging.
0xAE94	1	7:0	AGC_AGAIN_SP2L	R/W	U8.0	This register is used to set the minimum gain for SP2_LCG. User-set value x 0.1 [dB]

[CMN]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A74	3	17:0	VMAX	R/W	U18.0	This register indicates the number of lines in vertical sync. • Set a value that is a multiple of 2.

[FW_MODE_SENS]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xD828	2	15:0	FW_MODE_INTG_TIME_FINE_SP1	R/W	S15.0	This register is used to compensate for an exposure time error due to A/D conversion. • The number of offset clocks for SP1.
0xD82A	2	15:0	FW_MODE_INTG_TIME_FINE_SP2	R/W	S15.0	This register is used to compensate for an exposure time error due to A/D conversion. The number of offset clocks for SP2.

[FW_MODE_POST]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xD834	2	15:0	FW_MODE_HMAX	R/W	U16.0	This register indicates the number of driver clocks in horizontal sync.

[CTRL1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1C4C	1	1:0	IR_OP_OIF_AE_MSK_SEL	R/W	U2.0	This register is used to select the light metering masking to be used for AE. 0: No light metering masking is used. 1: Only elliptical masking is used. 2: Only rectangular masking is used. 3: Both elliptical and rectangular masking are used.

5.2.5.2. Output Registers

Table 5-26 Output Registers for the Exposure Control Function

[AE_COM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x6170	2	9:0	SENS_AGAIN0	R	U10.0	SP1_HCG's analog gain in dB
0x6175	1	7:0	AELEVEL	R	U8.0	This register indicates the AE control value including an amount of increase or decrease in gain level due to EV compensation and/or EVREF illuminance interlocking. The register's value x 0.7525 [dB]
0x6177	1	7:0	ILMLEVEL	R	U8.0	This register indicates the subject's illuminance. The register's value x 0.7525 [dB]
0x617C	2	15:0	ERRSCL	R	S15.0	This register indicates the amount of deviation from the optimal exposure. This register's value x 6.02 / 1024 [dB]
0x6182	1	7:0	DARK_LEVEL	R	U8.0	This register indicates the amount of deviation when the appropriate exposure cannot be achieved regardless of the settings of the maximum gain and exposure time in low illuminance. The register's value x 0.3 [dB]
0x6188	2	9:0	ISP_GAIN	R	U10.0	Digital Gain The register's value x 0.1 [dB]
0x61A2	2	15:0	SHT_TIME_SP1	R	U16.0	Exposure time of the SP1 line in units of 0.1 ms
0x61EB	1	1:0	FLCLESS_STS	R	U2.0	Output of flicker mitigation 0: Mitigation disabled 1: 50-Hz flicker mitigation 2: 60-Hz flicker mitigation

[AE_HDR_COM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x6480	2	9:0	SENS AGAIN1	R	U10.0	SP1_LCG's analog gain in dB
0x6484	2	9:0	SENS AGAIN2	R	U10.0	SP2H's analog gain in dB
0x6488	2	9:0	SENS AGAIN3	R	U10.0	SP2L's analog gain in dB
0x6494	2	15:0	SHT_TIME_SP2	R	U16.0	Exposure time of the SP2 line in units of 0.1 ms

5.3. White Balance Function

5.3.1. Functional Purpose

Colors appearing white in sunlight may appear as a different color when the color temperature of the light source changes. This is attributed to the change in the balance between blue (B) and red (R) due to the light source. Under this condition, adjusting the gain of R and B signals can reproduce white. This function is known as "White Balance." The White Balance function adjusts the ratio of the R, G and B signals of the sensor's output images.

5.3.2. Functional Overview

The White Balance function analyzes and adjusts the ratio of the R, G and B signals, obtained through the color filters (CF0, CF1, CF2, CF3). This function for adjusting the ratio of the R, G and B signals is known as "White Balance." In addition, the sensor can adjust a function (the Pre-White Balance function) to reduce variations which occur when capturing the image of the same light source by using multiple sensors. For details, refer to "[5.3.3.6 Pre-White Balance Function](#)".

◆ Note

The offset values of the Dark Shading Compensation function can be used to calculate the maximum value of the signal levels after the white balance adjustment. To use these values, set the AWB_WBCLIP_SPS_OFT_ON register to 0x1.

5.3.3. Functional Specifications

5.3.3.1. Selecting a Method of Adjusting White Balance Gain

There are three main methods used to adjust white balance gain by the sensor.

- Auto White Balance (AWB)
This method enables the sensor to calculate the adjustment level of white balance gain from the captured image and make adjustments.
- Manual White Balance (MWB)
This method enables the sensor to adjust White Balance gain using the adjustment level specified by the host using the sensor's dedicated registers.
- Hold
This method enables the sensor to retain the value adjusted using the AWB method.

A white balance gain adjustment method can be selected from the five types described in "[Table 5-27](#)" using the AWBMODE register. When the host does not use the white balance gain, set the WBGAIN_THMODE_EN register to 0x1.

Table 5-27 Selecting a Method of Adjusting White Balance Gain

Name	AWBMODE	Adjustment Method	Description	Remark
AWB	0	Auto Tracking White Balance (ATW)	The sensor estimates the light source and adjusts white balance gain within the specified range.	"5.3.3.2.2 Auto Tracking White Balance (ATW)"
	1	All Pull-in	The sensor estimates the light source and adjusts white balance gain on the entire screen.	"5.3.3.2.3 All Pull-in"
MWB	2	User Preset	The sensor adjusts the white balance gain using the value of the light source specified by the host.	"5.3.3.3.1 User Preset"
	3	Full MWB	The sensor adjusts white balance gain using the setting of dedicated registers configured by the host.	"5.3.3.3.2 Full Manual White Balance (Full MWB)"
Hold	4	Hold	The sensor retains the adjustment level of white balance gain which has been adjusted in the preceding mode. When the Hold method is valid at startup, the sensor makes adjustments using the value stored in the Serial NOR Flash device.	"5.3.3.4 Hold"

5.3.3.2. AWB

In the AWB method, the sensor uses a metering window consisting of 63 cells (9 horizontal x 7 vertical cells) to estimate the light source and adjusts white balance gain. The sensor uses the principle of the additive color mixing method: Colors change into achromatic by mixing the RGB components of light at the ratio of 1:1:1.

In the AWB method, the sensor makes adjustments and configures settings using the R/G-B/G coordinate system. For details, refer to "Figure 5-33." R/G in the figure indicates the ratio of red to green and B/G indicates the ratio of blue to green.

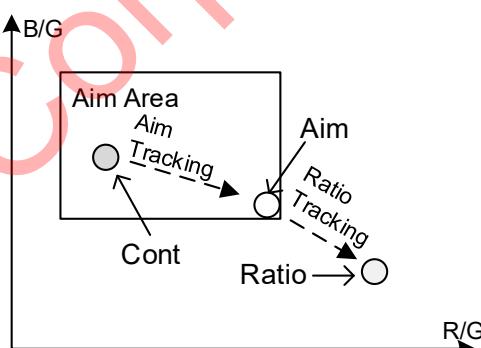


Figure 5-33 Relationship Between the R/G-B/G Coordinate System and the Coordinates Used to Calculate White Balance Gain by the ATW

The sensor uses the following coordinates to calculate the adjustment level of white balance gain.

Ratio

Ratio is coordinates plotted in the R/G-B/G coordinate system using the values calculated from the metering window.

Aim

Aim is coordinates plotted in the R/G-B/G coordinate system using the light source estimated from the **Ratio** point.

Cont

Cont is coordinates plotted in the R/G-B/G coordinate system using the white balance calculated from the **Aim** point.

The coordinates of the **Ratio**, **Aim** and **Cont** points vary depending on the calculated values from the metering window. For example, when the light source is changed, the metering window's calculated values change, causing the **Ratio** point to vary. Since the sensor estimates the light source based on the **Ratio** point, the sensor changes the **Aim** point by tracking the changed **Ratio** point. The **Cont** point gradually changes to track the **Aim** point, thereby mitigating a loss of color continuity in the output image. The sensor's white balance performs calculation from the **Cont** point. For this reason, the sensor can change the convergence speed of white balance by changing the tracking speed for the **Aim** point.

The sensor's AWB can be selected from the two types as follows:

Auto Tracking White Balance (ATW)

The host can restrict the area where **Aim** varies by setting the Operation Area and Aim Area in relation to the area where it is assumed to be originally an achromatic color corresponding to the light source.

All Pull-in

Since the sensor processes the **Aim** point and the **Ratio** point as the same value, the All Pull-in method enables the sensor to pull wide-ranging colors into the white balance target compared to the ATW. Unlike the ATW method, which estimates the light source, the All Pullin method enables the sensor to pull wide-ranging colors into white regardless of the color of the subject.

5.3.3.2.1. Configuring the Settings for Convergence Operations

The convergence operations can be set using three areas: Inner Dead Zone, Middle Dead Zone and Outer Dead Zone. “Figure 5-34” illustrates an overview of the register settings for each zone.

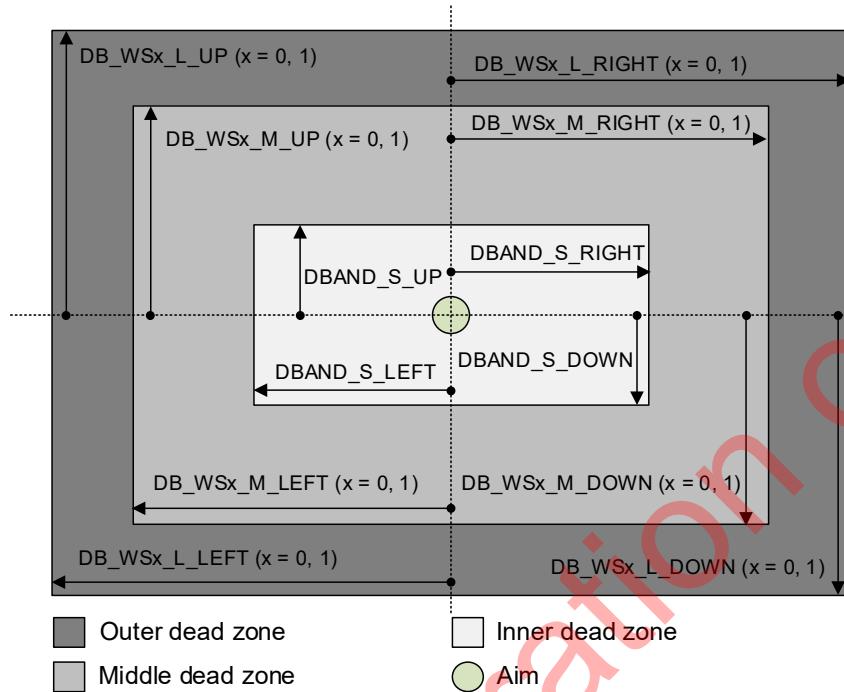


Figure 5-34 Overview of the Register Settings for Dead Zones

When the AWB status of the current frame is in a pull-in operation during sensor power-on (0x1) or a pull-in operation (0x4), the sensor moves the **Cont** point until it enters the inner dead zone. When the AWB status is in a pull-in operation (close to the target value) (0x3) and when the sensor detects any change in the white balance gain after convergence, the sensor moves the **Cont** point to the middle dead zone. The following describes the transition of the AWB status for each dead zone, corresponding to the **Cont** point position of the previous frame.

■ Inner dead zone

“Table 5-28” shows the transition of the AWB status when the **Cont** point of the previous frame is in the inner dead zone. This zone is used in ATW, All Pull-in and User Preset modes.

Table 5-28 The Transition of the AWB Status (Inner Dead Zone)

AWB Status of the Previous Frame	AWB Status of the Current Frame
0x1: Pull-in operation in progress during sensor power-on	0x2: Convergence state (stop state)*
0x2: Convergence state (stop state)	0x2: Convergence state (stop state)
0x3: Pull-in operation in progress (close to the target value)	0x2: Convergence state (stop state)*
0x4: Pull-in operation in progress	0x2: Convergence state (stop state)*

* In the case of ATW_CNT_EQ_AIM = 1, the position of the **Cont** point changes so that the **Cont** point matches the **Aim** point.

■ Middle dead zone

"**Table 5-29**" shows the transition of the AWB status when the **Cont** point of the previous frame is in the middle dead zone.

Table 5-29 The Transition of the AWB Status (Middle Dead Zone)

AWB Status of the Previous Frame	AWB Status of the Current Frame
0x1: Pull-in operation in progress during sensor power-on	0x1: Pull-in operation in progress during sensor power-on
0x2: Convergence state (stop state)	0x2: Convergence state (stop state)
0x3: Pull-in operation in progress (close to the target value)	0x2: Convergence state (stop state)*
0x4: Pull-in operation in progress	0x4: Pull-in operation in progress

* In the case of ATW_CNT_EQ_AIM = 1, the position of the **Cont** point changes so that the **Cont** point matches the **Aim** point.

This zone is used in ATW mode. For details, refer to "**5.3.3.2.2 Auto Tracking White Balance (ATW)**."

■ Outer dead zone

"**Table 5-30**" shows the transition of the AWB status when the **Cont** point of the previous frame is in the outer dead zone. This zone is used in ATW mode. For details, refer to "**5.3.3.2.2 Auto Tracking White Balance (ATW)**."

Table 5-30 The Transition of the AWB Status (Outer Dead Zone)

AWB Status of the Previous Frame	AWB Status of the Current Frame
0x1: Pull-in operation in progress during sensor power-on	0x1: Pull-in operation in progress during sensor power-on
0x2: Convergence state (stop state)	0x3: Pull-in operation in progress (close to the target value)*
0x3: Pull-in operation in progress (close to the target value)	0x3: Pull-in operation in progress (close to the target value)
0x4: Pull-in operation in progress	0x4: Pull-in operation in progress

* The convergence state is held under the following conditions:

- The **Cont** point continues to be outside the middle dead zone.
- Until the number of frames set in the ATW_DELAY register elapses.

5.3.3.2.2. Auto Tracking White Balance (ATW)

The ATW automatically adjusts the white balance gain within the specified range.

■ White Balance Scene (WB Scene)

The ATW switches WB scenes (WS0 for Light Source 1 and WS1 for Light Source 2) corresponding to the light source, using the WS_MODE register. When setting the WS_MODE register to 2, the ATW switches the WB scenes in accordance with the illuminance level.

The switching conditions for the WB scenes corresponding to the illuminance level (ILMLEVEL) are as follows:

- Switch to WS0 when the value of the ILMLEVEL register decreases to the value of the WS0_JUDGPOS register.
- Switch to WS1 when the value of the ILMLEVEL register exceeds the value of the WS1_JUDGPOS register.

◆ Note

Set these registers to satisfy the following condition: Value of the WS0_JUDGPOS register < Value of the WS1_JUDGPOS register

Table 5-31 The Conditions for Switching White Balance (WB) Scenes Corresponding to the Illuminance Level

Switching Conditions for WB Scenes	WB Scenes to Be Selected
ILMLEVEL ≤ WS0_JUDGPOS	WS0
ILMLEVEL ≥ WS1_JUDGPOS	WS1
Any other conditions	No change

Use the WS_INIT register to select one of the WB scenes.

The WB scene is gradually switched corresponding to the value of the WBSCENE_CHG_DIVNUM register.

■ Operation Area and Aim Area

The ATW can adjust the white balance gain corresponding to the light source by the host setting the Operation Area and Aim Area. Set the region which is assumed to be originally achromatic as the Operation Area. Alternatively, set the target positions for pull-in operations as the Aim Area.

The Operation Area and Aim Area vary for each light source. Therefore, define these areas using the 16 registers in “**Table 5-32**,” which represent the 16 points in the R/G-B/G coordinate system, for each WB scene.

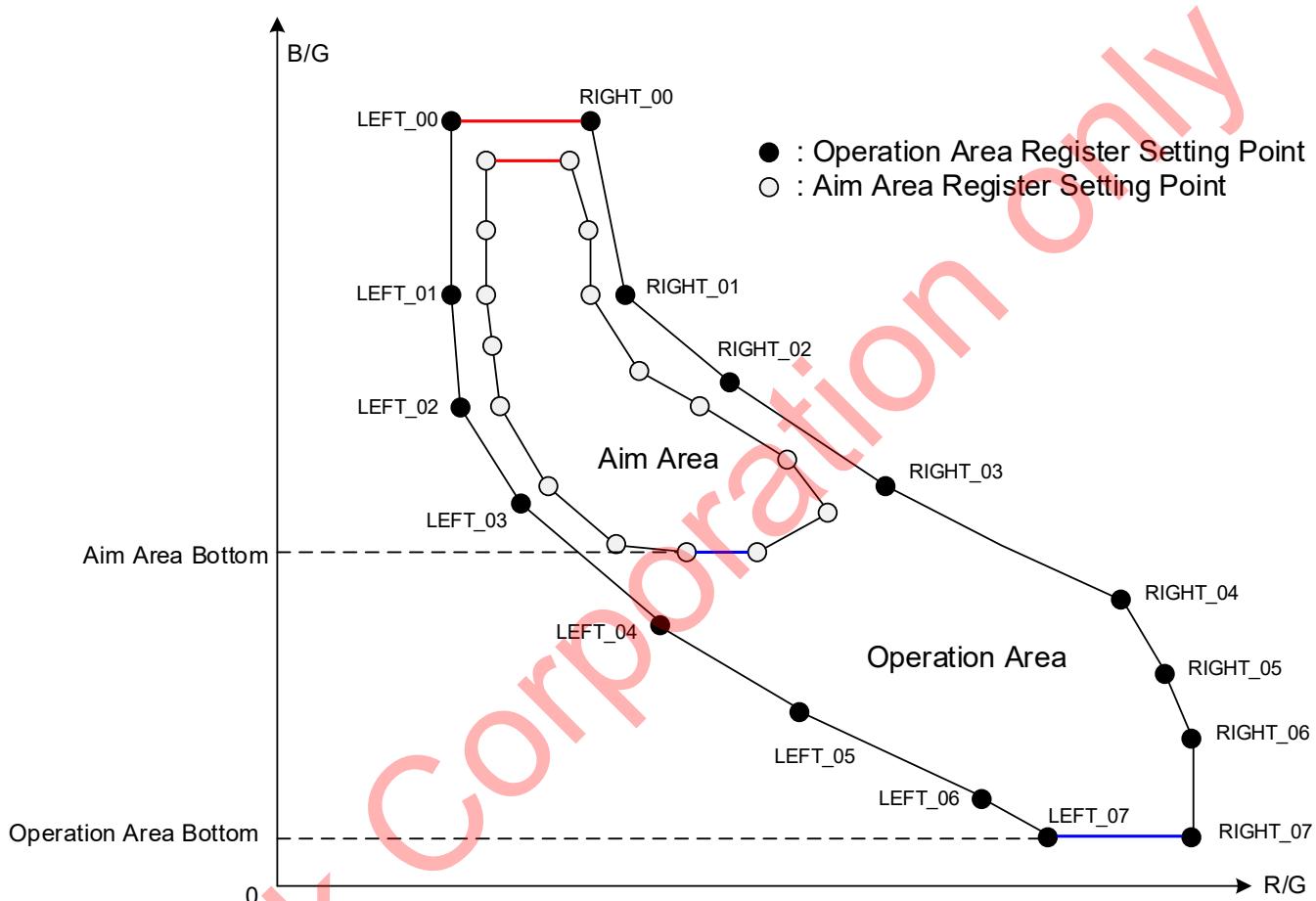


Figure 5-35 Registers for the Operation Area and the Aim Area

◇ **Memo**

The sensor automatically replaces each Y coordinate on the B/G axis of the upper limit (the red line in the figure) and the lower limit (the blue line in the figure) of the right profile of the Operation Area with the corresponding Y coordinate of the left profile.

Table 5-32 Registers Used to Set the Coordinates of the Operation Area and the Aim Area

Settings	Direction	Color	Register Name
Operation Area	Left	R/G	WSx_FRM_LEFT_00_R to WSx_FRM_LEFT_07_R (x = 0,1)
		B/G	WSx_FRM_LEFT_00_B to WSx_FRM_LEFT_07_B (x = 0,1)
	Right	R/G	WSx_FRM_RIGHT_00_R to WSx_FRM_RIGHT_07_R (x = 0,1)
		B/G	WSx_FRM_RIGHT_00_B to WSx_FRM_RIGHT_07_B (x = 0,1)
	Bottom	-	WSx_FRM_BTM_NUM (x = 0,1)

Settings	Direction	Color	Register Name
Aim Area	Left	R/G	WSx_AIM_LEFT_00_R to WSx_AIM_LEFT_07_R (x = 0,1)
		B/G	WSx_AIM_LEFT_00_B to WSx_AIM_LEFT_07_B (x = 0,1)
	Right	R/G	WSx_AIM_RIGHT_00_R to WSx_AIM_RIGHT_07_R (x = 0,1)
		B/G	WSx_AIM_RIGHT_00_B to WSx_AIM_RIGHT_07_B (x = 0,1)
	Bottom	-	WSx_AIM_BTM_NUM (x = 0,1)

Regarding the sensor, setting the ATW_FRM_CHK_F register to 1 enables the host to check whether the coordinates of the user-set Operation Area and Aim Area have been correctly set.

◆ Note

When the following conditions are not satisfied with the value of the ATW_FRM_CHK_F register set to 1, the sensor has been incorrectly configured using the AWBSTS register:

- Switching the coordinates of the left and right profiles is prohibited.
- Set the coordinates in ascending order.

(If either of the aforementioned conditions are not satisfied, the AWBSTS register is set to 7.)

- Position the Aim Area within the Operation Area.

(If the aforementioned condition is not satisfied, the AWBSTS register is set to 9.)

■ Adjusting the White Balance Gain

The sensor adjusts the white balance gain by estimating the **Aim** point from the **Ratio** point in order for the **Cont** point to track the **Aim** point. The **Aim** point is estimated on the border of the Aim Area as shown in “Figure 5-36” corresponding to the position of the **Ratio** point. When the **Ratio** point is within the Aim Area, the coordinates of the **Ratio** point will be the coordinates of the **Aim** point as is.

In the R/G and B/G coordinate system areas that contain a lot of green component, if only the red or blue component changes, the output image may appear unnatural in color. In this case, the sensor can set the area (indicated by the broken lines in “Figure 5-36”) where the sensor changes both the red and blue components at the same time to reduce any unnatural color.

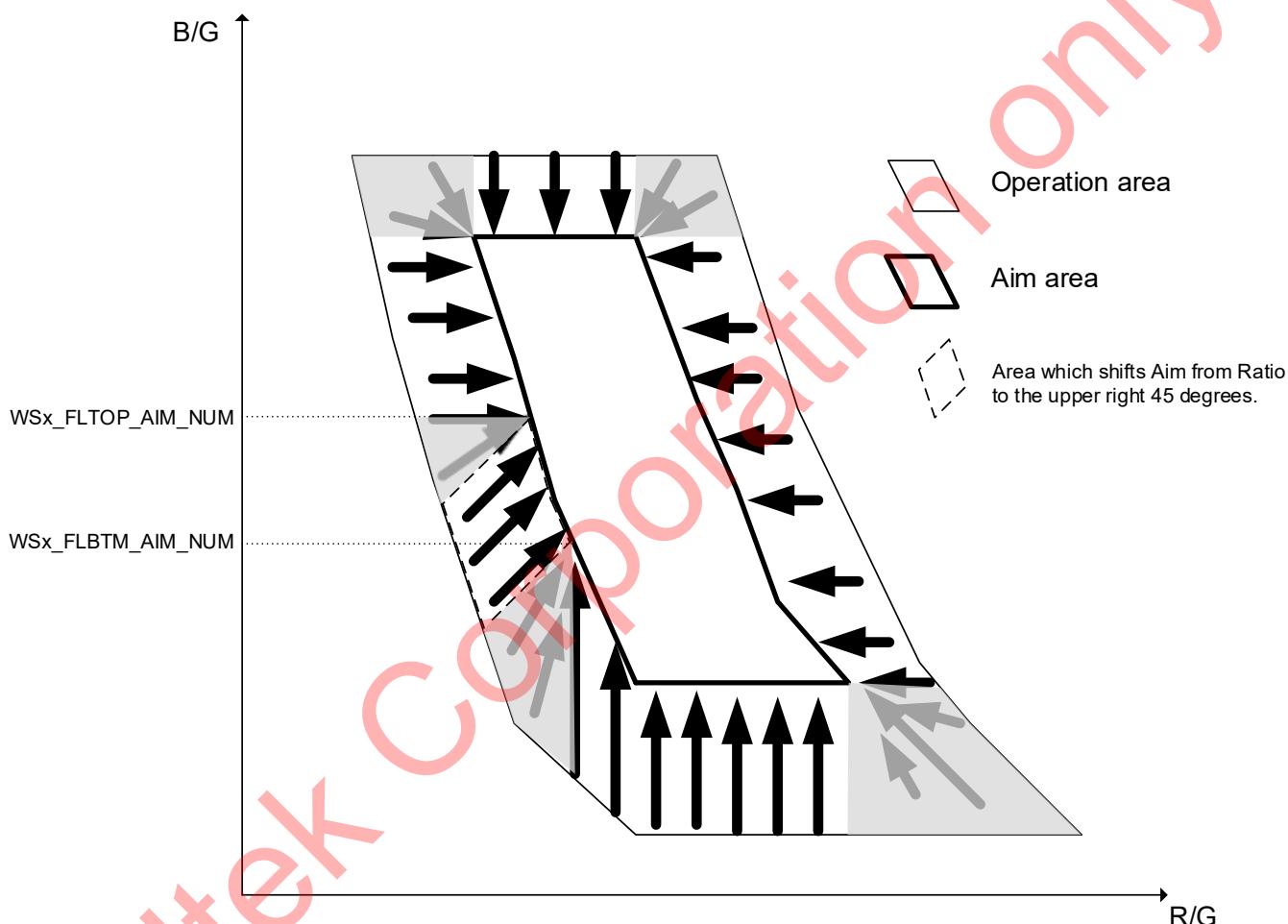


Figure 5-36 Directions of the Aim Point for the Positions of the Ratio Point

Regarding the area, where the user changes both red and blue components at the same time when adjusting the white balance gain, the user can configure the settings for each white balance scene by using the Operation and Aim Areas.

* “Figure 5-36” illustrates the settings of the Aim Area.

To set these areas, use the WS_x_FLTOP_FRM_NUM and WS_x_FLBTM_AIM_NUM registers ($x = 0, 1$). If these conditions are not satisfied, an error regarding the area settings will occur, causing the sensor to set the AWBTS register to 8.

- The magnitude conditions of the value of the registers must satisfy the following:
 $0 < \text{WS}_x\text{_FLTOP_FRM_NUM} \leq \text{WS}_x\text{_FLBTM_FRM_NUM} \leq \text{WS}_x\text{_FRM_BTM_NUM}$ ($x = 0, 1$)
 $0 < \text{WS}_x\text{_FLTOP_AIM_NUM} \leq \text{WS}_x\text{_FLBTM_AIM_NUM} \leq \text{WS}_x\text{_AIM_BTM_NUM}$ ($x = 0, 1$)
- Each straight line, which is formed by connecting the coordinate points from the point indicated by the WS_x_FLTOP_y_NUM ($x = 0, 1$) ($y = \text{FRM}, \text{AIM}$) register to the point indicated by the WS_x_FLBTM_y_NUM ($x = 0, 1$) ($y = \text{FRM}, \text{AIM}$) register, constitutes an angle of 45 degrees or greater with respect to the R/G coordinate axis.

The coordinate points indicated by the WSw_x_LEFT_y_z ($w = 0, 1$) ($x = \text{FRM}, \text{AIM}$) ($y = 00$ to 07) ($z = \text{R}, \text{B}$) registers are subject to the aforementioned conditions. "Figure 5-37" illustrates an example of an error regarding the region settings.

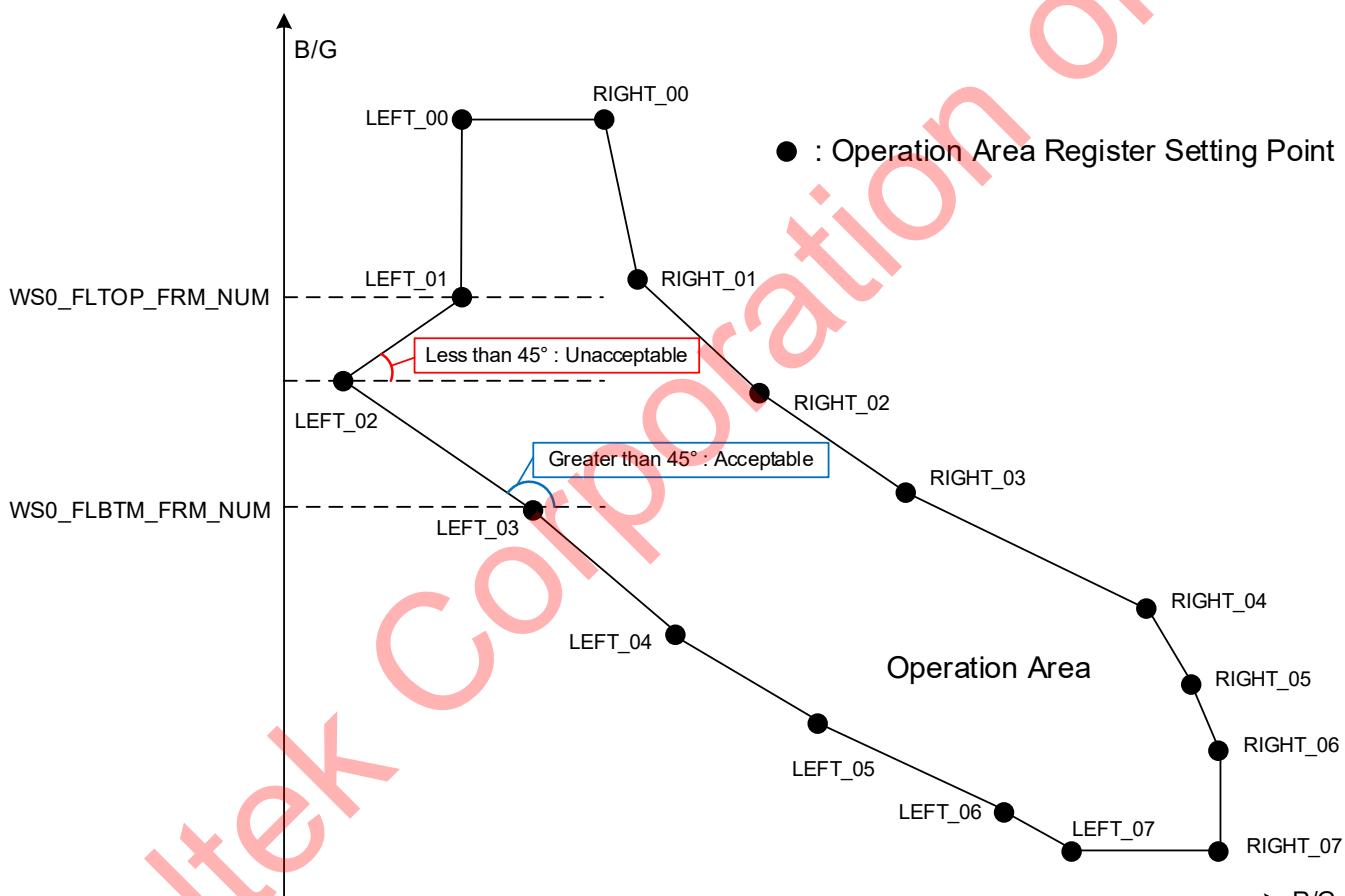


Figure 5-37 Example of a Region Settings Error

"Figure 5-37" illustrates the Operation Area for White Balance Scene 0 (WS0) when the WS0_FLTOP_FRM_NUM and WS0_FLBTM_FRM_NUM registers are set to 1 and 3, respectively. With these settings, the line connecting LEFT01 and LEFT02 will constitute an angle less than 45 degrees with respect to the R/G coordinate axis. Consequently, a region settings error will occur.

■ Determination of an Operation Area Error

The ATW function determines whether each coordinate point in the R/G-B/G coordinate system, calculated from the 63-cell metering window, is located inside or outside the Operation Area. If the number of coordinates (i.e., the value of the FRMIN_NUM register) located within the Operation Area is below the thresholds set in the FRMIN_JUDG_NUM_WSO and FRMIN_JUDG_NUM_WS1 registers, the sensor identifies this as an Operation Area error. The user can set the operation when an Operation Area error occurs using the FRMOUT_RATIO_CALC_EN register.

- When setting this register to 0, the sensor will stop adjusting the white balance gain and set the AWBSTS register to 5.
- When setting this register to 1, the sensor will adjust the white balance gain for the coordinates calculated using both the metering window and the Operation Area.

◇ Memo

- After waiting for the number of frames set in the AWB_ER_DELAY register, the sensor begins a pull-in operation.
- During a high-speed pull-in operation, if the sensor determines that a pull-in error continues for the number of frames set in the INITMOVE_GIVEUP_CNT register, the sensor completes the pull-in operation.

■ Configuring the Settings Immediately After Transitioning to Streaming State

Immediately after the transition to Streaming State, AE operations are unstable, causing light metering results to be unstable. In order to avoid unstable frames immediately after any transition to Streaming, the host can prevent ATW processing for the number of frames set by using the ATW_INITMASK register.

- Set the ATW_INITMASK register to a value greater than the number of AE convergence frames.
- Set the INIT_CONT_WSy_y ($x = 0, 1$) ($y = R, B$) registers to the coordinates of the **Aim** point (i.e., estimated light source coordinate position) and the **Cont** point (i.e., current coordinate point) at the start of ATW operation for each color filter.

Set each value of the INIT_CONT_WSy_y ($x = 0, 1$) ($y = R, B$) registers so that these values are within the Aim Area.

■ Convergence Speed

The host can change the convergence speed by setting the parameters for the pull-in adjustment. The convergence speed can be calculated by dividing the distance between the **Aim** point and the **Cont** point by the value of a gain step register. The upper limit of the convergence speed can be set using the value of a shift limit register. If a calculation result is greater than the value of a shift limit register, the convergence speed is determined by the value specified by the shift limit register. “Table 5-33” lists the registers used to configure the settings.

Table 5-33 Registers Used to Set the Parameters for the Convergence Speed Adjustment

Gain Step	Shift Limit	Description
ATW_GAINS_WSy	ATW_SFTLMT_WSy	This register is used to set the gain step and shift limit near the Aim point and outside the pull-in area.
ATW_GAINS_WSy_NR	ATW_SFTLMT_WSy_NR	This register is used to set the gain step and shift limit near the Aim point and within the pull-in area.
INIT_GAINS	INIT_SFTLMT	This register is used to set the gain step and shift limit at sensor start-up.

* $x = 0, 1$

The pull-in area near **Aim** can be set using the AIM_NR_TH_x (x =UP, DOWN, RIGHT, LEFT) registers.

5.3.3.2.3. All Pull-in

The All Pull-in operation adjusts the white balance gain for output images corresponding to the estimated light source. While using the All Pull-in operation, an **Aim** point is regarded as the same as a **Ratio** point. Consequently, colors in wider areas can be pulled into white, compared with ATW operations.

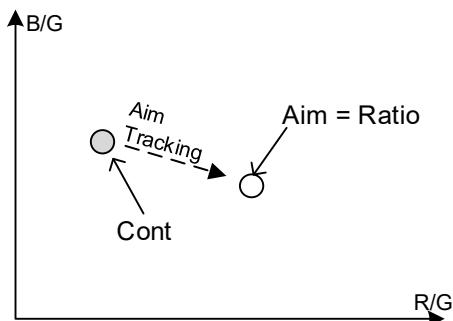


Figure 5-38 Example of All Pull-in Operation

■ Convergence Speed

The All Pull-in operation pulls in a **Cont** point in for each frame set by using the ALLWB_USER_DELAY register.

- The amount of one pull-in operation can be set using the ALLWB_USER_GAINS and ALLWB_USER_SFTLMT registers.
- The sensor sets the amount of one pull-in operation so that the value, which is calculated by dividing the distance from a **Cont** point to an **Aim** point by the ALLWB_USER_GAINS register's value, does not exceed the limit value set in the ALLWB_USER_SFTLMT register.
- The register used to set the convergence speed for the All Pull-in operation is also used in User Preset mode.

5.3.3.3. Manual White Balance (MWB)

5.3.3.3.1. User Preset

In User Preset mode, specify the position of an **Aim** point in the R/G-B/G coordinate system using the registers in "Table 5-34." Up to three **Aim** points can be set and these can be switched by using the AWBUSER_NO register.

Table 5-34 Registers Used to Set Aim Points

AWBUSER_NO	R/G	B/G
0	USER0_R	USER0_B
1	USER1_R	USER1_B
2	USER2_R	USER2_B

■ Convergence Speed

For the method used to set convergence speed in User Preset mode, refer to "5.3.3.2.3 All Pull-in."

5.3.3.3.2. Full Manual White Balance (Full MWB)

Full MWB is a method in which the host directly controls exposure time and gain instead of the sensor's AWB function. Adjustment values of white balance gain used for the Full MWB method are set in the FULLMWBGAIN_x (x = R, GR, GB, B) registers.

◆ Note

When the host does not use the sensor's white balance function, set the FULLMWBGAIN_x (x = R, GR, GB, B) registers to 0x100 (1.0x).

5.3.3.4. Hold

When setting the AWBMODE register to 4, the sensor changes the mode to Hold. In Hold mode, the sensor will hold the **Aim** and **Cont** points before changing the AWBMODE register.

Therefore, even if the subject is changed, the white balance gain does not change. However, the white balance gain for green will be fixed at 1.0x.

◇ Memo

If the user selects the Hold mode during sensor startup, the sensor will hold the initial values set in the Serial NOR Flash device.

5.3.3.5. Light Metering

Light metering for the White Balance function is performed using 63 cells consisting of 9 horizontal x 7 vertical cells. The user can adjust the size and position of these cells.

5.3.3.5.1. Adjusting the AWB Light Metering Window

The AWB light metering window consists of 63 cells (9 horizontal and 7 vertical cells). The host can adjust the size and position of the AWB light metering window.

To adjust the size, use the AWB_WND_MODE register. “**Table 5-35**” describes how to adjust the size in detail.

Table 5-35 Methods Used to Adjust the Size of the AWB Light Metering Window

AWB_WND_MODE	Description
0	<p>Specify the width and height for each of the 63 cells, which consist of 9 horizontal x 7 vertical cells, in multiples of 2.</p> <ul style="list-style-type: none"> • AWB_WND_SIZE_H register: Set the width of one cell. (Unit: pixel) • AWB_WND_SIZE_V register: Set the height of one cell. (Unit: pixel)
1	<p>Specify the width and height for each of the 63 cells, which consist of 9 horizontal x 7 vertical cells, using ratios with respect to the Active Area.</p> <ul style="list-style-type: none"> • AWB_WND_SIZE_H register: Specify the width of the metering window using a ratio with respect to the width of the Active Area.^{*1} The width of the cell: The width of the Active Area x (AWB_WND_SIZE_H / 256) / 9^{*3} The width of the light metering window: The width of one cell x 9 • AWB_WND_SIZE_V register: Specify the height of the metering window using a ratio with respect to the height of the Active Area.^{*2} The height of one cell: The height of the Active Area x (AWB_WND_SIZE_V / 256) / 7^{*3} The height of the light metering window: The height of one cell x 7

* ¹The value of the AWB_WND_SIZE_H register is within the range of 16 (0x10) to 256 (0x100). Any other settings are prohibited.

* ²The value of the AWB_WND_SIZE_V register is within the range of 4 (0x10) to 256 (0x100). Any other settings are prohibited.

* ³Round the calculated value down to the nearest value that is a multiple of 2. For example, if the calculated value is 61.8, round it down to 60. Likewise, round the value 62.2 down to 62.

To adjust the position of the light metering window, set the AWB_WND_OFFSET_H and AWB_WND_OFFSET_V registers to the amount of offset. “**Figure 5-39**” illustrates the relationship between the offset direction and the value of each of the registers.

- Horizontal direction (AWB_WND_OFFSET_H register): Positive to the right and negative to the left from the center of the Active Area.
- Vertical direction (AWB_WND_OFFSET_V register): Positive downward and negative upward from the center of the Active Area.

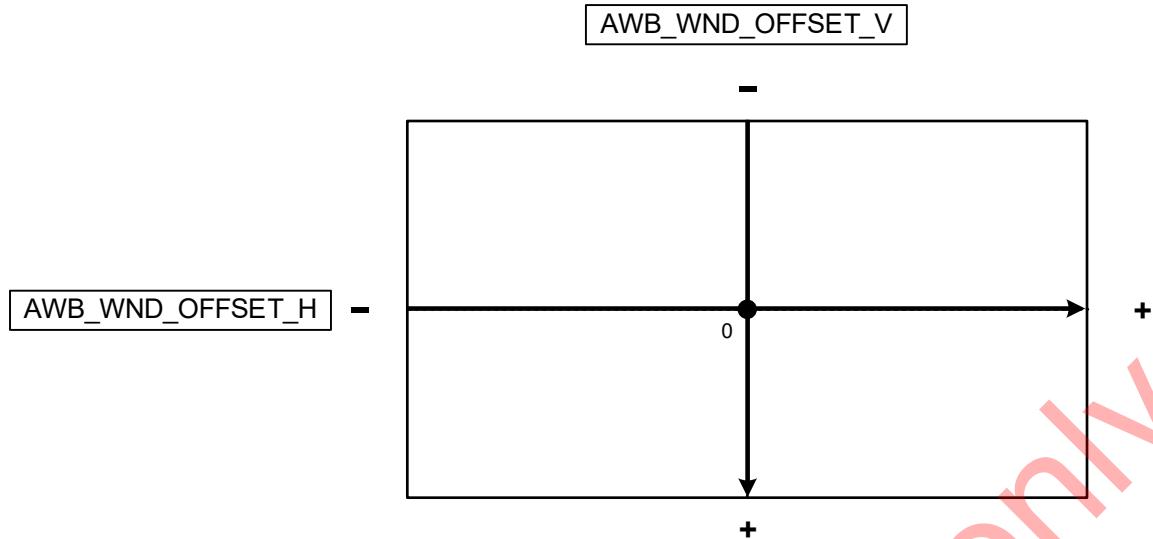


Figure 5-39 The Relationship Between the Offset Direction and the Value of Each of the Registers

◆ Note

When using the Horizontal/Vertical Flip function with the AWB_OPD_REVERSE_EN register set to 1, both of the aforementioned directions are reversed. For details regarding the AWB_OPD_REVERSE_EN register, refer to “[5.3.3.5.5 Interlocking with the Horizontal/Vertical Flip Function.](#)”

When adjusting the position, set the AWB light metering window so that it does not exceed the Active Area after adjustment.

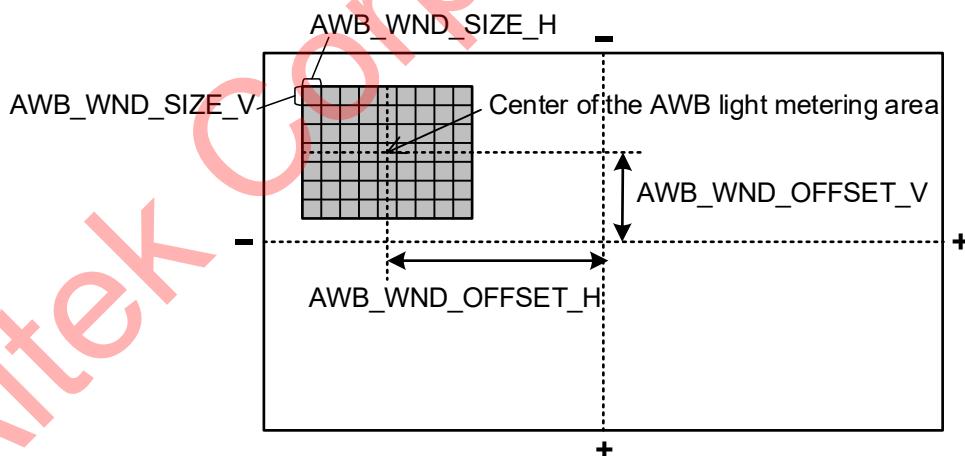


Figure 5-40 Adjustment of the AWB Light Metering Window’s Position (AWB_WND_MODE = 0)

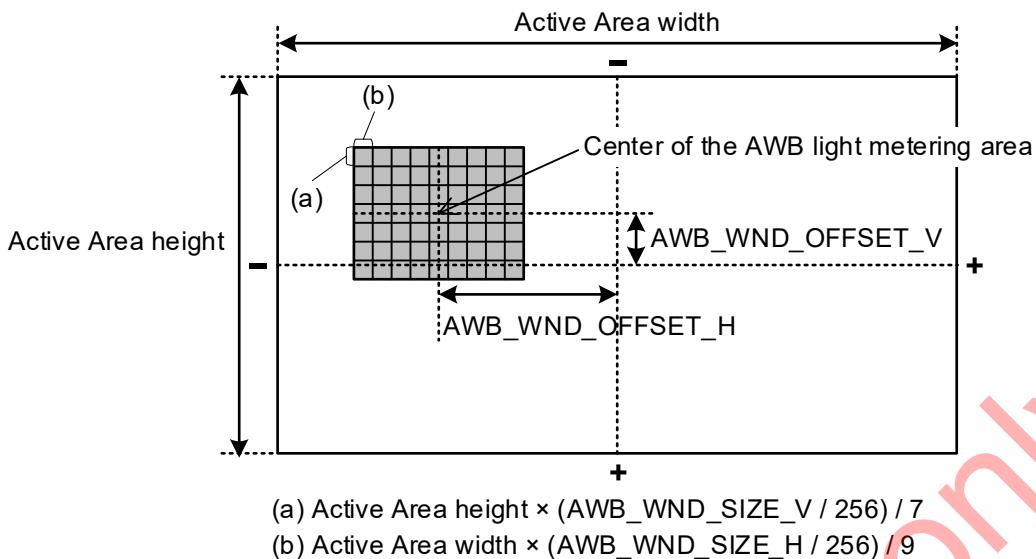


Figure 5-41 Adjustment of the AWB Light Metering Window's Position (AWB_WND_MODE = 1)

5.3.3.5.2. Light Metering Region Mask Function

The Light Metering Region Mask function excludes specific region(s) of the image from light metering. The user can set a maximum of eight rectangular regions or one elliptical region. The following describes how to mask rectangular or elliptical regions.

■ Light Metering Region Mask Function

As shown in “**Table 5-36**,” this function can be set using the IR_OP_OIF_AWB_MSK_SEL register.

Table 5-36 How to Set the Light Metering Region Mask Function

IR_OP_OIF_AWB_MSK_SEL	Light Metering Region Mask Function to Be Used
0	The Light Metering Region Mask function is disabled.
1	Only the elliptical region is masked.
2	Only rectangular region(s) are masked.
3	Both elliptical and rectangular regions are masked.

■ Rectangular Region

To use rectangular region(s), enable masking and configure the settings of these regions as shown in “**Table 5-37**.”

Table 5-37 Registers for Light Metering Window Mask Function (Rectangular Region)

Register Name	Description
AWB_OPD_MASK_EN_x (x = 00 to 07)	This register is used to enable or disable rectangular masking.
AWB_OPD_MASK_STAH_x (x = 00 to 07)	This register is used to set the horizontal starting point of Region x. • The left edge of the Active Area is defined as 0.
AWB_OPD_MASK_ENDH_x (x = 00 to 07)	This register is used to set the horizontal end point of Region x. • The left edge of the Active Area is defined as 0.
AWB_OPD_MASK_STAV_x (x = 00 to 07)	This register is used to set the vertical starting point of Region x.

Register Name	Description
AWB_OPD_MASK_ENDV_x (x = 00 to 07)	<ul style="list-style-type: none"> The upper edge of the Active Area is defined as 0. <p>This register is used to set the vertical end point of Region x.</p> <ul style="list-style-type: none"> The upper edge of the Active Area is defined as 0.

When setting rectangular region(s), consider the following conditions:

- The registers' values are in multiples of two with the upper-left corner of the Active Area defined as the origin (0,0).
- Start position < End position

"Figure 5-42" illustrates an example of setting rectangular regions.

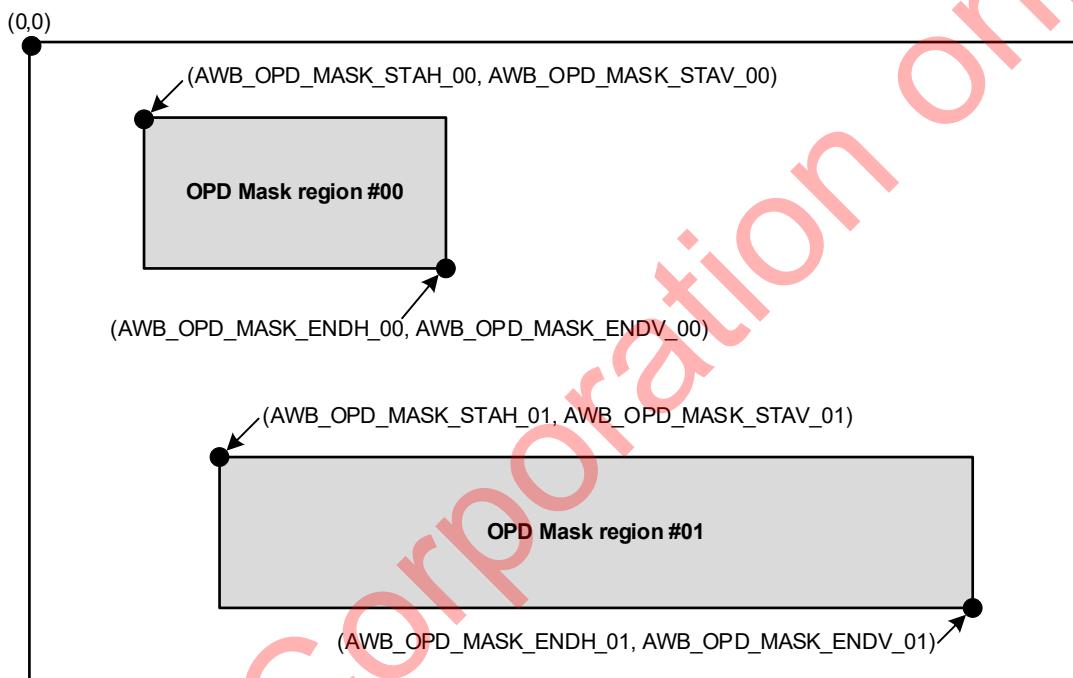


Figure 5-42 Rectangular Regions to Be Masked

■ Elliptical Region

The user can mask an image for white balance using the elliptical region. Please note that the settings of the elliptical region are the same as those of the AE light metering region. For details regarding how to configure the settings, refer to "[5.2.3.4.6 Light Metering Region Mask Function](#)".

5.3.3.5.3.

Setting Thresholds for the Pixels to Be Light Metered

The sensor adjusts the white balance gain frame by frame by using the integrated value of the metering results for each light metering cell. In this process, the host can set the conditions used to determine whether or not the pixels within each light metering cell are integrated. "[Table 5-38](#)" lists the registers used to set these conditions.

These pixels are integrated only when both the following conditions are satisfied:

- The Y signal of each cell is between the upper and lower thresholds which determine the luminance level.
- All RGB signals are below the saturation threshold.

Table 5-38 Registers Used to Set Thresholds

Register Name	Description
AWB_Y_PEAK	This register is used to set the upper threshold for determining the luminance level.
AWB_Y_DARK	This register is used to set the lower threshold for determining the luminance level.
AWB_R_PEAK	This register is used to set the upper threshold for determining the saturation of the R signal. This register is enabled only when the AWB_OPDIN_RGB_LMT_MODE register is 0x1.
AWB_G_PEAK	This register is used to set the upper threshold for determining the saturation of the G signal. This register is enabled only when the AWB_OPDIN_RGB_LMT_MODE register is 0x1.
AWB_B_PEAK	This register is used to set the upper threshold for determining the saturation of the B signal. This register is enabled only when the AWB_OPDIN_RGB_LMT_MODE register is 0x1.

5.3.3.5.4. Light Metering Error

If the sensor determines that a light metering result is as a "light metering error" (i.e., low reliability of the light measurement result), the sensor does not make the automatic white balance adjustment (i.e., the ATW and All Pull-in operations). If any of the conditions shown in "Table 5-39" are met, a "light metering error" will occur.

Table 5-39 Conditions for Light Metering Error Determination

Conditions
ILMLEVEL < INIT_ILMLEVEL_ALL
DARK_LEVEL = 0 AND ERRLEVEL > INIT_AEERR_ALL
DARK_LEVEL ≠ 0 AND DARK_LEVEL > INIT_AEDARK_ALL
R integrated value < AWB_OPDERR_TH_R
G integrated value < AWB_OPDERR_TH_G
B integrated value < AWB_OPDERR_TH_B

* INIT_ILMLEVEL, INIT_AEERR and INIT_AEDARK for the ATW operation

* INIT_ILMLEVEL_ALL, INIT_AEERR_ALL and INIT_AEDARK_ALL are for the All Pull-in operation

◇ **Memo**

In the case of an ATW operation only, the sensor can continue to retain an error state for the number of frames set in the AWB_ER_DELAY register.

5.3.3.5.5. Interlocking with the Horizontal/Vertical Flip Function

This section describes a function that adjusts the position of the AWB metering window, by interlocking this function the position with the Horizontal/Vertical Flip function. “**Table 5-40**” shows the variables for positional adjustments and the registers used to configure the interlocking settings.

Table 5-40 Variables and the Registers to Be Interlocked with the Horizontal/Vertical Flip Function

Variables for Window's Position Adjustment	Register Name
Position of the light metering window	AWB_OPD_REVERSE_EN
Position of the rectangular region(s) to be masked from light metering	AWB_OPD_MASK_REVERSE_EN

◆ **Note**

Set register values while the sensor is in Start-up State.

To interlock the light metering window with the Horizontal/Vertical Flip function, set the relevant register to 1. When setting the relevant register to 0, the light metering window will not be interlocked with the Horizontal/Vertical Flip function.

However, the cell ID numbers of each metering window for the AWB are not reversed. When individually configuring the settings for each metering window, take into consideration the reverse settings.

“**Figure 5-43**” illustrates interlocking between the Horizontal/Vertical Flip function and the light metering window when the AWB_OPD_REVERSE_EN register is set to 1.

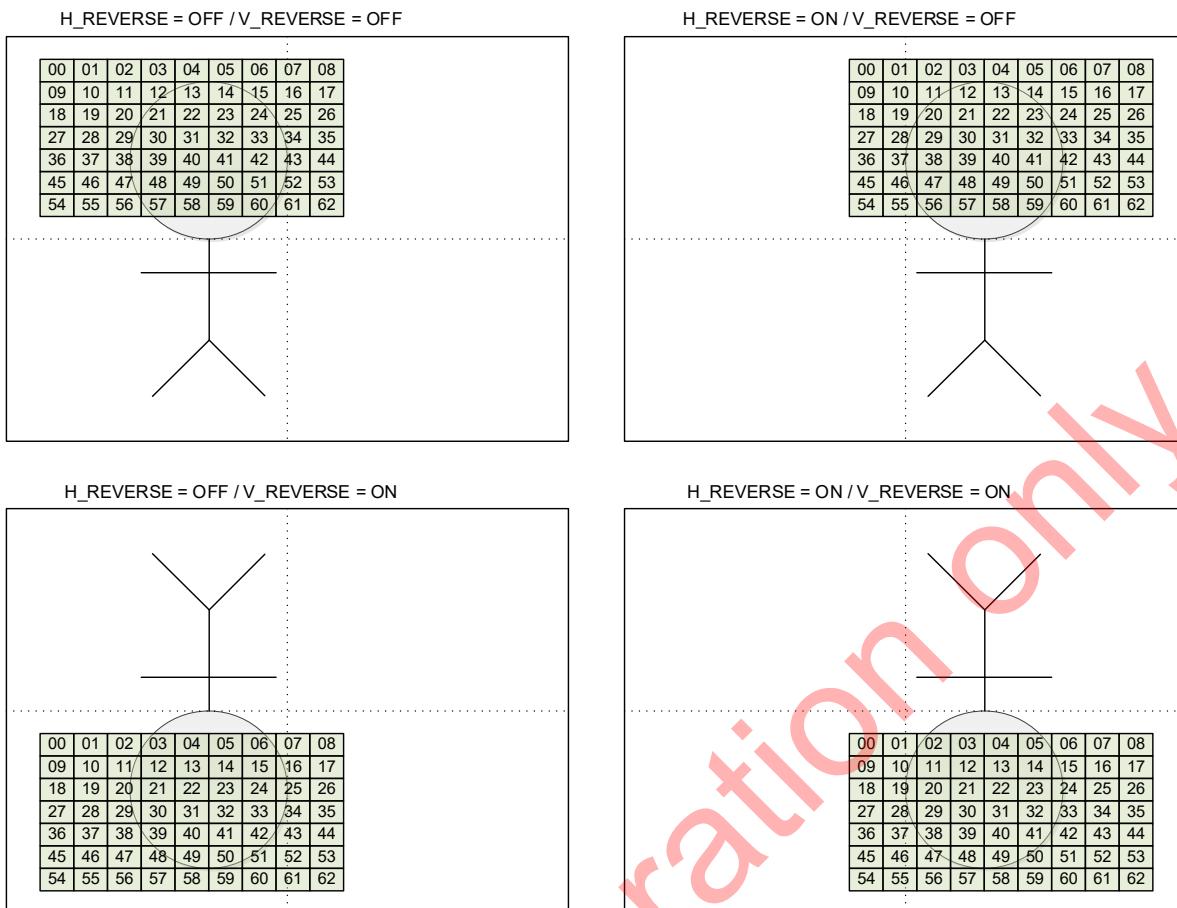


Figure 5-43 Example of Interlocking between the Horizontal/Vertical Flip Function and AWB Light Metering Window

5.3.3.5.6. Applying the IIR Filter

The IIR filter can be applied to the AWB light metering results by setting the WB_IIR_EN register to 1. When not applying the IIR filter, set the WB_IIR_EN register to 0. To enable or disable the application of the IIR filter, set the WB_IIR_EN register to 1 or 0 respectively. The IIR filter can be applied in ATW or All Pull-in modes.

■ Configuring the coefficients of the IIR filter

The coefficient of the IIR filter can be changed by interlocking the coefficient with the illuminance. Set the WB_IIR_TH_LOW and WB_IIR_COEF_LOW registers to the threshold and coefficient in lower illuminance, respectively. Set the WB_IIR_TH_HIGH and WB_IIR_COEF_HIGH registers to the threshold and coefficient at higher illuminance, respectively. The change in the coefficient in relation to the illuminance is illustrated in **Figure 5-44.**

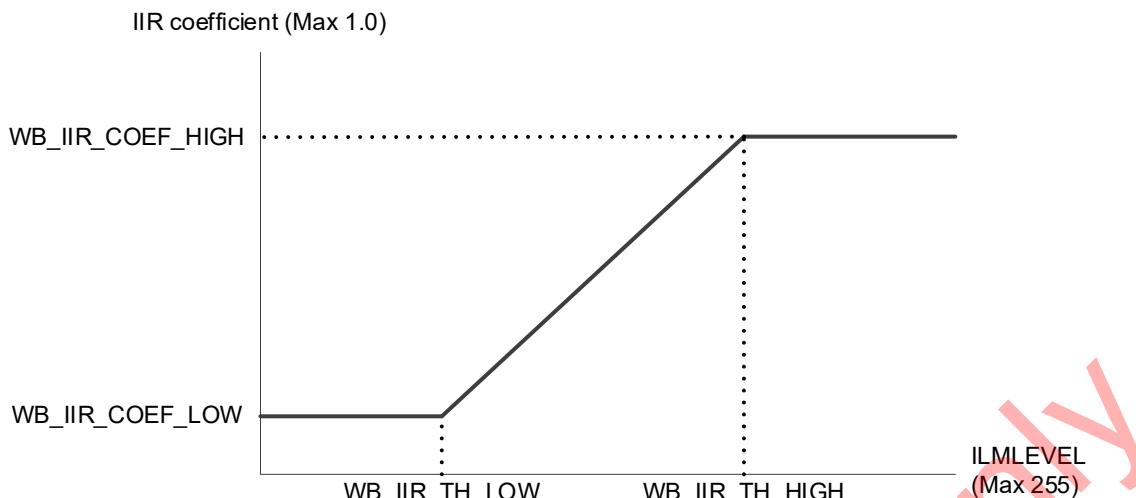


Figure 5-44 Setting of the Coefficients for the IIR Filter

When the coefficient is 1.0, the IIR filter is disabled, and the metering results of the current frame are the results as is. As the coefficient decreases, the ratio of the metering results of the preceding frame increases, resulting in a slow response to the change in the subject. When the coefficient is set to 0, the ratio of the current frame's metering results is 0. Therefore, the metering results remain unchanged from the value of the preceding frame.

■ Conditions for IIR filter coefficient resets

The IIR coefficient is reset by the sensor under any of the following conditions:

- The sensor determines that a light metering error has occurred.
- The sensor has transitioned to AWB mode instead of ATW or All Pull-in mode.
- The total amount of bit-shift exceeds the value of the WB_IIR_SHIFT_TH register when an integrated value is read out.

5.3.3.6. Pre-White Balance Function

When using multiple sensors to meter the same light source, the RGB input level may differ from sensor to sensor due to optical factors. In this case, the differential in RGB input levels can be reduced by adjusting the Pre-White Balance function. For details regarding the adjustment method, refer to the IMX623-AA** "Image Tuning Manual."

- To adjust the Pre-White Balance function, set the AWB_ADJ_F register to 1 and then set the adjustment variable(s) using the AWB_ADJ_SUB_MODE register.
- The compensation coefficients calculated in the Pre-White Balance adjustment is applied to the following registers:
 - * The PRER and PREB registers are set to the compensation coefficients at low color temperatures.
 - * The NORMR and NORMB registers are set to the compensation coefficients at high color temperatures.
- Regarding the AWB_ADJ_SUB_MODE register, as shown in “Table 5-41,” the host’s requests and the sensor’s responses are managed by one register.
- The values, which the host can set using the AWB_ADJ_SUB_MODE register, are 0x00, 0x01, 0x03 and 0xE0.

Table 5-41 Setting the Pre-White Balance Function

AWB_ADJ_F	AWB_ADJ_SUB_MODE	Calibration Register	Description
0	-	-	Pre-White Balance adjustment disabled
1	0x00	-	On standby for an adjustment request of the Pre-White Balance function
	0x01	PWB_LOW_COORD_R	Register adjustment request at low color temperatures
		PWB_LOW_COORD_B	<ul style="list-style-type: none"> After adjustment, the sensor changes the AWB_ADJ_SUB_MODE register to 0x02.
	0x02	-	Adjustment at low color temperatures is complete.
	0x03	PWB_HIGH_COORD_R	Register adjustment request at high color temperatures
		PWB_HIGH_COORD_B	<ul style="list-style-type: none"> After adjustment, the sensor changes the AWB_ADJ_SUB_MODE register to 0x04.
	0x04	-	Adjustment at high color temperatures is complete.
	0xE0	-	Adjustment cancellation request <ul style="list-style-type: none"> If adjustments are not completed, the sensor will restore the pre-adjustment state. Therefore, maintain the state until the AWB_ADJ_SUB_MODE register is changed to 0xE1.
	0xE1	-	Adjustment cancellation is complete.
	0xFE	-	Parameter setting error
	0xFF	-	Light Metering Error

5.3.3.6.1. Light Metering Results by the Pre-White Balance Function

Light metering results by the Pre-White Balance function are set to the following registers:

- PREWB_LOW_OPD_x (x = R, G, B) registers are set to the average values at low color temperatures.
- PREWB_HIGH_OPD_x (x = R, G, B) registers are set to the average values at high color temperatures.

The value of the PRER and PREB registers and the NORMR and NORMB registers are calculated from these values.

5.3.3.6.2. Completion of the Pre-White Balance Adjustment

The pre-white balance adjustment completes automatically after adjusting the compensation coefficients. The conditions for suspending the pre-white balance processing are shown below:

- The pre-white balance adjustment is cancelled.
- There is an error in specifying the parameters.
- The state of $\text{ERRLEVEL} \geq \text{PWB_AEERR}$ continues for the number of frames or greater set in the PWB_RETRY register, or the integrated value of the RGB signals is identified as a light metering error.

5.3.4. Interface

5.3.4.1. Input Registers

Table 5-42 Input Registers for the White Balance Function

[AWB]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB0F0	1	7:0	AWBMODE	R/W	U8.0	This register is used to select the control method of white balance. 0: ATW 1: All Pull-in 2: User preset 3: Full MWB 4: Hold Any other settings are prohibited.
0xB0F1	1	1:0	WS_MODE	R/W	U2.0	This register is used to set the WB scene. 0: WS0 1: WS1 2: Automatic switching 3: Setting prohibited
		2	WS_INIT	R/W	U1.0	This register is used to set the initial state of the WB scenes. Valid only when the value of the WS_MODE register is 2.
		3	ATW_CNT_EQ_AIM_EN	R/W	U1.0	This register is used to select the convergence completion condition for the ATW operation. 0x0: The sensor determines that the convergence is complete when the Cont point enters the "convergence completion" area. 0x1: After the Cont point enters this area, the sensor determines this as " Cont = Aim " and resumes tracking the Aim point.
		5	FRMOUT_RATIO_CALC_EN	R/W	U1.0	This register is used to set the operation when a Pull-in error occurs. 0: Output of a Pull-in error enabled 1: Calculation of the Ratio point even outside the Operation Area
		6	AWB_RATIO_CALC_F	R/W	U1.0	0x0: Luminance-dependent AWB 0x1: Area-dependent AWB
0xB0F2	1	1	WBGAIN_THMODE_EN	R/W	U1.0	This register is used to configure the pass-through settings of the white balance gain. 0x0: White balance gain applied 0x1: White balance gain not applied (Fixed at 1.0x)
		2	WB_IIR_EN	R/W	U1.0	This register is used to determine whether an IIR filter is applied to the AWB light metering results. 0: Not applied 1: Applied
		5	ATW2ALL_BLEND_EN	R/W	U1.0	[For ATW Operation] This register is used to enable or disable the blending between the ATW and the "All Cell-Average" Ratio point in low illuminance. 0x0: Blending disabled 0x1: Blending enabled

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
		6	ATW2ALL_FRMOUT_AIM_EN	R/W	U1.0	This register is used to enable or disable a function that sets the targets outside the Aim Area when the values of the ATW and the All-Pull-in Ratio point are blended. 0x0: Disabled 0x1: Enabled
0xB0F3	1	0	RATIO AGAIN	R/W	U1.0	This register is used to set the recalculation of the Ratio point. This is a setting to determine whether to reintegrate the Ratio point which has been calculated by means of weighted calculation using the Operation Area and the Aim Area. 0x0: Reintegration disabled 0x1: Reintegration enabled
		1	ATW_REFRESH_EN	R/W	U1.0	[For ATW Operation] This register is used to enable or disable the mode-refresh processing when fixed values and the light-metering-cell settings are changed. 0x0: Disabled 0x1: Enabled
0xB0F4	1	7:0	INITMOVE_GIVEUP_CNT	R/W	U8.0	The sensor begins a pull-in operation of the Cont point immediately after the WS0 and WS1 are switched. This register is used to set the number of frames, after which the sensor stops attempting to perform this pull-in operation.
0xB0F5	1	7:0	AWB_ER_DELAY	R/W	U8.0	[For ATW Operation] This register is used to set the threshold for an error-preservation frame. <ul style="list-style-type: none"> When a light metering error or a pull-in frame error occurs, the sensor continues to preserve an error state for the specified number of frames. After the specified number of frames has elapsed, the sensor resumes a pull-in operation.
0xB0F6	1	7:0	ATW_INITMASK	R/W	U8.0	[For ATW Operation] This register is used to set the number of frames, in which the sensor is on standby, after the sensor has transitioned to Streaming State.
0xB0F7	1	7:0	AWBUSER_NO	R/W	U8.0	[For User Preset] This register is used to switch the preset numbers. Available range: 0 to 2
0xB0F8	1	7:0	INIT_ILMLEVEL	R/W	U8.0	[For ATW Operation] This register is used to set the threshold to determine a light metering error corresponding to the illuminance level. <ul style="list-style-type: none"> When the value of the ILMLEVEL register is lower than the value of the INIT_ILMLEVEL register, the sensor identifies this as a light metering error and then suspends a pull-in operation.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB0F9	1	7:0	INIT_ILMLEVEL_ALL	R/W	U8.0	[For All Pull-in Operation] This register is used to set the threshold to determine a light metering error corresponding to the illuminance level. <ul style="list-style-type: none">When the value of the ILMLEVEL register is lower than the value of the INIT_ILMLEVEL register, the sensor identifies this as a light metering error and then suspends a pull-in operation.
0xB0FA	1	7:0	INIT_AEERR	R/W	U8.0	[For ATW Operation] This register is used to set the initial value of the error level by which the sensor determines whether to start an AWB operation. Available range: 0x0 to 0x80
0xB0FB	1	7:0	INIT_AEERR_ALL	R/W	U8.0	[For All Pull-in Operation] This register is used to set the initial value of the error level by which the sensor determines whether to start an AWB operation. Available range: 0x0 to 0x80
0xB0FC	1	7:0	INIT_AEDARK	R/W	U8.0	[For ATW Operation] This register is used to set the initial value of the error level by which the sensor determines whether to start an AWB operation. Available range: 0x0 to 0xFF
0xB0FD	1	7:0	INIT_AEDARK_ALL	R/W	U8.0	[For All Pull-in Operation] This register is used to set the initial value of the error level by which the sensor determines whether to start an AWB operation. Available range: 0x0 to 0xFF
0xB0FE	1	7:0	WS0_JUDGPOS	R/W	U8.0	Set the threshold for switching to the WS0 to satisfy the following condition: WS0_JUDGPOS < WS1_JUDGPOS
0xB0FF	1	7:0	WS1_JUDGPOS	R/W	U8.0	Set the threshold for switching to the WS1 to satisfy the following condition: WS0_JUDGPOS < WS1_JUDGPOS
0xB101	1	7:0	FRMIN_JUDG_NUM_WS 0	R/W	U8.0	This register is used to set the threshold for the minimum number of the Ratio points required to be present within the Operation Area. (For the WS0) Available range: 0x01 to 0x3F
0xB102	1	7:0	FRMIN_JUDG_NUM_WS 1	R/W	U8.0	This register is used to set the threshold for the minimum number of the Ratio points required to be present within the Operation Area. (For the WS1) Available range: 0x01 to 0x3F
0xB103	1	7:0	OPD_WEIGHT_FRMIN	R/W	U8.0	This register is used to set the weighting factors of the light metering cells within the Operation Area and outside the Aim Area.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB104	1	7:0	RATIO_SCOPE_UD	R/W	U8.0	<p>This register is used to set the range in order for the sensor to determine the Ratio point to be recalculated. (B/G coordinates)</p> <ul style="list-style-type: none"> When the RATIO AGAIN register is 0x1, the sensor recalculates the Ratio point using the light metering cells within the area defined by the RATIO_SCOPE_UD and RATIO_SCOPE_RL registers.
0xB105	1	7:0	RATIO_SCOPE_RL	R/W	U8.0	<p>This register is used to set the range in order for the sensor to determine the Ratio point to be recalculated. (R/G coordinates)</p> <ul style="list-style-type: none"> When the RATIO AGAIN register is 0x1, the sensor recalculates the Ratio point using the light metering cells within the area defined by the RATIO_SCOPE_UD and RATIO_SCOPE_RL registers.
0xB106	1	7:0	ATW2ALL_BLEND_STA	R/W	U8.0	[For ATW/All Pull-in Operation] This register is used to set the threshold for illuminance-interlocking of the Ratio point (brighter side).
0xB107	1	7:0	ATW2ALL_BLEND_END	R/W	U8.0	[For ATW/All Pull-in Operation] This register is used to set the threshold for illuminance-interlocking of the Ratio point (darker side).
0xB108	1	7:0	ATW2ALL_BLEND_MAX	R/W	U1.7	[For ATW/All Pull-in Operation] This register is used to set the blend ratio on the darkest side for illuminance-interlocking of the Ratio point. <ul style="list-style-type: none"> Setting a value of 0x80 disables the function.
0xB109	1	7:0	ILMLV_FRMERR_TH	R/W	U8.0	This register is used to set the threshold for the illuminance that enables the sensor to determine an Operation Area error.
0xB10A	1	7:0	ATW2ALL_FRMOUT_AIM_WEIGHT	R/W	U8.0	[For ATW/All Pull-in Operation] This register is used to set the ratio in relation to the target that exceeds the Aim Area when the sensor blends the average Ratio points of all 63 light metering cells and the Ratio point that the sensor calculates. Available range: 0x00 (0.0x) to 0x80 (1.0x) 0x00: The Aim point is set on the border of the Aim Area. 0x80: The Aim point is set at the same position as the Ratio point. Setting a value of 0x81 or greater is prohibited.
0xB10B	1	7:0	DB_WSO_L_UP	R/W	U8.0	This register is used to set the expansion coefficient of the outer dead zone (i.e., a coefficient for expanding the outer dead zone upward). (For WSO) <ul style="list-style-type: none"> Set this register to a value greater than the value of the DB_WSO_M_UP register.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB10C	1	7:0	DB_WSO_L_DOWN	R/W	U8.0	<p>This register is used to set the expansion coefficient of the outer dead zone (i.e., a coefficient for expanding the outer dead zone downward). (For WSO)</p> <ul style="list-style-type: none"> Set this register to a value greater than the value of the DB_WSO_M_DOWN register.
0xB10D	1	7:0	DB_WSO_L_RIGHT	R/W	U8.0	<p>This register is used to set the expansion coefficient of the outer dead zone (i.e., a coefficient for expanding the outer dead zone to the right). (For WSO)</p> <ul style="list-style-type: none"> Set this register to a value greater than the value of the DB_WSO_M_RIGHT register.
0xB10E	1	7:0	DB_WSO_L_LEFT	R/W	U8.0	<p>This register is used to set the expansion coefficient of the outer dead zone (i.e., a coefficient for expanding the outer dead zone to the left). (For WSO)</p> <ul style="list-style-type: none"> Set this register to a value greater than the value of the DB_WSO_M_LEFT register.
0xB10F	1	7:0	DB_WSO_M_UP	R/W	U8.0	<p>This register is used to set the expansion coefficient of the middle dead zone (i.e., a coefficient for expanding the middle dead zone upward). (For WSO)</p> <ul style="list-style-type: none"> Set this register to a value less than the value of the DB_WSO_L_UP register. Set this register to a value greater than the value of the DBAND_S_UP register.
0xB110	1	7:0	DB_WSO_M_DOWN	R/W	U8.0	<p>This register is used to set the expansion coefficient of the middle dead zone (i.e., a coefficient for expanding the middle dead zone downward). (For WSO)</p> <ul style="list-style-type: none"> Set this register to a value less than the value of the DB_WSO_L_DOWN register. Set this register to a value greater than the value of the DBAND_S_DOWN register.
0xB111	1	7:0	DB_WSO_M_RIGHT	R/W	U8.0	<p>This register is used to set the expansion coefficient of the middle dead zone (i.e., a coefficient for expanding the middle dead zone to the right). (For WSO)</p> <ul style="list-style-type: none"> Set this register to a value less than the value of the DB_WSO_L_RIGHT register. Set this register to a value greater than the value of the DBAND_S_RIGHT register.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB112	1	7:0	DB_WS0_M_LEFT	R/W	U8.0	<p>This register is used to set the expansion coefficient of the middle dead zone (i.e., a coefficient for expanding the middle dead zone to the left). (For WS0)</p> <ul style="list-style-type: none"> • Set this register to a value less than the value of the DB_WS0_L_LEFT register. • Set this register to a value greater than the value of the DBAND_S_LEFT register.
0xB113	1	7:0	DB_WS1_L_UP	R/W	U8.0	<p>This register is used to set the expansion coefficient of the outer dead zone (i.e., a coefficient for expanding the outer dead zone upward). (For WS1)</p> <ul style="list-style-type: none"> • Set this register to a value greater than the value of the DB_WS1_M_UP register.
0xB114	1	7:0	DB_WS1_L_DOWN	R/W	U8.0	<p>This register is used to set the expansion coefficient of the outer dead zone (i.e., a coefficient for expanding the outer dead zone downward). (For WS1)</p> <ul style="list-style-type: none"> • Set this register to a value greater than the value of the DB_WS1_M_DOWN register.
0xB115	1	7:0	DB_WS1_L_RIGHT	R/W	U8.0	<p>This register is used to set the expansion coefficient of the outer dead zone (i.e., a coefficient for expanding the outer dead zone to the right). (For WS1)</p> <ul style="list-style-type: none"> • Set this register to a value greater than the value of the DB_WS1_M_RIGHT register.
0xB116	1	7:0	DB_WS1_L_LEFT	R/W	U8.0	<p>This register is used to set the expansion coefficient of the outer dead zone (i.e., a coefficient for expanding the outer dead zone to the left). (For WS1)</p> <ul style="list-style-type: none"> • Set this register to a value greater than the value of the DB_WS1_M_LEFT register.
0xB117	1	7:0	DB_WS1_M_UP	R/W	U8.0	<p>This register is used to set the expansion coefficient of the middle dead zone (i.e., a coefficient for expanding the middle dead zone upward). (For WS1)</p> <ul style="list-style-type: none"> • Set this register to a value less than the value of the DB_WS1_L_UP register. • Set this register to a value greater than the value of the DBAND_S_UP register.
0xB118	1	7:0	DB_WS1_M_DOWN	R/W	U8.0	<p>This register is used to set the expansion coefficient of the middle dead zone (i.e., a coefficient for expanding the middle dead zone downward). (For WS1)</p> <ul style="list-style-type: none"> • Set this register to a value less than the value of the DB_WS1_L_DOWN register. • Set this register to a value greater than the value of the DBAND_S_DOWN register.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB119	1	7:0	DB_WS1_M_RIGHT	R/W	U8.0	<p>This register is used to set the expansion coefficient of the middle dead zone (i.e., a coefficient for expanding the middle dead zone to the right). (For WS1)</p> <ul style="list-style-type: none"> • Set this register to a value less than the value of the DB_WS1_L_RIGHT register. • Set this register to a value greater than the value of the DBAND_S_RIGHT register.
0xB11A	1	7:0	DB_WS1_M_LEFT	R/W	U8.0	<p>This register is used to set the expansion coefficient of the middle dead zone (i.e., a coefficient for expanding the middle dead zone to the left). (For WS1)</p> <ul style="list-style-type: none"> • Set this register to a value less than the value of the DB_WS1_L_LEFT register. • Set this register to a value greater than the value of the DBAND_S_LEFT register.
0xB11B	1	7:0	DBAND_S_UP	R/W	U8.0	<p>This register is used to set the expansion coefficient of the inner dead zone (i.e., a coefficient for expanding the inner dead zone upward).</p> <ul style="list-style-type: none"> • Set this register to a value less than the values of the DB_WS0_M_UP and DB_WS1_M_UP registers.
0xB11C	1	7:0	DBAND_S_DOWN	R/W	U8.0	<p>This register is used to set the expansion coefficient of the inner dead zone (i.e., a coefficient for expanding the inner dead zone downward).</p> <ul style="list-style-type: none"> • Set this register to a value less than the values of the DB_WS0_M_DOWN and DB_WS1_M_DOWN registers.
0xB11D	1	7:0	DBAND_S_RIGHT	R/W	U8.0	<p>This register is used to set the expansion coefficient of the inner dead zone (i.e., a coefficient for expanding the inner dead zone to the right).</p> <ul style="list-style-type: none"> • Set this register to a value less than the values of the DB_WS0_M_RIGHT and DB_WS1_M_RIGHT registers.
0xB11E	1	7:0	DBAND_S_LEFT	R/W	U8.0	<p>This register is used to set the expansion coefficient of the inner dead zone (i.e., a coefficient for expanding the inner dead zone to the left).</p> <ul style="list-style-type: none"> • Set this register to a value less than the values of the DB_WS0_M_LEFT and DB_WS1_M_LEFT registers.
0xB11F	1	7:0	ATW_GAINS_WS0_NR	R/W	U8.0	<p>[For ATW Operation]</p> <p>This register is used to set the gain step near the convergence target. (For WS0)</p> <ul style="list-style-type: none"> • When the gain step is set to 0x0, the gain step is assigned to 1 regardless.
0xB120	1	7:0	ATW_GAINS_WS0	R/W	U8.0	<p>[For ATW Operation]</p> <p>This register is used to set the gain step not near the convergence target. (For WS0)</p> <ul style="list-style-type: none"> • When the gain step is set to 0x0, the gain step is assigned to 1 regardless.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB121	1	7:0	ATW_GAINS_WS1_NR	R/W	U8.0	[For ATW Operation] This register is used to set the gain step near the convergence target. (For WS1) • When the gain step is set to 0x0, the gain step is assigned to 1 regardless.
0xB122	1	7:0	ATW_GAINS_WS1	R/W	U8.0	[For ATW Operation] This register is used to set the gain step not near the convergence target. (For WS1) • When the gain step is set to 0x0, the gain step is assigned to 1 regardless.
0xB123	1	7:0	AIM_NR_TH_UP	R/W	U8.0	This register is used to set the threshold for the area near the Aim point. (Upward)
0xB124	1	7:0	AIM_NR_TH_DOWN	R/W	U8.0	This register is used to set the threshold for the area near the Aim point. (downward)
0xB125	1	7:0	AIM_NR_TH_RIGHT	R/W	U8.0	This register is used to set the threshold for the area near the Aim point. (To the right)
0xB126	1	7:0	AIM_NR_TH_LEFT	R/W	U8.0	This register is used to set the threshold for the area near the Aim point. (To the left)
0xB127	1	7:0	ATW_DELAY	R/W	U8.0	This register is used to set the number of frames in which the sensor stops tracking an Aim point when a Cont point moves outside the inner dead zone.
0xB128	1	7:0	INIT_GAINS	R/W	U8.0	This register is used to set the gain step for a high-speed pull-in operation at sensor startup. • When the gain step is set to 0x0, the gain step is assigned to 1 regardless.
0xB12A	2	15:0	INIT_SFTLMT	R/W	U16.0	This register is used to set the shift limit for a high-speed pull-in operation at sensor startup. • When a value of 0x0 is set, the limit is cancelled.
0xB12C	1	7:0	ALLWB_USER_DELAY	R/W	U8.0	[For All Pull-in Operation] This register is used to set the number of frames to be ignored when restarting the All Pull-in operation from the convergence state.
0xB12D	1	7:0	ALLWB_USER_GAINS	R/W	U8.0	Convergence speed in the All Pull-in operation 0x01: Highest 0xFF: Lowest
0xB12E	2	15:0	ALLWB_USER_SFTLMT	R/W	U16.0	This register is used to set the limit value for convergence in the All Pull-in operation.
0xB130	2	15:0	ATW_SFTLMT_WS0_NR	R/W	U16.0	[For ATW Operation] This register is used to set the shift limit near the convergence target. (For WS0) • When a value of 0x0 is set, the limit is cancelled.
0xB132	2	15:0	ATW_SFTLMT_WS0	R/W	U16.0	[For ATW Operation] This register is used to set the shift limit not near the convergence target. (For WS0) • When a value of 0x0 is set, the limit is cancelled.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB134	2	15:0	ATW_SFTLMT_WS1_NR	R/W	U16.0	[For ATW Operation] This register is used to set the shift limit near the convergence target. (For WS1) • When a value of 0x0 is set, the limit is cancelled.
0xB136	2	15:0	ATW_SFTLMT_WS1	R/W	U16.0	[For ATW Operation] This register is used to set the shift limit not near the convergence target. (For WS1) • When a value of 0x0 is set, the limit is cancelled.
0xB138	2	15:0	INIT_CONT_WS0_R	R/W	U4.12	This register is used to set the R/G coordinate of the Cont point for the WS0 at start-up.
0xB13A	2	15:0	INIT_CONT_WS0_B	R/W	U4.12	This register is used to set the B/G coordinate of the Cont point for the WS0 at start-up.
0xB13C	2	15:0	INIT_CONT_WS1_R	R/W	U4.12	This register is used to set the R/G coordinate of the Cont point for the WS1 at start-up.
0xB13E	2	15:0	INIT_CONT_WS1_B	R/W	U4.12	This register is used to set the B/G coordinate of the Cont point for the WS1 at start-up.
0x9C28	2	11:0	FULLMWBGAIN_R	R/W	U4.8	This register is used to set the white balance gain for CF0 which is valid when the value of the AWBMODE register is 3. Example: 0x080, 0x100 and 0x400 are 0.5x, 1.0x and 4.0x, respectively.
0x9C2A	2	11:0	FULLMWBGAIN_GR	R/W	U4.8	This register is used to set the white balance gain for CF1 which is valid when the value of the AWBMODE register is 3. Example: 0x080, 0x100 and 0x400 are 0.5x, 1.0x and 4.0x, respectively.
0x9C2C	2	11:0	FULLMWBGAIN_GB	R/W	U4.8	This register is used to set the white balance gain for CF2 which is valid when the value of the AWBMODE register is 3. Example: 0x080, 0x100 and 0x400 are 0.5x, 1.0x and 4.0x, respectively.
0x9C2E	2	11:0	FULLMWBGAIN_B	R/W	U4.8	This register is used to set the white balance gain for CF3 which is valid when the value of the AWBMODE register is 3. Example: 0x080, 0x100 and 0x400 are 0.5x, 1.0x and 4.0x, respectively.
0xB148	1	7:0	WB_IIR_COEF_LOW	R/W	U1.7	The coefficient of the IIR filter for the results of the AWB light metering in low illuminance.
0xB149	1	7:0	WB_IIR_COEF_HIGH	R/W	U1.7	The coefficient of the IIR filter for the results of the AWB light metering at high illuminance.
0xB14A	1	7:0	WB_IIR_TH_LOW	R/W	U8.0	The illuminance when the coefficient of the IIR filter for the results of the AWB light metering equals the WB_IIR_COEF_LOW register's value.
0xB14B	1	7:0	WB_IIR_TH_HIGH	R/W	U8.0	The illuminance when the coefficient of the IIR filter for the results of the AWB light metering equals the WB_IIR_COEF_HIGH register's value.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB173	1	7:0	FRMOUT_AIM_WEIGHT	R/W	U1.7	<p>This register is used to set a weighting factor for setting the target position in relation to the Aim Area under the following conditions:</p> <ul style="list-style-type: none"> The sensor determines the white balance scene as WS0. The Ratio point exceeds the Aim Area. <p>0x00: The Aim point is set on the border of the Aim Area. 0x80: The setting of Aim = Ratio Available range: 0x00 (0.0) to 0x80 (1.0)</p>
0xB178	1	5:0	AWB_OPD_READ_VAL	R/W	U6.0	<p>This register is used to set the number of bits of the MSB when the sensor reads out an integrated value.</p> <ul style="list-style-type: none"> Any bits that are not read out are processed as 0.
0xB179	1	0	AWB_WBCLIP_SPS_OFT_ON	R/W	U1.0	<p>This register is used to enable or disable the use of an offset value of the Dark Shading function for the calculation of WB clipping.</p> <p>0x0: Disabled 0x1: Enabled</p>
		2	AWB_WBCLIP_PGA_SEL	R/W	U1.0	<p>This register is used to set the PGA gain to calculate the WBCLIP value.</p> <p>0x0: An actual gain to be used for calculation 0x1: A gain value equivalent to 1.0x to be used for calculation</p>
0xB17A	1	2	AWB_OPDSLICE_PGA_SEL	R/W	U1.0	<p>This register is used to set the PGA gain to calculate the OPDSLICE value.</p> <p>0x0: An actual gain to be used for calculation 0x1: A gain value equivalent to 1.0x to be used for calculation</p>
0xB195	1	7:0	WB_IIR_SHIFT_TH	R/W	U8.0	<p>This register is used to set the condition, under which the OPD IIR coefficient is reset.</p> <ul style="list-style-type: none"> The sensor resets the IIR coefficient when the amount of change in the value calculated from the OPDs exceeds the value of this register.
0xB196	2	15:0	USER0_R	R/W	U4.12	[For User Preset] The R/G coordinate of the Aim point of Preset Number 0.
0xB198	2	15:0	USER0_B	R/W	U4.12	[For User Preset] The B/G coordinate of the Aim point of Preset Number 0.
0xB19A	2	15:0	USER1_R	R/W	U4.12	[For User Preset] The R/G coordinate of the Aim point of Preset Number 1.
0xB19C	2	15:0	USER1_B	R/W	U4.12	[For User Preset] The B/G coordinate of the Aim point of Preset Number 1.
0xB19E	2	15:0	USER2_R	R/W	U4.12	[For User Preset] The R/G coordinate of the Aim point of Preset Number 2.
0xB1A0	2	15:0	USER2_B	R/W	U4.12	[For User Preset] The B/G coordinate of the Aim point of Preset Number 2.

[AWB_FRM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB1A4	1	7:0	WS0_FRM_LEFT_00_R	R/W	U8.0	This register is used to set the coordinate of Point #00 of the Operation Area's left profile on the R/G axis. (For the WS0)
0xB1A5	1	7:0	WS0_FRM_LEFT_00_B	R/W	U8.0	This register is used to set the coordinate of Point #00 of the Operation Area's left profile on the B/G axis. (For the WS0)
0xB1A6	1	7:0	WS0_FRM_LEFT_01_R	R/W	U8.0	This register is used to set the coordinate of Point #01 of the Operation Area's left profile on the R/G axis. (For the WS0)
0xB1A7	1	7:0	WS0_FRM_LEFT_01_B	R/W	U8.0	This register is used to set the coordinate of Point #01 of the Operation Area's left profile on the B/G axis. (For the WS0)
...		
0xB1B2	1	7:0	WS0_FRM_LEFT_07_R	R/W	U8.0	This register is used to set the coordinate of Point #07 of the Operation Area's left profile on the R/G axis. (For the WS0)
0xB1B3	1	7:0	WS0_FRM_LEFT_07_B	R/W	U8.0	This register is used to set the coordinate of Point #07 of the Operation Area's left profile on the B/G axis. (For the WS0)
0xB1B4	1	7:0	WS0_FRM_RIGHT_00_R	R/W	U8.0	This register is used to set the coordinate of Point #00 of the Operation Area's right profile on the R/G axis. (For the WS0)
0xB1B5	1	7:0	WS0_FRM_RIGHT_00_B	R/W	U8.0	This register is used to set the coordinate of Point #00 of the Operation Area's right profile on the B/G axis. (For the WS0)
0xB1B6	1	7:0	WS0_FRM_RIGHT_01_R	R/W	U8.0	This register is used to set the coordinate of Point #01 of the Operation Area's right profile on the R/G axis. (For the WS0)
0xB1B7	1	7:0	WS0_FRM_RIGHT_01_B	R/W	U8.0	This register is used to set the coordinate of Point #01 of the Operation Area's right profile on the B/G axis. (For the WS0)
...		
0xB1C2	1	7:0	WS0_FRM_RIGHT_07_R	R/W	U8.0	This register is used to set the coordinate of Point #07 of the Operation Area's right profile on the R/G axis. (For the WS0)
0xB1C3	1	7:0	WS0_FRM_RIGHT_07_B	R/W	U8.0	This register is used to set the coordinate of Point #07 of the Operation Area's right profile on the B/G axis. (For the WS0)
0xB1C4	1	7:0	WS0_AIM_LEFT_00_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #00 of the Aim Area's left profile. (For the WS0)
0xB1C5	1	7:0	WS0_AIM_LEFT_00_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #00 of the Aim Area's left profile. (For the WS0)
0xB1C6	1	7:0	WS0_AIM_LEFT_01_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #01 of the Aim Area's left profile. (For the WS0)
0xB1C7	1	7:0	WS0_AIM_LEFT_01_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #01 of the Aim Area's left profile. (For the WS0)
...		
0xB1D2	1	7:0	WS0_AIM_LEFT_07_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #07 of the Aim Area's left profile. (For the WS0)

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB1D3	1	7:0	WS0_AIM_LEFT_07_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #07 of the Aim Area's left profile. (For the WS0)
0xB1D4	1	7:0	WS0_AIM_RIGHT_00_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #00 of the Aim Area's right profile. (For the WS0)
0xB1D5	1	7:0	WS0_AIM_RIGHT_00_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #00 of the Aim Area's right profile. (For the WS0)
0xB1D6	1	7:0	WS0_AIM_RIGHT_01_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #01 of the Aim Area's right profile. (For the WS0)
0xB1D7	1	7:0	WS0_AIM_RIGHT_01_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #01 of the Aim Area's right profile. (For the WS0)
...		
0xB1E2	1	7:0	WS0_AIM_RIGHT_07_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #07 of the Aim Area's right profile. (For the WS0)
0xB1E3	1	7:0	WS0_AIM_RIGHT_07_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #07 of the Aim Area's right profile. (For the WS0)
0xB1E4	1	2:0	WS0_FRM_BTM_NUM	R/W	U3.0	This register is used to set the B/G coordinates of the Operation Area's lower limit. (For the WS0)
		5:3	WS0_AIM_BTM_NUM	R/W	U3.0	This register is used to set the B/G coordinates of the Aim Area's lower limit profile. (For the WS0)
0xB1E5	1	2:0	WS0_FLTOP_FRM_NUM	R/W	U3.0	This register is used to set the coordinate of the Operation Area's upper level on the B/G axis when a pull-in operation is performed diagonally downward to the right or left by an angle of 45 degrees. (For the WS0) User-set value x 256
		5:3	WS0_FLTOP_AIM_NUM	R/W	U3.0	This register is used to set the coordinate of the upper level of the Aim Area on the B/G axis when a pull-in operation is performed diagonally downward to the right or left by an angle of 45 degrees. (For the WS0) User-set value x 256
0xB1E6	1	2:0	WS0_FLBTM_FRM_NUM	R/W	U3.0	This register is used to set the coordinate of the lower level of the Operation Area on the B/G axis when a pull-in operation is performed diagonally downward to the right or left by an angle of 45 degrees. (For the WS0) User-set value x 256
		5:3	WS0_FLBTM_AIM_NUM	R/W	U3.0	This register is used to set the coordinate of the lower level of the Aim Area on the B/G axis when a pull-in operation is performed diagonally downward to the right or left by an angle of 45 degrees. (For the WS0) User-set value x 256
0xB1E7	1	7:0	WS1_FRM_LEFT_00_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #00 of the Operation Area's left profile. (For the WS1)
0xB1E8	1	7:0	WS1_FRM_LEFT_00_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #00 of the Operation Area's left profile. (For the WS1)

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB1E9	1	7:0	WS1_FRM_LEFT_01_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #01 of the Operation Area's left profile. (For the WS1)
0xB1EA	1	7:0	WS1_FRM_LEFT_01_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #01 of the Operation Area's left profile. (For the WS1)
...		
0xB1F5	1	7:0	WS1_FRM_LEFT_07_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #07 of the Operation Area's left profile. (For the WS1)
0xB1F6	1	7:0	WS1_FRM_LEFT_07_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #07 of the Operation Area's left profile. (For the WS1)
0xB1F7	1	7:0	WS1_FRM_RIGHT_00_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #00 of the Operation Area's right profile. (For the WS1)
0xB1F8	1	7:0	WS1_FRM_RIGHT_00_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #00 of the Operation Area's right profile. (For the WS1)
0xB1F9	1	7:0	WS1_FRM_RIGHT_01_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #01 of the Operation Area's right profile. (For the WS1)
0xB1FA	1	7:0	WS1_FRM_RIGHT_01_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #01 of the Operation Area's right profile. (For the WS1)
...		
0xB205	1	7:0	WS1_FRM_RIGHT_07_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #07 of the Operation Area's right profile. (For the WS1)
0xB206	1	7:0	WS1_FRM_RIGHT_07_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #07 of the Operation Area's right profile. (For the WS1)
0xB207	1	7:0	WS1_AIM_LEFT_00_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #00 of the Aim Area's left profile. (For the WS1)
0xB208	1	7:0	WS1_AIM_LEFT_00_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #00 of the Aim Area's left profile. (For the WS1)
0xB209	1	7:0	WS1_AIM_LEFT_01_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #01 of the Aim Area's left profile. (For the WS1)
0xB20A	1	7:0	WS1_AIM_LEFT_01_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #01 of the Aim Area's left profile. (For the WS1)
...		
0xB215	1	7:0	WS1_AIM_LEFT_07_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #07 of the Aim Area's left profile. (For the WS1)
0xB216	1	7:0	WS1_AIM_LEFT_07_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #07 of the Aim Area's left profile. (For the WS1)
0xB217	1	7:0	WS1_AIM_RIGHT_00_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #00 of the Aim Area's right profile. (For the WS1)

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB218	1	7:0	WS1主观_右_00_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #00 of the Aim Area's right profile. (For the WS1)
0xB219	1	7:0	WS1主观_右_01_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #01 of the Aim Area's right profile. (For the WS1)
0xB21A	1	7:0	WS1主观_右_01_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #01 of the Aim Area's right profile. (For the WS1)
...		
0xB225	1	7:0	WS1主观_右_07_R	R/W	U8.0	This register is used to set the R/G coordinate of Point #07 of the Aim Area's right profile. (For the WS1)
0xB226	1	7:0	WS1主观_右_07_B	R/W	U8.0	This register is used to set the B/G coordinate of Point #07 of the Aim Area's right profile. (For the WS1)
0xB227	1	2:0	WS1_FRM_BTM_NUM	R/W	U3.0	This register is used to set the B/G coordinates of the Operation Area's lower limit. (For the WS1)
		5:3	WS1主观_BTM_NUM	R/W	U3.0	This register is used to set the B/G coordinates of the Aim Area's lower limit profile. (For the WS1)
0xB228	1	2:0	WS1_FLTOP_FRM_NUM	R/W	U3.0	This register is used to set the coordinate of the upper level of the Operation Area on the B/G axis when a pull-in operation is performed diagonally downward to the right or left by an angle of 45 degrees. (For the WS1) User-set value x 256
		5:3	WS1_FLTOP主观_NUM	R/W	U3.0	This register is used to set the coordinate of the upper level of the Aim Area on the B/G axis when a pull-in operation is performed diagonally downward to the right or left by an angle of 45 degrees. (For the WS1) User-set value x 256
0xB229	1	2:0	WS1_FLBTM_FRM_NUM	R/W	U3.0	This register is used to set the coordinate of the lower level of the Operation Area on the B/G axis when a pull-in operation is performed diagonally downward to the right or left by an angle of 45 degrees. (For the WS1) User-set value x 256
		5:3	WS1_FLBTM主观_NUM	R/W	U3.0	This register is used to set the coordinate of the lower level of the Aim Area on the B/G axis when a pull-in operation is performed diagonally downward to the right or left by an angle of 45 degrees. (For the WS1) User-set value x 256
		7	ATW_FRM_CHK_F	R/W	U1.0	This register is used to enable or disable the checking of the coordinate settings for the Aim Area and Operation Area. 0: Disabled 1: Enabled

[AWB_OPD]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB22C	1	1:0	AWB_WND_MODE	R/W	U2.0	<p>Selection of the method used to specify the entire size of the AWB light metering window.</p> <p>0: Specify the width and height in pixels for each of the 63 cells, consisting of 9 horizontal x 7 vertical cells.</p> <p>1: Specifies using a width-height ratio with respect to the Active Area.</p> <ul style="list-style-type: none"> • Any other settings are prohibited.
		4:3	AWB_OPDIN_RGB_LMT_MODE	R/W	U2.0	<p>This register is used to set the upper limits of the RGB signals used for signal detection by AWB light metering.</p> <p>0x0: The maximum value (0xFFFF) is set.</p> <p>0x1: The threshold value for the AWB_x_PEAK (x = R, G, B) registers is set.</p> <ul style="list-style-type: none"> • Setting 0x2 or greater is prohibited.
		5	AWB_OPD_REVERSE_EN	R/W	U1.0	<p>This register is used to set the tracking of the entire AWB light metering window in horizontal and vertical directions</p> <p>0: Disabled</p> <p>1: Enabled</p>
0xB236	2	15:0	AWB_OPDERR_TH_R	R/W	U16.0	<p>This register is used to set the threshold in order for the sensor to determine a light metering error. (For the R pixels)</p> <ul style="list-style-type: none"> • If the OPD integrated value is less than the value of this register, the sensor identifies this as an OPD error.
0xB238	2	15:0	AWB_OPDERR_TH_G	R/W	U16.0	<p>This register is used to set the threshold in order for the sensor to determine a light metering error. (For the G pixels)</p> <ul style="list-style-type: none"> • If the OPD integrated value is less than the value of this register, the sensor identifies this as an OPD error.
0xB23A	2	15:0	AWB_OPDERR_TH_B	R/W	U16.0	<p>This register is used to set the threshold in order for the sensor to determine a light metering error. (For the B pixels)</p> <ul style="list-style-type: none"> • If the OPD integrated value is less than the value of this register, the sensor identifies this as an OPD error.
0xB23C	2	11:0	AWB_Y_PEAK	R/W	U12.0	<p>This register is used to set the upper threshold for the luminance signal.</p> <ul style="list-style-type: none"> • The sensor detects signals, the luminance signal of which falls under the following condition: AWB_Y_DARK ≤ Luminance Signal ≤ AWB_Y_PEAK.
0xB23E	2	11:0	AWB_Y_DARK	R/W	U12.0	<p>This register is used to set the lower threshold for the luminance signal.</p> <ul style="list-style-type: none"> • The sensor detects signals, the luminance signal of which falls under the following condition: AWB_Y_DARK ≤ Luminance Signal ≤ AWB_Y_PEAK.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB240	2	11:0	AWB_R_PEAK	R/W	U12.0	<p>This register is used to set the upper threshold for the saturation of the R pixels.</p> <ul style="list-style-type: none"> The sensor detects signals under the following conditions: R pixels \leq AWB_R_PEAK, G pixels \leq AWB_G_PEAK, and B pixels \leq AWB_B_PEAK
0xB242	2	11:0	AWB_G_PEAK	R/W	U12.0	<p>This register is used to set the upper threshold for the saturation of the G pixels.</p> <ul style="list-style-type: none"> The sensor detects signals under the following conditions: R pixels \leq AWB_R_PEAK, G pixels \leq AWB_G_PEAK, and B pixels \leq AWB_B_PEAK
0xB244	2	11:0	AWB_B_PEAK	R/W	U12.0	<p>This register is used to set the upper threshold for the saturation of the B pixels.</p> <ul style="list-style-type: none"> The sensor detects signals under the following conditions: R pixels \leq AWB_R_PEAK, G pixels \leq AWB_G_PEAK, and B pixels \leq AWB_B_PEAK
0xA060	2	15:0	AWB_WND_OFFSET_H	R/W	S15.0	This register is used to set the amount of horizontal offset from the center of the Active Area to the center of the AWB light metering window.
0xA062	2	15:0	AWB_WND_OFFSET_V	R/W	S15.0	This register is used to set the amount of vertical offset from the center of the Active Area to the center of the AWB light metering window.
0xA064	2	15:0	AWB_WND_SIZE_H	R/W	U16.0	<p>Setting of the width of the AWB light metering window.</p> <ul style="list-style-type: none"> When AWB_WND_MODE = 0, set the width of the cell, 63 (9 horizontal x 7 vertical cells) of which constitute the light metering window, using a value that is a multiple of 2. (Unit: U16.0) When AWB_WND_MODE = 1, set the width of the cell, 63 (9 horizontal x 7 vertical cells) of which constitute the light metering window, using a ratio with respect to the width of the Active Area. (Unit: U1.8) <p>Available range: 16 (0x10) to 256 (0x100)</p>
0xA066	2	15:0	AWB_WND_SIZE_V	R/W	U16.0	<p>This register is used to set the height of the AWB light metering window.</p> <ul style="list-style-type: none"> When AWB_WND_MODE = 0, set the height of the cell, 63 (9 horizontal x 7 vertical cells) of which constitute the light metering window, using a value that is a multiple of 2. (Unit: U16.0) When AWB_WND_MODE = 1, set the height of the cell, 63 (9 horizontal x 7 vertical cells) of which constitute the light metering window, using a ratio with respect to the height of the Active Area. (Unit: U1.8) <p>Available range: 4 (0x04) to 256 (0x100)</p>

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xA068	2	11:0	AWB_OPD_MASK_STA_H_00	R/W	U12.0	This register is used to set the horizontal start position. For the light metering window masking of the Rectangular Region #00 to be used for white balance
0xA06A	2	11:0	AWB_OPD_MASK_STAV_00	R/W	U12.0	This register is used to set the vertical start position. For the light metering window masking of the Rectangular Region #00 to be used for white balance
0xA06C	2	11:0	AWB_OPD_MASK_END_H_00	R/W	U12.0	This register is used to set the horizontal end position. For the light metering window masking of the Rectangular Region #00 to be used for white balance
0xA06E	2	11:0	AWB_OPD_MASK_END_V_00	R/W	U12.0	This register is used to set the vertical end position. For the light metering window masking of the Rectangular Region #00 to be used for white balance
0xA070	2	11:0	AWB_OPD_MASK_STA_H_01	R/W	U12.0	This register is used to set the horizontal start position. For the light metering window masking of the Rectangular Region #01 to be used for white balance
0xA072	2	11:0	AWB_OPD_MASK_STAV_01	R/W	U12.0	This register is used to set the vertical start position. For the light metering window masking of the Rectangular Region #01 to be used for white balance
0xA074	2	11:0	AWB_OPD_MASK_END_H_01	R/W	U12.0	This register is used to set the horizontal end position. For the light metering window masking of the Rectangular Region #01 to be used for white balance
0xA076	2	11:0	AWB_OPD_MASK_END_V_01	R/W	U12.0	This register is used to set the vertical end position. For the light metering window masking of the Rectangular Region #01 to be used for white balance
...		
0xA0A0	2	11:0	AWB_OPD_MASK_STA_H_07	R/W	U12.0	This register is used to set the horizontal start position. For the light metering window masking of the Rectangular Region #07 to be used for white balance
0xA0A2	2	11:0	AWB_OPD_MASK_STAV_07	R/W	U12.0	This register is used to set the vertical start position. For the light metering window masking of the Rectangular Region #07 to be used for white balance
0xA0A4	2	11:0	AWB_OPD_MASK_END_H_07	R/W	U12.0	This register is used to set the horizontal end position. For the light metering window masking of the Rectangular Region #07 to be used for white balance
0xA0A6	2	11:0	AWB_OPD_MASK_END_V_07	R/W	U12.0	This register is used to set the vertical end position. For the light metering window masking of the Rectangular Region #07 to be used for white balance

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB286	1	0	AWB_OPD_MASK_REV RSE_EN	R/W	U1.0	Setting the tracking of the light metering window in horizontal and vertical directions For the light metering window masking of the Rectangular Region to be used for white balance 0: Disabled 1: Enabled
0xA0A8	1	0	AWB_OPD_MASK_EN_0 0	R/W	U1.0	This register is used to enable or disable the Rectangular Mask #0 for white balance. 0: Disabled 1: Enabled
0xA0A9	1	0	AWB_OPD_MASK_EN_0 1	R/W	U1.0	This register is used to enable or disable the Rectangular Mask #1 for white balance. 0: Disabled 1: Enabled
...		
0xA0AF	1	0	AWB_OPD_MASK_EN_0 7	R/W	U1.0	This register is used to enable or disable the Rectangular Mask #7 for white balance. 0: Disabled 1: Enabled

[AWB_ADJ]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB294	2	15:0	NORMR	R/W	U4.12	This register is used to set the compensation coefficient for high color temperature. (For the R/G coordinate)
0xB296	2	15:0	NORMB	R/W	U4.12	This register is used to set the compensation coefficient for high color temperature. (For the B/G coordinate)
0xB298	2	11:0	PRER	R/W	U4.8	This register is used to set the compensation coefficient for low color temperature. (For the R/G coordinate)
0xB29A	2	11:0	PREB	R/W	U4.8	This register is used to set the compensation coefficient for low color temperature. (For the B/G coordinate)
0xB29C	1	7:0	PWB_RETRY	R/W	U8.0	This register is used to set the number of frames in which the sensor performs retries, due to a light metering error in the pre-white balance process. <ul style="list-style-type: none"> If the adjustment instruction after changing the light source is earlier than OPD convergence, the sensor ignores a light metering error and waits for the period of the specified number of frames.
0xB29D	1	7:0	PWB_AEERR	R/W	U8.0	This register is used to set the initial value of the amount of AE error in order for the sensor to determine the start of the pre-white balance adjustment. Available range: 0x0 to 0xFF
0xB29E	2	15:0	PWB_LOW_COORD_R	R/W	U16.0	This register is used to configure the settings of the Pre-White Balance adjustment for low color temperature. (For the R/G coordinate)
0xB2A0	2	15:0	PWB_LOW_COORD_B	R/W	U16.0	This register is used to configure the settings of the Pre-White Balance adjustment for low color temperature. (For the B/G coordinate)

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB2A2	2	15:0	PWB_HIGH_COORD_R	R/W	U16.0	This register is used to configure the settings of the Pre-White Balance adjustment for high color temperature. (For the R/G coordinate)
0xB2A4	2	15:0	PWB_HIGH_COORD_B	R/W	U16.0	This register is used to configure the settings of the Pre-White Balance adjustment for high color temperature. (For the B/G coordinate)
0xB2A8	4	31:0	PREWB_LOW_OPD_R	R/W	U32.0	This register indicates the integrated value obtained from the adjustment process at low-color temperature when the adjustment point at low-color temperature is changed. (For the R pixels)
0xB2AC	4	31:0	PREWB_LOW_OPD_G	R/W	U32.0	This register indicates the integrated value obtained from the adjustment process at low-color temperature when the adjustment point at low-color temperature is changed. (For the G pixels)
0xB2B0	4	31:0	PREWB_LOW_OPD_B	R/W	U32.0	This register indicates the integrated value obtained from the adjustment process at low-color temperature when the adjustment point at low-color temperature is changed. (For the B pixels)
0xB2B4	4	31:0	PREWB_HIGH_OPD_R	R/W	U32.0	This register indicates the integrated value obtained from the adjustment process at high-color temperature when the adjustment point at high-color temperature is changed. (For the R pixels)
0xB2B8	4	31:0	PREWB_HIGH_OPD_G	R/W	U32.0	This register indicates the integrated value obtained from the adjustment process at high-color temperature when the adjustment point at high-color temperature is changed. (For the G pixels)
0xB2BC	4	31:0	PREWB_HIGH_OPD_B	R/W	U32.0	This register indicates the integrated value obtained from the adjustment process at high-color temperature when the adjustment point at high-color temperature is changed. (For the B pixels)

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB2C0	1	7:0	AWB_ADJ_SUB_MODE	R/W	U8.0	<p>This register indicates the status of the Pre-White Balance adjustment.</p> <p>0: Before the adjustment of Pre-White Balance.</p> <p>1: Beginning of the low color temperature compensation coefficient adjustment.</p> <p>2: Completion of the low color temperature compensation coefficient adjustment.</p> <p>3: Beginning of the high color temperature compensation coefficient adjustment.</p> <p>4: Completion of the high color temperature compensation coefficient adjustment.</p> <p>0xE0: Cancellation of the Pre-White Balance adjustment.</p> <p>0xE1: Completion of the Cancellation of the Pre-White Balance adjustment.</p> <p>0xFE: Parameter selection error</p> <p>0xFF: Light metering error (AE has not converged or the light source's brightness is not sufficient.)</p> <ul style="list-style-type: none"> The host can only set values of 0, 1 and 3.
0xB2C1	1	0	AWB_ADJ_F	R/W	U1.0	<p>Setting of the Pre-White Balance Adjustment Mode</p> <p>0: Disabled</p> <p>1: Enabled</p> <p>Any other settings are prohibited.</p>

[PICT_CTRL]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB2F4	1	7:0	WBSCE_N_CHG_DIVNU_M	R/W	U8.0	This register is used to set the number of parameter-change divisions when switching WB scenes.

[CTRL1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1C4D	1	1:0	IR_OP_OIF_AWB_MSK_SEL	R/W	U2.0	<p>This register is used to set the Light Metering Region Mask function (AWB)</p> <p>0: No light metering masking is used.</p> <p>1: Only elliptical masking is used.</p> <p>2: Only rectangular masking is used.</p> <p>3: Both elliptical and rectangular masking are used.</p>

5.3.4.2. Output Registers

Table 5-43 Output Registers for the White Balance Function

[AWB_COM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x6594	1	7:0	AWBMODE_COM	R	U8.0	This register indicates the method for white balance. 0x0: ATW 0x1: All Pull-in 0x2: User preset 0x3: Full MWB 0x4: Hold
0x6595	1	7:0	AWBSTS	R	U8.0	This register is used to confirm the AWB state. 0: Before operation 1: Pull-in operation during power-up in progress. 2: Convergence state (stop state) 3: Pull-in operation in progress (close to the target value) 4: Pull-in operation in progress 5: Operation Area error 7: Error in the settings of the Operation Area or Aim Area 8: Error in the settings of the area, in which the user changes both red and blue at the same time for a pull-in operation. 9: Error in a correlation between the Operation and Aim Areas
0x6596	2	8:0	AWB_HVALID_BUF	R	U9.0	This register indicates the width of one cell in the AWB light metering window.
0x6598	2	8:0	AWB_VVALID_BUF	R	U9.0	This register indicates the height of one cell in the AWB light metering window.
0x659A	2	11:0	WBGAIN_R	R	U4.8	This register indicates the white balance gain. (For the R pixels)
0x659C	2	11:0	WBGAIN_B	R	U4.8	This register indicates the white balance gain. (For the B pixels)
0x659E	2	11:0	WBGAIN_G	R	U4.8	This register indicates the white balance gain. (For the G pixels) This register indicates the average values of the GR and GB pixels.
0x65A0	2	11:0	WBGAIN_GR	R	U4.8	This register indicates the white balance gain. (For the GR pixels)
0x65A2	2	11:0	WBGAIN_GB	R	U4.8	This register indicates the white balance gain. (For the GB pixels)
0x65A4	2	15:0	CONT_R	R	U16.0	This register indicates an output value. (For the R/G coordinate)
0x65A6	2	15:0	CONT_B	R	U16.0	This register indicates an output value. (For the B/G coordinate)
0x65A8	2	15:0	RATIO_R	R	U16.0	This register indicates the normalized current value. (For the R/G coordinate)
0x65AA	2	15:0	RATIO_B	R	U16.0	This register indicates the normalized current value. (For the B/G coordinate)
0x65AC	2	15:0	AIM_R	R	U16.0	This register indicates the target value. (For the R/G coordinate)
0x65AE	2	15:0	AIM_B	R	U16.0	This register indicates the target value. (For the B/G coordinate)
0x65C0	1	0	AWB_DATASAVE_ERR_P REWB	R	U1.0	This register indicates the error output of external memory recording during the pre-white balance adjustment. 0x0: No errors 0x1: Error detected

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
		1	WBSCENE_NUM	R	U1.0	This register indicates the result of the WB scene determination by the sensor. 0x0: WS0 0x1: WS1
0x65D0	1	7:0	FRMIN_NUM	R	U8.0	This register indicates the number of Ratio points within the Operation Area.

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5.4. Clamp Function

5.4.1. Functional Purpose

By matching the black level of the captured image to the 0 level during signal processing, the sensor can prevent coloring during white balance compensation or coloring in composite regions during HDR imaging.

5.4.2. Functional Overview

The Clamp function adds or subtracts the black level offset value so that the black level approaches 0. The sensor's Clamp function consists of the Analog Clamp function and Digital Clamp function. **“Figure 1-2”** shows the positions of the analog and digital Clamp functions as “Analog Clamp” and “Digital Clamp.” **“Table 5-44”** shows an overview of these two functions.

Table 5-44 Overview of the Analog Clamp and Digital Clamp Functions

Function	Description
Analog Clamp	<p>The Analog Clamp function converges the signal levels after A/D conversion closer to the black level.</p> <p>The sensor performs the Analog Clamp function by calculating the black level information of the preceding frame and the current frame. For this reason, the host cannot adjust this function.</p>
Digital Clamp	<p>The Digital Clamp function adjusts the black level for the signals after analog clamping.</p> <p>The sensor subtracts the following values as the black level's offset values from the Active Area (Analog Crop) and OB Area:</p> <ul style="list-style-type: none"> • The average value of pixel levels in the Sensor Clamp Area • IIR-calculated value of the average pixel levels in the Sensor Clamp Area • The value calculated by the sensor corresponding to temperature, gain and shutter time. • Values specified by the host

5.4.3. Functional Specifications

5.4.3.1. Relationship between the Digital Clamp Function and the OB Area

In the OB Area as described in the IMX623-AA** “Data Sheet,” there are two types of areas as listed in **“Table 5-45.”** In this document, the area with 4 lines is referred to as the OB Area and the area with 26 lines is referred to as the Sensor Clamp Area. See **“Figure 5-45”** for details.

Table 5-45 The OB Area and the Sensor Clamp Area

Name in the IMX623-AA** Data Sheet	Name in This Manual	Number of Lines
Vertical effective OB	OB Area	4
Optical black area (The sensor's internal use only)	Sensor Clamp Area	26

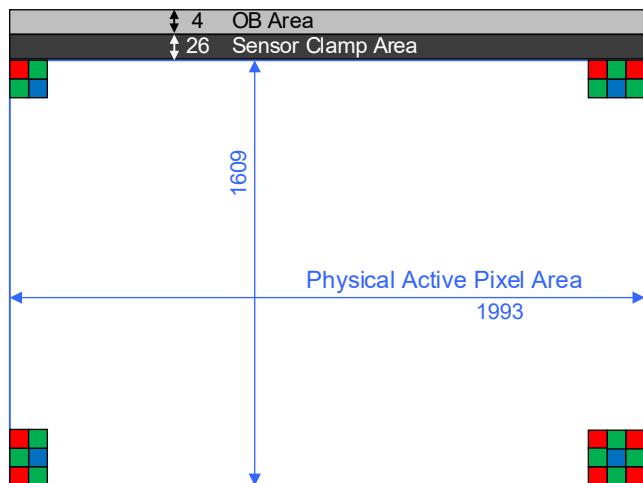


Figure 5-45 The Sensor's OB Area

As described in "**2.4.6 MIPI CSI-2 Frame Structure**," the pixel data of the OB area is transmitted via MIPI CSI-2.

The pixel level information of the Sensor Clamp Area is used to generate the OB information to be transmitted to the Front Embedded Data.

5.4.3.2. Digital Clamp Function

"Figure 5-46" illustrates an overview of the Digital Clamp function.

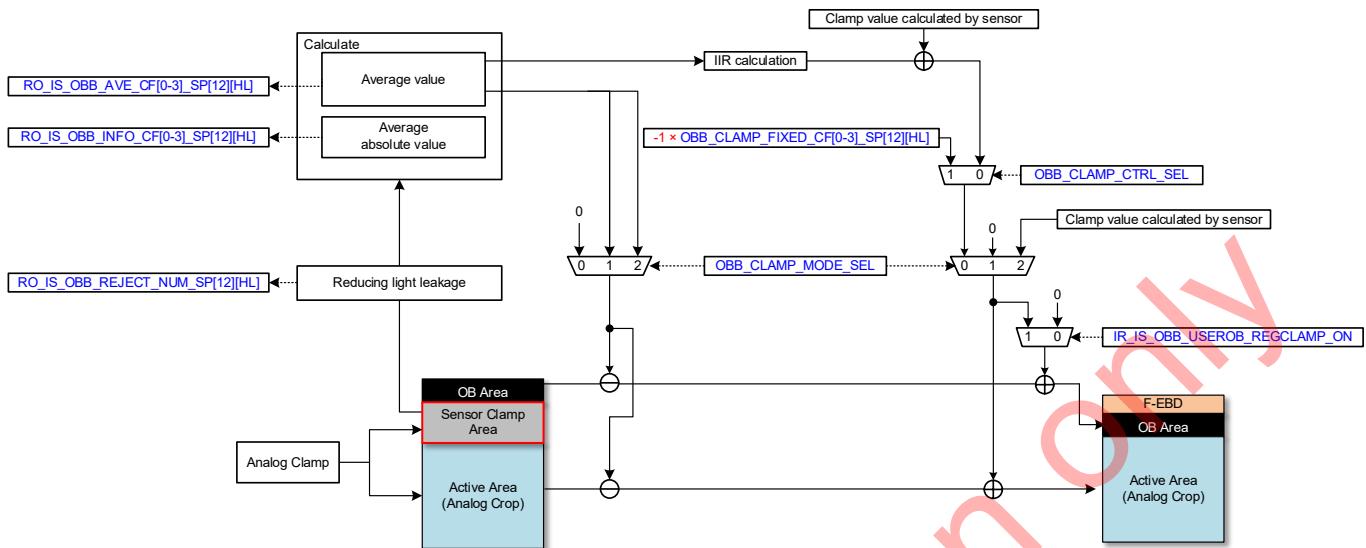


Figure 5-46 Overview of the Digital Clamp Function

■ Sensor clamp value

The Digital Clamp function reads out the pixels in the Sensor Clamp Area (the red box in "Figure 5-46"), which is a light-shielded physical pixel area. The pixels in the Sensor Clamp Area are the data after the black level has been compensated for by the Analog Clamp function. After having taken measures against light leakage into the Sensor Clamp Area, which will be described later in this document, the sensor calculates the average value of the pixel levels in the Sensor Clamp Area.

When the OBB_CLAMP_MODE_SEL register is set to 1 or 2, the sensor subtracts the average of the pixel levels in the Sensor Clamp Area as the black level's offset values from the Active Area (Analog Crop) and OB Area.

■ User clamp value

The sensor can add the values (A) and (B), which are listed as the user clamp values below, as the black level's offset values:

- (A): The value obtained by performing IIR calculation on the sensor clamp value. See "IIR Calculation" in "Figure 5-46."
- (B): The value calculated by the sensor corresponding to temperature, gain and shutter time. See "Clamp value calculated by sensor" in "Figure 5-46."
- (C): The value assigned to the OBB_CLAMP_FIXED_x_y (x = CF0, CF1, CF2, CF3)(y = SP1H, SP1L, SP2H, SP2L) registers.

"Table 5-46" shows the conditions that determine which value is set as the clamp value.

Table 5-46 Conditions That Determine Which Value Is Set as the Clamp Value

OBB_CLAMP_MODE_SEL	OBB_CLAMP_CTRL_SEL	Clamp Value
0	0	(A) + (B)
	1	(C)
1	-	Sensor clamp value
2	-	Sensor clamp value + (B)

When adding or subtracting the user clamp value to the pixels in the OB Area, set the IR_IS_OBB_USEROB_REGCLAMP_ON register to 1.

◇ **Memo**

- The Sensor Clamp Area is used by the Clamp function only.
- Regarding the value of each of the OBB_CLAMP_FIXED_x_y ($x = CF0, CF1, CF2, CF3$) ($y = SP1H, SP1L, SP2H, SP2L$) registers, setting a positive value decreases the signal level of the output image whereas setting a negative value increases the level.

5.4.3.2.1. Concerning Light Leakage into the Sensor Clamp Area

Should light leakage into the Sensor Clamp Area occur due to extremely bright light entering the sensor, the Digital Clamp function may not properly calculate offset values. To reduce light leakage into the Sensor Clamp Area, the sensor excludes the pixels in the Sensor Clamp Area which exceed thresholds when calculating the following values:

- The average value of pixel levels in the Sensor Clamp Area
- The average value of the absolute values of the pixel levels in the Sensor Clamp Area

The host can check the number of pixels excluded from the calculations using the Front Embedded Data and specific registers. For details, refer to "[5.4.3.2.3 Pixel Level Information in the Sensor Clamp Area](#)."

The sensor addresses light leakage into only the pixels in the Sensor Clamp Area. In other words, the OB Area and Active Area are not addressed.

5.4.3.2.2. Calculating the Average Value and the Average Absolute Values of the Pixel Levels in the Sensor Clamp Area

Regarding the pixels in the Sensor Clamp Area, which are used to calculate the average value of the pixel levels, the sensor first performs the following processing to calculate the average value:

- The sensor clips the pixels in the Sensor Clamp Area with a precision of S10.0.
- The sensor excludes the pixels exceeding the threshold as previously calculated based on light leakage into pixels in the Sensor Clamp Area. For details, refer to "[5.4.3.2.1 Concerning Light Leakage into the Sensor Clamp Area](#)."

The sensor calculates the following two types of values of the pixels, on which the sensor performs the aforementioned processing: values obtained by performing absolute-value conversion and those obtained without performing absolute-value conversion. Then, the sensor integrates these values for each line and for each color filter.

Following this, the sensor divides the integrated values by the number of pixels that can be obtained through integration so that the average value of the pixel level has a precision of S10.6.

The host can check the average value and the absolute average value of the pixel levels using the Front Embedded Data and the specific registers. Regarding the output information at this time, the average value of the calculated pixel levels has a precision of S10.5 and the average absolute value of the pixel levels has a precision of U10.5. Therefore, the sensor converts the calculated average values to meet the output precisions by rounding these values.

5.4.3.2.3. Pixel Level Information in the Sensor Clamp Area

The sensor transmits the pixel level information about the Sensor Clamp Area using the Front Embedded Data or relevant registers. The pixel level information about the Sensor Clamp Area, which is transmitted by the sensor, is the information that has been processed as described in “[5.4.3.2.1 Concerning Light Leakage into the Sensor Clamp Area](#).” “[Table 5-47](#)” shows this pixel level information.

Table 5-47 The Pixel Level Information of the Sensor Clamp Area

Pixel Level Information in the Sensor Clamp Area	Register Name	Front Embedded Data
Average value	RO_IS_OBB_AVE_x_y (x = CF0, CF1, CF2, CF3) (y = SP1H, SP1L, SP2H, SP2L)	“6.9.3.5.26 OB Information”
Average value of absolute values	RO_IS_OBB_INFO_x_y (x = CF0, CF1, CF2, CF3) (y = SP1H, SP1L, SP2H, SP2L)	
The number of pixels excluded from the Clamp function's calculations	RO_IS_OBB_REJECT_NUM_x (x = SP1H, SP1L, SP2H, SP2L)	

5.4.4. Interface

5.4.4.1. Input Registers

Table 5-48 Input Registers for the Clamp Function

[PICT_OB]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB45E	2	15:0	OBB_CLAMP_FIXED_CF0_SP1H	R/W	S10.5	SP1_HCG's black level offset for CF0 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB460	2	15:0	OBB_CLAMP_FIXED_CF1_SP1H	R/W	S10.5	SP1_HCG's black level offset for CF1 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB462	2	15:0	OBB_CLAMP_FIXED_CF2_SP1H	R/W	S10.5	SP1_HCG's black level offset for CF2 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB464	2	15:0	OBB_CLAMP_FIXED_CF3_SP1H	R/W	S10.5	SP1_HCG's black level offset for CF3 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB466	2	15:0	OBB_CLAMP_FIXED_CF0_SP1L	R/W	S10.5	SP1_LCG's black level offset for CF0 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB468	2	15:0	OBB_CLAMP_FIXED_CF1_SP1L	R/W	S10.5	SP1_LCG's black level offset for CF1 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB46A	2	15:0	OBB_CLAMP_FIXED_CF2_SP1L	R/W	S10.5	SP1_LCG's black level offset for CF2 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB46C	2	15:0	OBB_CLAMP_FIXED_CF3_SP1L	R/W	S10.5	SP1_LCG's black level offset for CF3 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB46E	2	15:0	OBB_CLAMP_FIXED_CF0_SP2H	R/W	S10.5	SP2H's black level offset for CF0 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB470	2	15:0	OBB_CLAMP_FIXED_CF1_SP2H	R/W	S10.5	SP2H's black level offset for CF1 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB472	2	15:0	OBB_CLAMP_FIXED_CF2_SP2H	R/W	S10.5	SP2H's black level offset for CF2 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB474	2	15:0	OBB_CLAMP_FIXED_CF3_SP2H	R/W	S10.5	SP2H's black level offset for CF3 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB476	2	15:0	OBB_CLAMP_FIXED_CF0_SP2L	R/W	S10.5	SP2L's black level offset for CF0 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB478	2	15:0	OBB_CLAMP_FIXED_CF1_SP2L	R/W	S10.5	SP2L's black level offset for CF1 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB47A	2	15:0	OBB_CLAMP_FIXED_CF2_SP2L	R/W	S10.5	SP2L's black level offset for CF2 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB47C	2	15:0	OBB_CLAMP_FIXED_CF3_SP2L	R/W	S10.5	SP2L's black level offset for CF3 when the value of the OBB_CLAMP_CTRL_SEL is set to 1
0xB488	1	1:0	OBB_CLAMP_MODE_SEL	R/W	U2.0	This register is used to set the clamp mode. 0: User clamp 1: Sensor clamp 2: Sensor clamp + user clamp 3: User clamp (equivalent to 0)

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB489	1	0	OBB_CLAMP_CTRL_SEL	R/W	U1.0	This register is used to specify the offset value of the black level. 0: The value calculated by the sensor is applied. 1: The value set by the host is applied.

[CONST1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x01D8	1	0	IR_IS_OBB_USEROB_REG CLAMP_ON	R/W	U1.0	This register is used to enable or disable the addition/subtraction of an offset value for the OB Area. 0: Disabled 1: Enabled

5.4.4.2. Output Registers

Table 5-49 Output Registers for the Clamp Function

[STATE]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1F60	2	15:0	RO_IS_OBB_REJECT_NUM_SP1H	R	U16.0	This register indicates the number of pixels in the SP1_HCG's Sensor Clamp Area excluded from the Digital Clamp function's calculations.
0x1F62	2	15:0	RO_IS_OBB_REJECT_NUM_SP1L	R	U16.0	This register indicates the number of pixels in the SP1_LCG's Sensor Clamp Area excluded from the Digital Clamp function's calculations.
0x1F64	2	15:0	RO_IS_OBB_REJECT_NUM_SP2H	R	U16.0	This register indicates the number of pixels in the SP2H's Sensor Clamp Area excluded from the Digital Clamp function's calculations.
0x1F66	2	15:0	RO_IS_OBB_REJECT_NUM_SP2L	R	U16.0	This register indicates the number of pixels in the SP2L's Sensor Clamp Area excluded from the Digital Clamp function's calculations.
0x1F68	2	14:0	RO_IS_OBB_INFO_CF0_SP1H	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_HCG and CF0)
0x1F6A	2	14:0	RO_IS_OBB_INFO_CF1_SP1H	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_HCG and CF1)
0x1F6C	2	14:0	RO_IS_OBB_INFO_CF2_SP1H	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_HCG and CF2)
0x1F6E	2	14:0	RO_IS_OBB_INFO_CF3_SP1H	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_HCG and CF3)
0x1F70	2	14:0	RO_IS_OBB_INFO_CF0_SP1L	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_LCG and CF0)
0x1F72	2	14:0	RO_IS_OBB_INFO_CF1_SP1L	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_LCG and CF1)
0x1F74	2	14:0	RO_IS_OBB_INFO_CF2_SP1L	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_LCG and CF2)
0x1F76	2	14:0	RO_IS_OBB_INFO_CF3_SP1L	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_LCG and CF3)
0x1F78	2	14:0	RO_IS_OBB_INFO_CF0_SP2H	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2H and CF0)
0x1F7A	2	14:0	RO_IS_OBB_INFO_CF1_SP2H	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2H and CF1)

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1F7C	2	14:0	RO_IS_OBB_INFO_CF2_SP2H	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2H and CF2)
0x1F7E	2	14:0	RO_IS_OBB_INFO_CF3_SP2H	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2H and CF3)
0x1F80	2	14:0	RO_IS_OBB_INFO_CF0_SP2L	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2L and CF0)
0x1F82	2	14:0	RO_IS_OBB_INFO_CF1_SP2L	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2L and CF1)
0x1F84	2	14:0	RO_IS_OBB_INFO_CF2_SP2L	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2L and CF2)
0x1F86	2	14:0	RO_IS_OBB_INFO_CF3_SP2L	R	U10.5	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2L and CF3)
0x1F88	2	15:0	RO_IS_OBB_AVE_CF0_SP1H	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP1_HCG and CF0)
0x1F8A	2	15:0	RO_IS_OBB_AVE_CF1_SP1H	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP1_HCG and CF1)
0x1F8C	2	15:0	RO_IS_OBB_AVE_CF2_SP1H	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP1_HCG and CF2)
0x1F8E	2	15:0	RO_IS_OBB_AVE_CF3_SP1H	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP1_HCG and CF3)
0x1F90	2	15:0	RO_IS_OBB_AVE_CF0_SP1L	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP1_LCG and CF0)
0x1F92	2	15:0	RO_IS_OBB_AVE_CF1_SP1L	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP1_LCG and CF1)
0x1F94	2	15:0	RO_IS_OBB_AVE_CF2_SP1L	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP1_LCG and CF2)
0x1F96	2	15:0	RO_IS_OBB_AVE_CF3_SP1L	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP1_LCG and CF3)
0x1F98	2	15:0	RO_IS_OBB_AVE_CF0_SP2H	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP2H and CF0)
0x1F9A	2	15:0	RO_IS_OBB_AVE_CF1_SP2H	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP2H and CF1)
0x1F9C	2	15:0	RO_IS_OBB_AVE_CF2_SP2H	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP2H and CF2)
0x1F9E	2	15:0	RO_IS_OBB_AVE_CF3_SP2H	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP2H and CF3)
0x1FA0	2	15:0	RO_IS_OBB_AVE_CF0_SP2L	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP2L and CF0)
0x1FA2	2	15:0	RO_IS_OBB_AVE_CF1_SP2L	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP2L and CF1)
0x1FA4	2	15:0	RO_IS_OBB_AVE_CF2_SP2L	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP2L and CF2)
0x1FA6	2	15:0	RO_IS_OBB_AVE_CF3_SP2L	R	S10.5	The average value of pixel levels in the Sensor Clamp Area (SP2L and CF3)

5.5. RAW Noise Reduction Function

5.5.1. Functional Purpose

The RAW Noise Reduction function reduces noise in each sub-pixel.

5.5.2. Functional Overview

The RAW Noise Reduction (RAW-NR) function reduces noise in RAW signals for each signal line (SP1_HCG, SP1_LCG, SP2H and SP2L). These RAW signals are then processed for HDR imaging.

“Figure 5-47” illustrates an overview of the RAW Noise Reduction (RAW-NR) function. The user can make simple adjustments to “Detection Sensitivity” and “Compensation Level,” both of which are calculated by the sensor using the Noise Reduction function.

- Detection sensitivity

The detection sensitivity indicates the noise detection level from each line’s signal (image). Although increasing the detection sensitivity increases the detection rate of the noise component, even the texture and edge components are detected as noise as well. Conversely, decreasing the detection sensitivity keeps the texture and edge components while the noise component detection rate decreases.

- Noise reduction level

When a component is identified as noise, the noise reduction level indicates the level, by which such a component is removed. The lower the level, the lower the reduction. Conversely, the higher the level, the higher the reduction.

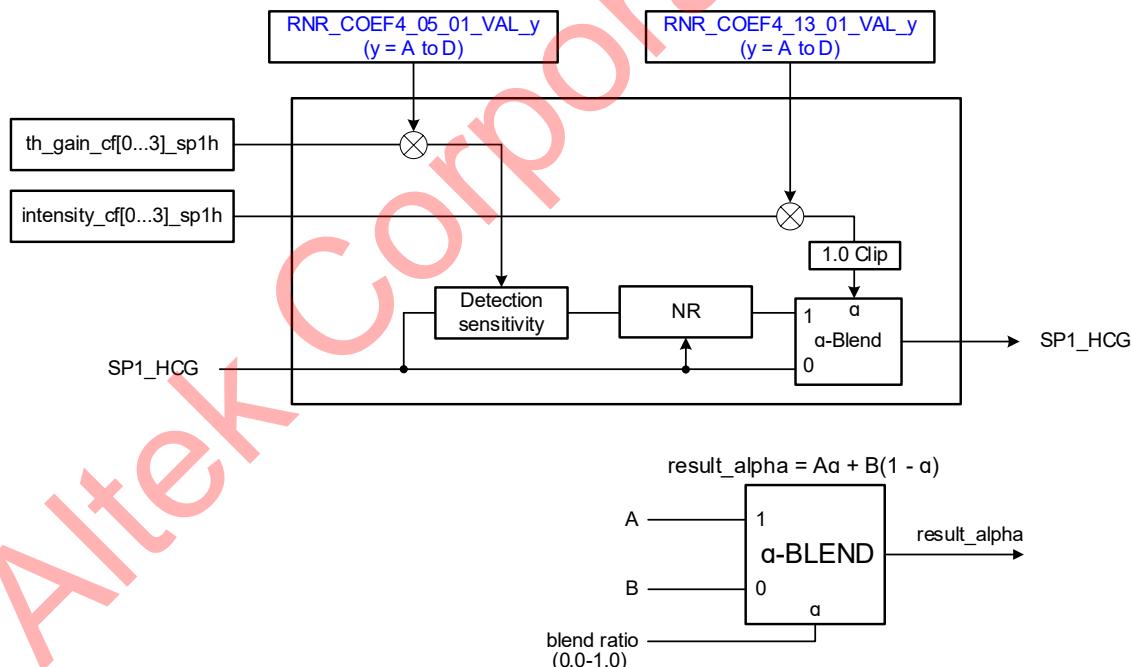


Figure 5-47 Overview of the RAW Noise Reduction (RAW-NR) Function in the Case of SP1_HCG

“Figure 5-47” applies to the SP1_LCG, SP2H, and SP2L lines as well as SP1_HCG. The Noise Reduction function is not operational for the OB Area.

5.5.3. Functional Specifications

5.5.3.1. Enabling or Disabling the RAW Noise Reduction (RAW-NR) Function

To enable or disable this function, set the IR_IS_RNR_ON register to 1 or 0 respectively.

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5.5.3.2. Configuring the Settings for the RAW-NR Function Corresponding to the Interlocking Type

RAW-NR is a function that reduces noise from RAW images by setting adjustment gains for the detection sensitivity and the reduction level corresponding to the illuminance. Configure the settings for this function using the registers in "Table 5-50."

Table 5-50 Registers for RAW-NR and Illuminance Interlocking

Register Used to Set the Interlocking Type	Settings	Registers for the Settings
RNR_COEF4_01_IL_TYPE_SEL	Detection sensitivity adjustment gain (SP1_HCG)	RNR_COEF4_05_01_VAL_y (y = A to D)
	Detection sensitivity adjustment gain (SP1_LCG)	RNR_COEF4_06_01_VAL_y (y = A to D)
	Detection sensitivity adjustment gain (SP2H)	RNR_COEF4_07_01_VAL_y (y = A to D)
	Detection sensitivity adjustment gain (SP2L)	RNR_COEF4_08_01_VAL_y (y = A to D)
	Noise reduction level adjustment gain (SP1_HCG)	RNR_COEF4_13_01_VAL_y (y = A to D)
	Noise reduction level adjustment gain (SP1_LCG)	RNR_COEF4_14_01_VAL_y (y = A to D)
	Noise reduction level adjustment gain (SP2H)	RNR_COEF4_15_01_VAL_y (y = A to D)
	Noise reduction level adjustment gain (SP2L)	RNR_COEF4_16_01_VAL_y (y = A to D)

"Figure 5-48" illustrates an example of how to set the noise reduction adjustment gain. The higher the noise reduction adjustment gain value, the higher the gains or the detection sensitivity or the reduction level, and vice versa.

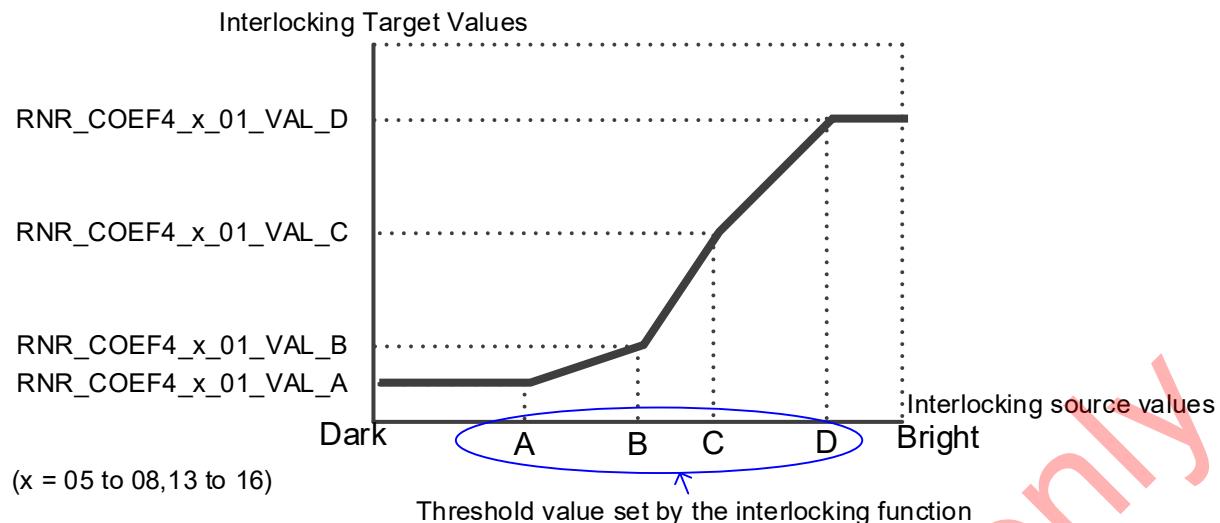


Figure 5-48 Example of Setting Adjustment-Related Gains

For details regarding illuminance interlocking, refer to "[6.6 Interlocking Control Function](#)".

5.5.3.2.1. Adjusting the Detection Sensitivity of the RAW-NR Function

Within the sensor, the detection sensitivity ($\text{th_gain_cf}[0..3]_x$ = sp1h, sp1l, sp2h, sp2l) is calculated for all four color filters of the SP1_HCG, SP1_LCG, SP2H, and SP2L lines. With the RAW-NR function, the detection sensitivity can be adjusted using the $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 05$ to 08) ($y = A$ to D) registers. The value of each of the $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 05$ to 08) ($y = A$ to D) registers is commonly applied to all color filters.

If the detection sensitivity calculated by the sensor is low, the effect of this function might not be able to be confirmed by adjusting the $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 05$ to 08) ($y = A$ to D) registers. Also, when $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 05$ to 08) ($y = A$ to D) registers are set to $0x0$, the RAW-NR function is effectively disabled. When the host does not need to make any adjustments, set $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 05$ to 08) ($y = A$ to D) registers to $0x40$.

5.5.3.2.2. Adjusting the Noise Reduction Level of the RAW-NR Function

The sensor calculates the noise reduction level (intensity_cf[0..3]_x, $x = \text{sp1h}, \text{sp1l}, \text{sp2h}, \text{sp2l}$) for all four color filters of the SP1_HCG, SP1_LCG, SP2H, and SP2L lines. With the RAW-NR function, the noise reduction level can be adjusted using the $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 13$ to 16) ($y = A$ to D) registers. The value of each of the $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 13$ to 16) ($y = A$ to D) registers is commonly applied to all color filters.

If the noise reduction level calculated by the sensor is low, the effect of this function might not be able to be confirmed by adjusting the $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 13$ to 16) ($y = A$ to D) registers. Alternatively, when the noise reduction level is 1.0 or approximately 1.0, even when any adjustment using the $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 13$ to 16) ($y = A$ to D) registers is made, adjustment effects may not be confirmed because the level is clipped at 1.0. Also, when the $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 13$ to 16) ($y = A$ to D) registers are set to $0x0$, the RAW-NR function is effectively disabled. When the host does not need to make any adjustments, set $\text{RNR_COEF4}_x_01_\text{VAL}_y$ ($x = 13$ to 16) ($y = A$ to D) registers to $0x40$.

5.5.4. Interface

5.5.4.1. Input Registers

Table 5-51 Input Registers for the RAW Noise Reduction Function

[CTRL1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1AF4	1	0	IR_IS_RNR_ON	R/W	U1.0	This register is used to enable or disable the RAW Noise Reduction function. 0: Disabled 1: Enabled

[PICT_RAWNR]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB684	1	7:0	RNR_COEF4_01_IL_TYPE_SEL	R/W	U8.0	This register is used to set illuminance interlocking for Group 01 (RAW-NR detection sensitivity and the adjustment gain for the noise reduction level) Setting of the interlocking type "the interlocking target and interlocking point"
0xB8F6	1	7:0	RNR_COEF4_05_01_VAL_A	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP1_HCG. Illuminance interlocking: Group 01 and Point A
0xB8F7	1	7:0	RNR_COEF4_05_01_VAL_B	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP1_HCG. Illuminance interlocking: Group 01 and Point B
0xB8F8	1	7:0	RNR_COEF4_05_01_VAL_C	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP1_HCG. Illuminance interlocking: Group 01 and Point C
0xB8F9	1	7:0	RNR_COEF4_05_01_VAL_D	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP1_HCG. Illuminance interlocking: Group 01 and Point D
0xB8FA	1	7:0	RNR_COEF4_06_01_VAL_A	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP1_LCG. Illuminance interlocking: Group 01 and Point A
0xB8FB	1	7:0	RNR_COEF4_06_01_VAL_B	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP1_LCG. Illuminance interlocking: Group 01 and Point B
0xB8FC	1	7:0	RNR_COEF4_06_01_VAL_C	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP1_LCG. Illuminance interlocking: Group 01 and Point C
0xB8FD	1	7:0	RNR_COEF4_06_01_VAL_D	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP1_LCG. Illuminance interlocking: Group 01 and Point D

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB8FE	1	7:0	RNR_COEF4_07_01_VAL_A	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP2H. Illuminance interlocking: Group 01 and Point A
0xB8FF	1	7:0	RNR_COEF4_07_01_VAL_B	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP2H. Illuminance interlocking: Group 01 and Point B
0xB900	1	7:0	RNR_COEF4_07_01_VAL_C	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP2H. Illuminance interlocking: Group 01 and Point C
0xB901	1	7:0	RNR_COEF4_07_01_VAL_D	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP2H. Illuminance interlocking: Group 01 and Point D
0xB902	1	7:0	RNR_COEF4_08_01_VAL_A	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP2L. Illuminance interlocking: Group 01 and Point A
0xB903	1	7:0	RNR_COEF4_08_01_VAL_B	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP2L. Illuminance interlocking: Group 01 and Point B
0xB904	1	7:0	RNR_COEF4_08_01_VAL_C	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP2L. Illuminance interlocking: Group 01 and Point C
0xB905	1	7:0	RNR_COEF4_08_01_VAL_D	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR detection sensitivity of SP2L. Illuminance interlocking: Group 01 and Point D
0xB916	1	7:0	RNR_COEF4_13_01_VAL_A	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP1_HCG. Illuminance interlocking: Group 01 and Point A
0xB917	1	7:0	RNR_COEF4_13_01_VAL_B	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP1_HCG. Illuminance interlocking: Group 01 and Point B
0xB918	1	7:0	RNR_COEF4_13_01_VAL_C	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP1_HCG. Illuminance interlocking: Group 01 and Point C
0xB919	1	7:0	RNR_COEF4_13_01_VAL_D	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP1_HCG. Illuminance interlocking: Group 01 and Point D
0xB91A	1	7:0	RNR_COEF4_14_01_VAL_A	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP1_LCG. Illuminance interlocking: Group 01 and Point A

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB91B	1	7:0	RNR_COEF4_14_01_VAL_B	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP1_LCG. Illuminance interlocking: Group 01 and Point B
0xB91C	1	7:0	RNR_COEF4_14_01_VAL_C	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP1_LCG. Illuminance interlocking: Group 01 and Point C
0xB91D	1	7:0	RNR_COEF4_14_01_VAL_D	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP1_LCG. Illuminance interlocking: Group 01 and Point D
0xB91E	1	7:0	RNR_COEF4_15_01_VAL_A	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP2H. Illuminance interlocking: Group 01 and Point A
0xB91F	1	7:0	RNR_COEF4_15_01_VAL_B	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP2H. Illuminance interlocking: Group 01 and Point B
0xB920	1	7:0	RNR_COEF4_15_01_VAL_C	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP2H. Illuminance interlocking: Group 01 and Point C
0xB921	1	7:0	RNR_COEF4_15_01_VAL_D	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP2H. Illuminance interlocking: Group 01 and Point D
0xB922	1	7:0	RNR_COEF4_16_01_VAL_A	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP2L. Illuminance interlocking: Group 01 and Point A
0xB923	1	7:0	RNR_COEF4_16_01_VAL_B	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP2L. Illuminance interlocking: Group 01 and Point B
0xB924	1	7:0	RNR_COEF4_16_01_VAL_C	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP2L. Illuminance interlocking: Group 01 and Point C
0xB925	1	7:0	RNR_COEF4_16_01_VAL_D	R/W	U2.6	This register is used to set the adjustment gain for the RAW-NR level of SP2L. Illuminance interlocking: Group 01 and Point D

5.6. Spot Pixel Compensation Function

5.6.1. Functional Purpose

In the absence of light, some pixels may appear brighter than their surrounding pixels. Conversely, under uniform light, some pixels may appear darker than their surrounding pixels. The Spot Pixel Compensation function compensates for these pixels using the information of their adjacent, same-colored pixels.

5.6.2. Functional Overview

The sensor has two Spot Pixel Compensation functions: Static and Dynamic. This function uses the factory-default spot pixel coordinates stored in the OTP to compensate for spot pixels. This function detects and compensates for spot pixels frame by frame.

5.6.3. Functional Specifications

5.6.3.1. Static Spot Pixel Compensation

The Static Spot Pixel Compensation function uses the default compensation position coordinates in the OTP ROM.

5.6.3.1.1. Enabling or Disabling Static Spot Pixel Compensation

As shown in “**Table 5-52**,” the Static Spot Pixel Compensation function can be disabled for all signal lines simultaneously. Alternatively, this function can be enabled or disabled individually for each line.

Table 5-52 Enabling or Disabling Static Spot Pixel Compensation

STC_ON	STC_ON_x	Description
0	Don't Care	Static spot pixel compensation is disabled.
1	0	Static spot pixel compensation for the x signal line is disabled.
	1	Static spot pixel compensation for the x signal line is enabled.

* x represents SP1H, SP1L, SP2H or SP2L to be used. For example, the STC_ON_SP1H register is used to enable or disable spot pixel compensation for the SP1_HCG line.

5.6.3.1.2. Change in the Compensation Positions of Static Spot Pixel Compensation

The sensor controls static spot pixel compensation by interlocking this with the Optical Center Compensation function and the Horizontal/Vertical Flip function. For details, refer to “[6.2 Optical Center Compensation Function](#)” and “[6.3 Horizontal/Vertical Flip Function](#).” Even when changing the settings of the Optical Center Compensation and Horizontal/Vertical Flip functions by using the registers in “[Table 5-53](#),” it is not necessary for the host to set the compensation position of the spot pixels again.

Table 5-53 Registers for the Position of Spot Pixels, Each Value of Which Is Updated by the Sensor When the Sensor Changes the Settings

Register Name	Function Name
WND_SHIFT_H_	“6.2 Optical Center Compensation Function”
WND_SHIFT_V_	“6.3 Horizontal/Vertical Flip Function”
H_REVERSE_	
V_REVERSE_	

The registers in “[Table 5-53](#)” are compatible with the Application Lock function. For details, refer to “[3.1.5 Application Lock Function](#).”

5.6.3.1.3. The Origin of the Compensation Positions of Static Spot Pixel Compensation

The Static Spot Pixel Compensation function uses the coordinate information relative to the origin (0,0) in the Physical Active Pixel Area for spot pixel compensation. “[Figure 5-49](#)” illustrates the origin of the spot pixels’ coordinates in the Physical Active Pixel Area. This figure illustrates an example under the following conditions:

- 1936 x 1552 output
- Normal image orientation
- Values of the WND_SHIFT_H and WND_SHIFT_V registers used to compensate for the optical center are 0.

For details, refer to;

- [“6.2 Optical Center Compensation Function”](#)
- [“6.3 Horizontal/Vertical Flip Function”](#)
- The IMX623-AA** “Data Sheet” for the Physical Active Pixel Area

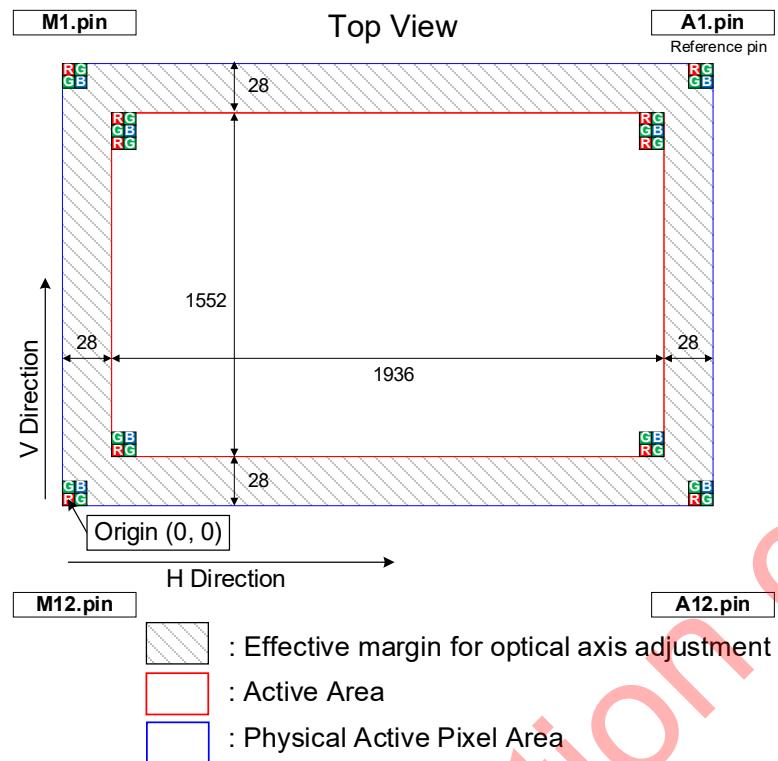


Figure 5-49 The Origin of the Spot Pixels' Coordinates (Example in Cases of Disabled Optical Center Compensation, 1936 x 1552 Output and Normal Orientation)

5.6.3.1.4. Reading Out the Compensation Position(s) of Spot Pixels

At the time of shipment, the sensor contains up to 1024 spot pixels' H and V coordinates in the OTP area with reference to the origin (0,0) to be used for static spot pixel compensation.

The coordinate information for the spot pixels have been stored in the order: SP1 then SP2.

When checking the coordinate information about SP2, start with the register with the number of SP1's registrations added as an offset.

■ Coordinates of spot pixels

The number of spot pixels recorded in the OTP ROM can be checked using the registers as follows:

- V coordinate: STC OTP ADR_Vx (x = 0 to 1023) registers
- H coordinate: STC OTP ADR_Hx (x = 0 to 1023) registers

■ The number of recorded spot pixels

The number of spot pixels stored in the OTP ROM can be checked using the following registers:

- STC OTP_NUM_SP1 register for the number of SP1's spot pixels recorded in the OTP ROM
- STC OTP_NUM_SP2 register for the number of SP2's spot pixels recorded in the OTP ROM

◆ Note

When the sum of the SP1 and SP2 lines' spot pixels which have already been stored in the OTP ROM is less than 1024 pixels, the value of the coordinate-information registers with no coordinates stored, is 0.

◆ Memo

To compensate for any unrecorded spot pixels in the OTP ROM, up to 100 pixels can be additionally recorded. For details, refer to “[5.6.3.1.5 Additional Registration of Spot Pixel Compensation Position](#).”

■ Example of checking spot pixels of SP1 and SP2

When the number of the SP1 line's recorded spot pixels is 20 (STC OTP_NUM_SP1 = 20) and the SP2 line's is 30 (STC OTP_NUM_SP2 = 30),

- SP1's spot pixels
 - V coordinate: STC OTP ADR_V0 to STC OTP ADR_V19 registers
 - H coordinate: STC OTP ADR_H0 to STC OTP ADR_H19 registers
- SP2's spot pixels
 - V coordinate: STC OTP ADR_V20 to STC OTP ADR_V49 registers
 - H coordinate: STC OTP ADR_H20 to STC OTP ADR_H49 registers
- A register value is 0.
 - V coordinate: STC OTP ADR_V50 register or greater
 - H coordinate: STC OTP ADR_H50 register or greater

5.6.3.1.5. Additional Registration of Spot Pixel Compensation Position

In addition to the 1,024 spot pixels recorded in the OTP ROM, the sensor can record up to 100 coordinates of spot pixels. To record additional spot pixels, set the coordinate information based on the origin illustrated in “[Figure 5-49](#)” to the following registers in ascending order:

The same coordinates cannot be specified for the coordinate information of the spot pixels to be additionally recorded.

- STC_PIX_ADR_Vx (x = 0 to 99) registers: V coordinates for the additionally recorded spot pixels
- STC_PIX_ADR_Hx (x = 0 to 99) register: H coordinates for the additionally recorded spot pixels

After having completed recording the coordinate information of the spot pixels, set the number of the additionally-recorded spot pixels for each line to the following registers:

- STC_PIX_NUM_SP1 register: Number of the recorded spot pixels for SP1
- STC_PIX_NUM_SP2 register: Number of the recorded spot pixels for SP2

◇ Memo

To apply the changed value(s), write these values to the Serial NOR Flash device in accordance with the procedure as described in “[4.9.2 When Writing the Current Register Value\(s\) to the Serial NOR Flash Device](#).”

5.6.3.2. Dynamic Spot Pixel Compensation Function

The Dynamic Spot Pixel Compensation function performs detection and compensation when a pixel value is extremely large or small in comparison with the values of its adjacent pixels in the same frame. This function can compensate for the signals from all lines (SP1_HCG, SP1_LCG, SP2H and SP2L).

5.6.3.2.1. Enabling or Disabling the Dynamic Spot Pixel Compensation Function

To enable or disable this function, set the DYC_ON register to 1 or 0, respectively.

5.6.4. Interface

5.6.4.1. Input Registers

Table 5-54 Input Registers for the Spot Pixel Compensation Function

[PICT_STC]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB48C	1	0	STC_ON	R/W	U1.0	Enabling or Disabling Static Spot Pixel Compensation 0: Disabled 1: Enabled
		1	STC_ON_SP1H	R/W	U1.0	Enabling static spot pixel compensation for SP1_HCG 0: Disabled 1: Enabled
		2	STC_ON_SP1L	R/W	U1.0	Enabling static spot pixel compensation for SP1_LCG 0: Disabled 1: Enabled
		3	STC_ON_SP2H	R/W	U1.0	Enabling static spot pixel compensation for SP2H 0: Disabled 1: Enabled
		4	STC_ON_SP2L	R/W	U1.0	Enabling static spot pixel compensation for SP2L 0: Disabled 1: Enabled

[PICT_STC_PIX]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB494	2	10:0	STC_PIX_ADR_V0	R/W	U11.0	This register is used to set the vertical coordinate for the additionally-recorded spot pixel #00. (The address is shared between SP1 and SP2.)
0xB496	2	10:0	STC_PIX_ADR_H0	R/W	U11.0	This register is used to set the horizontal coordinate for the additionally-recorded spot pixel #00. (The address is shared between SP1 and SP2.)
0xB498	2	10:0	STC_PIX_ADR_V1	R/W	U11.0	This register is used to set the vertical coordinate for the additionally-recorded spot pixel #01. (The address is shared between SP1 and SP2.)
0xB49A	2	10:0	STC_PIX_ADR_H1	R/W	U11.0	This register is used to set the horizontal coordinate for the additionally-recorded spot pixel #01. (The address is shared between SP1 and SP2.)
...		
0xB620	2	10:0	STC_PIX_ADR_V99	R/W	U11.0	This register is used to set the vertical coordinate for the additionally-recorded spot pixel #99. (The address is shared between SP1 and SP2.)
0xB622	2	10:0	STC_PIX_ADR_H99	R/W	U11.0	This register is used to set the horizontal coordinate for the additionally-recorded spot pixel #99. (The address is shared between SP1 and SP2.)
0xB624	2	10:0	STC_PIX_NUM_SP1	R/W	U11.0	The number of SP1's spot pixels to be additionally recorded.
0xB626	2	10:0	STC_PIX_NUM_SP2	R/W	U11.0	The number of SP2's spot pixels to be additionally recorded.

[PICT_DYC]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB67D	1	0	DYC_ON	R/W	U1.0	This register is used to enable or disable the Dynamic Spot Pixel Compensation function. 0: Disabled 1: Enabled

5.6.4.2. Output Registers

Table 5-55 Output Registers for the Spot Pixel Compensation Function

[PICT_STC OTP COM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x6DC4	2	10:0	STC OTP ADR_V0	R	U11.0	The V coordinate for the additionally-recorded spot pixel #0000 in the OTP area. (The address is shared between SP1 and SP2.)
0x6DC6	2	10:0	STC OTP ADR_H0	R	U11.0	The H coordinate for the additionally-recorded spot pixel #0000 in the OTP area. (The address is shared between SP1 and SP2.)
0x6DC8	2	10:0	STC OTP ADR_V1	R	U11.0	The V coordinate for the additionally-recorded spot pixel #0001 in the OTP area. (The address is shared between SP1 and SP2.)
0x6DCA	2	10:0	STC OTP ADR_H1	R	U11.0	The H coordinate for the additionally-recorded spot pixel #0001 in the OTP area. (The address is shared between SP1 and SP2.)
...		
0x7DC0	2	10:0	STC OTP ADR_V1023	R	U11.0	The V coordinate for the additionally-recorded spot pixel #1023 in the OTP area. (The address is shared between SP1 and SP2.)
0x7DC2	2	10:0	STC OTP ADR_H1023	R	U11.0	The H coordinate for the additionally-recorded spot pixel #1023 in the OTP area. (The address is shared between SP1 and SP2.)
0x7DC4	2	10:0	STC OTP NUM_SP1	R	U11.0	The number of SP1's spot pixels recorded in the OTP area.
0x7DC6	2	10:0	STC OTP NUM_SP2	R	U11.0	The number of SP2's spot pixels recorded in the OTP area.

5.7. Dark Shading Compensation Function

5.7.1. Functional Purpose

The Dark Shading Compensation function compensates for dark shading that represents the deviations of the black level caused by uneven offsets on the sensor's surface.

5.7.2. Functional Overview

The Dark Shading Compensation function individually compensates for dark shading in four lines, SP1_HCG, SP1_LCG and SP2H, and SP2L.

- This function compensates for the signals from these lines and for each color filter.
- The Pixel Shading Compensation function performs compensation by using the compensation level, which has been set to 90 control points (Knot Points), as the reference. These Knot Points consist of 10 horizontal x 9 vertical points.
- When compensating for the black level, this function calculates the compensation levels for each pixel by using two-dimensional interpolation based on these Knot Points.

◇ **Memo**

The sensor controls the Dark Shading Compensation function by interlocking this function with the Horizontal/Vertical Flip function (Section “**6.3 Horizontal/Vertical Flip Function**”). Even when changing the settings of the Horizontal/Vertical Flip function, it is not necessary for the host to set the Knot Points again.

5.7.3. Functional Specifications

5.7.3.1. Knot Points

As illustrated in “**Figure 5-50**,” the Pixel Shading Compensation function calculates the compensation level by using 90 Knot Points, consisting of 10 horizontal x 9 vertical points, which have been set to the sensor’s surface.

◇ Memo

A Knot Point is located at the center of each Knot Area. Each Knot Area consists of 256 horizontal x 256 vertical pixels. Therefore, each Knot Point is located between the 128th and 129th pixels. The position of the Knot Areas is fixed in relation to the sensor’s surface area. The top left corner of the Physical Active Pixel Area (origin) is equivalent to the top left corner of Knot Area 11. The positional relationship between Knot Areas and the Physical Active Pixel Area does not change due to, for example, the settings of the Angle-of-View Adjustment function.

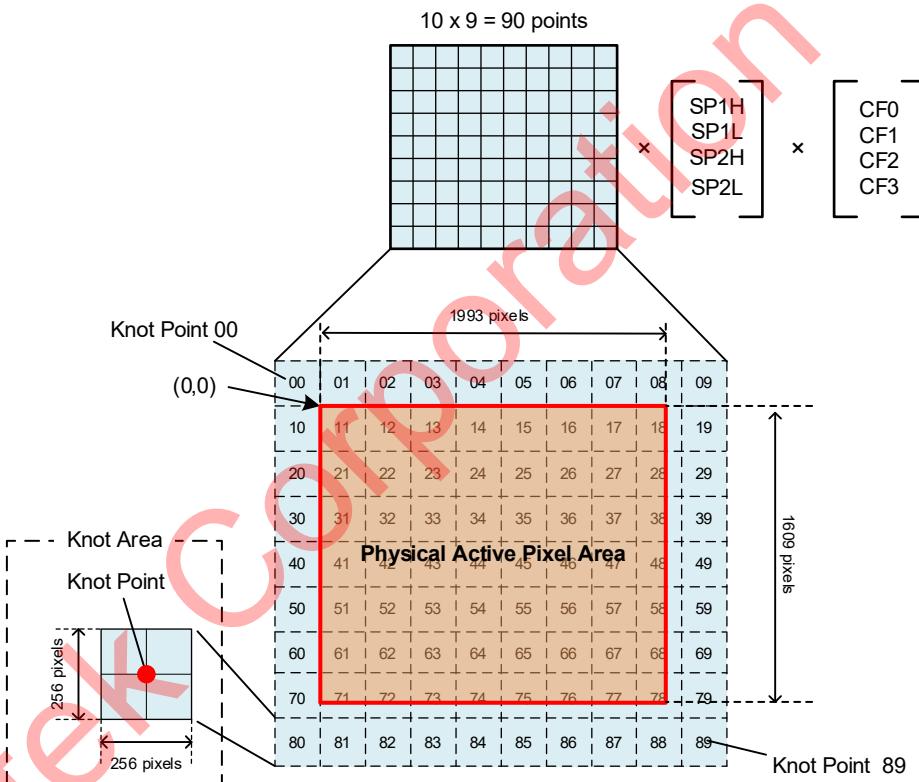


Figure 5-50 Knot Points for the Dark Shading Compensation Function

- This function calculates the compensation level for each pixel by using the compensation levels for the Knot Area where the pixel is present and its surrounding Knot Areas.

5.7.3.2. Enabling or Disabling the Dark Shading Compensation Function

The Dark Shading Compensation and Pixel Shading Compensation functions can be disabled simultaneously using the SPS_ON register. In addition, dark shading compensation can be individually enabled or disabled using the SPS_OFS_ON register when the value of the SPS_ON register is 1.

"**Table 5-56**" illustrates the relationship between the SPS_ON register and the settings for enabling or disabling the Dark Shading Compensation function.

Table 5-56 Enabling or Disabling the Dark Shading Compensation Function

SPS_ON	SPS_OFS_ON	Description
0	Don't Care	The Dark Shading Compensation and Pixel Shading Compensation functions disabled
1	0	The Dark Shading Compensation function disabled
	1	The Dark Shading Compensation function enabled

For details, refer to "**5.8 Pixel Shading Compensation Function.**"

5.7.4. Interface

5.7.4.1. Input Registers

Table 5-57 Input Registers for the Dark Shading Compensation Function

[PICT_SPSHD]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB9D7	1	0	SPS_ON	R/W	U1.0	Enabling or disabling the Dark and Pixel Shading Compensation functions. 0: Compensation disabled 1: Compensation enabled
0xB9D8	1	0	SPS_OFS_ON	R/W	U1.0	Enabling or disabling the Dark Shading Compensation function. 0: Compensation disabled 1: Compensation enabled This register is enabled when the value of the SPS_ON register is 1.

5.8. Pixel Shading Compensation Function

5.8.1. Functional Purpose

The Pixel Shading Compensation function compensates for pixel shading, in which sensitivity ratios between sub-pixels and those between color filters change depending on the position of each pixel. These changes can mainly be caused by optical factors.

5.8.2. Functional Overview

The Pixel Shading Compensation function individually compensates for dark shading in four lines, SP1_HCG, SP1_LCG and SP2H, and SP2L.

- This function compensates for the signals from these lines and for each color filter.
- The Pixel Shading Compensation function performs compensation by using the compensation level, which has been set to 90 control points (Knot Points), as the reference. These Knot Points consist of 10 horizontal x 9 vertical points.
- When compensating for the output level, this function calculates the compensation levels for each pixel by using two-dimensional interpolation based on these Knot Points.

◇ Memo

The sensor controls the Pixel Shading Compensation function by interlocking this function with the Horizontal/Vertical Flip function. For details, refer to “**6.3 Horizontal/Vertical Flip Function**.” Even when changing the settings of the Horizontal/Vertical Flip function, it is not necessary for the host to set the Knot Points again.

5.8.3. Functional Specifications

5.8.3.1. Knot Points

As illustrated in “**Figure 5-51**,” the Pixel Shading Compensation function calculates the compensation level by using 90 Knot Points, consisting of 10 horizontal x 9 vertical points, which have been set to the sensor’s surface.

◇ Memo

A Knot Point is located at the center of each Knot Area. Each Knot Area consists of 256 horizontal x 256 vertical pixels. Therefore, each Knot Point is located between the 128th and 129th pixels. The position of the Knot Areas is fixed in relation to the sensor’s surface area. The top left corner of the Physical Active Pixel Area (origin) is equivalent to the top left corner of Knot Area 11. The positional relationship between Knot Areas and the Physical Active Pixel Area does not change due to, for example, the settings of the Angle-of-View Adjustment function.

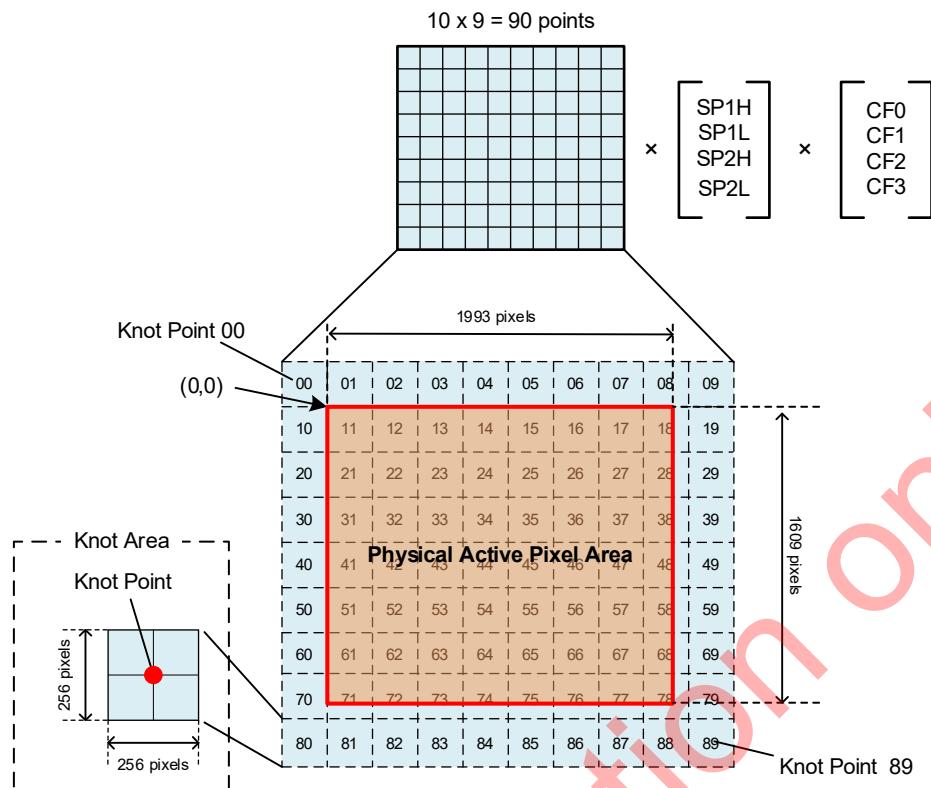


Figure 5-51 Knot Points for the Pixel Shading Compensation Function

- Each compensation value corresponds to the SPS_GAIN_KNOT x _CF y _z ($x = 00$ to 89) ($y = 0$ to 3) ($z = SP1H, SP1L, SP2H, SP2L$) registers, and can be set for each color filter and for each signal line.
- This function calculates the compensation level for each pixel by using the compensation levels for the Knot Area where the pixel is present and its surrounding Knot Areas.

5.8.3.2. Enabling or Disabling the Pixel Shading Compensation Function

The Dark Shading Compensation and Pixel Shading Compensation functions can be disabled simultaneously using the SPS_ON register. In addition, pixel shading compensation can be individually enabled or disabled using the SPS_GAIN_ON register when the value of the SPS_ON register is 1.

"**Table 5-58**" shows how to enable or disable the Pixel Shading Compensation function using the SPS_ON register.

Table 5-58 How to Enable or Disable the Pixel Shading Compensation Function

SPS_ON	SPS_GAIN_ON	Description
0	Don't Care	Both the Dark Shading Compensation and Pixel Shading Compensation functions disabled
1	0	The Pixel Shading Compensation function disabled
	1	The Pixel Shading Compensation function enabled

For details, refer to "**5.7 Dark Shading Compensation Function.**"

5.8.4. Interface

5.8.4.1. Input Registers

Table 5-59 Input Registers for the Pixel Shading Compensation Function

[PICT_SPSHD]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB9D7	1	0	SPS_ON	R/W	U1.0	Enabling or disabling the Dark and Pixel Shading Compensation functions. 0: Compensation disabled 1: Compensation enabled
0xB9D9	1	0	SPS_GAIN_ON	R/W	U1.0	Enabling or disabling the Pixel Shading Compensation function. 0: Compensation disabled 1: Compensation enabled This register is enabled when the value of the SPS_ON register is 1.

[PICT_SPSHD_GAIN_OTP]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xE340	2	10:0	SPS_GAIN_KNOT00_CF0_SP2L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP2L's CF0.
0xE342	2	10:0	SPS_GAIN_KNOT00_CF0_SP2H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP2H's CF0.
0xE344	2	10:0	SPS_GAIN_KNOT00_CF0_SP1L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP1L's CF0.
0xE346	2	10:0	SPS_GAIN_KNOT00_CF0_SP1H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP1H's CF0.
0xE348	2	10:0	SPS_GAIN_KNOT00_CF1_SP2L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP2L's CF1.
0xE34A	2	10:0	SPS_GAIN_KNOT00_CF1_SP2H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP2H's CF1.
0xE34C	2	10:0	SPS_GAIN_KNOT00_CF1_SP1L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP1L's CF1.
0xE34E	2	10:0	SPS_GAIN_KNOT00_CF1_SP1H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP1H's CF1.
0xE350	2	10:0	SPS_GAIN_KNOT00_CF2_SP2L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP2L's CF2.
0xE352	2	10:0	SPS_GAIN_KNOT00_CF2_SP2H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP2H's CF2.
0xE354	2	10:0	SPS_GAIN_KNOT00_CF2_SP1L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP1L's CF2.
0xE356	2	10:0	SPS_GAIN_KNOT00_CF2_SP1H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP1H's CF2.
0xE358	2	10:0	SPS_GAIN_KNOT00_CF3_SP2L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP2L's CF3.
0xE35A	2	10:0	SPS_GAIN_KNOT00_CF3_SP2H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP2H's CF3.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xE35C	2	10:0	SPS_GAIN_KNOT00_CF3_SP1L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP1L's CF3.
0xE35E	2	10:0	SPS_GAIN_KNOT00_CF3_SP1H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 00 for SP1H's CF3.
...		
0xEE60	2	10:0	SPS_GAIN_KNOT89_CF0_SP2L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP2L's CF0.
0xEE62	2	10:0	SPS_GAIN_KNOT89_CF0_SP2H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP2H's CF0.
0xEE64	2	10:0	SPS_GAIN_KNOT89_CF0_SP1L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP1L's CF0.
0xEE66	2	10:0	SPS_GAIN_KNOT89_CF0_SP1H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP1H's CF0.
0xEE68	2	10:0	SPS_GAIN_KNOT89_CF1_SP2L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP2L's CF1.
0xEE6A	2	10:0	SPS_GAIN_KNOT89_CF1_SP2H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP2H's CF1.
0xEE6C	2	10:0	SPS_GAIN_KNOT89_CF1_SP1L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP1L's CF1.
0xEE6E	2	10:0	SPS_GAIN_KNOT89_CF1_SP1H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP1H's CF1.
0xEE70	2	10:0	SPS_GAIN_KNOT89_CF2_SP2L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP2L's CF2.
0xEE72	2	10:0	SPS_GAIN_KNOT89_CF2_SP2H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP2H's CF2.
0xEE74	2	10:0	SPS_GAIN_KNOT89_CF2_SP1L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP1L's CF2.
0xEE76	2	10:0	SPS_GAIN_KNOT89_CF2_SP1H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP1H's CF2.
0xEE78	2	10:0	SPS_GAIN_KNOT89_CF3_SP2L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP2L's CF3.
0xEE7A	2	10:0	SPS_GAIN_KNOT89_CF3_SP2H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP2H's CF3.
0xEE7C	2	10:0	SPS_GAIN_KNOT89_CF3_SP1L	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP1L's CF3.
0xEE7E	2	10:0	SPS_GAIN_KNOT89_CF3_SP1H	R/W	U3.8	This register is used to set the gain compensation level of Knot Point 89 for SP1H's CF3.

5.9. Lens Shading Compensation Function

5.9.1. Functional Purpose

Due to the peripheral dimming characteristics of lenses, the light intensity on the periphery of an image may decrease compared with the center. The Lens Shading Compensation function can compensate for reduced signal levels caused by a decrease in light intensity on the periphery.

5.9.2. Functional Overview

This function can compensate for shading caused by the optical characteristics of lenses for each color filter. The compensation curve used by the sensor to calculate the compensation levels also applies to all lines (SP1_HCG, SP1_LCG, SP2H and SP2L).

5.9.3. Functional Specifications

5.9.3.1. Enabling or Disabling the Lens Shading Compensation Function

To enable or disable this function, set the IR_IS_SHD_ON register to 1 or 0, respectively.

5.9.3.2. Setting the Center of the Lens Shading Compensation Function

This function compensates for a reduction in light intensity which can be observed as concentric circles or concentric ellipses with respect to the optical center.

- The compensation level is controlled corresponding to the geometric distance from the center to each of the 13 control points (CPs).
- When using the Lens Shading Compensation function, set the optical center position corresponding to the optical characteristics of the lens.

With the upper-left corner of the Physical Active Pixel Area as the origin, set the FW_MODE_I1_CMN_HCENTER_SHD and FW_MODE_I1_CMN_VCENTER_SHD registers to the optical center's horizontal and vertical coordinates respectively.

"**Figure 5-52**" illustrates an example when the FW_MODE_I1_CMN_HCENTER_SHD register is set to 996 and the FW_MODE_I1_CMN_VCENTER_SHD register is set to 804, which is equivalent to a case when the optical center of the lens is approximately at the center of the sensor's Physical Active Pixel Area.

- In this figure, circles indicate that all CPs on these circles have the same geometric distance from the center (i.e., CPs to which the same compensation level is applied).

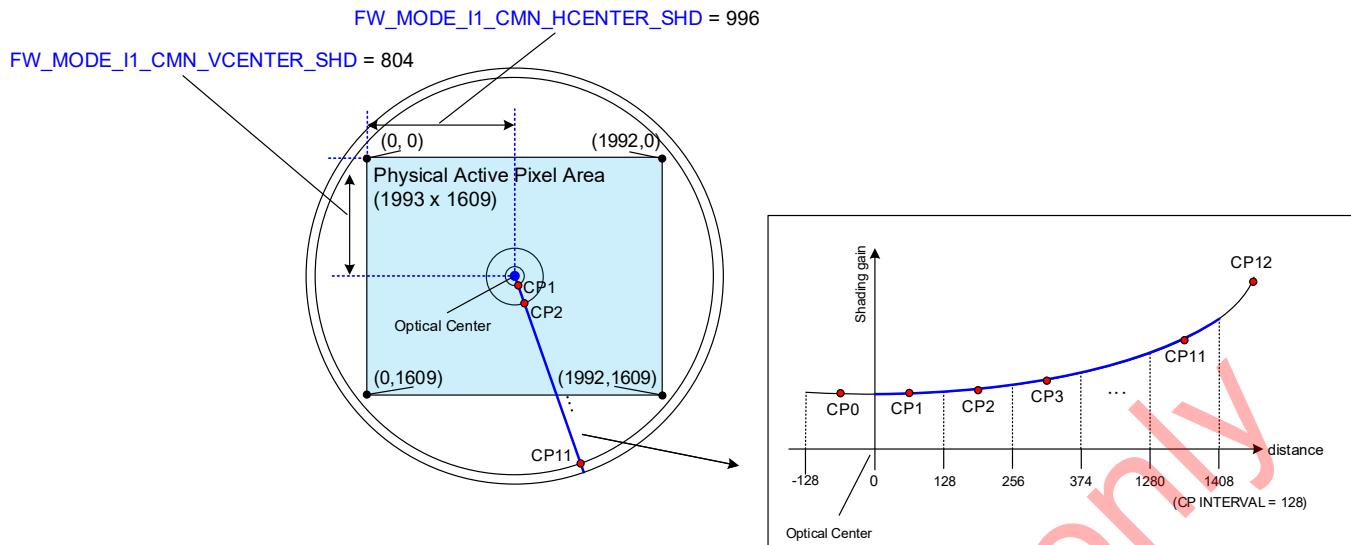


Figure 5-52 Setting of Lens Shading Compensation in Relation to the Sensor

5.9.3.3. Setting the CP Interval for the Lens Shading Compensation Function

A CP interval for this function can be set to either 128, 256 or 512 by using the IR_IS_SHD_GAIN_CP_INTERVAL register. The range available for compensation (the blue curve in "Figure 5-53") differs, depending on the CP interval.

The following are the range available for interpolation, corresponding to the setting of the CP interval:

- When the CP interval is 128, the range is 1407 or less from the optical center.
- When the CP interval is 256, the range is 2815 or less from the optical center.
- When the CP interval is 512, the range is 5631 or less from the optical center.

In "Figure 5-53," the value on the horizontal axis (distance) indicates the number of pixels in the horizontal and vertical directions where the geometric distance from the optical center to each CP point is equal.

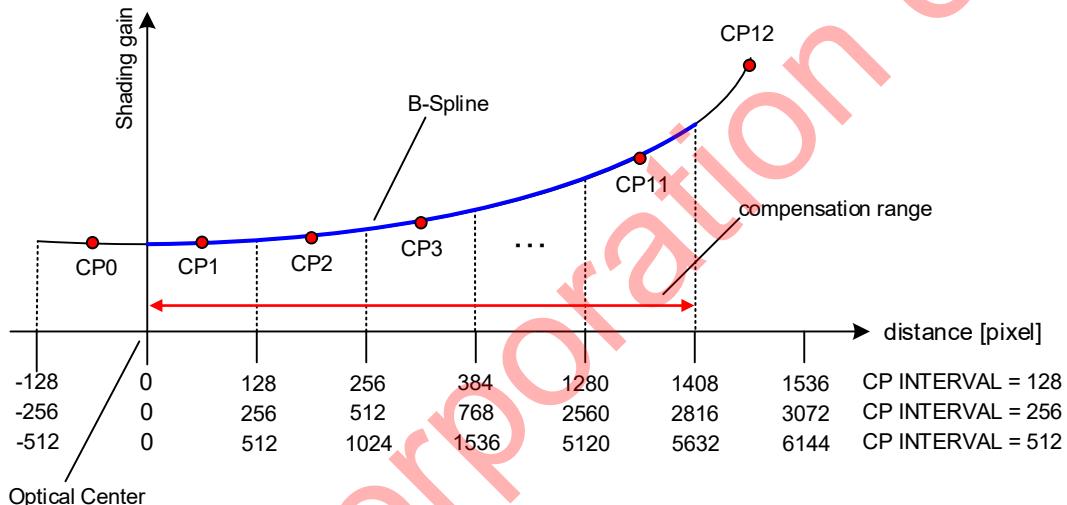


Figure 5-53 CP Intervals and the Compensation Range

5.9.3.3.1. Compensation Level of the Lens Shading Compensation Value

The compensation level is a parameter for adjusting the compensation value for the Lens Shading function.

The compensation level is controlled by illuminance interlocking. For details, refer to "6.6 Interlocking Control Function." "Table 5-60" lists the registers used to set the compensation level.

The register value can be set in the range from 0x00 (0x) to 0x80 (1.0x).

Table 5-60 Registers for the Compensation Level and Illuminance Interlocking

Register Used to Set the Interlocking Type	Settings	Registers for the Settings
SHD_GAIN4_01_IL_TYPE_SEL	Compensation Level of the Lens Shading Compensation	SHD_GAIN_STRENGTH_GAIN4_01_VAL_A SHD_GAIN_STRENGTH_GAIN4_01_VAL_B SHD_GAIN_STRENGTH_GAIN4_01_VAL_C SHD_GAIN_STRENGTH_GAIN4_01_VAL_D

◇ Memo

- When the compensation level is 0x, the Lens Shading function is effectively disabled.
- When the compensation level is 1.0x, the sensor performs compensation at the maximum compensation level (100%) which is calculated by using B-Spline interpolation between CPs.

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5.9.3.4. Setting the Elliptical Coefficient for Lens Shading Compensation

The Lens Shading Compensation function can appropriately reduce a decrease in the signal level caused by light fall-off on the periphery of any images, even for lenses with different curvatures in the horizontal and vertical directions such as aspherical lenses. The sensor uses an elliptical coefficient to adjust the compensation range corresponding to an aspherical lens. The elliptical coefficient indicates the ratio of the major axis to the minor axis of aspherical lenses.

Regarding the method used to set the elliptical coefficient, refer to “**Figure 5-54.**”

- H direction: IR_IS_SHD_INV_ELLIP_COEF_H register
- V direction: IR_IS_SHD_INV_ELLIP_COEF_V register

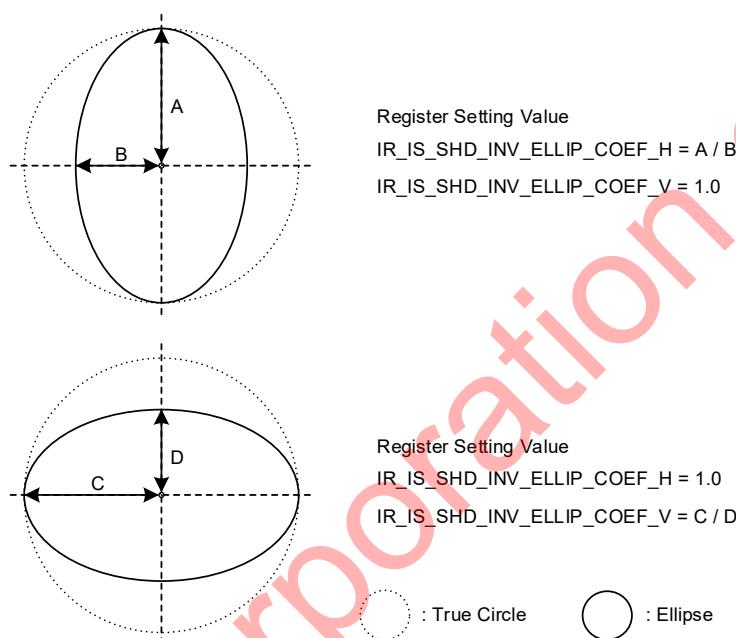


Figure 5-54 Example of Setting the Elliptical Coefficient

◆ Note

When not using the elliptical coefficient, configure the following settings:

- IR_IS_SHD_INV_ELLIP_COEF_H = 1.0
- IR_IS_SHD_INV_ELLIP_COEF_V = 1.0

When using the elliptical coefficient, satisfy the following conditions:

- IR_IS_SHD_INV_ELLIP_COEF_H ≥ 1.0
- IR_IS_SHD_INV_ELLIP_COEF_V ≥ 1.0

Set either the IR_IS_SHD_INV_ELLIP_COEF_H or _V register to 1.0.

◇ Memo

As illustrated in “**Figure 5-54.**” by setting the elliptical coefficient to a value greater than 1.0, the host can change the correction range from a true circle to an ellipse. At this time, the interval between CPs becomes shorter corresponding to the elliptical coefficient and the angle of the ellipse.

5.9.4. Conditions

This section describes the conditions for the area, to which Lens Shading Compensation is applied, and the Physical Active Pixel Area size.

■ Target area

When performing lens shading compensation on the entire output image, the Physical Active Pixel Area must be within the target area. The radius in pixels of the target area varies depending on the CP interval (i.e., 128, 256 or 512) specified in the IR_IS_SHD_GAIN_CP_INTERVAL register. The target area is determined corresponding to the value of the IR_IS_SHD_GAIN_CP_INTERVAL register as follows:

- When the value is 0, the target area is the yellow area with the radius of 1407.
- When the value is 1, the target area is the green area with the radius of 2815.
- When the value is 2 or 3, the target area is the blue area with the radius of 5631.

A narrower CP interval causes the Physical Active Pixel Area that can be compensated to become smaller. For this reason, depending on the elliptical coefficient and the optical center position, the Physical Active Pixel Area (the red rectangle) may not fit within the yellow area in which is defined when setting the IR_IS_SHD_GAIN_CP_INTERVAL register to 0. See “**Figure 5-55**” for details.

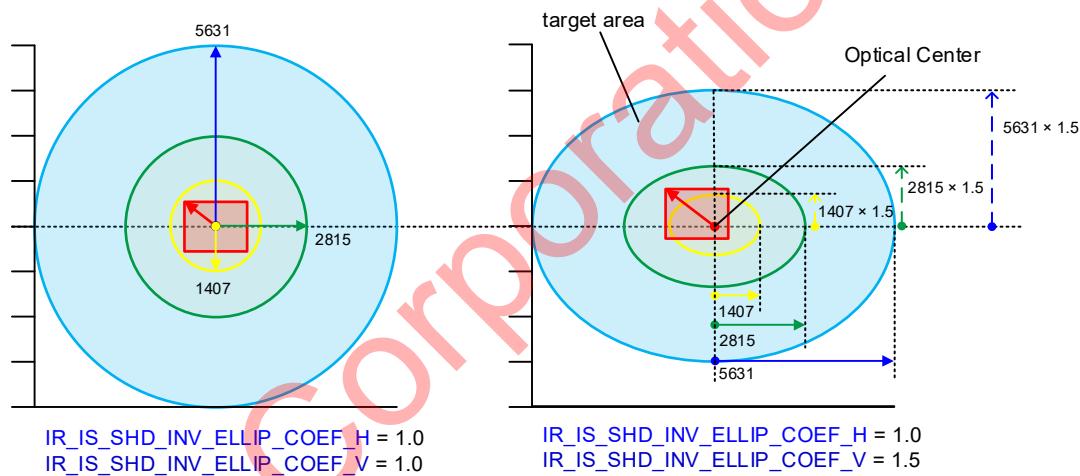


Figure 5-55 The Relationship between the Area Controlled by Lens Shading Compensation and the Image Size

To determine whether the Physical Active Pixel Area fits within the target area, calculate the distance between the optical center and the furthest corner of the target area.

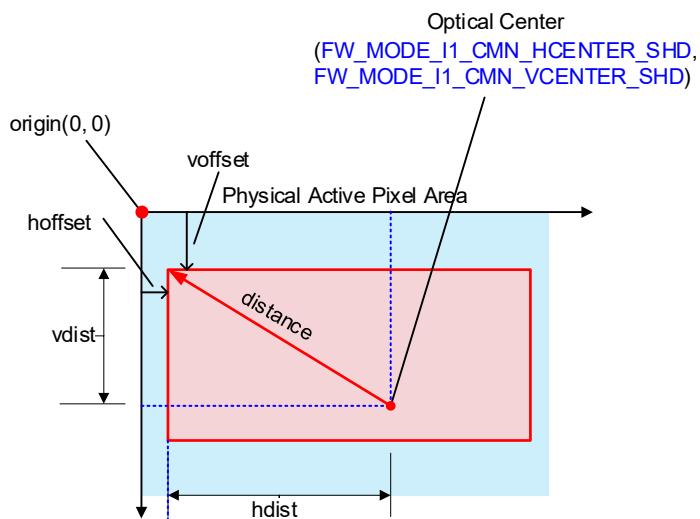


Figure 5-56 Parameters Used to Calculate the Compensation Distance

This section describes the equations to calculate the distance as illustrated in “**Figure 5-56**” by using the registers and parameters, both of which determine the drive mode, optical center compensation and the elliptical coefficient.

The MAX function returns the maximum value from the values specified by the arguments, and the ABS function returns the absolute value of the numeric value specified by the argument. For details regarding the Optical Center Compensation function and the WND_SHIFT_H and WND_SHIFT_V registers, refer to “**6.2 Optical Center Compensation Function**.”

■ When the drive mode is the all-pixel scan mode

hoffset: $28 + \text{WND_SHIFT_H}$

voffset: $28 + \text{WND_SHIFT_V}$

hdist:MAX (ABS (hoffset - FW_MODE_I1_CMN_HCENTER_SHD), ABS (hoffset + 1936 - 1 - FW_MODE_I1_CMN_HCENTER_SHD))

vdist:MAX (ABS (voffset - FW_MODE_I1_CMN_HCENTER_SHD), ABS (voffset + 1552 - 1 - FW_MODE_I1_CMN_VCENTER_SHD))

distance: $\sqrt{(hdist \cdot IR_IS_SHD_INV_ELLIP_COEF_H)^2 + (vdist \cdot IR_IS_SHD_INV_ELLIP_COEF_V)^2}$

Select the interval of CPs so that the calculated distance fits within the target area.

◆ Note

Even when the interval of CPs is changed to 512, the **distance** may exceed the target area, depending on the optical center position and the value of the elliptical coefficient. In that case, narrow the adjustment range of the optical center.

5.9.5. Interface

5.9.5.1. Input Registers

Table 5-61 Input Registers for the Lens Shading Compensation Function

[PICT_SHD]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB9F8	1	7:0	SHD_GAIN4_01_I L_TYPE_SEL	R/W	U8.0	Illuminance interlocking for Group 01 (compensation level for lens shading compensation) • Select the interlocking type "the interlocking target and interlocking point."
0xB9FA	1	7:0	SHD_GAIN_STRE NGTH_GAIN4_0 1_VAL_A	R/W	U1.7	Adjusting the lens shading compensation level Illuminance interlocking: Group 01 and Point A Available range: 0x00 (0x) to 0x80 (1.0x) 0x81 to 0xFF: Setting Prohibited
0xB9FB	1	7:0	SHD_GAIN_STRE NGTH_GAIN4_0 1_VAL_B	R/W	U1.7	Adjusting the lens shading compensation level Illuminance interlocking: Group 01 and Point B Available range: 0x00 (0x) to 0x80 (1.0x) 0x81 to 0xFF: Setting Prohibited
0xB9FC	1	7:0	SHD_GAIN_STRE NGTH_GAIN4_0 1_VAL_C	R/W	U1.7	Adjusting the lens shading compensation level Illuminance interlocking: Group 01 and Point C Available range: 0x00 (0x) to 0x80 (1.0x) 0x81 to 0xFF: Setting Prohibited
0xB9FD	1	7:0	SHD_GAIN_STRE NGTH_GAIN4_0 1_VAL_D	R/W	U1.7	Adjusting the lens shading compensation level Illuminance interlocking: Group 01 and Point D Available range: 0x00 (0x) to 0x80 (1.0x) 0x81 to 0xFF: Setting Prohibited

[FW_MODE_POST]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xD880	2	11:0	FW_MODE_I1_C MN_HCENTER_S HD	R/W	U12.0	Horizontal coordinate of the optical center for the Lens Shading Compensation function
0xD882	2	11:0	FW_MODE_I1_C MN_VCENTER_S HD	R/W	U12.0	Vertical coordinate of the optical center for the Lens Shading Compensation function

[CONST1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x01F8	2	12:0	IR_IS_SHD_INV_E LLIP_COEF_H	R/W	U1.12	Elliptical coefficient in the horizontal direction
0x01FA	2	12:0	IR_IS_SHD_INV_E LLIP_COEF_V	R/W	U1.12	Elliptical coefficient in the vertical direction
0x01FC	1	1:0	IR_IS_SHD_GAIN _CP_INTERVAL	R/W	U2.0	CP interval for lens shading 0: Intervals of 128 1: Intervals of 256 2 and 3: Intervals of 512

[CTRL1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1B7C	1	0	IR_IS_SHD_ON	R/W	U1.0	This register is used to enable or disable lens shading compensation. 0: Lens shading compensation disabled 1: Lens shading compensation enabled

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5.10. PWL Function (Gradation Compression Function)

5.10.1. Functional Purpose

Although the HDR images result in a range of up to 24 bits, depending on the compositing gain, performing gradation compression using polylines enables the sensor to transmit images in the bit width corresponding to the MIPI CSI-2 interface of the host.

5.10.2. Functional Overview

It is possible to set the relationship between the input and output levels using polylines, which are defined by specifying the x-y coordinate (x: input signal level, y: output signal level) of Control Points (CPs). In addition, by adding the pedestal level to the PWL function's input signal, negative values in the input level can be saved.

5.10.3. Functional Specifications

5.10.3.1. PWL Control Mode

Regarding the PWL function, the following two modes can be switched using the PWL_MODE register:

- PWL manual control mode (PWL_MODE = 0)
- PWL through control mode (PWL_MODE = 1)

In PWL manual control mode, the sensor performs gradation compression corresponding to the xy coordinates of a CP.

Alternatively, in PWL through control mode, the sensor transmits uncompressed signals.

◆ Note

When the value of the HDRON_register is 0, the PWL function transmits uncompressed signals regardless of the value of the PWL_MODE register.

Whether to perform gradation compression on the OB Area can be selected using the IR_IS_PWL_OB_MODE register. In order for the PWL function to transmit compressed or uncompressed signals, set the register to 1 or 0 respectively.

5.10.3.1.1. Setting the PWL Manual Control Mode

Set the PWL_CP(n)_X (n = 01 to 17) registers to the xy coordinates of each CP.

When setting the xy coordinates of each CP, be sure to satisfy the following conditions:

- PWL_CP(n + 1)_X >= PWL_CP(n)_X (n = 01 to 16)
- PWL_CP(n + 1)_Y >= PWL_CP(n)_Y (n = 01 to 16)
- The gradient between CPs has a precision of U1.24. Set the gradient between CPs so that the gradient is 1.999999940395355224609375 (i.e., the maximum value of U1.24) or less.

As shown in “**Table 5-62**,” the host can select whether to perform gradation compression on the negative side using the IR_IS_PWL_MINUS_MODE register.

Table 5-62 The Selection of Gradation Compression Processing on the Negative Side

IR_IS_PWL_MINUS_MODE	Processing on Negative Values	Remark
0	Pass-through processing	“ Figure 5-57 ”
1	Gradation compression processing	“ Figure 5-58 ”

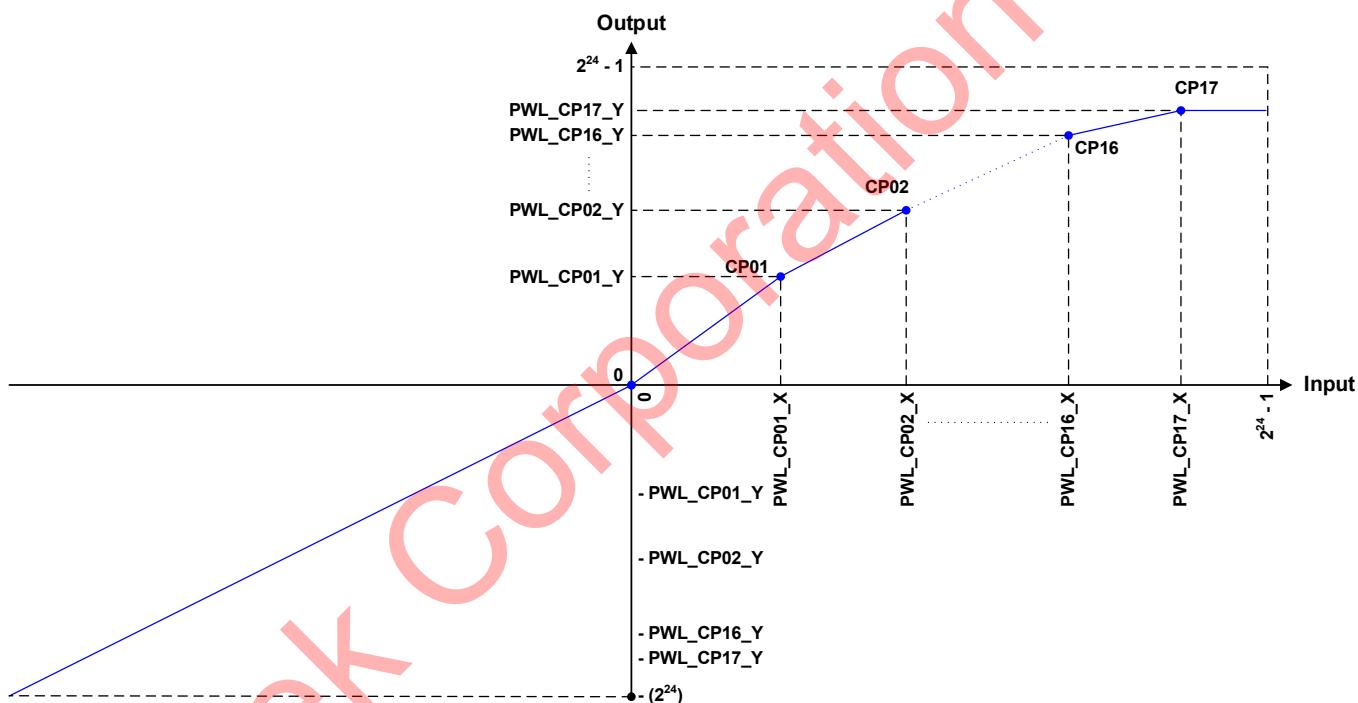


Figure 5-57 Example of Setting the PWL_CP_(n) (n = 01 to 17) Registers When IR_IS_PWL_MINUS_MODE = 0

◇ Memo

When gradation compression is selected on the negative side, the sensor performs compression between a specified CP's xy coordinates and its point-symmetric coordinates on the positive side in relation to the origin.

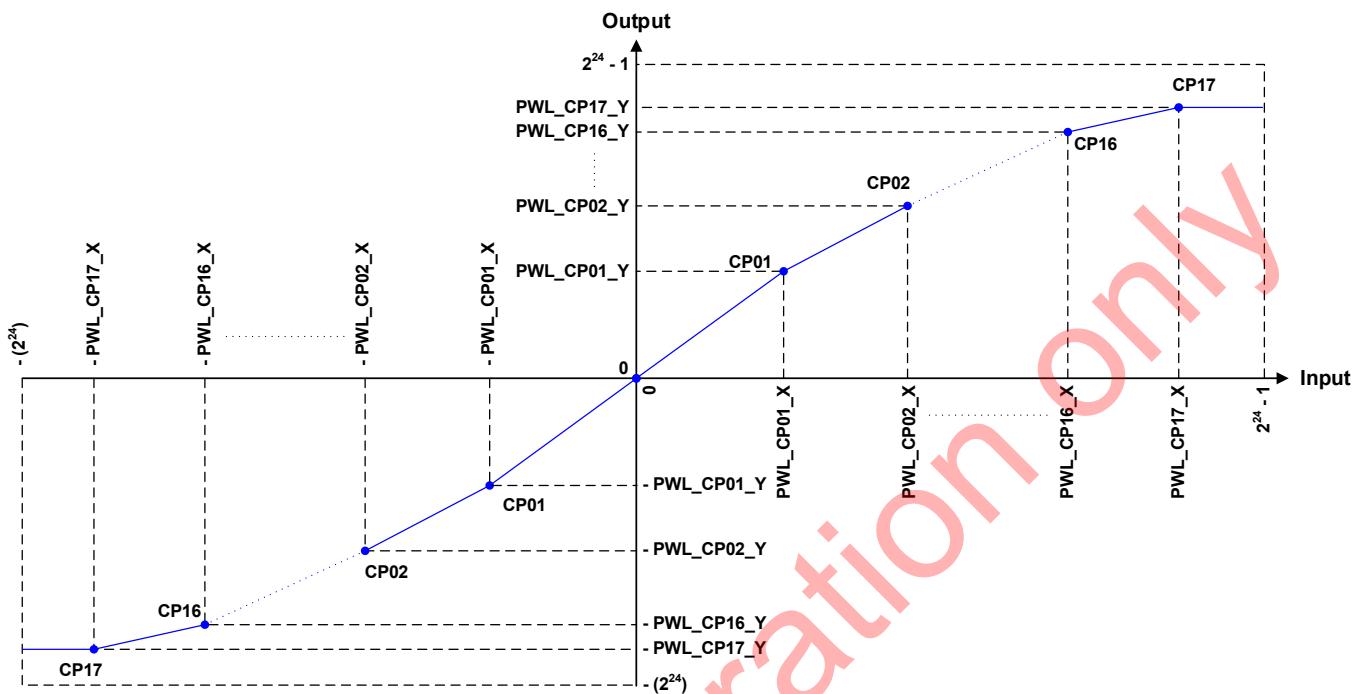


Figure 5-58 Example of Setting the PWL_CP_(n) (n = 01 to 17) Registers When IR_IS_PWL_MINUS_MODE = 1

For the method to calculate the output signal level, refer to “**Table 5-63**” and “**Table 5-64**.“ The blue notations in the table are the registers’ names with “PWL_” omitted.

◆ Note

Note that the calculation methods in “**Table 5-63**” and “**Table 5-64**” differ from the calculation accuracy actually performed within the sensor due to the bit precision during calculation processes. Therefore, the calculation results using the following calculation methods may differ from the sensor’s calculation results.

Table 5-63 Method for Calculating PWL Polyline When IR_IS_PWL_MINUS_MODE = 0

Range of the X Coordinate (Input Signal to the PWL Function)	Calculation Method for the Output Signal Level
$X \leq 0$	X
$0 < X < CP01_X$	$X \times \frac{CP01_Y}{CP01_X}$
$CP(n - 1)_X \leq X < CP(n)_X$ ($(02 \leq n \leq 17)$)	$(X - CP(n-1)_X) \times \frac{CP(n)_Y - CP(n-1)_Y}{CP(n)_X - CP(n-1)_X} + CP(n-1)_Y$
$CP17_X \leq X$	$CP17_Y$

Table 5-64 Method for Calculating PWL Polyline When IR_IS_PWL_MINUS_MODE = 1

Range of the X Coordinate (Input Signal to the PWL Function)	Calculation Method for the Output Signal Level
$X \leq -CP(17)_X$	$-CP(17)_Y$
$-CP(n)_X \leq X < -CP(n - 1)_X$ ($(02 \leq n \leq 17)$)	$(X + CP(n-1)_X) \times \frac{CP(n)_Y - CP(n-1)_Y}{CP(n)_X - CP(n-1)_X} - CP(n-1)_Y$
$-CP01_X < X < CP01_X$	$X \times \frac{CP01_Y}{CP01_X}$
$CP(n - 1)_X \leq X < CP(n)_X$ ($(02 \leq n \leq 17)$)	$(X - CP(n-1)_X) \times \frac{CP(n)_Y - CP(n-1)_Y}{CP(n)_X - CP(n-1)_X} + CP(n-1)_Y$
$CP17_X \leq X$	$CP17_Y$

Although the user can set the number of CPs up to 17, when setting the number of CPs to 16 or less, use one of the following methods:

- The Method for setting CPs from CP01 to CPn
Set the desired values to the xy coordinates of CPs (CP1 to CPn). Then, set the same xy coordinates of CPn to the xy coordinates of CPs (CPn+1 to CP17).
- The Method for setting CPs from CPn to CP17
Set the xy coordinates of CPs (CP01 to CPn) to 0. Then, set the desired values to the xy coordinates of CPs (CPn+1 to CP17).

“**Table 5-65**” illustrates an example of setting a polyline using three points.

- Regarding the method for setting CPs from CP01 to CPn, set the points shown in blue (the xy coordinates from CP04 to CP17) to the same xy coordinates as CP03.
- Regarding the method for setting CPs from CPn to CP17, set the points shown in blue (the xy coordinates from CP01 to CP14) to 0.

Table 5-65 Example of 3-Point-Based PWL Settings

n	Method for Setting CPs From CP01 to CPn		Method for Setting CPs From CPn to CP17	
	PWL_CP(n)_X	PWL_CP(n)_Y	PWL_CP(n)_X	PWL_CP(n)_Y
01	0x00_1000	0x00_0800	0x00_0000	0x00_0000
02	0x01_0000	0x00_0C00	0x00_0000	0x00_0000
03	0x0F_0000	0x00_OEE0	0x00_0000	0x00_0000
04-14	0x0F_0000	0x00_OEE0	0x00_0000	0x00_0000
15	0x0F_0000	0x00_OEE0	0x00_1000	0x00_0800
16	0x0F_0000	0x00_OEE0	0x01_0000	0x00_0C00
17	0x0F_0000	0x00_OEE0	0x0F_0000	0x00_OEE0

5.10.3.2. Setting the Pedestal Level

5.10.3.2.1. Avoiding Noise Clipping by Setting the Pedestal Level

Adding the pedestal level to the PWL function's input signal makes it possible for the sensor to produce image output by offsetting negative noise components to the positive side. When performing appropriate signal processing on output images including negative components, the host can obtain much accurate gradations in dark regions. If the host does not process any negative components of the HDR data, do not add the pedestal value.

As shown in “**Figure 5-59**,” when negative components which are contained in the noise in the dark area is clipped at 0, which has been selected as the lower limit, the average noise level in the dark area increases.

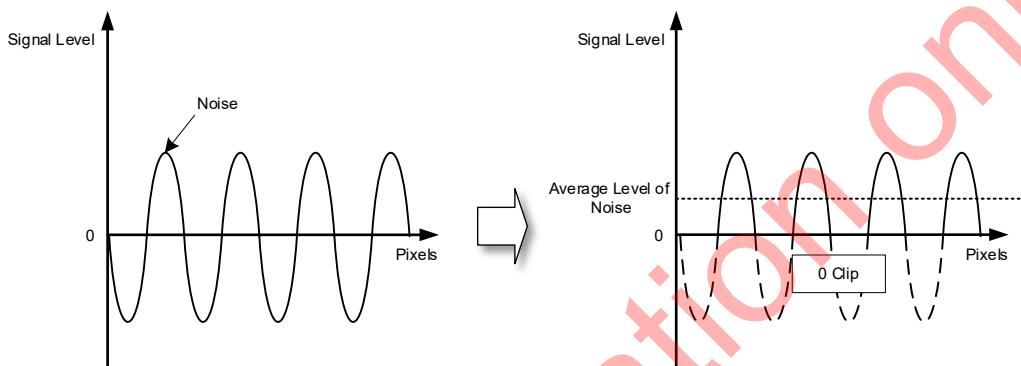


Figure 5-59 Clipping of Noise Component in the Dark Area

However, when a signal is amplified by the Exposure Control function and when the negative noise components' levels in the dark area increase, some negative noise components may be clipped regardless of the addition of the pedestal level.

“**Figure 5-60**” illustrates an example where the sensor increases the pedestal level of an output image and then the host subtracts the pedestal level of the output image. Adding the pedestal level to the PWL function's input signal makes it possible to prevent negative noise components in the dark area, the signal level of which has become 0 or higher, from being clipped in the sensor's output images.

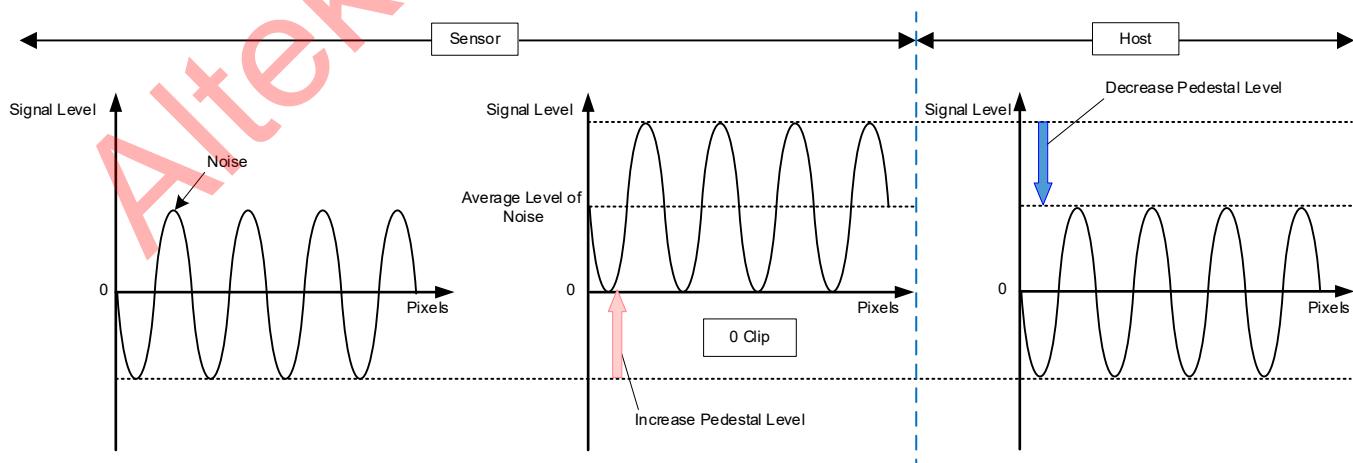


Figure 5-60 Increasing and Decreasing the Pedestal Level

5.10.3.2.2. How to Set the Pedestal Level

The user can select the sensor's pedestal level addition process from the following methods:

- Pre-PWL Pedestal Addition Method (PEDESTAL_SEL = 0)
The sensor adds the pedestal level, set in the PRE_PEDESTAL register, before PWL processing.
- Post-PWL Pedestal Addition Method (PEDESTAL_SEL = 1)
The sensor adds the pedestal level, set in the POST_PEDESTAL register, after PWL processing.

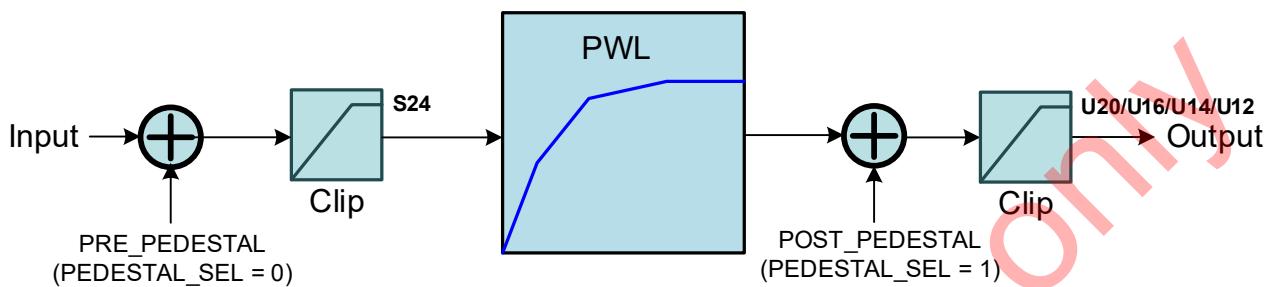


Figure 5-61 Positions of Pedestal Level Addition

PWL compression is passed through unprocessed in Normal mode (HDR disabled) and HDR (Line / Line) mode, and then the sensor adds the pedestal level only.

When setting the pedestal level, please note the following depending on the position of this level:

- When using the pre-PWL pedestal level addition method (PEDESTAL_SEL = 0)
If the sum of the maximum level before PWL processing and the pedestal level exceeds S24.0, the sum of these values is clipped to S24.0. To retain signals in high luminance regions, make adjustments considering the addition of the pedestal level to the HDR signal.
- When using the post-PWL pedestal level addition method (PEDESTAL_SEL = 1)
Adding the pedestal level after PWL processing may incur clipping at the upper limit of output format. To avoid clipping, configure the PWL settings so that the total value between "the maximum level after the PWL processing" and "the added pedestal level" does not exceed the bit width specified by the MIPI CSI-2 interface.

◇ Memo

Change the value of each of the pedestal level registers (PEDESTAL_SEL, PRE_PEDESTAL and POST_PEDESTAL) by setting the PEDESTAL_DATA_SEL register to 1 while the sensor is in Start-up State.

“Figure 5-62” illustrates an example of how to configure the PWL settings in RAW20 output when using the post-PWL pedestal level addition method. For example, when setting the POST_PEDESTAL register to 0x00_00F0, ensure that the maximum value after the PWL processing is less than or equal to 0x0F_FFOF. This setting makes it possible to prevent high luminance regions from being clipped at 0x0F_FFFF, which is the maximum level of the RAW20 output, due to the post-PWL pedestal level addition method.

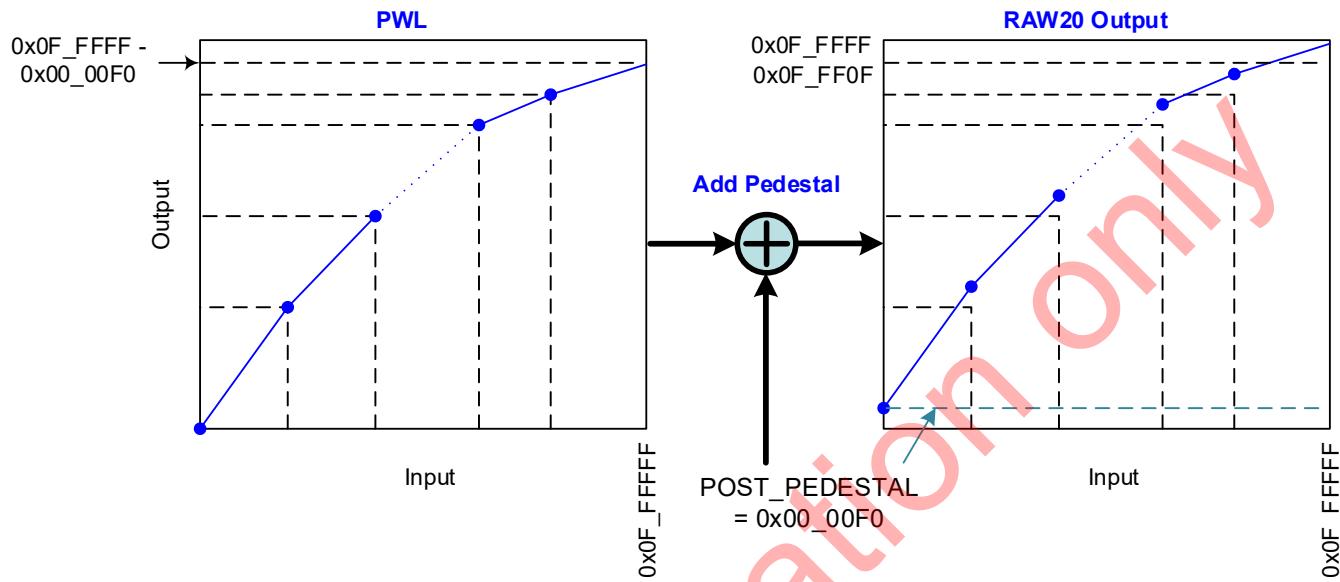


Figure 5-62 Example of the PWL Settings Considering the Added Pedestal Level after PWL Processing

5.10.3.3. Decompressing Signals by the Host

In order for the host to decompress the signal, which has been compressed and sent out using the sensor's PWL function, perform the following procedure: The blue notations in the table are the registers' names with "PWL_" omitted.

■ When using the pre-PWL pedestal level addition method (PEDESTAL_SEL = 0)

1. Decompress the sensor's output signal level (Y) in accordance with "Table 5-66."
2. Subtract the pedestal level from the decompressed signal level (X), which is obtained in Step 1.

$$\text{Signal Level prior to PWL Processing} = X - \text{PRE_PEDESTAL}$$

Table 5-66 Decompression of the Sensor's Output Signal Level Using the Pre-PWL Pedestal Level Addition Method

Range of the Y Coordinate (Input signal to the Host)	Decompression Method
$0 < Y < CP01_Y$	$X = Y \times \frac{CP01_X}{CP01_Y}$
$CP(n-1)_Y \leq Y < CP(n)_Y$ ($02 \leq n \leq 17$)	$X = (Y - CP(n-1)_Y) \times \frac{CP(n)_X - CP(n-1)_X}{CP(n)_Y - CP(n-1)_Y} + CP(n-1)_X$
$CP17_Y \leq Y$	$X = CP17_X$

■ When using the post-PWL pedestal level addition method (PEDESTAL_SEL = 1)

1. Subtract the pedestal level from the sensor's output signal level.

$$Y = \text{Signal Level} - \text{POST_PEDESTAL}$$

2. Perform decompression calculations corresponding to the value Y.

Perform the decompression operation corresponding to the value Y. When the IR_IS_PWL_MINUS_MODE register is 0, refer to "Table 5-67." When the value is 1, refer to "Table 5-68."

$$\text{Signal Level prior to PWL Processing} = X$$

Each calculation is the inverse calculation shown in "Table 5-63" and "Table 5-64." Refer to "Figure 5-57" and "Figure 5-58" for the relationship between each register and the signal level.

Table 5-67 Decompression of the Sensor's Output Signal Level Using the Post-PWL Pedestal Level Addition Method (in the Case of IR_IS_PWL_MINUS_MODE = 0)

Range of the Y Coordinate (Input signal to the Host)	Decompression Method
$Y \leq 0$	$X = Y$
$0 < Y < CP01_Y$	$X = Y \times \frac{CP01_X}{CP01_Y}$
$CP(n-1)_Y \leq Y < CP(n)_Y$ ($02 \leq n \leq 17$)	$X = (Y - CP(n-1)_Y) \times \frac{CP(n)_X - CP(n-1)_X}{CP(n)_Y - CP(n-1)_Y} + CP(n-1)_X$
$CP17_Y \leq Y$	$X = CP17_X$

Table 5-68 Decompression of the Sensor's Output Signal Level Using the Post-PWL Pedestal Level Addition

Method (in the Case of IR_IS_PWL_MINUS_MODE = 1)

Range of the Y Coordinate (Input signal to the Host)	Decompression Method
$Y \leq -CP17_Y$	$X = -CP(n-1)_X$
$-CP(n-1)_Y \leq Y < -CP(n)_Y$ ($02 \leq n \leq 17$)	$X = (Y + CP(n-1)_Y) \times \frac{CP(n)_X - CP(n-1)_X}{CP(n)_Y - CP(n-1)_Y} - CP(n-1)_X$
$-CP01_Y < Y < CP01_Y$	$X = Y \times \frac{CP01_X}{CP01_Y}$
$CP(n-1)_Y \leq Y < CP(n)_Y$ ($02 \leq n \leq 17$)	$X = (Y - CP(n-1)_Y) \times \frac{CP(n)_X - CP(n-1)_X}{CP(n)_Y - CP(n-1)_Y} + CP(n-1)_X$
$CP17_Y \leq Y$	$X = CP17_X$

5.10.4.Conditions

When the host executes the PWL function, set the registers in accordance with the following restrictions:

- $PWL_CP(n + 1)_X \geq PWL_CP(n)_X$ ($n = 01$ to 16)
- $PWL_CP(n + 1)_Y \geq PWL_CP(n)_Y$ ($n = 01$ to 16)
- Set the gradient between CPs so that the gradient is $1.999999940395355224609375$ (i.e., the maximum value of U1.24) or less.

If the value of the PWL_MODE register is 1 or the value of the HDRON_ is 0, the following registers' settings are invalid:

- PWL_CP(n)_X ($n = 01$ to 17)
- PWL_CP(n)_Y ($n = 01$ to 17)
- IR_IS_PWL_OB_MODE
- IR_IS_PWL_MINUS_MODE

5.10.5.Interface

5.10.5.1. Input Registers

Table 5-69 Input Registers for the PWL Function

[PWL]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB064	1	0	PWL_MODE	R/W	U1.0	This register is used to select the PWL Control mode. 0: PWL manual control mode 1: PWL pass-through control mode
0x9F88	3	23:0	PWL_CP01_X	R/W	U24.0	The X coordinate of the PWL Control Point 1
0x9F8C	3	23:0	PWL_CP01_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 1
0x9F90	3	23:0	PWL_CP02_X	R/W	U24.0	The X coordinate of the PWL Control Point 2
0x9F94	3	23:0	PWL_CP02_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 2
0x9F98	3	23:0	PWL_CP03_X	R/W	U24.0	The X coordinate of the PWL Control Point 3
0x9F9C	3	23:0	PWL_CP03_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 3
0x9FA0	3	23:0	PWL_CP04_X	R/W	U24.0	The X coordinate of the PWL Control Point 4
0x9FA4	3	23:0	PWL_CP04_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 4
0x9FA8	3	23:0	PWL_CP05_X	R/W	U24.0	The X coordinate of the PWL Control Point 5
0x9FAC	3	23:0	PWL_CP05_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 5
0x9FB0	3	23:0	PWL_CP06_X	R/W	U24.0	The X coordinate of the PWL Control Point 6
0x9FB4	3	23:0	PWL_CP06_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 6
0x9FB8	3	23:0	PWL_CP07_X	R/W	U24.0	The X coordinate of the PWL Control Point 7
0x9FBC	3	23:0	PWL_CP07_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 7
0x9FC0	3	23:0	PWL_CP08_X	R/W	U24.0	The X coordinate of the PWL Control Point 8
0x9FC4	3	23:0	PWL_CP08_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 8

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x9FC8	3	23:0	PWL_CP09_X	R/W	U24.0	The X coordinate of the PWL Control Point 9
0x9FCC	3	23:0	PWL_CP09_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 9
0x9FD0	3	23:0	PWL_CP10_X	R/W	U24.0	The X coordinate of the PWL Control Point 10
0x9FD4	3	23:0	PWL_CP10_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 10
0x9FD8	3	23:0	PWL_CP11_X	R/W	U24.0	The X coordinate of the PWL Control Point 11
0x9fdc	3	23:0	PWL_CP11_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 11
0x9fe0	3	23:0	PWL_CP12_X	R/W	U24.0	The X coordinate of the PWL Control Point 12
0x9fe4	3	23:0	PWL_CP12_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 12
0x9fe8	3	23:0	PWL_CP13_X	R/W	U24.0	The X coordinate of the PWL Control Point 13
0x9fec	3	23:0	PWL_CP13_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 13
0x9ff0	3	23:0	PWL_CP14_X	R/W	U24.0	The X coordinate of the PWL Control Point 14
0x9ff4	3	23:0	PWL_CP14_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 14
0x9ff8	3	23:0	PWL_CP15_X	R/W	U24.0	The X coordinate of the PWL Control Point 15
0x9ffc	3	23:0	PWL_CP15_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 15
0xA000	3	23:0	PWL_CP16_X	R/W	U24.0	The X coordinate of the PWL Control Point 16
0xA004	3	23:0	PWL_CP16_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 16
0xA008	3	23:0	PWL_CP17_X	R/W	U24.0	The X coordinate of the PWL Control Point 17
0xA00C	3	23:0	PWL_CP17_Y	R/W	U24.0	The Y coordinate of the PWL Control Point 17

[CMN]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8AB2	1	0	PEDESTAL_SEL	R/W	U1.0	This register is used to set the position of pedestal level addition. 0: Before PWL processing 1: After PWL processing
0x8AB4	2	11:0	PRE_PEDESTAL	R/W	U12.0	This register is used to set the pedestal level value for pre-PWL pedestal addition method. This register is enabled when the value of the PEDESTAL_SEL register is 0.
0x8AB6	2	11:0	POST_PEDESTAL	R/W	U12.0	This register is used to set the pedestal level value for post-PWL pedestal addition method. This register is enabled when the value of the PEDESTAL_SEL register is 1.

[SYS_CTRL]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8ADA	1	1	PEDESTAL_DATA_SEL	R/W	U1.0	This register is used to set the pedestal level value. 0: The initial value corresponding to the drive mode 1: The value of the PEDESTAL_SEL register

[CONST1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x0200	1	0	IR_IS_PWL_OB_MODE	R/W	U1.0	This register is used to select gradation compression processing for the OB Area. 0: Disabled 1: Enabled
0x0201	1	0	IR_IS_PWL_MINUS_MODE	R/W	U1.0	This register is used to select gradation compression processing on the negative side. 0: Disabled 1: Enabled

Chapter 6 Extension Functions

This chapter describes the sensor's extension functions for the user's intended applications.

Table 6-1 List of Extension Functions

Function Name	Applications
Sync Function	Uses multiple sensors in synchronization.
Optical Center Compensation Function	Configures the settings in accordance with the installation position of the optical system and/or a camera.
Horizontal/Vertical Flip Function	
Crop Function	
First Pixel Color Selection Function	Configures the settings in accordance with the installation position of the optical system and/or a camera.
Interlocking Control Function	Controls the parameters interlocked with illuminance.
Context Switch Function	Switches registers' values at one time.
Output Mask Function	Masks output images at sensor startup or at the desired timing.
Information Output Function	Indicates the internal conditions of the sensor.
OTP Function	Enables the user to read or write to the OTP ROM.

6.1. Sync Function

6.1.1. Functional Purpose

The Synchronization function enables the sensor to synchronize itself with other devices, using the vertical sync signal.

6.1.2. Functional Overview

The sensor has three types of synchronization methods

- Internal synchronization that enables the sensor to supply the external sync signal to other sensors
- External pulse-based synchronization that enables the sensor to perform synchronization using the external sync signal from the host or other sensors
- Shutter trigger synchronization The host can switch the synchronization methods using the SG_MODE_ register. “**Table 6-2**” shows an overview of each synchronization method.

Table 6-2 An Overview of the Synchronization Methods

Mode	SG_MODE_	Synchronization Adjustment Method	Fsync Pin
Internal Sync	0	-	Available for output settings
External Pulse-Based Sync	1	In this mode, the sensor starts a Read operation using the sync signal that the sensor receives via the FSYNC pin.	Input only
Shutter Trigger-	2	In this mode, the sensor	Input only

Mode	SG_MODE_	Synchronization Adjustment Method	FSYNC Pin
Based Sync		starts a shutter operation using the sync signal that the sensor receives via the FSYNC pin.	

◆ **Note**

- Switch the sync methods while the sensor is in Start-up State.
- The available range for the sensor's exposure time to be set varies depending on the sync mode. For details regarding the available range for the exposure time, refer to "[5.2.4.2 Available Range for the Exposure Time.](#)"

The SG_MODE_ register is compatible with the Application Lock function. For details, refer to "[“3.1.5 Application Lock Function.”](#)"

The sensor can correct the external pulse-based sync within two lines. For how to set the FSYNC pin for the Sync function, refer to "[“2.1.4 FSYNC Pin.”](#)"

◇ **Memo**

To apply the changed value(s) from the next sensor startup, write these values to the Serial NOR Flash device in accordance with the procedure as described in "[“4.9.2 When Writing the Current Register Value\(s\) to the Serial NOR Flash Device.”](#)"

6.1.3. Functional Specifications

6.1.3.1. Internal Synchronization

In internal synchronization, the sensor operates autonomously in sync with the frame rate which has been set for the sensor. In this synchronization, the sensor can transmit the external sync signal via the FSYNC pin. For the AC characteristics of the external sync signal that the sensor transmits, refer to the IMX623-AA** "Data Sheet" provided separately by SSS.

To enable internal synchronization, set the SG_MODE_ register to 0.

6.1.3.2. External Pulse-Based Synchronization

The following shows an overview of the external pulse-based synchronization.

- The sensor begins a Read operation in sync with the external sync signal.
- After the beginning of image output and when there is no external sync signal input, the sensor begins operating autonomously.
- The sensor adjusts the start time of a read operation in units of a minimum of 2 lines.

"[Figure 6-1](#)" illustrates an example of the configuration of the external pulse-based synchronization. For the AC characteristics of the external sync signal to the sensor, refer to the IMX623-AA** "Data Sheet" provided separately by SSS.

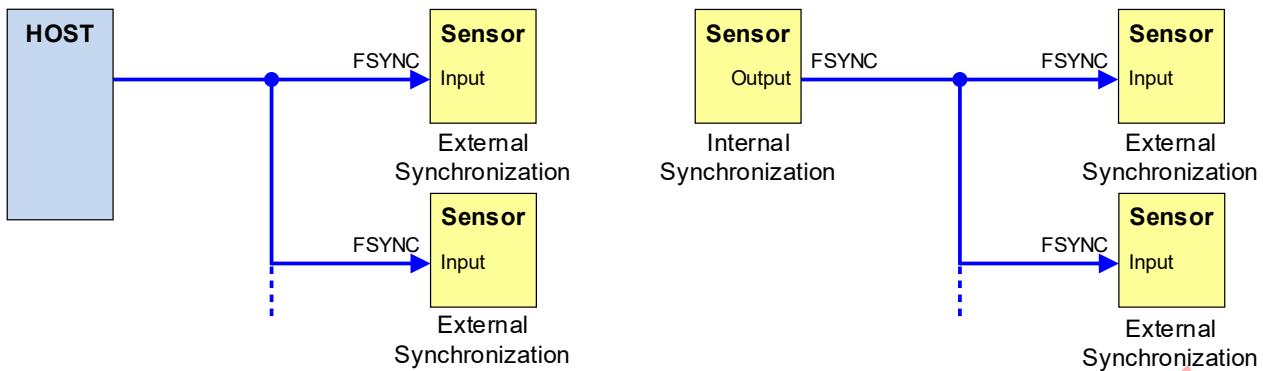


Figure 6-1 Example of the External Sync Signal Configuration

To enable external pulse-based sync, set the SG_MODE_ register to 0x1.

When the external pulse-based sync is selected, the sensor operates as follows:

- After the sensor has transitioned to Streaming State, it begins image output when it receives the external sync signal via the FSYNC pin.
- Following image output, the sensor begins operating autonomously. For this reason, there is no need to send the external sync signal frame by frame to the sensor.
- As illustrated in “**Figure 6-2**,” when the sensor receives the external sync signal after the sensor begins operating autonomously, the sensor adjusts the vertical sync signal based on the time differential between the internal vertical sync signal input and the vertical sync signal of the sensor. The VSYNC signal in “**Figure 6-2**” is a virtual timing signal that indicates the assumed time when the sensor receives the external sync signal that makes the adjustment level 0.

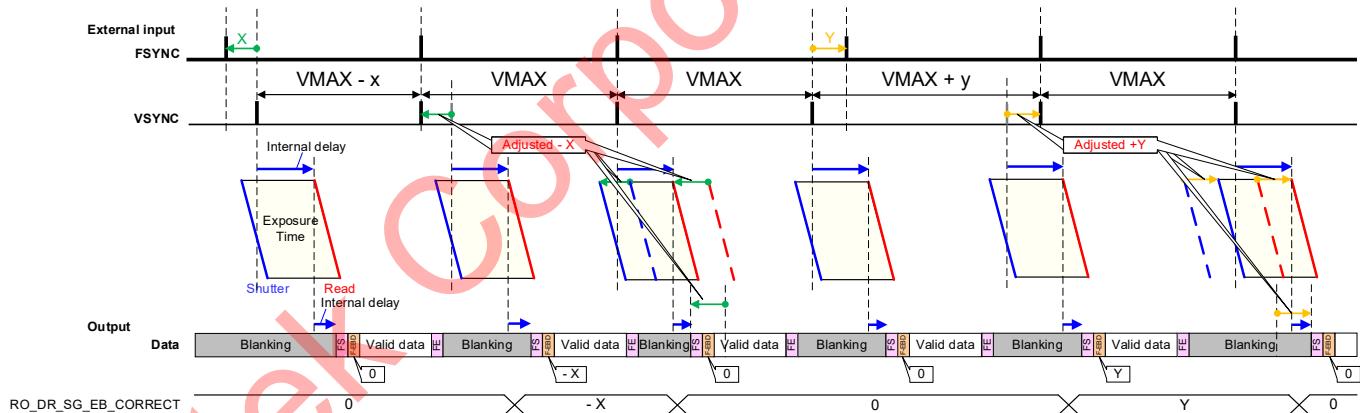


Figure 6-2 External Pulse-Based Sync in Master Mode

The host can confirm the adjustment level for the vertical sync signal using the RO_DR_SG_EB_CORRECT register or the Front Embedded Data.

◆ Note

- The vertical sync signal is adjusted in units of 2 lines. Therefore, if the adjustment level is less than 2 lines, the sensor does not make an adjustment.
- However, without the external sync signal, there may be a delay in operations between the sensor and “the host/other sensors” since the sensor cannot correct timing for these operations.

◇ **Memo**

- For how to start up the sensor in external pulse-based sync, refer to “**4.3.3 Power-on Sequence in Shutter Trigger-Based Sync.**”
- For details regarding the VMAX (the maximum number of lines of the vertical sync signal), refer to “**5.2.3.2.1 Units of Exposure Time.**”
- For details, refer to “**6.9.3.5 Front Embedded Data.**”

6.1.3.2.1. Setting a Data Output Timing Delay

In external pulse-based sync, the user can adjust when the sensor begins internal processing. To adjust when the sensor begins image output after the sync signal, set the IR_DR_SG_VRESET_VDLY register to the desired amount of delay.

“Figure 6-3” illustrates the following:

- an operation when a delay is not set (Output Data A)
- an operation when a delay of 10 lines is set (Output Data B)

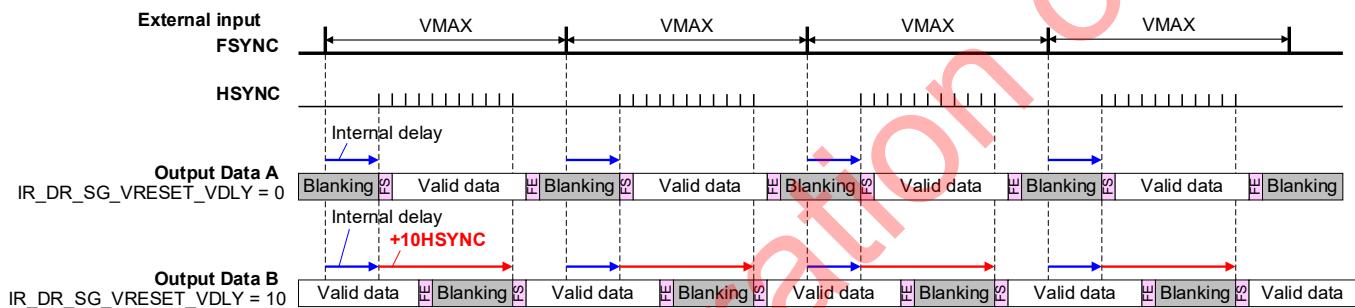


Figure 6-3 Adjustment of When the Sensor Begins Internal Processing in External Pulse-Based Sync

◆ **Note**

Set the IR_DR_SG_VRESET_VDLY register to a value less than “VMAX - 31.” For the VMAX, refer to “**Table 5-9.**”

6.1.3.2.2. Points to Note When Performing Long Exposure While the External Pulse-Based Sync Is in Operation

When the sensor has performed long exposure while the external pulse-based sync is enabled, the sensor does not adjust its synchronization with the external sync signal during the period of extension frame output. The sensor adjusts its synchronization with the external sync signal in the last frame of the subsequent long exposure period.

When the sensor receives multiple pulses of the external sync signal, the sensor adjusts its synchronization based on the time differential between an internal signal generated and the last sync signal received. For details, see “**Figure 6-4.**”

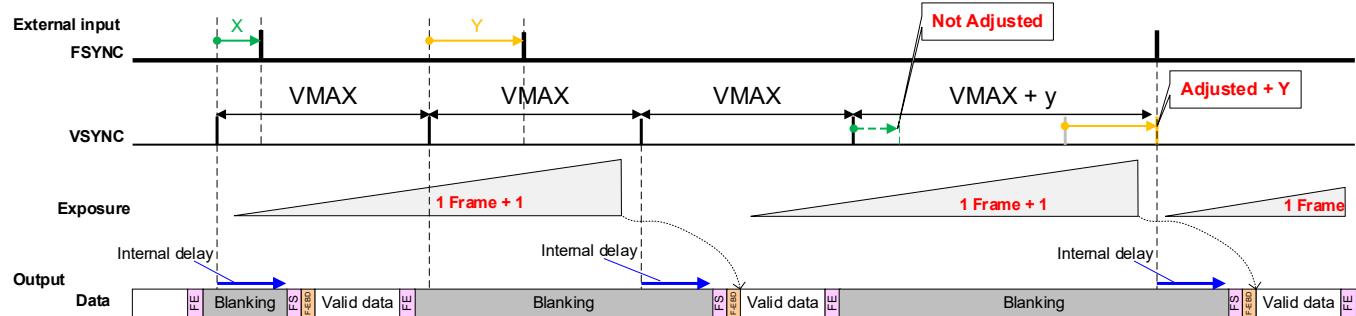


Figure 6-4 External Pulse-Based Sync When the Sensor Performs Long Exposure (One Frame Extended)

6.1.3.3. Shutter Trigger-Based Synchronization

The following shows an overview of the shutter trigger-based synchronization.

- The sensor begins exposure in sync with the external sync signal.
- After the beginning of image output and when there is no external sync signal input, the sensor does not operate autonomously.
- The sensor can operate autonomously by selecting the autonomous operating mode.

To enable the shutter trigger-based sync, set the SG_MODE_ register to 0x2.

When the shutter trigger-based sync is selected, the sensor operates as follows:

- The sensor begins exposure when the sensor receives the external sync signal via the FSYNC pin, after the sensor has transitioned to Streaming State. The sensor performs exposure automatically only in the first frame. From the second frame onward, the sensor performs exposure when the sensor receives the external sync signal.
- As illustrated in “**Figure 6-5**,” the sensor does not operate autonomously after the beginning of image output. In order for the sensor to produce image output, the sensor needs to receive the external sync signal or the host is required to select the autonomous operating mode in advance.

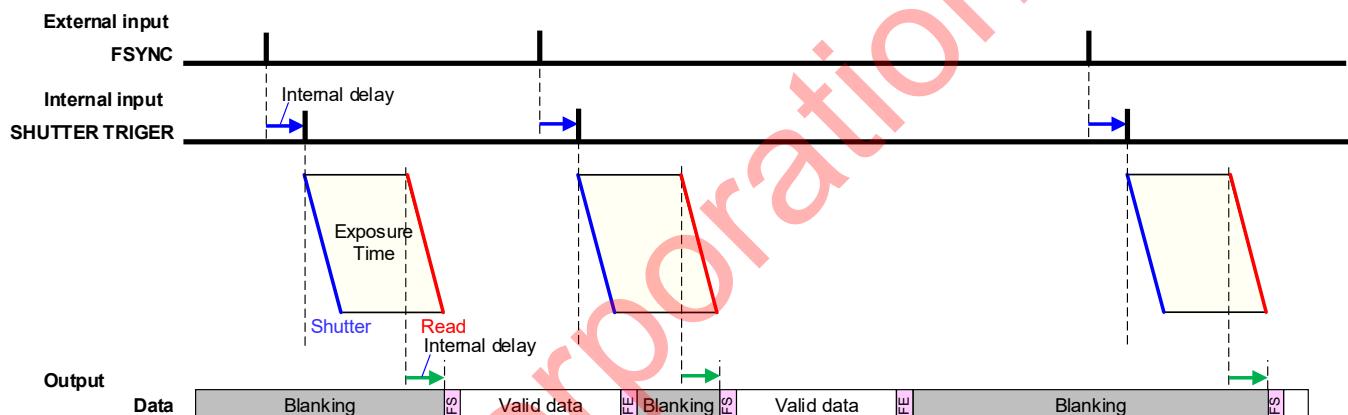


Figure 6-5 Example of an Operation in Shutter Trigger-Based Sync

In external trigger-based synchronization, the sensor can operate autonomously even when there are no pulse inputs of the external sync signal by enabling the following two autonomous operating modes:

- Level detection auto mode: A mode in which the sensor operates autonomously while the host continues to send the polarity level signal that makes the external sync signal active, via the FSYNC pin

As shown in “**Table 6-3**,” the user can enable or disable these autonomous operating modes using the SG_TRG_AUTOMODE register.

Table 6-3 The Selection of the Sensor’s Autonomous Operating Mode

SG_TRG_AUTOMODE	Autonomous Operating Mode
0	Level detection auto mode disabled
1	Level detection auto mode enabled

◆ Note

When the shutter trigger-based synchronization is selected, setting the long exposure is prohibited. For details, refer to “[5.2.3.2.3 Long Exposure](#).”

6.1.3.3.1. Level Detection Auto Mode

In level detection auto mode, the sensor operates autonomously while the host continues to send the polarity level signal that makes the external sync signal active, via the FSYNC pin. As illustrated in “[Figure 6-6](#),” while the sensor operates autonomously, the sensor produces image output in sync with the frame rate which has been set for the sensor. “[Figure 6-6](#)” illustrates an example in which the polarity of the external sync signal is active high.

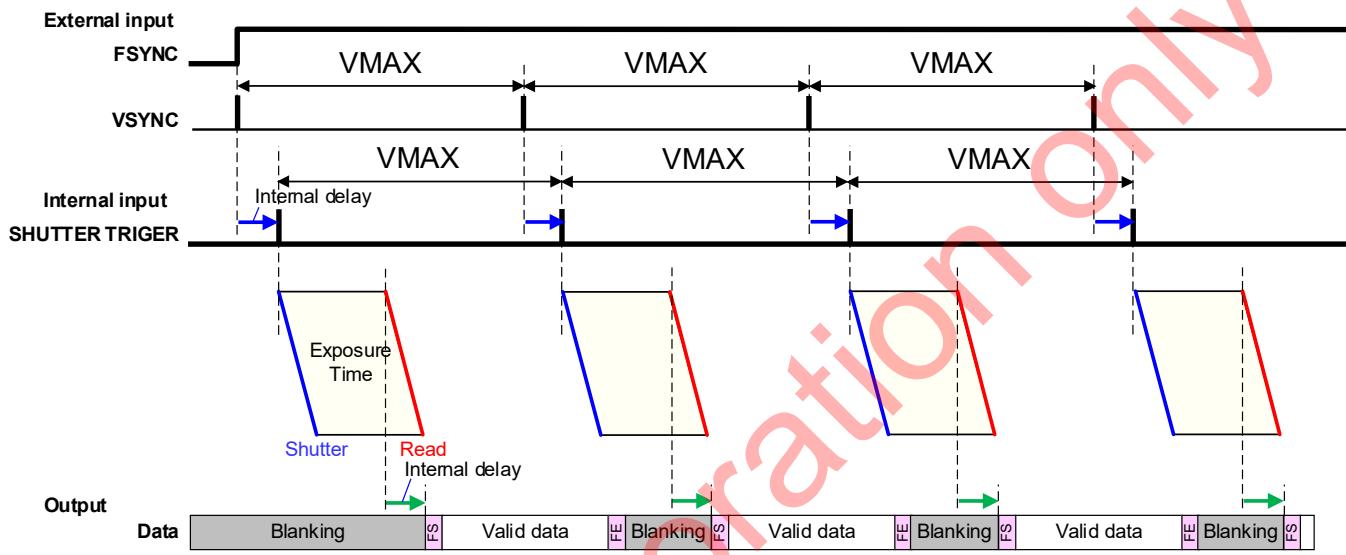


Figure 6-6 Shutter Trigger-Based Sync with the Level Detection Auto Mode Enabled

◆ Memo

- The VSYNC signal in “[Figure 6-6](#)” is a virtual timing signal, indicating that the assumed time when the sensor begins exposure coincides with the sensor’s internal synchronization.
- For details regarding the VMAX (the maximum number of lines of the vertical sync signal), refer to “[5.2.3.2.1 Units of Exposure Time](#).”

6.1.3.4. Line Count Extension Function

Line Count Extension is a function that extends the number of lines within one frame by specifying an offset value for the VMAX. This function enables the user to dynamically adjust the frame rate without changing the drive mode.

“**Figure 6-7**” illustrates an example of this function’s operation. This sensor adjusts the vertical sync signal by adjusting the frame blanking period of the subsequent frame after the frame in which the offset value has been set. Set the offset value for each line using the VMAX_OFFSET register.

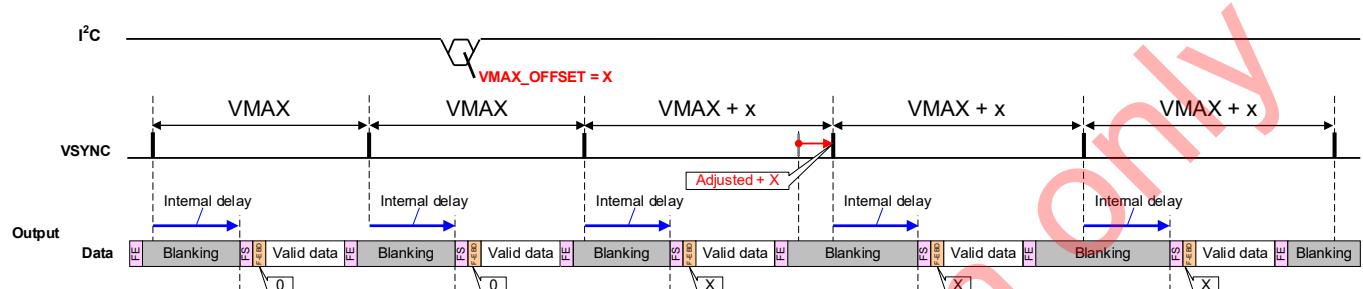


Figure 6-7 Example of the Line Count Extension Function’s Operation

◆ Note

The VMAX_OFFSET register can only be set to an even number.

◇ Memo

- “**Figure 6-7**” illustrates an example of an operation in the case of internal sync. The Line Count Extension function works regardless of the sync method (internal sync, external pulse-based sync and shutter trigger-based sync).
- For details regarding the VMAX (the maximum number of lines of the vertical sync signal), refer to “**5.2.3.2.1 Units of Exposure Time**.”
- The number of lines extended by the Line Count Extension function can be confirmed using the Front Embedded Data. For details, refer to “**6.9.3.5.21 Extended Frame and Extended Line Information**.”

6.1.4. Conditions

6.1.4.1. Condition on External Pulse-Based Synchronization

- Set the value of the IR_DR_SG_VRESET_VDLY register within the range as follows:
 $VMAX - 31 > IR_DR_SG_VRESET_VDLY$

6.1.5. Interface

6.1.5.1. Input Registers

Table 6-4 Input Registers for the Sync Function

[CMN]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A70	3	17:0	VMAX_OFFSET	R/W	U18.0	This register is used to set an offset value (i.e., the number of extended lines) for the VMAX. Only even numbers can be set for each line.

[SG_CTRL]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8AF0	1	1:0	SG_MODE_	R/W	U2.0	This register is used to select the sync method. 0: Internal sync 1: External pulse-based sync 2: Shutter trigger-based sync 3: Setting prohibited
0x8AF1	1	1:0	SG_TRG_AUTOMODE	R/W	U2.0	This register is used to select the autonomous operating mode. 0: Level detection auto mode disabled 1: Level detection auto mode enabled 2 and 3: Setting prohibited

[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBF14	1	1:0	SG_MODE_APL	R/W	U2.0	This register is used to be compared with the SG_MODE_ register for the Application Lock function.

[CONST1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x0144	2	15:0	IR_DR_SG_VRESET_VDLY	R/W	U16.0	This register is used to set the amount of delay for each line after which the sensor begins internal processing in the case of external pulse-based sync. Available range: $VMAX - 31 > IR_DR_SG_VRESET_VDLY$

6.1.5.2. Output Register

Table 6-5 The Output Register for the Sync Function

[STATE]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1F4A	2	15:0	RO_DR_SG_EB_CORRECT	R	S15.0	This register indicates the adjustment level of the vertical sync signal in external pulse-based sync.

6.2. Optical Center Compensation Function

6.2.1. Functional Purpose

If there is a shift between the lens's optical axes and the sensor's output image center, vignetting may occur on the periphery. The Optical Center Compensation function enables the user to change the sensor's pixel readout position in relation to the optical axes of the lens and to align the center of the optical axes with the center of the Active Area.

6.2.2. Functional Overview

The sensor has the Optical Center Compensation Area outside the Active Area. By adjusting the pixel readout position within the Optical Center Compensation Area, the center of the Active Area is aligned with the optical axes of the lens.

"Figure 6-8" illustrates an example of optical center compensation.

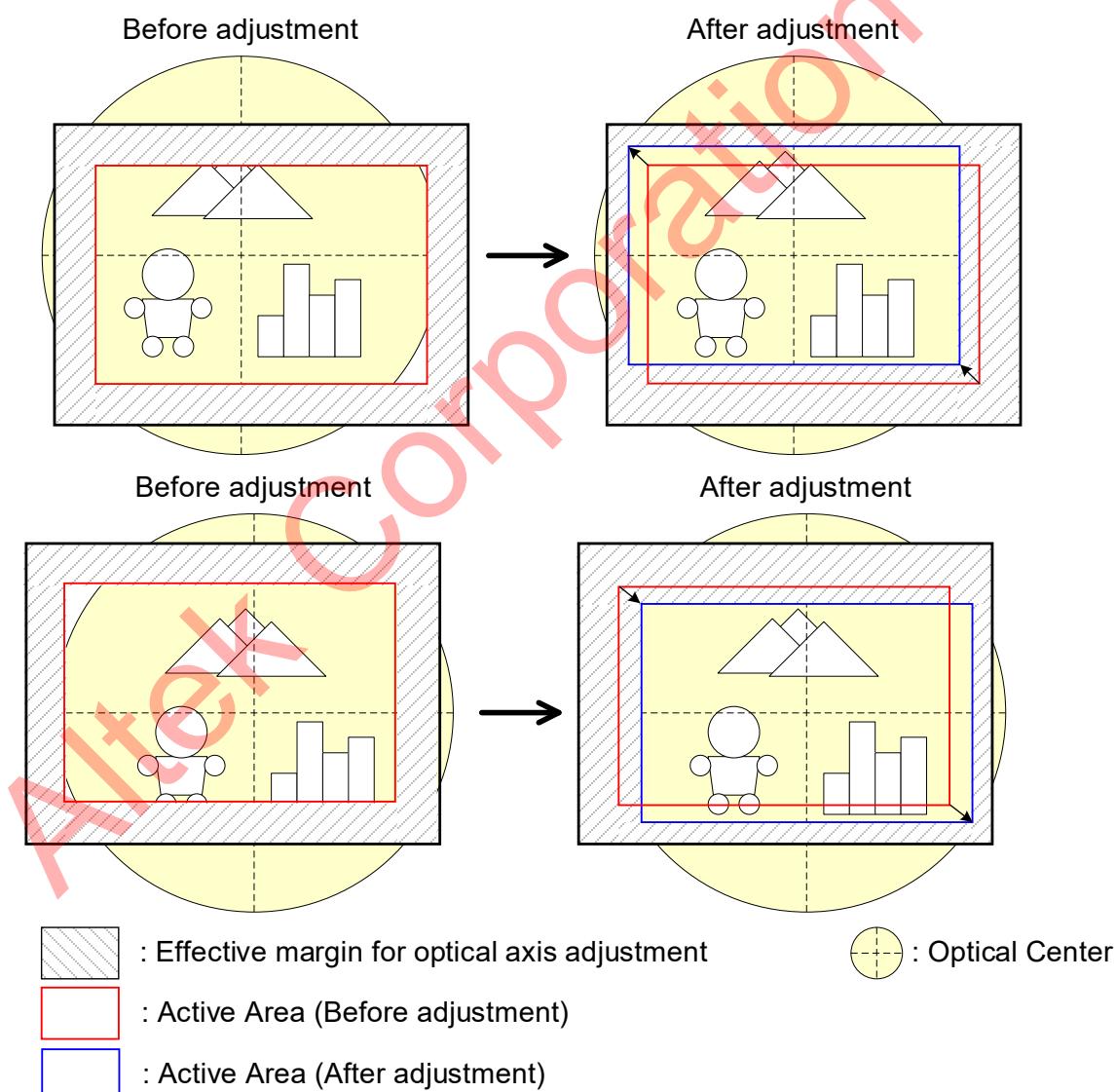


Figure 6-8 Example of Optical Center Compensation

◇ Memo

When optical center compensation is performed, then perform shading compensation.

6.2.3. Functional Specifications

6.2.3.1. Setting the Registers Used to Control the Optical Center Compensation Function

Align the center of the Active Area with the center of the optical axes by using the following registers while the sensor is in Start-up:

- WND_SHIFT_H register for the horizontal setting
- WND_SHIFT_V register for the vertical setting

The WND_SHIFT_H_ and WND_SHIFT_V_ registers are compatible with the Application Lock function. For details, refer to “**3.1.5 Application Lock Function**.”

◆ Note

The settings of the WND_SHIFT_H_ and WND_SHIFT_V_ registers cannot be changed while the sensor is in Streaming. Reset the sensor by performing one of the following:

- Change the corresponding register's value while the sensor is in Start-up State.
- Update the Serial NOR Flash device after changing the corresponding register's value.

The Optical Center Compensation Area is determined by the image data size of the drive mode. Set the area that is a multiple of 2 and within the ranges as shown in “**Table 6-6**.”

Table 6-6 The Optical Center Compensation Area

Active Area (Width x Height)	Compensation Area	
	Horizontal [Pixel]	Vertical [Line]
1936 x 1552	±28	±28

◇ Memo

To start up the sensor with the changed value(s) applied, write these values to the Serial NOR Flash device in accordance with the procedure as described in “**4.9.2 When Writing the Current Register Value(s) to the Serial NOR Flash Device**.”

■ Horizontal/Vertical Flip Function and Optical Center Compensation

When the values of the WND_SHIFT_H and WND_SHIFT_V registers have been changed, the shift direction of the pixel readout position varies depending on the settings of the Horizontal/Vertical Flip function.

“**Figure 6-9**” illustrates the change in the pixel readout position when individually setting the WND_SHIFT_H and WND_SHIFT_V registers to negative values.

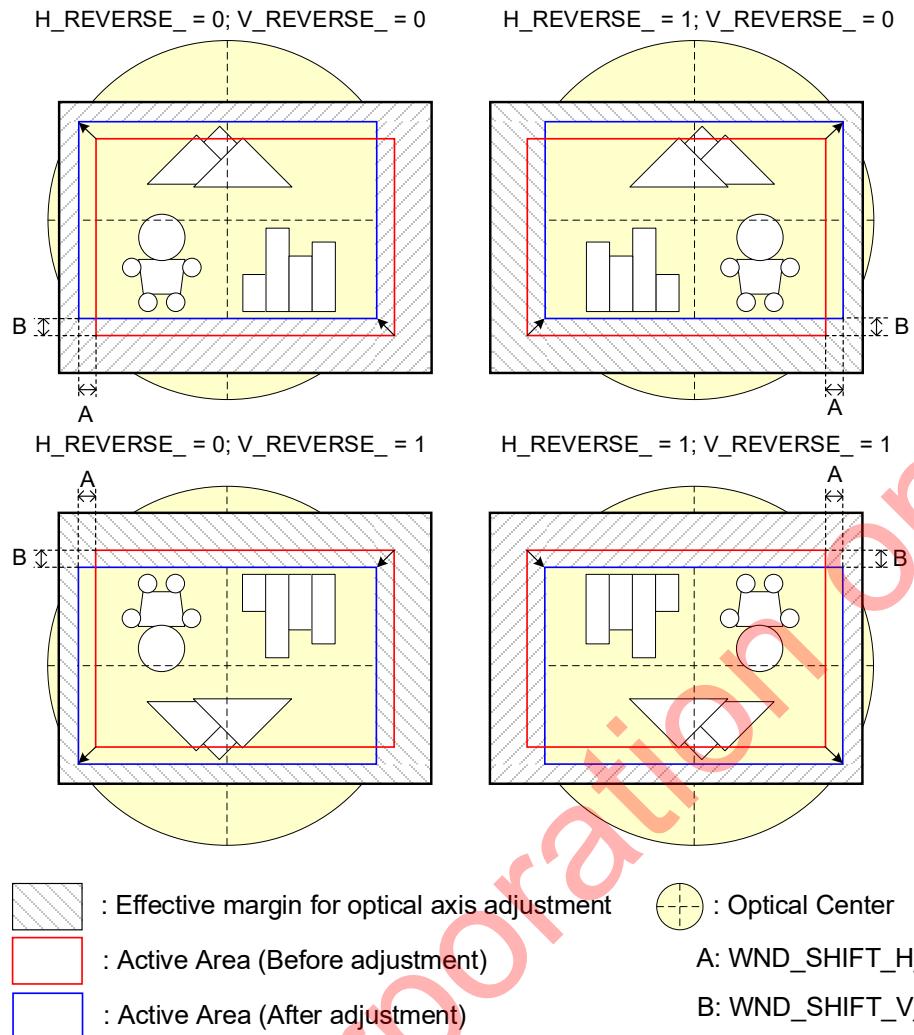


Figure 6-9 Horizontal/Vertical Flip Function and Optical Center Compensation

◇ Memo

For details regarding the Horizontal/Vertical Flip function, refer to “**6.3 Horizontal/Vertical Flip Function.**”

6.2.4. Interface

6.2.4.1. Input Registers

Table 6-7 Input Registers for the Optical Center Compensation Function

[CONFIG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A40	2	15:0	WND_SHIFT_H_	R/W	S15.0	<p>This register is used to set the number of pixels to shift the readout position horizontally.</p> <ul style="list-style-type: none"> Negative values shift the position to the left and positive values shift the position to the right. In the case of horizontal flipping, negative values shift the position to the right and positive values shift the position to the left. <p>Condition: Set a value that is a multiple of 2.</p>
0x8A42	2	15:0	WND_SHIFT_V_	R/W	S15.0	<p>This register is used to set the number of Lines to shift the readout position vertically.</p> <ul style="list-style-type: none"> Negative values shift the position upward and positive values shift the position downward. In the case of vertical flipping, negative values shift the position downward and positive values shift the position upward. <p>Condition: Set a value that is a multiple of 2.</p>

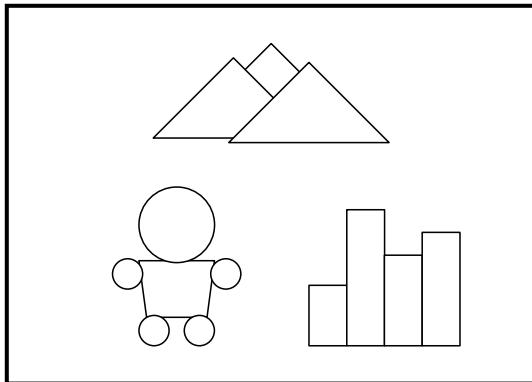
[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBEF8	2	15:0	WND_SHIFT_H_APL	R/W	S15.0	This register is used to be compared with the WND_SHIFT_H_ register for the Application Lock function.
0xBEFA	2	15:0	WND_SHIFT_V_APL	R/W	S15.0	This register is used to be compared with the WND_SHIFT_V_ register for the Application Lock function.

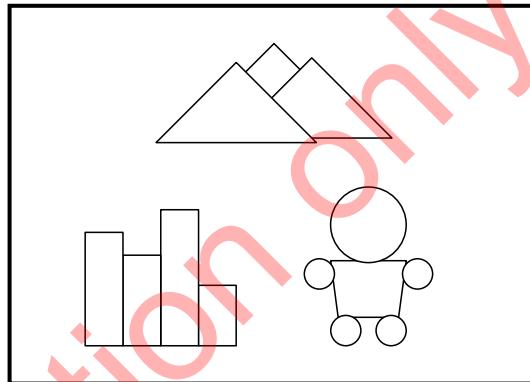
6.3. Horizontal/Vertical Flip Function

6.3.1. Functional Purpose

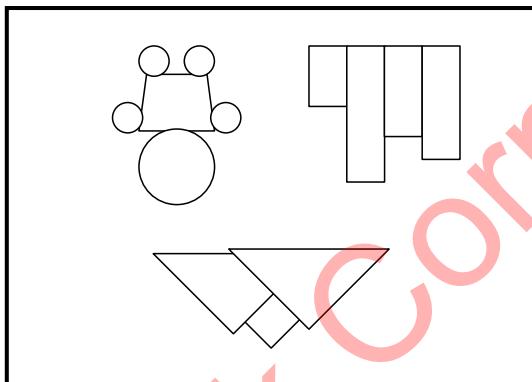
The Horizontal/Vertical Flip function can flip output images horizontally or vertically at the user's discretion. **Figure 6-10** illustrates the function's executions. For example, when the sensor is installed flipped from the upper-left image of **Figure 6-10** by 180 degrees, the Horizontal/Vertical Flip function enables the sensor to read out the image data regardless of the sensor's installation orientation.



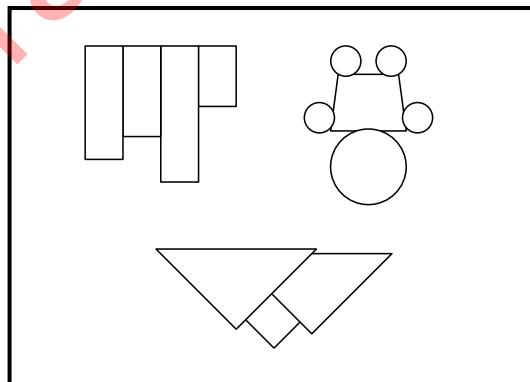
H_REVERSE_= 0
V_REVERSE_= 0



H_REVERSE_= 1
V_REVERSE_= 0



H_REVERSE_= 0
V_REVERSE_= 1



H_REVERSE_= 1
V_REVERSE_= 1



: Image data

Figure 6-10 Examples of the Horizontal/Vertical Flip Function's Operations

6.3.2. Functional Overview

The Horizontal/Vertical Image Flip function can flip output images horizontally and vertically at the user's discretion by switching the image's readout start position and the readout direction. As described in “**Table 6-8**,” the readout direction of the image changes by a flip operation. However, regardless of flip directions, the color filter of the first pixel to be read out the one that has been selected using the First Pixel Color Selection function. For details, refer to “**6.5 First Pixel Color Selection Function.**”

Table 6-8 Changes to the Readout Direction Due to Flip Operations

Name	Description
Horizontal flipping	The pixel area to be read out is shifted horizontally by one pixel.
Vertical flipping	The pixel area to be read out is shifted vertically by one pixel.
Horizontal and vertical flipping	The pixel area to be read out is shifted horizontally and vertically by one pixel each.

“**Figure 6-11**” illustrates the readout in the case of flipping an image horizontally, vertically and both “horizontally and vertically.”

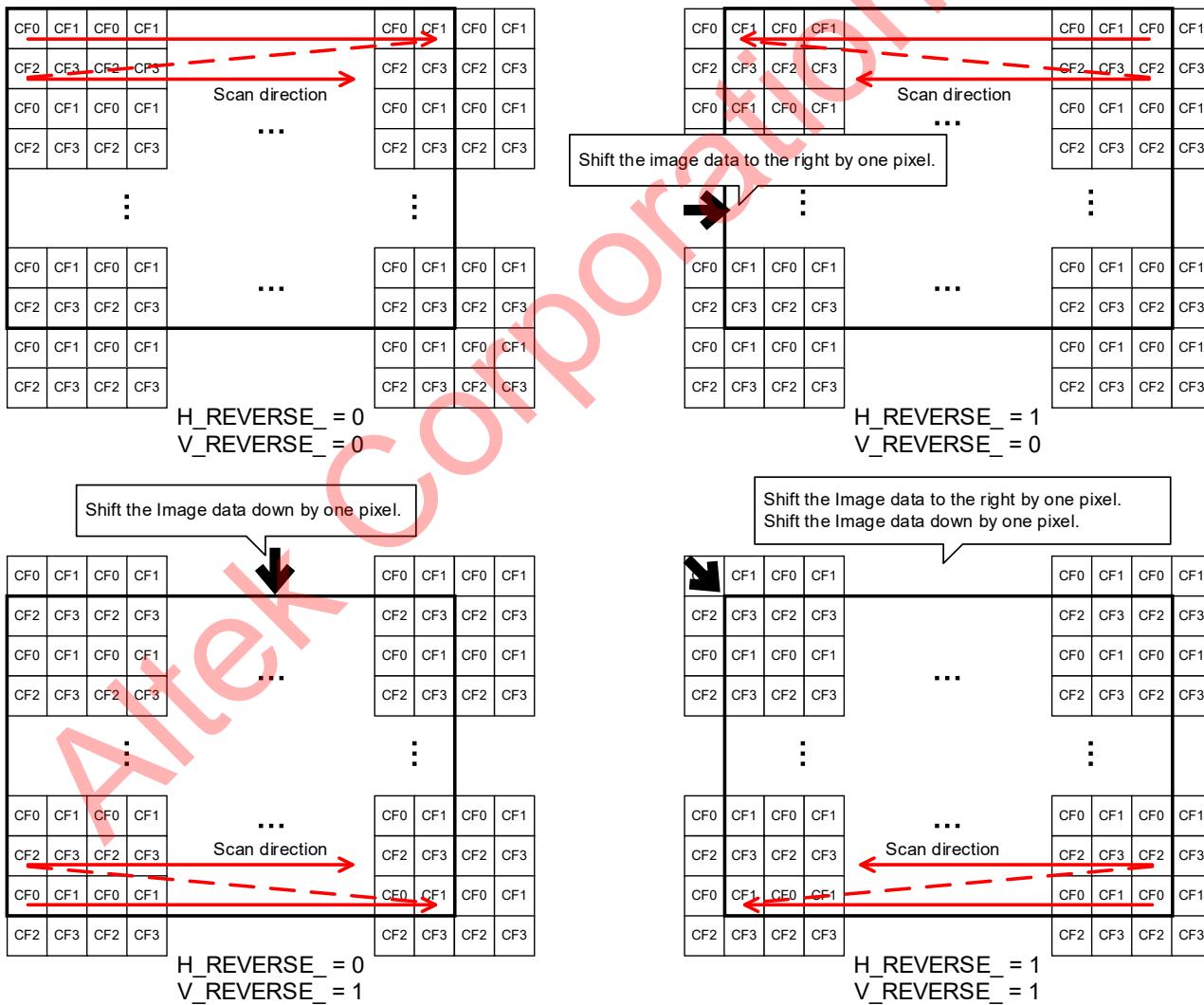


Figure 6-11 Example of Image Readout After Executing Horizontal/Vertical Flipping

6.3.3. Functional Specifications

6.3.3.1. Setting the Horizontal/Vertical Flip Function's Control Registers

The Horizontal/Vertical Flip function can be controlled using the H_REVERSE_ and V_REVERSE_ registers. When setting horizontal flipping, write 0x4 to the address 0x1810 [4:0]. In addition, to restore the image orientation from horizontally flipped to normal, write 0x1 to the address 0x1810 [4:0].

The H_REVERSE_ and V_REVERSE_ registers are compatible with the Application Lock function. For details, refer to “[3.1.5 Application Lock Function](#).”

◆ **Note**

The settings of the H_REVERSE_ register, the V_REVERSE_ register and the address 0x1810[4:0] cannot be changed while the sensor is in Streaming State. Reset the sensor by performing one of the following:

- Change the corresponding register's value while the sensor is in Start-up State.
- Update the Serial NOR Flash device after changing the corresponding register's value.

6.3.4. Interface

6.3.4.1. Input Registers

Table 6-9 Input Registers for the Horizontal/Vertical Flip Function

[CMN]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A68	1	0	H_REVERSE_	R/W	U1.0	Horizontal flipping 0: Flipping disabled 1: Flipping enabled
0x8A69	1	0	V_REVERSE_	R/W	U1.0	Vertical flipping 0: Flipping disabled 1: Flipping enabled

[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBEFE	1	0	H_REVERSE_APL	R/W	U1.0	This register is used to be compared with the H_REVERSE_ register for the Application Lock function.
0xBEFF	1	0	V_REVERSE_APL	R/W	U1.0	This register is used to be compared with the V_REVERSE_ register for the Application Lock function.

6.4. Crop Function

6.4.1. Functional Purpose

The Crop function crops the desired area of the sensor's output image.

6.4.2. Functional Overview

The Crop function produces image output with the desired angle of view, by setting the crop position and crop size from the image data size.

- Adjust the value of each register so that the final output image size is greater than or equal to 320 x 240, which is the minimum output image size of the Crop function.
- For the relationship between the drive mode and the image data size, refer to “[Table 2-20](#).”

6.4.3. Functional Specifications

6.4.3.1. Setting the Control Registers for the Crop Function

To enable this function, set the registers shown in “[Table 6-10](#).”

The registers shown in “[Table 6-10](#)” are compatible with the Application Lock function. For details, refer to “[3.1.5 Application Lock Function](#).”

Table 6-10 Control Registers for the Crop Function

Settings	Register Name
Enabling or disabling the Crop function	DCROP_ON_register
Crop start position	DCROP_HOFFSET_register for the horizontal setting DCROP_VOFFSET_register for the vertical setting
Crop size	DCROP_HSIZE_register for the horizontal setting DCROP_VSIZE_register for the vertical setting

◆ **Note**

- When changing the registers in “[Table 6-10](#)” while the sensor is in Start-up State, set the DCROP_DATA_SEL register to 1.
- Set the crop size using the aforementioned registers so that the crop area is within the image size.
- Set the crop start position and crop size using values that are multiples of 2. However, when the output format for the drive mode is RAW14, set the horizontal crop size using a value that is a multiple of 4.

“[Figure 6-12](#)” illustrates an example of cropping an image.

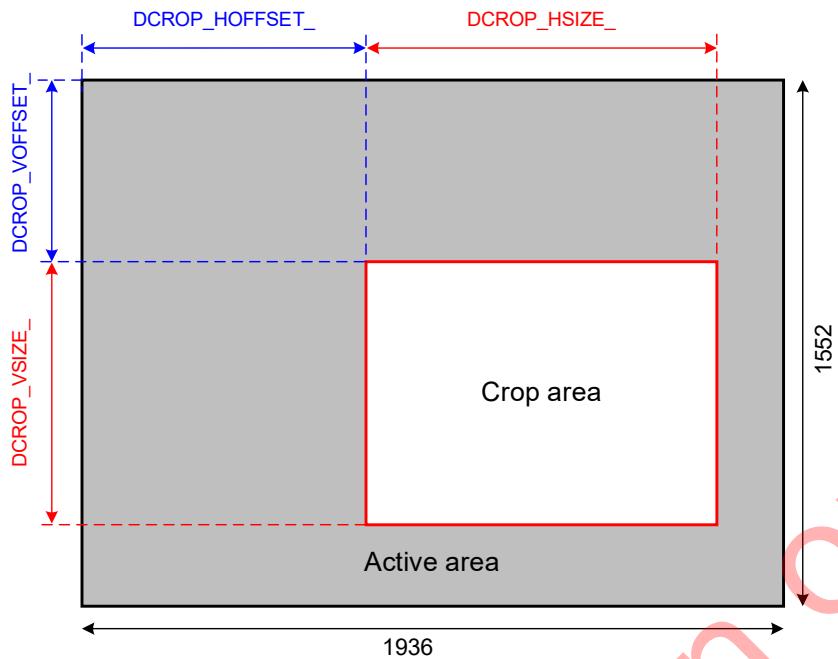


Figure 6-12 Example of a Cropped Image

6.4.3.2. Data Output After Cropping an Image

6.4.3.2.1. MIPI CSI-2

"Figure 6-13" illustrates an example of image output when executing the Crop function in the case of MIPI CSI-2 output.

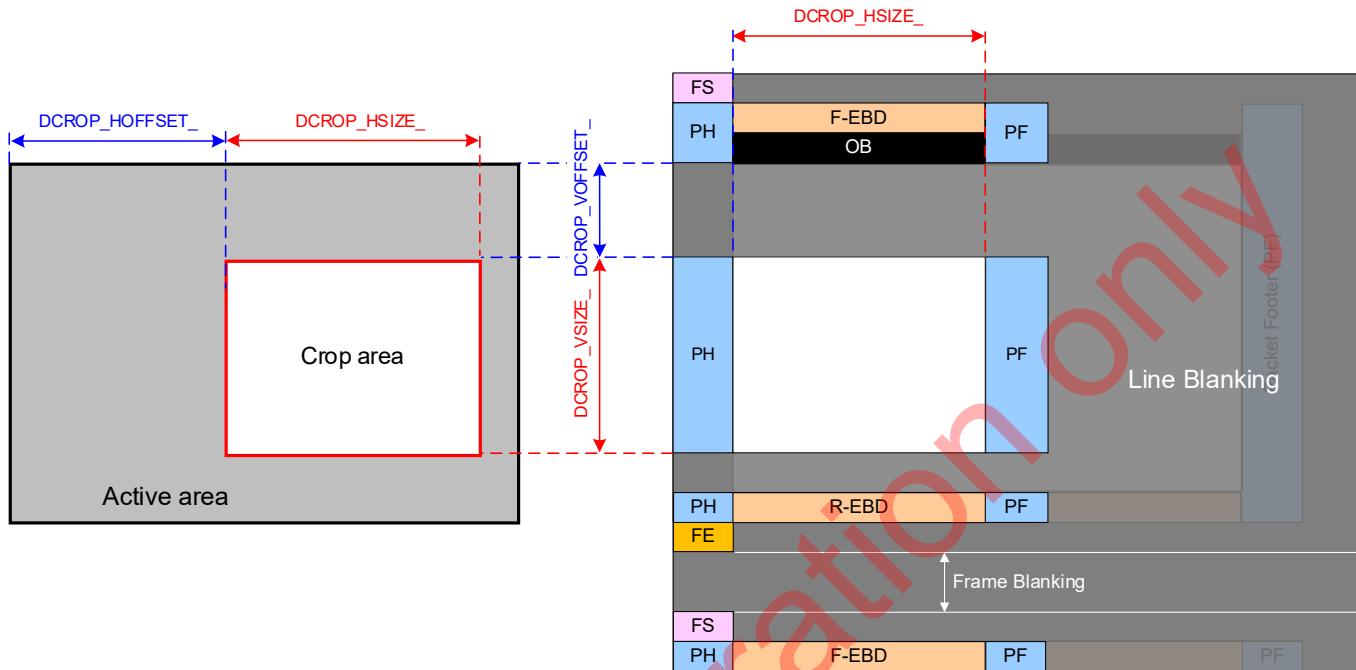


Figure 6-13 Example of MIPI CSI-2 Output When Executing the Crop Function

The sensor outputs a cropped image as follows, corresponding to the direction of cropping:

- When cropping an image vertically, lines which are not transmitted change into line blanking output.
- In the case of horizontal cropping, the cropped image is condensed from the left side of the cropped image for output. For this reason, the line blanking period following each output line becomes longer.

6.4.4. Interface

6.4.4.1. Input Registers

Table 6-11 Input Registers for the Crop Function

[CMN]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8AA8	1	0	DCROP_ON_	R/W	U1.0	This register is used to enable or disable the Crop function. 0: Disabled 1: Enabled
0x8AAA	2	11:0	DCROP_HSIZE_	R/W	U12.0	This register is used to set the Horizontal output image size of a crop area. Condition: Set a value that is a multiple of 2. When the output format for the drive mode is RAW14, set the horizontal crop size using a value that is a multiple of 4.
0x8AAC	2	11:0	DCROP_HOFFSET_	R/W	U12.0	This register is used to set the horizontal offset value of a crop area. Condition: Set a value that is a multiple of 2.
0x8AAE	2	13:0	DCROP_VSIZE_	R/W	U14.0	This register is used to set the vertical output image size of a crop area. Condition: Set a value that is a multiple of 2.
0x8AB0	2	13:0	DCROP_VOFFSET_	R/W	U14.0	This register is used to set the vertical offset value of a crop area. Condition: Set a value that is a multiple of 2.

[SYS_CTRL]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8ADA	1	0	DCROP_DATA_SEL	R/W	U1.0	This register is used to select the value for the Crop function while the sensor is in Start-up State. 0: The initial value corresponding to the drive mode 1: The value of the registers in order for the sensor to control the Crop function

[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBF04	1	0	DCROP_ON_APL	R/W	U1.0	This register is used to be compared with the DCROP_ON_ register for the Application Lock function.
0xBF06	2	11:0	DCROP_HSIZE_APL	R/W	U12.0	This register is used to be compared with the DCROP_HSIZE_ register for the Application Lock function.
0xBF08	2	11:0	DCROP_HOFFSET_APL	R/W	U12.0	This register is used to be compared with the DCROP_HOFFSET_ register for the Application Lock function.
0xBF0A	2	13:0	DCROP_VSIZE_APL	R/W	U14.0	This register is used to be compared with the DCROP_VSIZE_ register for the Application Lock function.
0xBF0C	2	13:0	DCROP_VOFFSET_APL	R/W	U14.0	This register is used to be compared with the DCROP_VOFFSET_ register for the Application Lock function.

6.5. First Pixel Color Selection Function

6.5.1. Functional Purpose

The First Pixel Color Selection function enables the user to select the type of color filter that specifies the first pixel from which the sensor begins reading in the Active Area (Analog Crop).

6.5.2. Functional Overview

The user can select a color filter from the following four types to define the pixel from which the sensor begins reading. As illustrated in “**Figure 6-14**,” when the settings are changed, the starting pixel to be read out is shifted.

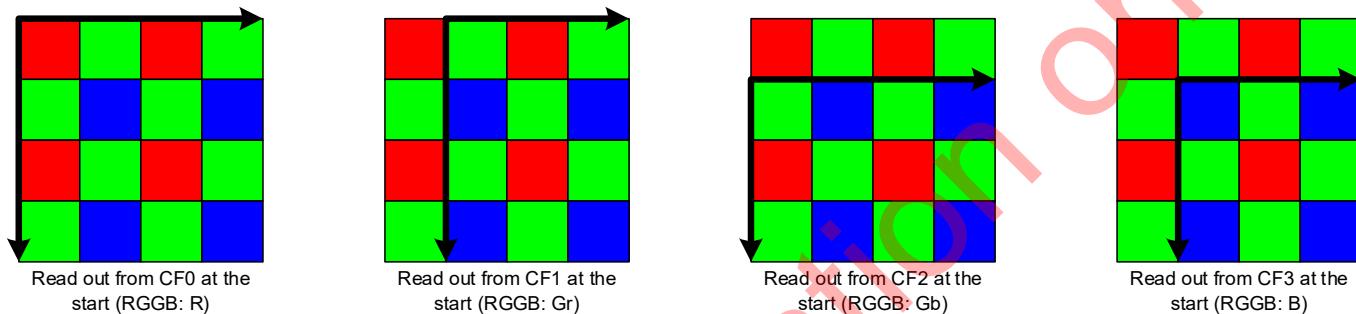


Figure 6-14 The Readout Directions When the First Pixel Is Selected (In the Case of RGGB)

6.5.3. Functional Specifications

The First Pixel Color Selection function enables the user to select the desired color for the first pixel from among the pixel colors, which constitute the color filter. To change the first pixel color, configure the LID_, BID_, and OBBID_ registers as shown in “**Table 6-12**.”

◆ **Note**

The OBBID register is used to set the first pixel color in the OB Area. Be sure to assign the same value to this register as that of the BID register.

Table 6-12 Pixel Colors for Register Settings

LID_	BID_	OBBID_	First Pixel
0	0	0	CF0
0	1	1	CF1
1	0	0	CF2
1	1	1	CF3

The LID_, BID_, and OBBID_ registers are compatible with the Application Lock function. For details, refer to “**3.1.5 Application Lock Function**.”

6.5.3.1. Horizontal/Vertical Image Flipping When the First Pixel Color Selection Function Is Selected

When changing the first pixel color, the area to be read also changes corresponding to the settings of the first pixel color in cases where an image is flipped horizontally and/or vertically.

For details, see “**Figure 6-15.**” For details regarding the Horizontal/Vertical Flip function, refer to “**6.3 Horizontal/Vertical Flip Function.**”

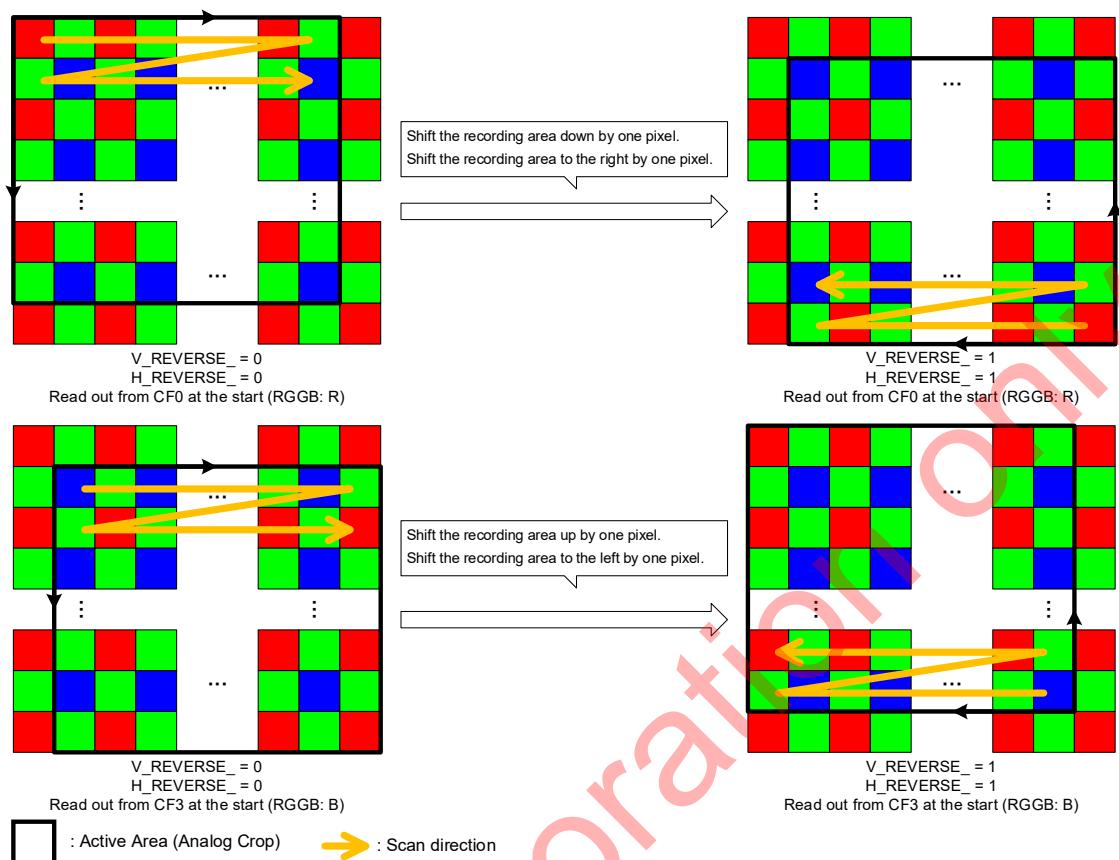


Figure 6-15 Horizontal/Vertical Flipping When the First Pixel Color Is Changed (In the Case of RGGB)

6.5.4. Conditions

Change the first pixel color to satisfy the following condition:

- The values of the BID_ and OBBID_ registers are the same.

6.5.5. Interface

6.5.5.1. Input Registers

Table 6-13 Input Registers for the First Pixel Color Selection Function

[CMN]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A6A	1	0	LID_	R/W	U1.0	This register is used to select the first pixel color in the Active Area (Analog Crop) in the combination of the BID_ register. (LID, BID_): First pixel color (0, 0): CF0 (0, 1): CF1 (1, 0): CF2 (1, 1): CF3
0x8A6C	1	0	BID_	R/W	U1.0	This register is used to select the first pixel color in the Active Area (Analog Crop) in the combination of the LID_ register. (LID, BID_): First pixel color (0, 0): CF0 (0, 1): CF1 (1, 0): CF2 (1, 1): CF3
0x8A6D	1	0	OBBID_	R/W	U1.0	This register is used to select the first pixel color in the OB Area. 0: CF0 and CF2 1: CF1 and CF3

[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBF0E	1	0	LID_APL	R/W	U1.0	This register is used to be compared with the LID_ register for the Application Lock function.
0xBF10	1	0	BID_APL	R/W	U1.0	This register is used to be compared with the BID_ register for the Application Lock function.
0xBF11	1	0	OBBID_APL	R/W	U1.0	This register is used to be compared with the OBBID_ register for the Application Lock function.

6.6. Interlocking Control Function

6.6.1. Functional Purpose

Configuring the settings corresponding to the illuminance or color temperature enables the host to change the sensor's settings without the host performing real-time control.

6.6.2. Functional Overview

The Interlocking Control function consists of the following two types:

- Illuminance interlocking: This function interlocks some of the sensor's settings with the output information of the Exposure Control function.
- Color temperature interlocking: This function interlocks some of the sensor's settings with the output information of the White Balance function.

◇ Memo

Regarding interlocking control, the information such as illuminance and color temperature, which are the basis for changing the sensor's calculated values, are defined as an interlocking source.

6.6.3. Functional Specifications

6.6.3.1. Illuminance Interlocking

Illuminance interlocking updates the sensor's calculated values by interlocking them with illuminance or analog gain.

"Figure 6-16" illustrates an example of setting illuminance interlocking when the sensor's calculated values increase as the illuminance, which is the interlocking source, increases.

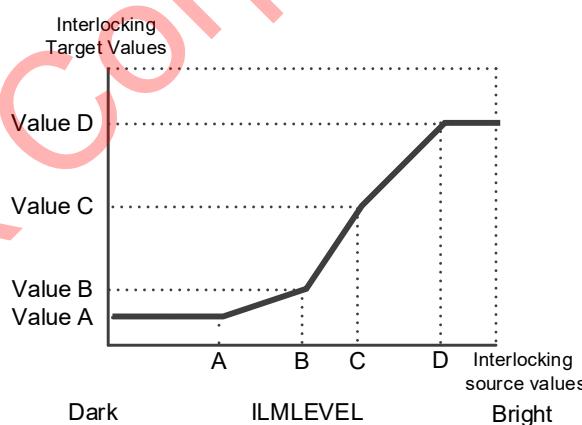


Figure 6-16 Example of Setting Illuminance Interlocking When the Interlocking Source Is the ILMLEVEL Register

To perform illuminance interlocking, set the desired four points (A, B, C and D) for an interlocking source and their corresponding values (Value A, Value B, Value C and Value D). The sensor performs linear interpolation using these four points to calculate the values of the interlocking targets, corresponding to the interlocking sources.

6.6.3.1.1. Setting interlocking source(s)

For illuminance interlocking, the user can set the output information of the Exposure Control function as the interlocking source information. “**Table 6-14**” shows the interlocking source information that can be set for illuminance interlocking. For the information of the interlocking source with the suffix “_STB,” use the value with the IIR filter applied.

Table 6-14 Interlocking Source Information that can Be Set for Illuminance Interlocking

Information of Interlocking Sources	Register Values	Conditions	Unit
THERM	0	$A \geq B \geq C \geq D$	[°C]
THERM_STB	1		[°C]
ILMLEVEL	2	$A \leq B \leq C \leq D$	0.7525 [dB]
ILMLEVEL_STB	3		0.7525 [dB]
DARK_LEVEL	4	$A \geq B \geq C \geq D$	0.3 [dB]
DARK_LEVEL_STB	5		0.3 [dB]
AELEVEL	6	$A \geq B \geq C \geq D$	0.7525 [dB]
AELEVEL_STB	7		0.7525 [dB]
SHT_TIME_SP1	8	$A \geq B \geq C \geq D$	0.1 [ms]
SHT_TIME_SP2	9		0.1 [ms]
SENS_GAIN_SP1H	10	$A \geq B \geq C \geq D$	0.1 [dB]
SENS_GAIN_SP1L	12		0.1 [dB]
SENS_GAIN_SP2H	14	$A \geq B \geq C \geq D$	0.1 [dB]
SENS_GAIN_SP2L	16		0.1 [dB]
AGC_GAIN_SP1H	18	$A \geq B \geq C \geq D$	0.1 [dB]
AGC_GAIN_SP1L	20		0.1 [dB]
AGC_GAIN_SP2H	22	$A \geq B \geq C \geq D$	0.1 [dB]
AGC_GAIN_SP2L	24		0.1 [dB]
MANUAL_LEVELx (x = 1 to 8)	27 to 34	None	-

Set the information about interlocking sources to be used, by using the following registers:

- 2-point interlocking (using A and B): INTERLOCK2_TYPEEx (x = 0 to 3)
- 4-point interlocking (using A, B, C and D): INTERLOCK4_TYPEEx (x = 0 to 19)

After setting the information, set the following registers to the four points (A, B, C and D) corresponding to each interlocking source:

- 2-point interlocking: GAIN2_TH_y_TYPEEx(y = A, B)(x = 0 to 3)
- 4-point interlocking: GAIN4_TH_y_TYPEEx(y = A, B, C, D)(x = 0 to 19)

Note

When setting the aforementioned four points, be sure to satisfy the conditions shown in “**Table 6-14**.”

■ Example of configuring the settings of registers

“**Figure 6-17**” illustrates an example in which the INTERLOCK4_TYPE1 register is set to 2 and the INTERLOCK4_TYPE2 register is set to 6.

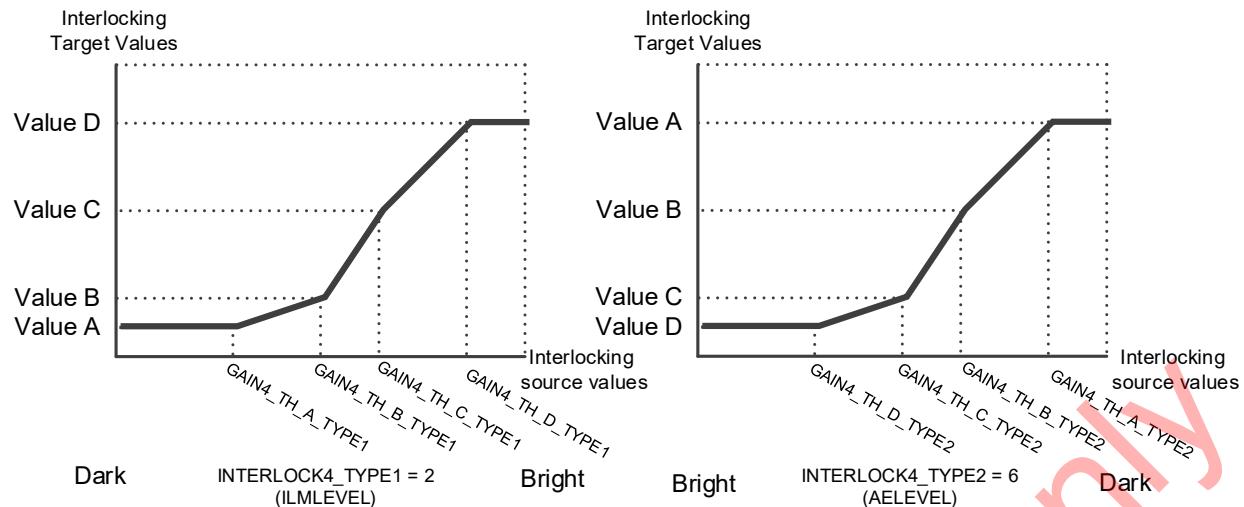


Figure 6-17 Example of Setting Interlocking Source(s)

6.6.3.1.2. Setting the interlocking type

The user can set the interlocking type for each function that is controlled by illuminance interlocking. The interlocking type is the name of the interlocking source settings, configured using the INTERLOCKx_TYPEy (x = 2, 4)(y = 0 to 19) registers as described in “[6.6.3.1.1 Setting interlocking source\(s\)](#).” When selecting the interlocking type for each function, set the registers shown in “[Table 6-15](#)” to the suffix x of the INTERLOCK4_TYPEx (x = 0 to 19) or INTERLOCK2_TYPEx (x = 0 to 3) register.

Table 6-15 Registers for Selecting the Interlocking Type of Illuminance Interlocking

Register for the Interlocking Type	The Function to Be Interlocked
RNR_COEF4_01_IL_TYPE_SEL	“ 5.5 RAW Noise Reduction Function ”
SHD_GAIN4_01_IL_TYPE_SEL	“ 5.9 Lens Shading Compensation Function ”

■ Example of configuring the settings of registers

To use the interlocking source set in the INTERLOCK4_TYPE4 register for the Lens Shading Compensation function as the interlocking type, set the SHD_GAIN4_01_IL_TYPE_SEL register to 4.

■ When not performing illuminance interlocking:

When not performing illuminance interlocking, set the registers in “[Table 6-15](#)” to 0xFF. With this setting, the value of the representative point A will become valid regardless of the interlocking source. See “[Figure 6-18](#)” for details.



Figure 6-18 Illuminance Interlocking Control Disabled

6.6.3.2. Color Temperature Interlocking Function

Color temperature interlocking updates the sensor's calculated values by interlocking them with the values for white balance control. To perform color temperature interlocking, configure the settings using the R/G-B/G coordinate system. The R/G axis represents the ratio of red to green whereas the B/G axis represents the ratio of blue to green. "Figure 6-19" illustrates an example of setting color temperature interlocking.

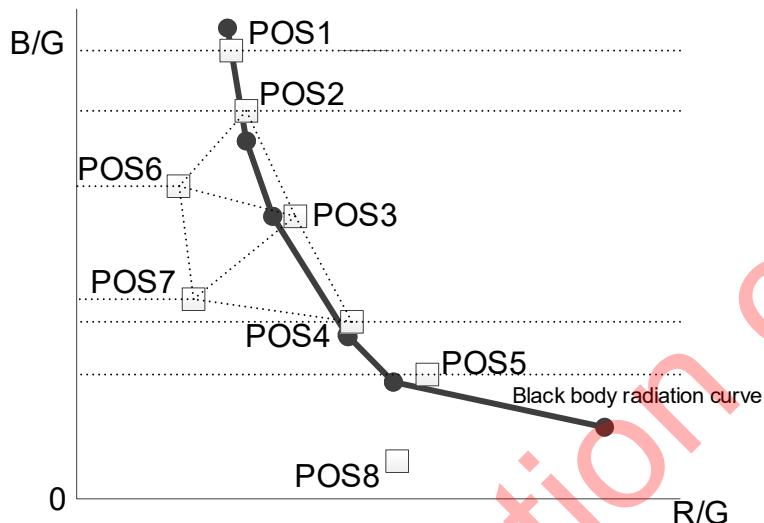


Figure 6-19 Example of Setting Color Temperature Interlocking

To perform color temperature interlocking, set the eight points (POS1 to POS8) to identify the light source and set the interlocking method. The sensor calculates values from the white balance control value and these eight points in accordance with the interlocking method.

6.6.3.2.1. Identifying the light source

The sensor identifies the source using the eight points from POS1 to POS8. Set these eight points in the target area in the R/G-B/G coordinate system. For POS8, unlike the other seven points, set the pull-in area together with the coordinates of itself. Set the registers shown in "Table 6-16" from POS1 to POS8.

Table 6-16 Registers for Setting the Representative Points and Areas for Color Temperature Interlocking

POS	Register Name	Description
POS1 to POS7	POSx_R (x = 1 to 7)	This register is used to set the R/G coordinate of POSx (x = 1 to 7).
	POSx_B (x = 1 to 7)	This register is used to set the B/G coordinate value of POSx (x = 1 to 7).
POS8	POS8_R	This register is used to set the R/G coordinate of POS8.
	POS8_B	This register is used to set the B/G coordinate of POS8.
	POS8_WIDTH_UP_R	This register is used to set the pull-in area for POS8. This register is used to set the right-side width between the coordinate center and the inner frame in the R/G direction.
	POS8_WIDTH_DOWN_R	This register is used to set the pull-in area for POS8. This register is used to set the left-side width between the coordinate center and the inner frame in the R/G direction.
	POS8_OFFSET_UP_R	This register is used to set the pull-in area for POS8.

POS	Register Name	Description
		This register is used to set the right-side width between the inner and outer frames in the R/G direction.
	POS8_OFFSET_DOWN_R	This register is used to set the pull-in area for POS8. This register is used to set the left-side width between the inner and outer frames in the R/G direction.
	POS8_WIDTH_UP_B	This register is used to set the pull-in area for POS8. This register is used to set the upper-side width between the coordinate center and the inner frame in the B/G direction.
	POS8_WIDTH_DOWN_B	This register is used to set the pull-in area for POS8. This register is used to set the lower-side width between the coordinate center and the inner frame in the B/G direction.
	POS8_OFFSET_UP_B	This register is used to set the pull-in area for POS8. This register is used to set the upper-side width between the inner and outer frames in the B/G direction.
	POS8_OFFSET_DOWN_B	This register is used to set the pull-in area for POS8. This register is used to set the lower-side width between the inner and outer frames in the B/G direction.

“Figure 6-20” illustrates an example of register settings for the coordinates and areas for light source identification in the R/G-B/G coordinate system.

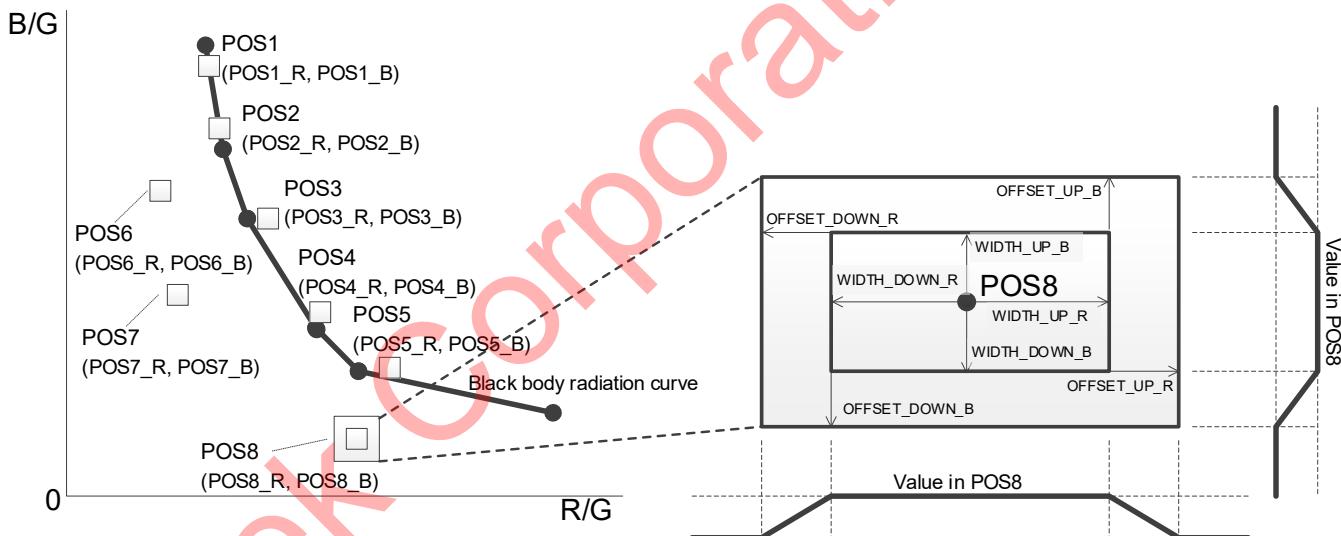


Figure 6-20 Example of Register Settings for the Coordinates and Areas to Identify the Light Source

The POS8 area consists of the inner and outer frames. The following describes the calculate methods corresponding to the area where the control value of the White Balance function is present:

- When the control value is present inside the inner frame, use POS8.
- When the control value is present between the inner and outer frames, use the neighboring POSs and POS8.
- When the control value is present outside the outer frame, use the neighboring POSs excluding POS8.

For details regarding how to configure the settings, refer to the IMX623-AA** "Image Tuning Manual."

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6.6.3.2.2. The Interlocking Method for Color Temperature Interlocking

The user can set the interlocking method for each function that is controlled by color temperature interlocking. "Table 6-17" shows the interlocking method for color temperature interlocking.

Table 6-17 Interlocking Method for Color Temperature Interlocking

Number	Interlocking Method
0	Use the value of POS8
1	Use the value of POS1
2	Use the value of POS2
...	...
8	Use the value of POS8
9	The interlocking function applies the value calculated by the sensor from the relationship between the white balance control values and "POS1 to POS7."
10	The interlocking function applies the value calculated by the sensor from the relationship between the white balance control values and "POS1 to POS8."

6.6.4. Interface

6.6.4.1. Input Registers

Table 6-18 Input Registers for the Interlocking Control Function

[PICT_INTERLOCKTYPE]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB304	1	7:0	INTERLOCK4_TYPE0	R/W	U8.0	<p>This register is used to set the source parameter for illuminance interlocking. (For Type 0 for 4-point interlocking)</p> <p>0: THERM 1: THERM_STB 2: ILMLEVEL 3: ILMLEVEL_STB 4: DARK_LEVEL 5: DARKLEVEL_STB 6: AELEVEL 7: AELEVEL_STB 8: SHT_TIME_SP1 9: SHT_TIME_SP2 10: SENS_GAIN_SP1H 12: SENS_GAIN_SP1L 14: SENS_GAIN_SP2H 16: SENS_GAIN_SP2L 18: AGC_GAIN_SP1H 20: AGC_GAIN_SP1L 22: AGC_GAIN_SP2H 24: AGC_GAIN_SP2L 27: MANUAL_LEVEL1 28: MANUAL_LEVEL2 29: MANUAL_LEVEL3 30: MANUAL_LEVEL4 31: MANUAL_LEVEL5 32: MANUAL_LEVEL6 33: MANUAL_LEVEL7 34: MANUAL_LEVEL8</p> <p>Any other settings are prohibited.</p>
0xB305	1	7:0	INTERLOCK4_TYPE1	R/W	U8.0	<p>This register is used to set the source parameter for illuminance interlocking. (For Type 1 for 4-point interlocking)</p> <p>0: THERM 1: THERM_STB 2: ILMLEVEL 3: ILMLEVEL_STB 4: DARK_LEVEL 5: DARKLEVEL_STB 6: AELEVEL 7: AELEVEL_STB 8: SHT_TIME_SP1 9: SHT_TIME_SP2 10: SENS_GAIN_SP1H 12: SENS_GAIN_SP1L 14: SENS_GAIN_SP2H 16: SENS_GAIN_SP2L 18: AGC_GAIN_SP1H 20: AGC_GAIN_SP1L 22: AGC_GAIN_SP2H 24: AGC_GAIN_SP2L 27: MANUAL_LEVEL1 28: MANUAL_LEVEL2 29: MANUAL_LEVEL3 30: MANUAL_LEVEL4 31: MANUAL_LEVEL5 32: MANUAL_LEVEL6 33: MANUAL_LEVEL7</p>

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
						34: MANUAL_LEVEL8 Any other settings are prohibited.
...	
0xB317	1	7:0	INTERLOCK4_TYPE19	R/W	U8.0	This register is used to set the source parameter for illuminance interlocking. (For Type 19 for 4-point interlocking) 0: THERM 1: THERM_STB 2: ILMLEVEL 3: ILMLEVEL_STB 4: DARK_LEVEL 5: DARKLEVEL_STB 6: AELEVEL 7: AELEVEL_STB 8: SHT_TIME_SP1 9: SHT_TIME_SP2 10: SENS_GAIN_SP1H 12: SENS_GAIN_SP1L 14: SENS_GAIN_N_SP2H 16: SENS_GAIN_SP2L 18: AGC_GAIN_SP1H 20: AGC_GAIN_SP1L 22: AGC_GAIN_SP2H 24: AGC_GAIN_SP2L 27: MANUAL_LEVEL1 28: MANUAL_LEVEL2 29: MANUAL_LEVEL3 30: MANUAL_LEVEL4 31: MANUAL_LEVEL5 32: MANUAL_LEVEL6 33: MANUAL_LEVEL7 34: MANUAL_LEVEL8 Any other settings are prohibited.
0xB318	1	7:0	INTERLOCK2_TYPE0	R/W	U8.0	This register is used to set the source parameter for illuminance interlocking. (For Type 0 for 2-point interlocking) 0: THERM 1: THERM_STB 2: ILMLEVEL 3: ILMLEVEL_STB 4: DARK_LEVEL 5: DARKLEVEL_STB 6: AELEVEL 7: AELEVEL_STB 8: SHT_TIME_SP1 9: SHT_TIME_SP2 10: SENS_GAIN_SP1H 12: SENS_GAIN_SP1L 14: SENS_GAIN_SP2H 16: SENS_GAIN_SP2L 18: AGC_GAIN_SP1H 20: AGC_GAIN_SP1L 22: AGC_GAIN_SP2H 24: AGC_GAIN_SP2L 27: MANUAL_LEVEL1 28: MANUAL_LEVEL2 29: MANUAL_LEVEL3 30: MANUAL_LEVEL4 31: MANUAL_LEVEL5 32: MANUAL_LEVEL6 33: MANUAL_LEVEL7 34: MANUAL_LEVEL8 Any other settings are prohibited.
0xB319	1	7:0	INTERLOCK2_TYPE1	R/W	U8.0	This register is used to set the source parameter for illuminance interlocking. (For Type 1 for 2-point interlocking) 0: THERM

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
						1: THERM_STB 2: ILMLEVEL 3: ILMLEVEL_STB 4: DARK_LEVEL 5: DARKLEVEL_STB 6: AELEVEL 7: AELEVEL_STB 8: SHT_TIME_SP1 9: SHT_TIME_SP2 10: SENS_GAIN_SP1H 12: SENS_GAIN_SP1L 14: SENS_GAIN_SP2H 16: SENS_GAIN_SP2L 18: AGC_GAIN_SP1H 20: AGC_GAIN_SP1L 22: AGC_GAIN_SP2H 24: AGC_GAIN_SP2L 27: MANUAL_LEVEL1 28: MANUAL_LEVEL2 29: MANUAL_LEVEL3 30: MANUAL_LEVEL4 31: MANUAL_LEVEL5 32: MANUAL_LEVEL6 33: MANUAL_LEVEL7 34: MANUAL_LEVEL8 Any other settings are prohibited.
0xB31A	1	7:0	INTERLOCK2_TYPE2	R/W	U8.0	This register is used to set the source parameter for illuminance interlocking. (For Type 2 for 2-point interlocking) 0: THERM 1: THERM_STB 2: ILMLEVEL 3: ILMLEVEL_STB 4: DARK_LEVEL 5: DARKLEVEL_STB 6: AELEVEL 7: AELEVEL_STB 8: SHT_TIME_SP1 9: SHT_TIME_SP2 10: SENS_GAIN_SP1H 12: SENS_GAIN_SP1L 14: SENS_GAIN_SP2H 16: SENS_GAIN_SP2L 18: AGC_GAIN_SP1H 20: AGC_GAIN_SP1L 22: AGC_GAIN_SP2H 24: AGC_GAIN_SP2L 27: MANUAL_LEVEL1 28: MANUAL_LEVEL2 29: MANUAL_LEVEL3 30: MANUAL_LEVEL4 31: MANUAL_LEVEL5 32: MANUAL_LEVEL6 33: MANUAL_LEVEL7 34: MANUAL_LEVEL8 Any other settings are prohibited.
0xB31B	1	7:0	INTERLOCK2_TYPE3	R/W	U8.0	This register is used to set the source parameter for illuminance interlocking. (For Type 3 for 2-point interlocking) 0: THERM 1: THERM_STB 2: ILMLEVEL 3: ILMLEVEL_STB 4: DARK_LEVEL 5: DARKLEVEL_STB 6: AELEVEL 7: AELEVEL_STB 8: SHT_TIME_SP1

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
						9: SHT_TIME_SP2 10: SENS_GAIN_SP1H 12: SENS_GAIN_SP1L 14: SENS_GAIN_SP2H 16: SENS_GAIN_SP2L 18: AGC_GAIN_SP1H 20: AGC_GAIN_SP1L 22: AGC_GAIN_SP2H 24: AGC_GAIN_SP2L 27: MANUAL_LEVEL1 28: MANUAL_LEVEL2 29: MANUAL_LEVEL3 30: MANUAL_LEVEL4 31: MANUAL_LEVEL5 32: MANUAL_LEVEL6 33: MANUAL_LEVEL7 34: MANUAL_LEVEL8 Any other settings are prohibited.
0xB31C	1	7:0	GAIN4_TH_A_TYPE0	R/W	U8.0	This register is used to set Point A for the source parameter which is set by using the INTERLOCK4_TYPE0.
0xB31D	1	7:0	GAIN4_TH_B_TYPE0	R/W	U8.0	This register is used to set Point B for the source parameter which is set by using the INTERLOCK4_TYPE0.
0xB31E	1	7:0	GAIN4_TH_C_TYPE0	R/W	U8.0	This register is used to set Point C for the source parameter which is set by using the INTERLOCK4_TYPE0.
0xB31F	1	7:0	GAIN4_TH_D_TYPE0	R/W	U8.0	This register is used to set Point D for the source parameter which is set by using the INTERLOCK4_TYPE0.
0xB320	1	7:0	GAIN4_TH_A_TYPE1	R/W	U8.0	This register is used to set Point A for the source parameter which is set by using the INTERLOCK4_TYPE1.
0xB321	1	7:0	GAIN4_TH_B_TYPE1	R/W	U8.0	This register is used to set Point B for the source parameter which is set by using the INTERLOCK4_TYPE1.
0xB322	1	7:0	GAIN4_TH_C_TYPE1	R/W	U8.0	This register is used to set Point C for the source parameter which is set by using the INTERLOCK4_TYPE1.
0xB323	1	7:0	GAIN4_TH_D_TYPE1	R/W	U8.0	This register is used to set Point D for the source parameter which is set by using the INTERLOCK4_TYPE1.
...	
0xB368	1	7:0	GAIN4_TH_A_TYPE19	R/W	U8.0	This register is used to set Point A for the source parameter which is set by using the INTERLOCK4_TYPE19.
0xB369	1	7:0	GAIN4_TH_B_TYPE19	R/W	U8.0	This register is used to set Point B for the source parameter which is set by using the INTERLOCK4_TYPE19.
0xB36A	1	7:0	GAIN4_TH_C_TYPE19	R/W	U8.0	This register is used to set Point C for the source parameter which is set by using the INTERLOCK4_TYPE19.
0xB36B	1	7:0	GAIN4_TH_D_TYPE19	R/W	U8.0	This register is used to set Point D for the source parameter which is set by using the INTERLOCK4_TYPE19.
0xB36C	1	7:0	GAIN2_TH_A_TYPE0	R/W	U8.0	This register is used to set Point A for the source parameter which is set by using the INTERLOCK2_TYPE0.
0xB36D	1	7:0	GAIN2_TH_B_TYPE0	R/W	U8.0	This register is used to set Point B for the source parameter which is set by using the INTERLOCK2_TYPE0.
0xB36E	1	7:0	GAIN2_TH_A_TYPE1	R/W	U8.0	This register is used to set Point A for the source parameter which is set by using the INTERLOCK2_TYPE1.
0xB36F	1	7:0	GAIN2_TH_B_TYPE1	R/W	U8.0	This register is used to set Point B for the source parameter which is set by

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
						using the INTERLOCK2_TYPE1.
0xB370	1	7:0	GAIN2_TH_A_TYPE2	R/W	U8.0	This register is used to set Point A for the source parameter which is set by using the INTERLOCK2_TYPE2.
0xB371	1	7:0	GAIN2_TH_B_TYPE2	R/W	U8.0	This register is used to set Point B for the source parameter which is set by using the INTERLOCK2_TYPE2.
0xB372	1	7:0	GAIN2_TH_A_TYPE3	R/W	U8.0	This register is used to set Point A for the source parameter which is set by using the INTERLOCK2_TYPE3.
0xB373	1	7:0	GAIN2_TH_B_TYPE3	R/W	U8.0	This register is used to set Point B for the source parameter which is set by using the INTERLOCK2_TYPE3.

[PICT_CTRL]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB2C4	2	15:0	POS1_R	R/W	U16.0	This register is used to set the R/G coordinate value of POS1 for color temperature interlocking.
0xB2C6	2	15:0	POS1_B	R/W	U16.0	This register is used to set the B/G coordinate value of POS1 for color temperature interlocking.
0xB2C8	2	15:0	POS2_R	R/W	U16.0	This register is used to set the R/G coordinate value of POS2 for color temperature interlocking.
0xB2CA	2	15:0	POS2_B	R/W	U16.0	This register is used to set the B/G coordinate value of POS2 for color temperature interlocking.
...		
0xB2E0	2	15:0	POS8_R	R/W	U16.0	This register is used to set the R/G coordinate value of POS8 for color temperature interlocking.
0xB2E2	2	15:0	POS8_B	R/W	U16.0	This register is used to set the B/G coordinate value of POS8 for color temperature interlocking.
0xB2E4	2	15:0	POS8_WIDTH_UP_R	R/W	U16.0	This register is used to set the pull-in area of POS8 to be used for color temperature interlocking. This register is used to set the right-side width between the coordinate center and the inner frame in the R/G direction.
0xB2E6	2	15:0	POS8_WIDTH_DOWN_R	R/W	U16.0	This register is used to set the pull-in area of POS8 to be used for color temperature interlocking. This register is used to set the left-side width between the coordinate center and the inner frame in the R/G direction.
0xB2E8	2	15:0	POS8_OFFSET_UP_R	R/W	U16.0	This register is used to set the pull-in area of POS8 to be used for color temperature interlocking. This register is used to set the right-side width between the inner and outer frames in the R/G direction.
0xB2EA	2	15:0	POS8_OFFSET_DOWN_R	R/W	U16.0	This register is used to set the pull-in area of POS8 to be used for color temperature interlocking. This register is used to set the left-side width between the inner and outer frames in the R/G direction.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB2EC	2	15:0	POS8_WIDTH_UP_B	R/W	U16.0	This register is used to set the pull-in area of POS8 to be used for color temperature interlocking. This register is used to set the upper-side width between the coordinate center and the inner frame in the R/G direction.
0xB2EE	2	15:0	POS8_WIDTH_DOWN_B	R/W	U16.0	This register is used to set the pull-in area of POS8 to be used for color temperature interlocking. This register is used to set the lower-side width between the coordinate center and the inner frame in the R/G direction.
0xB2F0	2	15:0	POS8_OFFSET_UP_B	R/W	U16.0	This register is used to set the pull-in area of POS8 to be used for color temperature interlocking. This register is used to set the upper-side width between the inner and outer frames in the R/G direction.
0xB2F2	2	15:0	POS8_OFFSET_DOWN_B	R/W	U16.0	This register is used to set the pull-in area of POS8 to be used for color temperature interlocking. This register is used to set the lower-side width between the inner and outer frames in the R/G direction.
0xB2F6	2	8:0	ILMSCL_STB_COEF	R/W	U1.8	This register is used to set the coefficient to be used for illuminance interlocking. (ILMLEVEL_STB) 0x000: Current value at 100% 0x100: Past value at 100%
0x9C30	1	7:0	MANUAL_LEVEL1	R/W	U8.0	For manual interlocking 1
0x9C31	1	7:0	MANUAL_LEVEL2	R/W	U8.0	For manual interlocking 2
...		
0x9C37	1	7:0	MANUAL_LEVEL8	R/W	U8.0	For manual interlocking 8

6.7. Context Switch Function

6.7.1. Functional Purpose

The Context Switch function enables the user to dynamically switch the sensor's register values by switching the register value tables.

6.7.2. Functional Overview

The Context Switch function can be used after performing the following two operations:

1. Record scene lookup tables by combining user-set values and the registers used to switch these values.
2. Set the method for switching the recorded lookup tables.

There are two methods for switching scene lookup tables as follows:

- User Selection Method: A method in which the user directly selects the scene lookup table ID number.
- Event-Driven Method: A method in which the user switches the scene lookup table ID numbers by interlocking the table ID number with a desired register's value.

6.7.3. Functional Specifications

6.7.3.1. Recording a Scene Lookup Table

A scene lookup table contains four regions: Config, Event, Param and Data. Record each scene lookup table in the following order: Config, Event, Param and then Data Regions.

◇ **Memo**

When using this function, setting the Config, Param and Data Regions is required. In the case of the event-driven method only, setting the Event Region is also required.

6.7.3.1.1. Config Region

The Config Region is five bytes of fixed-length data and set one Config Region to each scene lookup table. "Table 6-19" describes the parameters of the Config Region.

Table 6-19 Config Region

Parameter Name	Size [Bytes]	Description
Scene Set Length	2	<p>Bits [13:0] This parameter is used to set the number of data bytes of a scene lookup table.</p> <ul style="list-style-type: none"> Set the total number of bytes of the Config, Event, Param and Data Regions. <p>Bit 14 (Available only for the event-driven method) This bit is used to enable or disable a scene lookup table. 0: Enabled 1: Disabled</p>
Parameter Number	1	This parameter indicates the number of registers to be specified in the Param Region. Available range: 1 to 255
Data Table Number	1	This parameter indicates the number of data tables to be specified in the Data Region. Available range: 1 to 255
Select Table Number	1	Data table number used by the sensor (0 to 254)
		<ul style="list-style-type: none"> Set 255 when using the event-driven method.

6.7.3.1.2. Event Region

The sensor has a function (Event function) to switch data tables, interlocked with the desired value of the register. “**Table 6-20**” describes the fixed length to be set for the Event Region. “**Table 6-21**” shows the settings for the conditions for an event’s occurrence.

◇ **Memo**

For one scene lookup table, only one parameter from those in “**Table 6-20**” can be set, whereas multiple parameters from those in “**Table 6-21**” can be set.

Table 6-20 Event Region

Parameter Name	Size [Bytes]	Description
Event Length	2	This parameter indicates the total number of bytes of the Event Region.
Event Target Category Number	1	This parameter indicates the register’s category number, which is used as the condition of an event’s occurrence.
Event Target Address Offset	2	This parameter indicates the address offset of the register, which is used as the condition of an event’s occurrence.
Mask Pattern	1	The sensor compares the following: <ul style="list-style-type: none"> The result of the logical conjunction AND operation between the register’s value, which is used as the condition of an event’s occurrence and the user-set Mask Pattern parameter The Event Pattern that is defined in the variable-length part of the Mask Pattern parameter When a register size of 2 bytes or greater is used as an Event target, the lowest-order byte is used for the logical conjunction AND operation.

Table 6-21 Definition Part of the Determination Process in the Event Region

Parameter Name	Size [Bytes]	Description
Event Pattern	1	This parameter is used to compare the following: <ul style="list-style-type: none"> The logical conjunction AND operation between “the lower one byte of the register’s value that is used as “the condition of an event’s occurrence” and “the Mask Pattern parameter” The user-set value for the Event Pattern parameter
Select Table Number	1	This parameter is used to set the data table number to be applied when matches the Event Pattern parameter.

Parameter Name	Size [Bytes]	Description
		Available range: 0 to 254

"Table 6-22" describes an example when switching the data table numbers (0 to 3) corresponding to the user-set value of the first byte of the USER_002 register (Offset: 0x0008) in the User category (Category number 61 (0x3D)).

Table 6-22 Example of Setting the Event Region

Parameter Name	User-Set Value	Description
Event Length	0x000E	This parameter indicates the total number of bytes of the Event Region.
Event Target Category Number	0x3D	This parameter indicates the User category.
Event Target Address Offset	0x0008	This parameter indicates the first byte of the USER_002 register.
Mask Pattern	0xFF	This parameter indicates the value to be used for a logical AND operation.
Event Pattern	0x00	These parameters indicate the following: When a logical AND operation between the first byte of the USER_002 register and the value 0xFF is 0x00, the sensor selects the data table 0.
Select Table Number	0x00	
Event Pattern	0x40	These parameters indicate the following: When a logical AND operation between the first byte of the USER_002 register and the value 0xFF is 0x40, the sensor selects the data table 1.
Select Table Number	0x01	
Event Pattern	0x80	These parameters indicate the following: When a logical AND operation between the first byte of the USER_002 register and the value 0xFF is 0x80, the sensor selects the data table 2.
Select Table Number	0x02	
Event Pattern	0xC0	These parameters indicate the following: When a logical AND operation between the first byte of the USER_002 register and the value 0xFF is 0xC0, the sensor selects the data table 3.
Select Table Number	0x03	

6.7.3.1.3. Param Region

The Param Region consists of the number of registers which is specified using the "Parameter Number." The "Parameter Number" consists of the Config Region multiplied by four bytes.

"Table 6-23" describes the parameters of the Param region.

Table 6-23 Param Region

Parameter Name	Size [Bytes]	Description
Category Number	1	This parameter indicates the category number of the register used to switch settings.
Address Offset	2	This parameter indicates the address offset of the register used to switch settings.
Parameter Byte Length	1	This parameter indicates the byte length of the user-set value to be switched.

6.7.3.1.4. Data Region

The Data Region consists of the number of user-set values. This number is the product of the "Parameter Number" and the "Data Table Number" parameters, both of which are set in the Config Region. Save user-set values in the order: Data Table 0, Data Table 1 of the first register and continue onward. "Table 6-24" describes the parameter of the Data Region.

Table 6-24 Data Region

Parameter Name	Size [Bytes]	Description
Value	1 to 255	This parameter indicates the value of the registers to be switched.

6.7.3.1.5. Saving Scene Lookup Tables

The host is requested to save lookup tables to the register in the SCENE_DATA category. The size of each lookup table is variable.

- Set the first lookup table, starting with the SCENE_DATA_0000 register in the SCENE_DATA category.
- When recording multiple lookup tables, consecutively set the subsequent lookup table at the end of the preceding lookup table. For details, see “[Figure 6-21](#).”

For an example of how to set scene lookup tables, refer to “[6.7.3.3 Example of How to Set Scene Lookup Tables](#).”

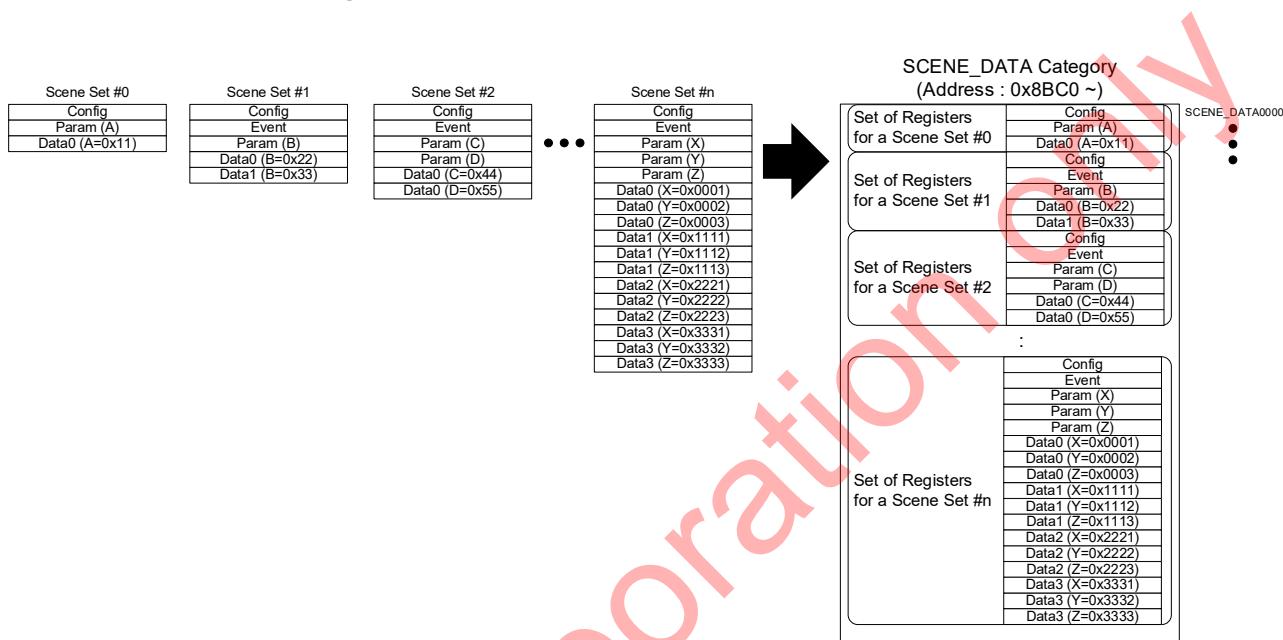


Figure 6-21 Saving Scene Lookup Tables

6.7.3.2. Enabling or Disabling Scene Lookup Tables

When enabling lookup tables, the user can set the size and the number of these tables using the SCN_USER_DATA_SIZE and SCN_USER_SET_NUM registers, respectively. In addition, in the case of the event-driven method only, the user can individually disable lookup tables by setting the value of bit 14 of the Scene Set Length parameter in the Config Region to 1. For details regarding the “Scene Set Length,” refer to “[Table 6-19](#).”

6.7.3.3. Example of How to Set Scene Lookup Tables

The following describes an example of setting two scene lookup tables:

- In the first example, the host sets the AE (Hold) mode for every frame.
- In the second example, the host alternates the AWB (Hold) mode and the ATW mode for every 128 frames.

“[Table 6-25](#)” shows the register settings.

Table 6-25 List of the Registers Used to Set Scene Lookup Tables

Scene Lookup Table ID #	Settings	Register Name	Category No.	Address Offset	User- Set Value	Remark
0	Select AE (Hold)	AEMODE	17 (0x11)	0x0000	1	"5.2.3.1 Exposure Control Methods"
1	Select AWB (Hold)	AWBMODE	34 (0x22)	0x0000	4	"5.3.3.1 Selecting a Method of Adjusting White Balance Gain"
	Select the ATW	AWBMODE	34 (0x22)	0x0000	0	

Check the Frame Count using the DIF_FRMINFO_FRAME_COUNT register.

The DIF_FRMINFO_FRAME_COUNT register has a 4-byte length. In this example, an event occurs when the result of the logical conjunction AND operation between the lowest-order byte of the DIF_FRMINFO_FRAME_COUNT register and the Mask Pattern (0xFF) is either 0x00 or 0x80.

Consequently, the AWB (Hold) mode and the ATW mode switch every 128 frames. "Table 6-26" shows the settings of these two examples.

Table 6-26 Parameter Values for Scene Lookup Tables

Region	Parameter Name	Size [Bytes]	User-Set Value	
			Scene Lookup Table #0	Scene Lookup Table #1
Config Region	Scene Set Length	2	0x000A	0x0015
	Parameter Number	1	0x01	0x01
	Data Table Number	1	0x01	0x02
	Select Table Number	1	0x00	0xFF
Event Region	Event Length	2	-	0x000A
	Event Target Category Number	1	-	0x61
	Event Target Address Offset	2	-	0x0000
	Mask Pattern	1	-	0xFF
	Event Pattern	1	-	0x00
	Select Table Number	1	-	0x00
	Event Pattern	1	-	0x80
	Select Table Number	1	-	0x01
Param Region	Category Number	1	0x11	0x22
	Address Offset	2	0x0000	0x0000
	Parameter Byte Length	1	0x01	0x01
Data Region	Value	1, 2 or 4	0x01	0x04
	Value	1, 2 or 4	-	0x00

When converting user-set values of 2 bytes or greater into the little-endian byte order and then arranging the result, the data string is as follows:

0A, 00, 01, 01, 00, 11, 00, 00, 01, 01, 15, 00, 01, 02, FF, 0A, 00, 61, 00, 00, FF, 00, 00, 80, 01, 22, 00, 00, 01, 04, 00

When separating this data string in units of 4 bytes, it is divided into eight 4-byte data as follows:

0101000A, 00001100, 00150101, 0AFF0201, 00006100, 800000FF, 00002201, 00000401

Save sequentially the 4-byte data from the SCENE_DATA_0000 register.

There are two lookup tables to be set. The total size of the SCENE_DATA category that needs to be set is 32 bytes. Set the SCN_USER_SET_NUM and SCN_USER_DATA_SIZE registers to values corresponding to the number of lookup tables to be added and their sizes respectively.

“**Table 6-27**” lists user-set values for each register.

Table 6-27 Register Values

Category Name (Category No.)	Register Name	User-Set Value
SCENE_DATA (32)	SCENE_DATA_0000	0x0101000A
	SCENE_DATA_0001	0x00001100
	SCENE_DATA_0002	0x00150101
	SCENE_DATA_0003	0x0AFF0201
	SCENE_DATA_0004	0x00006100
	SCENE_DATA_0005	0x800000FF
	SCENE_DATA_0006	0x00002201
	SCENE_DATA_0007	0x00000401
SCENE_CFG (31)	SCN_USER_SET_NUM	0x2
	SCN_USER_DATA_SIZE	0x20

6.7.3.4. The Execution Timing of the Context Switch Function

In general, the Context Switch function is executed for each frame. However, the host can adjust when the sensor executes this function. To perform the Context Switch function at a desired time, the following two settings must be configured:

- Suspend the automatic execution of the Context Switch function.
- Perform the Context Switch function manually.

■ Suspending the automatic execution of the Context Switch function

To suspend the automatic execution of the Context Switch function, set the SCN_LOCK_ENABLE register to 1. With this setting, this function does not operate even when the scene lookup tables are updated.

■ Executing the Context Switch function manually

When the automatic execution of the Context Switch function is suspended, the sensor determines whether to perform this function corresponding to the value of the SCN_DATA_UPDATE register.

As illustrated in “**Figure 6-22**,” every time the host changes the value of the SCN_DATA_UPDATE register, the sensor performs the Context Switch function only in the subsequent frame after the frame in which this value has been changed.

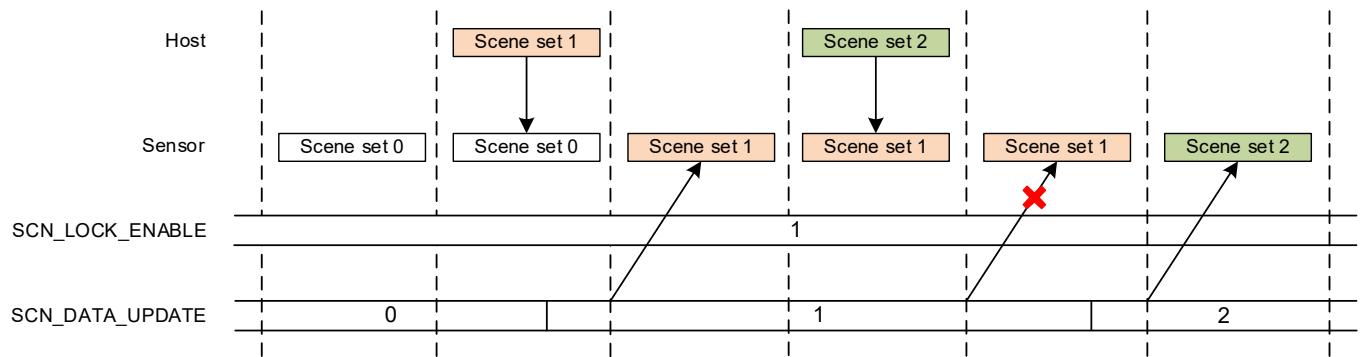


Figure 6-22 Example of Manual Execution of the Context Switch Function

6.7.3.5. N Frame Sequence Function

The N Frame Sequence function assigns an identifier (i.e., Frame ID) to the data tables within each lookup table for switching the data tables using the Frame ID. For the sensor, the host can directly specify the Frame ID or automatically switch Frame IDs for each frame.

By switching Frame IDs automatically for each frame, the host can periodically obtain images with image-capturing conditions switched. For details, see “[Figure 6-23](#).”

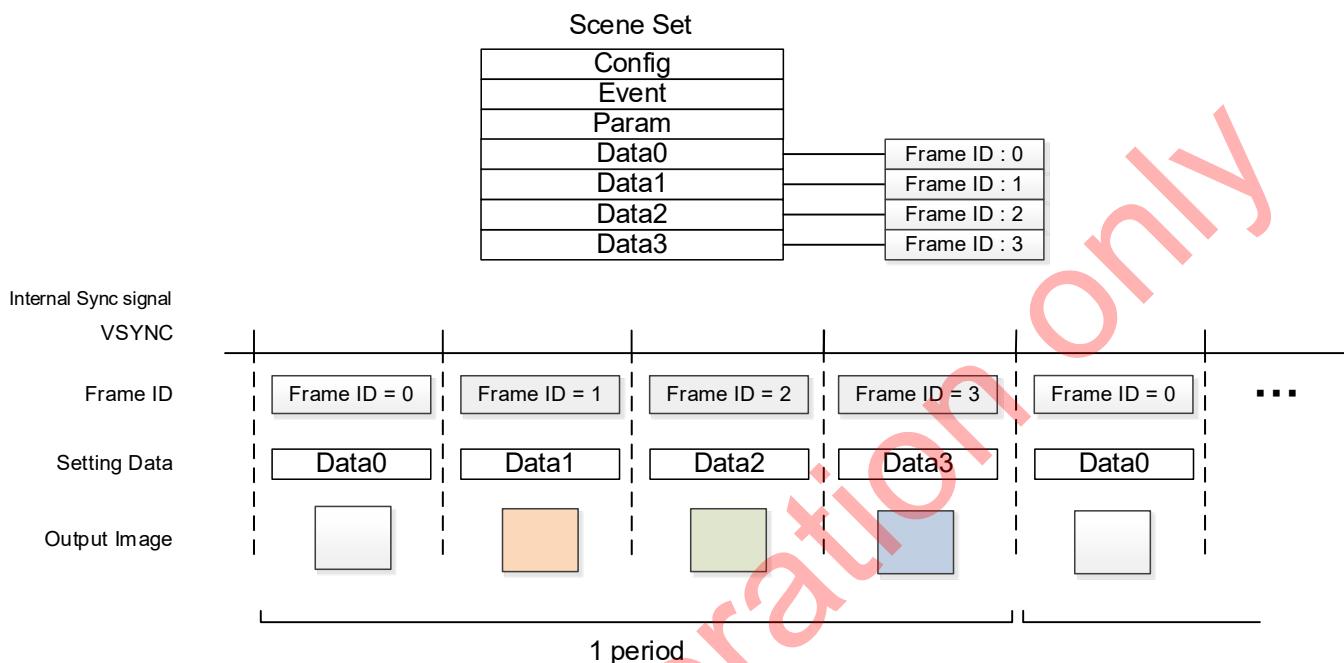


Figure 6-23 Example of the N Frame Sequence Function’s Operations

◇ **Memo**

The VSYNC signal in “[Figure 6-23](#)” is the internal signal that indicates the time when the frames are switched.

6.7.3.5.1. Setting Scene Lookup Tables

“[Table 6-28](#)” shows how to set scene lookup tables for the N Frame Sequence function.

◇ **Memo**

The settings of the Config, Param and Data Regions (excluding the Event Region) are the same as those of a scene lookup table when the event-driven method is used.

Table 6-28 Event Region When the Sensor Performs the N Frame Sequence Function

● Fixed Length

Parameter Name	Size [Bytes]	Description
Event Length	2	This parameter indicates the total number of bytes of the Event Region.
-	1	Fixed at 0x02
-	1	Fixed at 0x27
-	1	Fixed at 0xFF

- Definition Part of the Determination Process in the Event Region

Parameter Name	Size [Bytes]	Description
Frame ID	1	This parameter is used to set the Frame ID. Available range: 0 to 5
Data Table Number	1	This parameter is used to set the data table number to be linked with the Frame ID.

6.7.3.5.2. Frame ID

The Frame ID can be set up to 6 IDs from 0 through 5. As shown in “**Table 6-29**”, to switch the Frame ID, there are two methods:

- The host directly specifies the Frame ID.
- The sensor automatically increments the Frame ID frame by frame. Use the SCN_NFRAME_AUTO_CNT_EN register to select the method.

Table 6-29 The Method to Switch Frame IDs

SCN_NFRAME_AUTO_CNT_EN	Method for Switching Frame IDs	Description
0	Direct	<p>The host directly specifies the Frame ID using the SCN_NFRAME_ID register.</p> <ul style="list-style-type: none"> Unless the host changes the value of the SCN_NFRAME_ID register, the sensor continues to use the Frame ID specified by the host.
1	Automatic incremental method	<p>In this method, the sensor automatically increments the Frame ID to be switched frame by frame.</p> <ul style="list-style-type: none"> The Frame ID is incremented frame by frame starting from 0. When the Frame ID reaches the value of the SCN_NFRAME_MAX register, it reverts to 0 in the subsequent frame and then it continues to be incremented. By setting the SG_NFRM_ID_CLR register to 1, the Frame ID reverts to 0 in a desired time frame.

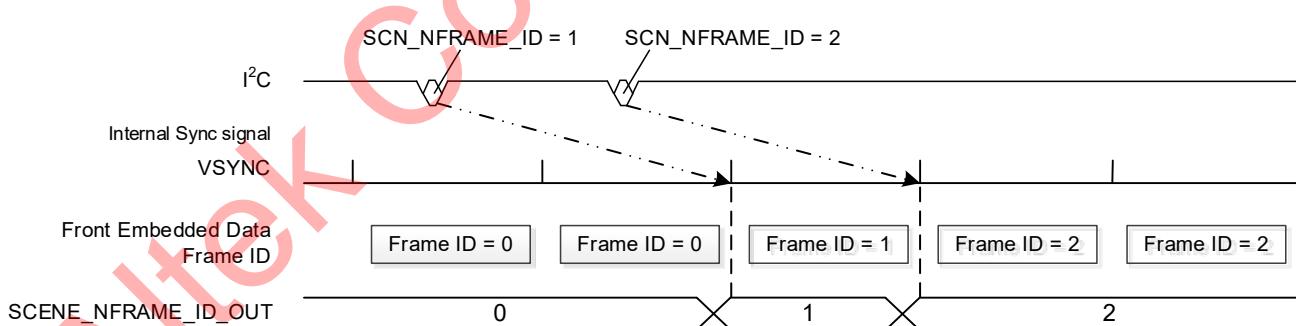


Figure 6-24 Example of the Sensor’s Operation When the Host Directly Specifies the Frame ID (Initial Value of the SCN_NFRAME_ID = 0)

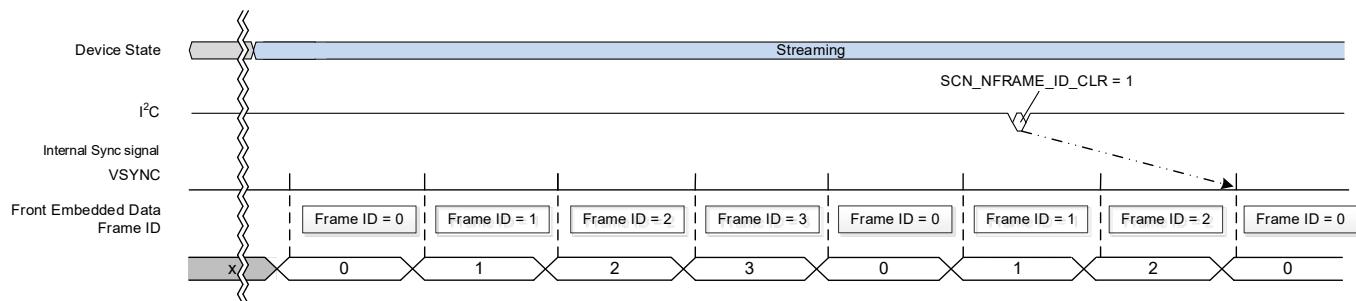


Figure 6-25 Automatic Incremental Method When SCN_NFRAME_MAX = 4

The host can confirm the Frame ID, which has been set by either the host or the sensor, using the SCENE_NFRAME_ID_OUT register of the Front Embedded Data. The host can identify which of the data tables have been applied to the output image, by checking the Frame ID.

◆ **Note**

The method for switching the Frame ID cannot be changed while the sensor is in Streaming State. Reset the sensor by performing one of the following:

- Change the corresponding register's value while the sensor is in Start-up State.
- Update the Serial NOR Flash device after changing the corresponding register's value.

◇ **Memo**

- The VSYNC signal in “**Figure 6-24**” and “**Figure 6-25**” is the internal signal that indicates the time when the frames are switched.
- For details regarding the Front Embedded Data, refer to “**6.9.3.5 Front Embedded Data**.”

6.7.3.5.3. About the Registers, the Address of Which Varies for Each Frame ID

When the N Frame Sequence function is enabled, there are registers with different I²C addresses for each Frame ID. “Table 6-30” lists these registers.

Table 6-30 List of the Registers, the I²C Address of Which Varies for Each Frame ID

Register Name	Register Unit	Bit	Address					
			ID = 0	ID = 1	ID = 2	ID = 3	ID = 4	ID = 5
FME_SHTVAL	4	31:0	0x9C08	0x9C94	0x9D20	0x9DAC	0x9E38	0x9EC4
FME_SHTVAL_UNIT	1	7:0	0x9C0C	0x9C98	0x9D24	0x9DB0	0x9E3C	0x9EC8
FME_SHTVAL_S1	4	31:0	0x9C10	0x9C9C	0x9D28	0x9DB4	0x9E40	0x9ECC
FME_SHTVAL_S1_UNIT	1	7:0	0x9C14	0x9CA0	0x9D2C	0x9DB8	0x9E44	0x9ED0
FME_SESAGAIN	2	9:0	0x9C18	0x9CA4	0x9D30	0x9DBC	0x9E48	0x9ED4
FME_SESAGAIN_S1	2	9:0	0x9C1A	0x9CA6	0x9D32	0x9DBE	0x9E4A	0x9ED6
FME_SESAGAIN_S2	2	9:0	0x9C1C	0x9CA8	0x9D34	0x9DC0	0x9E4C	0x9ED8
FME_SESAGAIN_S3	2	9:0	0x9C1E	0x9CAA	0x9D36	0x9DC2	0x9E4E	0x9EDA
FME_ISPGAIN	2	9:0	0x9C20	0x9CAC	0x9D38	0x9DC4	0x9E50	0x9EDC
NORM_GAIN_Y1	4	31:0	0x9C24	0x9CB0	0x9D3C	0x9DC8	0x9E54	0x9EE0
FULLMWBGAIN_R	2	11:0	0x9C28	0x9CB4	0x9D40	0x9DCC	0x9E58	0x9EE4
FULLMWBGAIN_GR	2	11:0	0x9C2A	0x9CB6	0x9D42	0x9DCE	0x9E5A	0x9EE6
FULLMWBGAIN_GB	2	11:0	0x9C2C	0x9CB8	0x9D44	0x9DD0	0x9E5C	0x9EE8
FULLMWBGAIN_B	2	11:0	0x9C2E	0x9CBA	0x9D46	0x9DD2	0x9E5E	0x9EEA
MANUAL_LEVEL1	1	7:0	0x9C30	0x9CBC	0x9D48	0x9DD4	0x9E60	0x9EEC
...
MANUAL_LEVEL8	1	7:0	0x9C37	0x9CC3	0x9D4F	0x9DDB	0x9E67	0x9EF3
HDR_SGAIN_ADJ_SP1_R	2	14:0	0x9C38	0x9CC4	0x9D50	0x9DDC	0x9E68	0x9EF4
HDR_SGAIN_ADJ_SP1_GR	2	14:0	0x9C3A	0x9CC6	0x9D52	0x9DDE	0x9E6A	0x9EF6
HDR_SGAIN_ADJ_SP1_GB	2	14:0	0x9C3C	0x9CC8	0x9D54	0x9DE0	0x9E6C	0x9EF8
HDR_SGAIN_ADJ_SP1_B	2	14:0	0x9C3E	0x9CCA	0x9D56	0x9DE2	0x9E6E	0x9EFA
HDR_SGAIN_ADJ_SP2_R	2	14:0	0x9C40	0x9CCC	0x9D58	0x9DE4	0x9E70	0x9EFC
HDR_SGAIN_ADJ_SP2_GR	2	14:0	0x9C42	0x9CCE	0x9D5A	0x9DE6	0x9E72	0x9EFE
HDR_SGAIN_ADJ_SP2_GB	2	14:0	0x9C44	0x9CD0	0x9D5C	0x9DE8	0x9E74	0x9F00
HDR_SGAIN_ADJ_SP2_B	2	14:0	0x9C46	0x9CD2	0x9D5E	0x9DEA	0x9E76	0x9F02
HDR_SGAIN_ADJ_SP12_R	2	14:0	0x9C48	0x9CD4	0x9D60	0x9DEC	0x9E78	0x9F04
HDR_SGAIN_ADJ_SP12_GR	2	14:0	0x9C4A	0x9CD6	0x9D62	0x9DEE	0x9E7A	0x9F06
HDR_SGAIN_ADJ_SP12_GB	2	14:0	0x9C4C	0x9CD8	0x9D64	0x9DF0	0x9E7C	0x9F08
HDR_SGAIN_ADJ_SP12_B	2	14:0	0x9C4E	0x9CDA	0x9D66	0x9DF2	0x9E7E	0x9F0A
IR_IS_FBK_LMX_COEF_C00_SP2H	2	9:0	0x9C50	0x9CDC	0x9D68	0x9DF4	0x9E80	0x9F0C
IR_IS_FBK_LMX_COEF_C01_SP2H	2	9:0	0x9C52	0x9CDE	0x9D6A	0x9DF6	0x9E82	0x9F0E
IR_IS_FBK_LMX_COEF_C02_SP2H	2	9:0	0x9C54	0x9CE0	0x9D6C	0x9DF8	0x9E84	0x9F10
IR_IS_FBK_LMX_COEF_C03_SP2H	2	9:0	0x9C56	0x9CE2	0x9D6E	0x9DFA	0x9E86	0x9F12
IR_IS_FBK_LMX_COEF_C10_SP2H	2	9:0	0x9C58	0x9CE4	0x9D70	0x9DFC	0x9E88	0x9F14
IR_IS_FBK_LMX_COEF_C11_SP2H	2	9:0	0x9C5A	0x9CE6	0x9D72	0x9DFE	0x9E8A	0x9F16
IR_IS_FBK_LMX_COEF_C12_SP2H	2	9:0	0x9C5C	0x9CE8	0x9D74	0x9E00	0x9E8C	0x9F18
IR_IS_FBK_LMX_COEF_C13_SP2H	2	9:0	0x9C5E	0x9CEA	0x9D76	0x9E02	0x9E8E	0x9F1A
IR_IS_FBK_LMX_COEF_C20_SP2H	2	9:0	0x9C60	0x9CEC	0x9D78	0x9E04	0x9E90	0x9F1C
IR_IS_FBK_LMX_COEF_C21_SP2H	2	9:0	0x9C62	0x9CEE	0x9D7A	0x9E06	0x9E92	0x9F1E
IR_IS_FBK_LMX_COEF_C22_SP2H	2	9:0	0x9C64	0x9CF0	0x9D7C	0x9E08	0x9E94	0x9F20
IR_IS_FBK_LMX_COEF_C23_SP2H	2	9:0	0x9C66	0x9CF2	0x9D7E	0x9E0A	0x9E96	0x9F22
IR_IS_FBK_LMX_COEF_C30_SP2H	2	9:0	0x9C68	0x9CF4	0x9D80	0x9E0C	0x9E98	0x9F24

Register Name	Register Unit	Bit	Address					
			ID = 0	ID = 1	ID = 2	ID = 3	ID = 4	ID = 5
IR_IS_FBK_LMX_COEF_C31_SP2H	2	9:0	0x9C6A	0x9CF6	0x9D82	0x9E0E	0x9E9A	0x9F26
IR_IS_FBK_LMX_COEF_C32_SP2H	2	9:0	0x9C6C	0x9CF8	0x9D84	0x9E10	0x9E9C	0x9F28
IR_IS_FBK_LMX_COEF_C33_SP2H	2	9:0	0x9C6E	0x9CFA	0x9D86	0x9E12	0x9E9E	0x9F2A
IR_IS_FBK_LMX_COEF_C00_SP2L	2	9:0	0x9C70	0x9CFC	0x9D88	0x9E14	0x9EA0	0x9F2C
IR_IS_FBK_LMX_COEF_C01_SP2L	2	9:0	0x9C72	0x9CFE	0x9D8A	0x9E16	0x9EA2	0x9F2E
IR_IS_FBK_LMX_COEF_C02_SP2L	2	9:0	0x9C74	0x9D00	0x9D8C	0x9E18	0x9EA4	0x9F30
IR_IS_FBK_LMX_COEF_C03_SP2L	2	9:0	0x9C76	0x9D02	0x9D8E	0x9E1A	0x9EA6	0x9F32
IR_IS_FBK_LMX_COEF_C10_SP2L	2	9:0	0x9C78	0x9D04	0x9D90	0x9E1C	0x9EA8	0x9F34
IR_IS_FBK_LMX_COEF_C11_SP2L	2	9:0	0x9C7A	0x9D06	0x9D92	0x9E1E	0x9EAA	0x9F36
IR_IS_FBK_LMX_COEF_C12_SP2L	2	9:0	0x9C7C	0x9D08	0x9D94	0x9E20	0x9EAC	0x9F38
IR_IS_FBK_LMX_COEF_C13_SP2L	2	9:0	0x9C7E	0x9D0A	0x9D96	0x9E22	0x9EAE	0x9F3A
IR_IS_FBK_LMX_COEF_C20_SP2L	2	9:0	0x9C80	0x9D0C	0x9D98	0x9E24	0x9EB0	0x9F3C
IR_IS_FBK_LMX_COEF_C21_SP2L	2	9:0	0x9C82	0x9D0E	0x9D9A	0x9E26	0x9EB2	0x9F3E
IR_IS_FBK_LMX_COEF_C22_SP2L	2	9:0	0x9C84	0x9D10	0x9D9C	0x9E28	0x9EB4	0x9F40
IR_IS_FBK_LMX_COEF_C23_SP2L	2	9:0	0x9C86	0x9D12	0x9D9E	0x9E2A	0x9EB6	0x9F42
IR_IS_FBK_LMX_COEF_C30_SP2L	2	9:0	0x9C88	0x9D14	0x9DA0	0x9E2C	0x9EB8	0x9F44
IR_IS_FBK_LMX_COEF_C31_SP2L	2	9:0	0x9C8A	0x9D16	0x9DA2	0x9E2E	0x9EBA	0x9F46
IR_IS_FBK_LMX_COEF_C32_SP2L	2	9:0	0x9C8C	0x9D18	0x9DA4	0x9E30	0x9EBC	0x9F48
IR_IS_FBK_LMX_COEF_C33_SP2L	2	9:0	0x9C8E	0x9D1A	0x9DA6	0x9E32	0x9EBE	0x9F4A
PWL_CP01_X	3	24:0	0x9F88	0xA0B4	0xA1E0	0xA30C	0xA438	0xA564
PWL_CP01_Y	3	24:0	0x9F8C	0xA0B8	0xA1E4	0xA310	0xA43C	0xA568
...
PWL_CP17_X	3	24:0	0xA008	0xA134	0xA260	0xA38C	0xA4B8	0xA5E4
PWL_CP17_Y	3	24:0	0xA00C	0xA138	0xA264	0xA390	0xA4BC	0xA5E8
AE_WND_OFFSET_H	2	15:0	0xA010	0xA13C	0xA268	0xA394	0xA4C0	0xA5EC
AE_WND_OFFSET_V	2	15:0	0xA012	0xA13E	0xA26A	0xA396	0xA4C2	0xA5EE
AE_WND_SIZE_H	2	15:0	0xA014	0xA140	0xA26C	0xA398	0xA4C4	0xA5F0
AE_WND_SIZE_V	2	15:0	0xA016	0xA142	0xA26E	0xA39A	0xA4C6	0xA5F2
OPD_MASK_EN_00	1	0	0xA018	0xA144	0xA270	0xA39C	0xA4C8	0xA5F4
...
OPD_MASK_EN_07	1	0	0xA01F	0xA14B	0xA277	0xA3A3	0xA4CF	0xA5FB
OPD_MASK_STAH_00	2	11:0	0xA020	0xA14C	0xA278	0xA3A4	0xA4D0	0xA5FC
OPD_MASK_STAV_00	2	11:0	0xA022	0xA14E	0xA27A	0xA3A6	0xA4D2	0xA5FE
OPD_MASK_ENDH_00	2	11:0	0xA024	0xA150	0xA27C	0xA3A8	0xA4D4	0xA600
OPD_MASK_ENDV_00	2	11:0	0xA026	0xA152	0xA27E	0xA3AA	0xA4D6	0xA602
...
OPD_MASK_STAH_07	2	11:0	0xA058	0xA184	0xA2B0	0xA3DC	0xA508	0xA634
OPD_MASK_STAV_07	2	11:0	0xA05A	0xA186	0xA2B2	0xA3DE	0xA50A	0xA636
OPD_MASK_ENDH_07	2	11:0	0xA05C	0xA188	0xA2B4	0xA3E0	0xA50C	0xA638
OPD_MASK_ENDV_07	2	11:0	0xA05E	0xA18A	0xA2B6	0xA3E2	0xA50E	0xA63A
AWB_WND_OFFSET_H	2	15:0	0xA060	0xA18C	0xA2B8	0xA3E4	0xA510	0xA63C
AWB_WND_OFFSET_V	2	15:0	0xA062	0xA18E	0xA2BA	0xA3E6	0xA512	0xA63E
AWB_WND_SIZE_H	2	15:0	0xA064	0xA190	0xA2BC	0xA3E8	0xA514	0xA640
AWB_WND_SIZE_V	2	15:0	0xA066	0xA192	0xA2BE	0xA3EA	0xA516	0xA642
AWB_OPD_MASK_STAH_00	2	11:0	0xA068	0xA194	0xA2C0	0xA3EC	0xA518	0xA644
AWB_OPD_MASK_STAV_00	2	11:0	0xA06A	0xA196	0xA2C2	0xA3EE	0xA51A	0xA646
AWB_OPD_MASK_ENDH_00	2	11:0	0xA06C	0xA198	0xA2C4	0xA3F0	0xA51C	0xA648
AWB_OPD_MASK_ENDV_00	2	11:0	0xA06E	0xA19A	0xA2C6	0xA3F2	0xA51E	0xA64A
...

Register Name	Register Unit	Bit	Address					
			ID = 0	ID = 1	ID = 2	ID = 3	ID = 4	ID = 5
AWB_OPD_MASK_STAH_07	2	11:0	0xA0A0	0xA1CC	0xA2F8	0xA424	0xA550	0xA67C
AWB_OPD_MASK_STAV_07	2	11:0	0xA0A2	0xA1CE	0xA2FA	0xA426	0xA552	0xA67E
AWB_OPD_MASK_ENDH_07	2	11:0	0xA0A4	0xA1D0	0xA2FC	0xA428	0xA554	0xA680
AWB_OPD_MASK_ENDV_07	2	11:0	0xA0A6	0xA1D2	0xA2FE	0xA42A	0xA556	0xA682
AWB_OPD_MASK_EN_00	1	0	0xA0A8	0xA1D4	0xA300	0xA42C	0xA558	0xA684
...
AWB_OPD_MASK_EN_07	1	0	0xA0AF	0xA1DB	0xA307	0xA433	0xA55F	0xA68B

◇ **Memo**

When the sensor does not perform the N Frame Sequence function, each I²C address of the registers shown in “**Table 6-30**” is the value in the Address column when the ID equals 0.

◆ **Note**

The registers shown in “**Table 6-30**” cannot be used for the following functions:

- Context Switch Function
- Information Output Function (Information Regarding Host-Selected Register(s))

6.7.3.6. Executing the Context Switch Function

To enable or disable this function, set the SCN_USER_ENABLE register to 1 or 0, respectively.

6.7.3.7. The Execution Results of the Context Switch Function

The host can check the execution results of the Context Switch function using the value of the registers shown in “**Table 6-31**.”

Table 6-31 Registers that Indicate the Results of the Context Switch Function’s Executions

Register Name	Description
SCENE_USER_CHECK_RESULT	This register indicates the results of the Context Switch function’s executions. 0: No errors 1: Error in the Config Region 2: Error in the Event Region 3: Error in the Param Region 4: Data size error (When the user has not fully entered the data of a scene lookup table) 5: Exceeding data size error (When the user sets the SCN_USER_DATA_SIZE register to a value exceeding 0x7D0 (2000))
SCENE_USER_NFRAME_ID_ERR	This register indicates the result when the sensor checks the Frame ID. 0: No errors 1: Frame ID maximum value error (When the user sets the SCN_NFRAME_MAX register to a value other than 1 to 6) 2: Frame ID setting error (When the value of the SCN_NFRAME_ID register is greater than the value of the SCN_NFRAME_MAX register)
SCENE_USER_ERR_CFG_SET_NUM	This register indicates the ID number of the lookup table in which an error has been detected. • The scene lookup table ID number starts from 0.
SCENE_USER_ERR_EVENT_SET_NUM	This register indicates the index number of the data table that has been designated when an error is

Register Name	Description
	detected. <ul style="list-style-type: none">The data table number starts from 0.
SCENE_USER_ERR_PARAM_SET_NUM	This register indicates the index number of the Param Region that has detected an error. <ul style="list-style-type: none">The Param Region number starts from 0.

The Context Switch function executes processing in ascending order of the scene lookup table ID number. Even if there are errors in multiple lookup tables, the error information transmitted to the registers as shown in “**Table 6-31**” is the first ID number in which the error has been detected.

◇ **Memo**

Even if error information is transmitted, the Context Switch function performs processing on the lookup table with a smaller ID number than the ID number in which the error has been detected. For example, if the user has set three lookup tables (ID #0, #1 and #2) and the sensor has detected an error in the lookup table (ID #1), the Context Switch function does not perform processing on the lookup tables (#1 and #2), but does on the lookup table (ID #0).

6.7.4. Interface

6.7.4.1. Input Registers

Table 6-32 Input Registers for the Context Switch Function

[SCENE_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8B34	1	0	SCN_USER_ENABLE	R/W	U1.0	This register is used to enable or disable the Context Switch function. 0: Disabled 1: Enabled
0x8B35	1	7:0	SCN_USER_SET_NUM	R/W	U8.0	This register indicates the number of valid lookup tables.
0x8B36	2	15:0	SCN_USER_DATA_SIZE	R/W	U16.0	This register indicates a total amount of data of valid lookup tables.
0x8B3E	1	0	SCN_NFRAME_AUTO_CNT_EN	R/W	U1.0	This register is used to enable or disable the automatic incrementing of the Frame ID. 0: Disabled 1: Enabled <i>Available only for the N Frame Sequence function</i>
		7:4	SCN_NFRAME_MAX			This register indicates the number of Frame IDs that the user can set. Available range: 1 to 6
0x8B3F	1	3:0	SCN_NFRAME_ID	R/W	U4.0	The Frame ID to be used for the N Frame Sequence function.
0x8B40	1	0	SCN_NFRAME_ID_CLR	R/W	U1.0	This register is used to enable or disable the sequence in which the Frame ID is reset to 0 and then it continues to be incremented. 0: Disabled 1: Enabled • This register is enabled only when the value of the SCN_NFRAME_AUTO_CNT_EN register is 1.
0x8B41	1	0	SCN_LOCK_ENABLE	R/W	U1.0	This register is used to enable or disable the automatic execution of the Context Switch function. 0: Disabled 1: Enabled
0x8B42	1	7:0	SCN_DATA_UPDATE	R/W	U8.0	After the host changes the value of this register, the sensor updates the scene lookup table and then performs the Context Switch function only once. • This register is enabled only when the value of the SCN_LOCK_ENABLE register is 1.

[SCENE_DATA]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8BC0	4	31:0	SCENE_DATA_0000	R/W	U32.0	The Scene Data Area #0000
0x8BC4	4	31:0	SCENE_DATA_0001	R/W	U32.0	The Scene Data Area #0001
...		
0x9BBC	4	31:0	SCENE_DATA_1023	R/W	U32.0	The Scene Data Area #1023

6.7.4.2. Output Register

Table 6-33 Output Registers for the Context Switch Function

[SYS_SOUT]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x609C	1	7:0	SCENE_USER_CHECK_RESULT	R	U8.0	<p>This register indicates the results of the Context Switch function's executions.</p> <p>0: No errors 1: Error in the Config Region 2: Error in the Event Region 3: Error in the Param Region 4: Data size error (When the user has not fully entered the data of a scene lookup table) 5: Exceeding data size error (When the user sets the SCN_USER_DATA_SIZE register to a value exceeding 0x7D0 (2000))</p>
0x609D	1	7:0	SCENE_USER_NFRAME_ID_ERR	R	U8.0	<p>This register indicates the result when the sensor checks the Frame ID.</p> <p>0: No errors 1: Frame ID maximum value error (When the user sets the SCN_NFRAME_MAX register to a value other than 1 to 6) 2: Frame ID setting error (When the value of the SCN_NFRAME_ID register is greater than the value of the SCN_NFRAME_MAX register)</p>
0x609E	2	15:0	SCENE_USER_ERR_CFG_SET_NUM	R	U16.0	<p>This register indicates the ID number of the lookup table in which an error has been detected.</p> <ul style="list-style-type: none"> The scene lookup table ID number starts from 0.
0x60A0	2	15:0	SCENE_USER_ERR_EVENT_SET_NUM	R	U16.0	<p>This register indicates the index number of the data table that has been designated when an error is detected.</p> <ul style="list-style-type: none"> The data table number starts from 0.
0x60A2	2	15:0	SCENE_USER_ERR_PARAM_SET_NUM	R	U16.0	<p>This register indicates the index number of the Param Region that has detected an error.</p> <ul style="list-style-type: none"> The Param Region number starts from 0.
0x60AF	1	3:0	SCENE_NFRAME_ID_OUT	R	U4.0	Frame ID that is selected by the sensor.

6.8. Output Mask Function

6.8.1. Functional Purpose

With regard to an extended frame immediately after start-up or during extended frames due to a long exposure, the sensor transmits an invalid image. The Output Mask function enables the sensor to notify the host of those invalid images or change (i.e., mask) part of output signals.

6.8.2. Functional Overview

There are three conditions under which the sensor performs the Output Mask function:

- Sensor startup
- The occurrence of extended frames due to long exposure
- Mask settings configured by the host

The output masking method can be selected except for the case in which extended frames are generated due to a long exposure. In addition, the mask period can be set in the mask settings at sensor startup.

The following describes the image output when mask processing is performed by the Output Mask function:

- MIPI CSI-2 Output:

The user can select either "Unmasked image output," "Muted image output" or "No output of MIPI CSI-2 frames (No image output.)"

Muted images are images generated by the sensor with the same image sizes as the captured images to transmit, instead of images captured by the sensor.

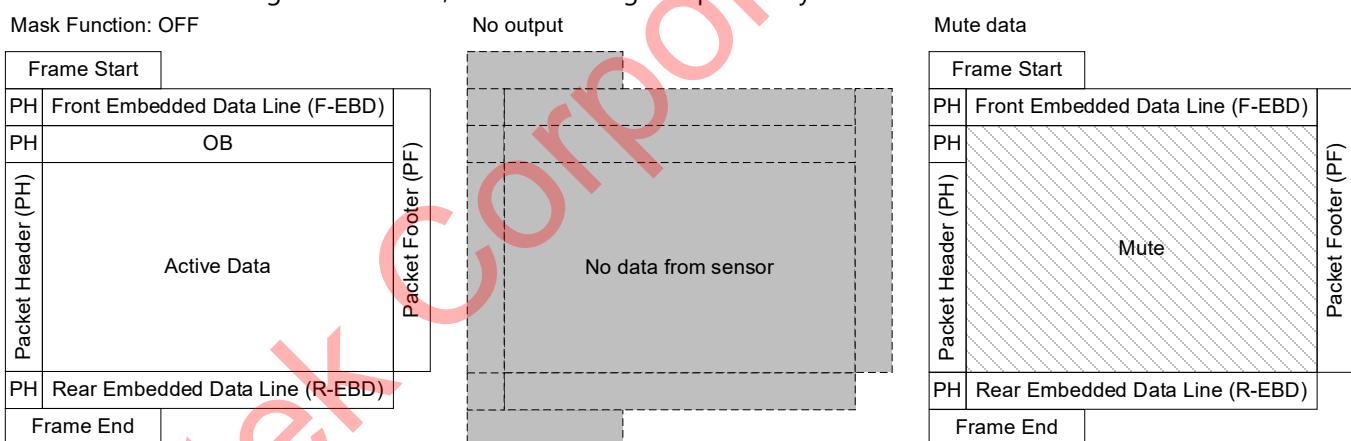


Figure 6-26 Output Mask Processing Methods for MIPI CSI-2 Output

6.8.3. Functional Specifications

6.8.3.1. Startup Mask Function

The Startup Mask function can mask invalid output images immediately after the sensor transitions to Streaming. This function controls masking by dividing this transition into the following two periods:

- Period 1: This function masks all output signals.
- Period 2: This function masks the Data Type.

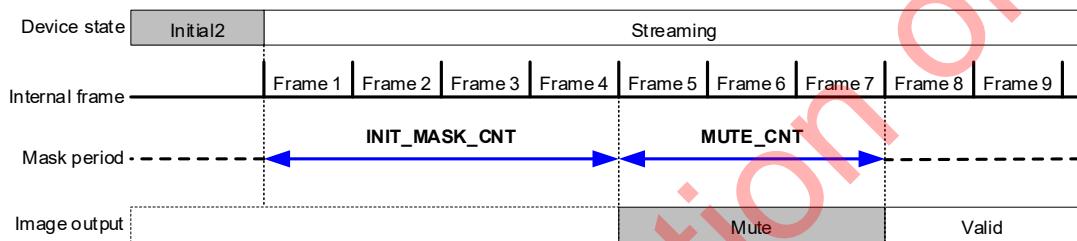
Set the INIT_MASK_CNT and MUTE_CNT registers to the number of frames for Period 1 and Period 2 respectively. This can be set by using the registers shown in "**Table 6-34.**"

Table 6-34 Registers for the Startup Mask Function

Register Name	Description
INIT_MUTE_DATA_MASK_EN_	This register is used to enable or disable the masking of the image data during the period set by using the MUTE_CNT_ register at startup. 0: Disabled 1: Enabled
INIT_MUTE_VALID_MASK_EN_	This register is used to replace the Data Type with the following values during the period set by using the MUTE_CNT register at sensor startup: • In the case of MIPI CSI-2 output: The Data Type of the Packet Header is replaced with either the initial value corresponding to the drive mode or the value set by using the IFD_DATATYPE_VISIBLE_INVALID register. 0: Replacing disabled 1: Replacing enabled

"Figure 6-27" illustrates an operating example with the following settings:

User-set values: INIT_MASK_CNT_ = 4, MUTE_CNT_ = 3, INIT_MUTE_DATA_MASK_EN_ = 1

**Figure 6-27 Example of Startup Masking**

The INIT_MASK_CNT_ and MUTE_CNT_ registers, and the registers shown in **"Table 6-34"** are compatible with the Application Lock function. For details, refer to **"3.1.5 Application Lock Function."**

6.8.3.2. Masking Extended Frames

The Extended Frame Mask function masks the frames extended by long exposure. The sensor produces expanded frames as blanking output. The masking method cannot be selected.

“Figure 6-28” illustrates an example of this operation. For details, refer to “**5.2.3.2.3 Long Exposure.**”

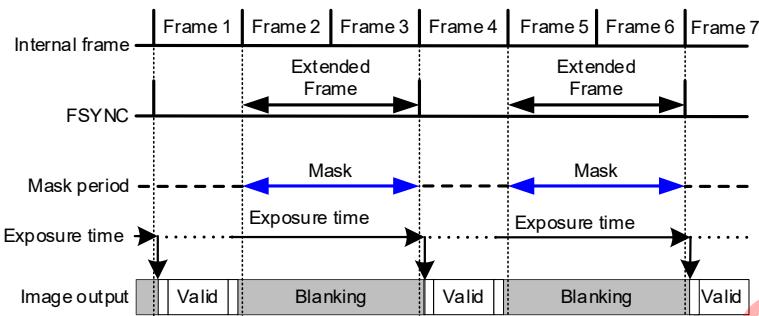


Figure 6-28 Timing of Masking for Extended Frames

6.8.3.3. Host Communication Mask Function

The Host Communication Mask function masks output frames at any time specified by the host. **“Table 6-35”** describes the registers used to set the Host Communication Mask function.

Table 6-35 Registers for the Host Communication Mask Function

Register Name	Description
VID_DATA_MASK_EN_	This register is used to enable or disable the masking of image data output. 0: Disabled 1: Enabled
VID_VALID_MASK_EN_	This register is used to enable or disable the replacement of the Data Type with other values. <ul style="list-style-type: none"> • In the case of MIPI CSI-2 output: The Data Type of the Packet Header is replaced with either the initial value corresponding to the drive mode or the value set by using the IFD_DATATYPE_VISIBLE_INVALID register. 0: Replacing disabled 1: Replacing enabled

The registers in **“Table 6-35”** are compatible with the Application Lock function. For details, refer to **“3.1.5 Application Lock Function.”**

6.8.4. Interface

6.8.4.1. Input Registers

Table 6-36 Input Registers for the Output Mask Function

[CONFIG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A5C	1	7:0	INIT_MASK_CNT_	R/W	U8.0	This register is used to select the number of frames which the sensor does not transmit, immediately after the sensor has transitioned to Streaming State.
0x8A5D	1	7:0	MUTE_CNT_	R/W	U8.0	This register is used to set the number of frames for each signal to be masked after the sensor has transitioned to Streaming State and after "the number* of frames." Note: Number = the INIT_MASK_CNT_ register's value The sensor masks the signals which are set to 1 by using the INIT_MUTE_x_MASK_EN (x = DATA, VALID) registers.

[VIF]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBDA8	1	0	VID_DATA_MASK_EN_	R/W	U1.0	This register is used to enable or disable the masking of image data output. 0: Disabled 1: Enabled
		3	VID_VALID_MASK_EN_	R/W	U1.0	This register is used to replace the value of the Data Type with another value. • The Data Type of the Packet Header is replaced with either the initial value corresponding to the drive mode or the value set by using the IFD_DATATYPE_VISIBLE_INVALID register. 0: Replacing disabled 1: Replacing enabled
0xBDA9	1	0	INIT_MUTE_DATA_MASK_EN_	R/W	U1.0	This register is used to enable or disable the masking of the image data during the period set by using the MUTE_CNT_ register at startup. 0: Disabled 1: Enabled
		3	INIT_MUTE_VALID_MASK_EN_	R/W	U1.0	This register is used to replace the value of the Data Type with another value during the period set by using the MUTE_CNT_ register at sensor startup. • The Data Type of the Packet Header is replaced with either the initial value corresponding to the drive mode or the value set by using the IFD_DATATYPE_VISIBLE_INVALID register. 0: Replacing disabled 1: Replacing enabled
0xBDF9	1	3	IFD_DATATYPE_VISIBLE_INVALID_CTRLSEL	R/W	U1.0	This register is used to select the value when changing the Data Type within the MIPI CSI-2 Packet Header by using the Output Mask function. 0: The initial value corresponding to the drive mode 1: The value of the IFD_DATATYPE_VISIBLE_INVALID register

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBDFF	1	5:0	IFD_DATATYPE_VISIBLE_INVALID	R/W	U6.0	<p>This register is used to set the Data Type value when changing the Data Type within the MIPI CSI-2 Packet Header by using the Output Mask function.</p> <p>Default: 0x3F</p> <p>Available range: 0x10 to 0x3F</p> <ul style="list-style-type: none"> This register is enabled when the value of the IFD_DATATYPE_VISIBLE_INVALID_CTRLSEL register is 1.

[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBF15	1	7:0	INIT_MASK_CNT_APL	R/W	U8.0	This register is used to be compared with the INIT_MASK_CNT register for the Application Lock function.
0xBF16	1	7:0	MUTE_CNT_APL	R/W	U8.0	This register is used to be compared with the MUTE_CNT register for the Application Lock function.
0xBF17	1	0	VID_DATA_MASK_EN_APL	R/W	U1.0	This register is used to be compared with the VID_DATA_MASK_EN register for the Application Lock function.
0xBF1A	1	0	VID_VALID_MASK_EN_APL	R/W	U1.0	This register is used to be compared with the VID_VALID_MASK_EN register for the Application Lock function.
0xBF1C	1	0	INIT_MUTE_DATA_MASK_EN_APL	R/W	U1.0	This register is used to be compared with the INIT_MUTE_DATA_MASK_EN register for the Application Lock function.
0xBF1F	1	0	INIT_MUTE_VALID_MASK_EN_APL	R/W	U1.0	This register is used to be compared with the INIT_MUTE_VALID_MASK_EN register for the Application Lock function.

6.9. Information Output Function

6.9.1. Functional Purpose

The Information Output function adds the sensor's image information to the output image.

6.9.2. Functional Overview

The Information Output function transmits output image information to the Front Embedded Data and Rear Embedded Data of MIPI CSI-2 output. Regarding the Embedded Data, the Embedded IDs are assigned to each byte in the data field for management.

6.9.3. Functional Specifications

6.9.3.1. Enabling or Disabling the Output of the Embedded Data

The host can enable or disable the output of the Front Embedded Data and the Rear Embedded Data using the IR_DR_I2I_FEBD_EN and IR_DR_I2I_REBD_EN registers, respectively. To enable or disable data output, set the corresponding register to 1 or 0, respectively. "Figure 6-29" illustrates the frame structure when the output of the Front Embedded Data and Rear Embedded Data is enabled or disabled.

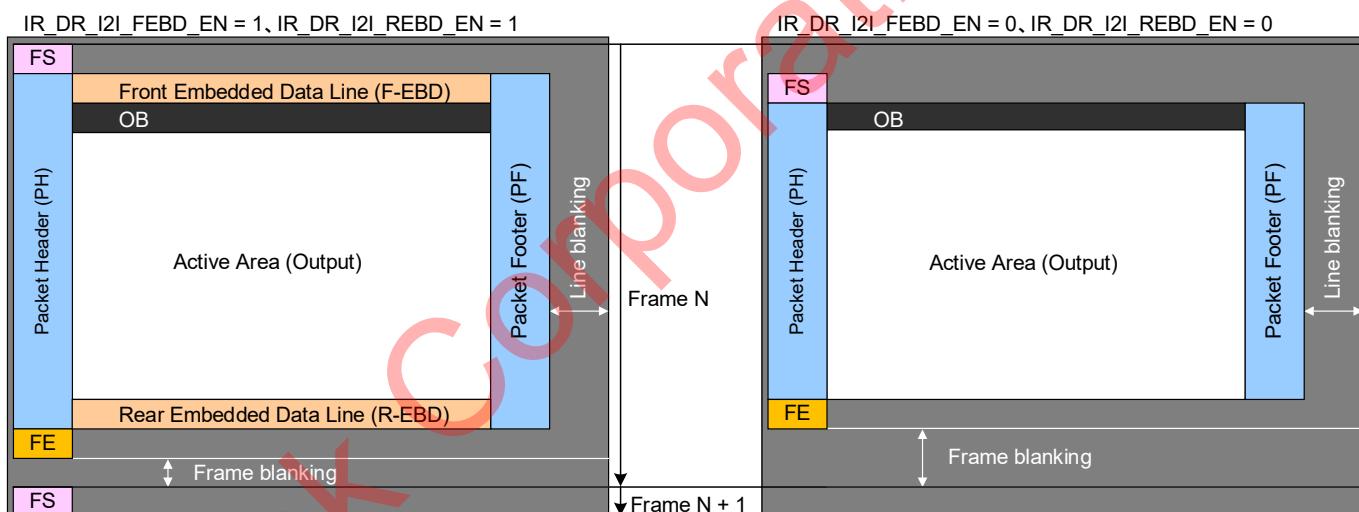
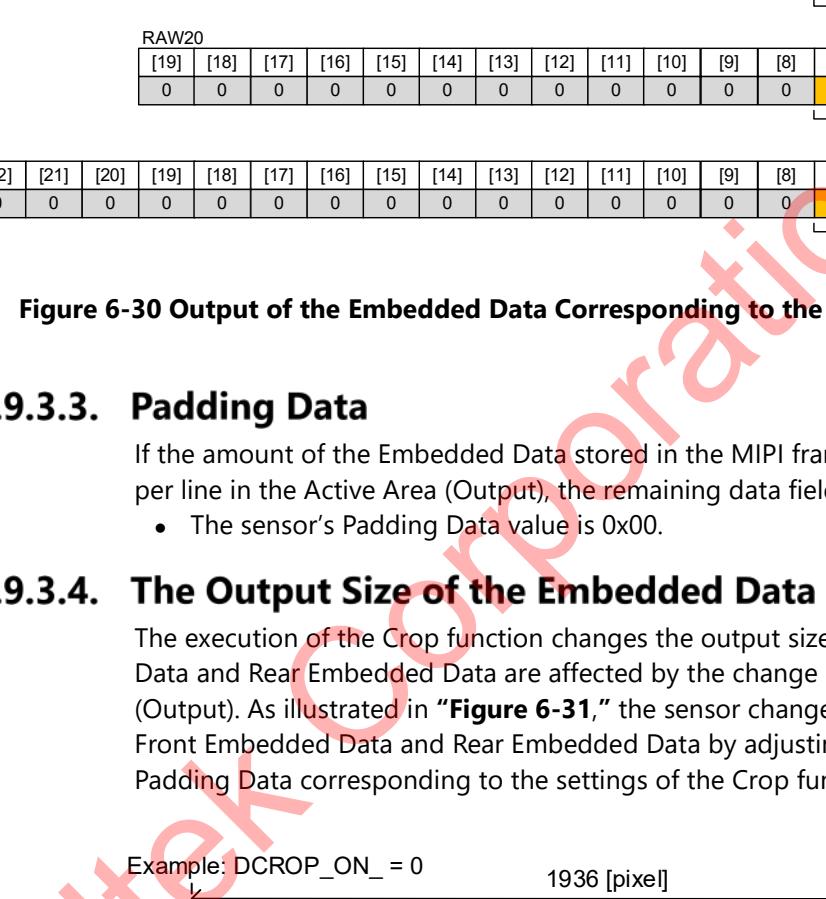


Figure 6-29 The Difference in the Embedded Data

6.9.3.2. The Embedded Data Format

As illustrated in “**Figure 6-30**,” the sensor stores the Front Embedded Data to handle the output size width that is specified by the MIPI CSI-2 output format.



RAW12	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
	0	0	0	0	0	7	6	5	4	3	2	1	0

RAW14	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
	0	0	0	0	0	0	0	7	6	5	4	3	2	1	0

RAW16	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
	0	0	0	0	0	0	0	0	7	6	5	4	3	2	1	0

RAW20	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
	0	0	0	0	0	0	0	0	0	0	0	0	0	7	6	5	4	3	2	1	0

RAW24	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7	6	5	4	3	2	1	0

Figure 6-30 Output of the Embedded Data Corresponding to the MIPI CSI-2 Output Format

6.9.3.3. Padding Data

If the amount of the Embedded Data stored in the MIPI frame is less than the number of pixels per line in the Active Area (Output), the remaining data field is filled with padding data.

- The sensor’s Padding Data value is 0x00.

6.9.3.4. The Output Size of the Embedded Data

The execution of the Crop function changes the output size per line since the Front Embedded Data and Rear Embedded Data are affected by the change of the output size of the Active Area (Output). As illustrated in “**Figure 6-31**,” the sensor changes the size of the output line of the Front Embedded Data and Rear Embedded Data by adjusting the area which is filled with the Padding Data corresponding to the settings of the Crop function.

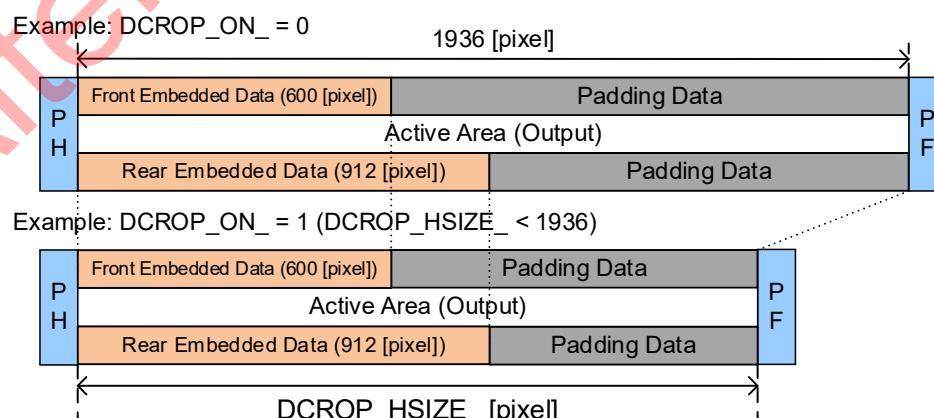


Figure 6-31 The Front Embedded Data and Rear Embedded Data After the Execution of the Crop Function

■ When changing the crop size:

If the horizontal crop size is less than the size of the Front Embedded Data and Rear Embedded Data, both are lost. The size of the Front Embedded Data and Rear Embedded Data is as follows:

- Front Embedded Data: 600 [pixel]
- Rear Embedded Data: 912 [pixel]

In order for the sensor to transmit all the information about the Embedded Data, crop the image with the horizontal sizes greater than the aforementioned sizes.

◆ Note

When the Line Information has been assigned, the information regarding the Front Embedded Data and Rear Embedded Data is lost unless the horizontal crop size is increased by an additional 4 pixels. For details, refer to "[2.4.5 Line Information](#)."

◇ Memo

- If the horizontal crop size is less than the size of the Front Embedded Data and Rear Embedded Data, the information regarding the Front Embedded Data and Rear Embedded Data is lost in units of four pixels.
- Information loss occurs in units of four pixels from the data with the highest Embedded ID. However, the CRC information, which is also part of the Embedded Data information, is not lost. For details, refer to "[6.9.3.5 Front Embedded Data](#)" and "[6.9.3.6 Rear Embedded Data](#)."

■ When changing the crop start position:

The output data from the Active Area (Output) is changed to the same position as the head of the Front Embedded Data and Rear Embedded Data. Consequently, the output of the Front Embedded Data and Rear Embedded Data are not affected.

For details, refer to "[6.4 Crop Function](#)."

6.9.3.5. Front Embedded Data

The Front Embedded Data is the information regarding the sensor's output images. "Table 6-37" shows this information transmitted as the Front Embedded Data.

- The information about Embedded IDs not listed in this table is Reserved.

Table 6-37 List of the Front Embedded Data Information

Embedded IDs	Name	Output Image Information ^{*1}	Remark
E01 - E02	Data Count Information	Current	"6.9.3.5.1 Data Count Information"
E4	HDR ID Information	Current	"6.9.3.5.2 HDR ID Information"
E05 - E08	Header CRC	-	"6.9.3.6.7 CRC"
E13 - E14 E17 - E20 E225 - E226	Individual information	Previous	"6.9.3.5.3 Individual information"
E21 - E30	Information Regarding Host-Selected Register(s)	Current	"6.9.3.5.4 Information Regarding Host-Selected Register(s)"
E37 - E40	Frame Count Information	Current	"6.9.3.5.5 Frame Count Information"
E40 - E41	Frame ID Information	Current	"6.9.3.5.6 Frame ID Information"
E43	Frame Mask Information	Current	"6.9.3.5.7 Frame Mask Information"
E49 - E50	The compensation level Information in external sync	Previous	"6.9.3.5.8 Information Regarding the Adjustment Level Determined by External Pulse-Based Sync"
E53 - E56	Temperature information	Current	"6.9.3.5.9 Temperature Information"
E61 - E66	Internal error information	Current	"6.9.3.5.10 Internal Error Information"
E31 - E36	Exposure Control Information	Current	"6.9.3.5.11 Exposure Control Information"
E101 - E106		Subsequent	
E121 - E128	Analog Gain Information	Current	"6.9.3.5.12 Analog Gain Information"
E141 - E155	Digital Gain Information	Current	"6.9.3.5.13 Digital Gain Information"
E165 - E168	Optical Center Compensation Information	Current	"6.9.3.5.14 Optical Center Compensation Information"
E169 - E170	Horizontal/Vertical flip Information	Current	"6.9.3.5.15 Horizontal/Vertical Image Flip Information"
E171	First Pixel Color Information	Current	"6.9.3.5.16 First Pixel Color Information"
E181 - E188	Crop Information	Current	"6.9.3.5.17 Crop function information"
E197	Drive Mode Information	Current	"6.9.3.5.18 Drive Mode Information"
E201 - E203	Sync Mode Information	Current	"6.9.3.5.19 Sync Mode Information"
E205 - E212	Period of Time Information	Current	"6.9.3.5.20 Period of Time Information"
E213 - E216	Extended Frame and Extended Line Information	Current	"6.9.3.5.21 Extended Frame and Extended Line Information"
E217 - E223	Function Operating State Information	Current	"6.9.3.5.22 Function Operating State Information"
E249 - E256	White Balance Information	Current	"6.9.3.5.23 White Balance Information"
E257 - E362	PWL Information	Current	"6.9.3.5.24 PWL Information"
E373 - E404	Clamp Information	Current	"6.9.3.5.25 Clamp Information"
E405 - E476	OB Information	Current	"6.9.3.5.26 OB Information"
E477 - E529	Compositing Gain Information	Current	"6.9.3.5.27 Compositing Gain Information"
E533 - E560	Sensitivity Ratio Information	Current	"6.9.3.5.28 Sensitivity Ratio Information"
E597 - E600	Footer CRC	Current	"6.9.3.6.7 CRC"

* The descriptions of the image information for output are as follows:

Previous: Information related to the output image of the frame preceding the current frame

Current: Information related to the output image of the current frame

Subsequent: Information related to the output image in the frame immediately after the current frame

◇ **Memo**

- For the information output of the Front Embedded Data and the bit assignment in the Embedded ID, click and refer to the corresponding section in "**Table 6-37.**"
- The output information of the Front Embedded Data may be different from the value that can be checked using the corresponding register. This is because this value is modified considering the restrictions and conditions on the sensor.
- The symbol "-" in the table represents the following:
 - There is a possibility that a register value may change.
 - The register used to check image information may not exist.

6.9.3.5.1. Data Count Information

The Data Count Information indicates the number of bytes (588) of the Front Embedded Data from the subsequent data after the header CRC (E09) to the preceding data before the footer CRC (E596).

Table 6-38 Front Embedded Data Bit Assignment for the Data Count Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U16.0	-	-	E02[7:0]	E01[7:0]	This register indicates the number of bytes of data from the subsequent data after the header CRC to the preceding data before the footer CRC. Fixed at 588

6.9.3.5.2. HDR ID Information

The HDR ID Information indicates the signal line and the type of image which is currently being transmitted.

Table 6-39 Front Embedded Data Bit Assignment for the HDR ID Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U2.0	-	-	-	E04[2:0]	This register indicates the type of output images. <ul style="list-style-type: none"> When HDRON_ = 1, this register indicates 0. When HDRON_ = 0, the type is as follows: SP1H: 1 SP1L: 2 SP2H: 3 SP2L: 4

6.9.3.5.3. Individual information

The Individual Information indicates the sensor's model name and Chip ID.

Table 6-40 Front Embedded Data Bit Assignment for the Individual Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U12.0	-	-	E14[3:0]	E13[7:0]	This register indicates the CHIP ID.

-	U8.0	-	-	-	E17[7:0]	This register indicates the CHIP ID.
-	U8.0	-	-	-	E18[7:0]	This register indicates the CHIP ID.
-	U16.0	-	-	E20[7:0]	E19[7:0]	This register indicates the CHIP ID.
-	U12.0	-	-	E226[3:0]	E225[7:0]	This register indicates the type of the sensor.
-	U4.0	-	-	-	E226[7:4]	This register indicates the CHIP ID.

6.9.3.5.4. Information Regarding Host-Selected Register(s)

The sensor transmits the information about the register selected by the host to the Front Embedded Data in bytes. The register information for output can be set as follows:

1. Set the FEBD_REG_INFO_CAT_x (x = 0 to 9) registers to the category number of these registers.
2. Set the FEBD_REG_INFO_OFFSET_x (x = 0 to 9) registers to address offset values.
3. Set the FEBD_REG_INFO_EN_x (x = 0 to 9) registers to 1.

◆ Note

- Of the CONST1, CTRL1, SM_CONST, SM_STATE, STATE, and MODE1 categories, the registers with the following category numbers are not allowed to be set:
Category numbers: 111, 112, from 162 through 173, 204 and greater.
- For the category number of each register, refer to the IMX623-AA** "Register Map."

Table 6-41 Front Embedded Data Bit Assignment for the Host-Selected Register Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U32.0	E24[7:0]	E23[7:0]	E22[7:0]	E21[7:0]	
-	U32.0	E28[7:0]	E27[7:0]	E26[7:0]	E25[7:0]	
-	U32.0	-	-	E30[7:0]	E29[7:0]	This register indicates the information in bytes regarding a register selected by the host.

◆ Memo

- The Embedded ID is assigned in ascending order by the register number (x = 0 to 9). For example, the register information set by using the register number 0 is assigned to E21.
- The sensor transmits 0 when the FEBD_REG_INFO_EN_x (x = 0 to 9) registers are 0 or when the host selects a category number or the offset address where no register exists.

6.9.3.5.5. Frame Count Information

The Frame Count Information is a 32-bit counter to increment the count for the output of every single frame. Note that this count is different from the Frame Number stored in the FS/FE packet of the MIPI CSI-2 output. The Frame Count operates as follows:

- The Frame Count counts up to the maximum value set in the IR_DR_I2I_FEBD_FRMCNT_MAX register.
- The Frame Count's value of 1 is defined as the first output frame after the sensor has transitioned to Streaming State.
- When the Frame Count's value reaches the value set in the IR_DR_I2I_FEBD_FRMCNT_MAX, the count value will revert to 1 in the subsequent frame.
- When the value of the IR_DR_I2I_FEBD_FRMCNT_MAX register is changed while the sensor is in Streaming State, the Frame Count is reset to 1. To avoid this reset due to a change to this register, set the IR_DR_I2I_FEBD_FRMCNT_MAX_RESET register to 0.
- To reset the Frame Number at the desired time, set the WO_DR_I2I_FEBD_FRMCNT_CLR

register to 1.

- When not using the Frame Count, set the IR_DR_I2I_FEBD_FRMCNT_MAX register to 0. With this setting, the sensor always transmits 0.

Table 6-42 Front Embedded Data Bit Assignment for the Frame Count Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
DIF_FRMINFO_FRAME_COUNT	U32.0	E40[7:0]	E39[7:0]	E38[7:0]	E37[7:0]	This register indicates the frame count.

◇ **Memo**

The Frame Count does not increment when no Frame Output has been selected using the Output Mask function. For details, refer to “[6.8 Output Mask Function](#).”

6.9.3.5.6. Frame ID Information

This information indicates the Frame IDs, which have been set for the N Frame Sequence function. For details, refer to “[6.7.3.5 N Frame Sequence Function](#).”

Table 6-43 Front Embedded Data Bit Assignment for the Frame ID Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U1.0	-	-	-	E41[0]	This register indicates the setting for enabling or disabling the automatic incrementing of the Frame ID. 0: Disabled 1: Enabled
-	U8.0	-	-	-	E42[7:0]	This register indicates the Frame ID.

6.9.3.5.7. Frame Mask Information

The Frame Mask Information indicates whether the Output Mask function is performing masking on the current output frame. For details, refer to “[6.8 Output Mask Function](#).”

Table 6-44 Front Embedded Data Bit Assignment for the Frame Mask Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U1.0	-	-	-	E43[0]	This register indicates the information about the Data Type replacement. 0: Replacing disabled 1: Replacing enabled
-	U1.0	-	-	-	E43[1]	This register indicates the masking state of the output image data. 0: Masking disabled 1: Masking enabled

6.9.3.5.8. Information Regarding the Adjustment Level Determined by External Pulse-Based Sync

This register indicates the adjustment level of the vertical sync signal, which is determined by the external pulse-based sync. For details, refer to “[6.1.3.2 External Pulse-Based Synchronization](#).”

Table 6-45 Front Embedded Data Bit Assignment for the Adjustment Level Information in the Case of

External Pulse-Based Sync

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
RO_DR SG EB CORRECT	S15.0	-	-	E50[7:0]	E49[7:0]	This register indicates the adjustment level of the vertical sync signal in external pulse-based sync.

6.9.3.5.9. Temperature Information

The sensor is equipped with two on-chip temperature sensors which can measure temperatures from -40 °C to 125 °C.

- The host can check the sensor's temperature information using the RO_CD_DU_TEMP_SEN0_OUT register, RO_CD_DU_TEMP_SEN1_OUT register or the Front Embedded Data.

To convert the temperature information of the sensor into the temperature in Celsius, use the following equation:

- The sensor's temperature [°C] = the sensor's temperature information / 16 – 50

“Table 6-46” shows the accuracy of the temperature sensor's measurement values.

Table 6-46 The Accuracy of the Temperature Sensors

Measurable Range	Error
- 40°C ≤ Tj ≤ 125°C	+/- 5°C

Table 6-47 Front Embedded Data Bit Assignment for Temperature

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
RO_CD_DU_TEMP_SEN0_OUT	U8.4	-	-	E54[3:0]	E53[7:0]	This register indicates the temperature information.
RO_CD_DU_TEMP_SEN1_OUT	U8.4	-	-	E56[3:0]	E55[7:0]	The sensor's temperature [°C] = the sensor's temperature information / 16 – 50

6.9.3.5.10. Internal Error Information

The Internal Error Information contains information about the sensor's safety mechanisms. For details regarding the safety mechanisms, refer to the IMX623-AA** “Safety Application Note.”

Table 6-48 Front Embedded Data Bit Assignment for the Internal Error Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U8.0	-	-	-	E61[7:0]	Refer to the IMX623-AA** “Safety Application Note.”
-	U8.0	-	-	-	E62[7:0]	
-	U8.0	-	-	-	E63[7:0]	
-	U8.0	-	-	-	E64[7:0]	
-	U8.0	-	-	-	E65[7:0]	
-	U8.0	-	-	-	E66[7:0]	

6.9.3.5.11. Exposure Control Information

This information indicates exposure times, set by using the Exposure Control function.

Table 6-49 Front Embedded Data Bit Assignment for the Exposure Control Information in the Case of Internal Sync or External Pulse-Based Sync

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U18.0	-	E33[1:0]	E32[7:0]	E31[7:0]	SP1's exposure time in units of lines
-	U18.0	-	E36[1:0]	E35[7:0]	E34[7:0]	SP2's exposure time in units of lines

Table 6-50 Front Embedded Data Bit Assignment for the Exposure Control Information in the Case of Shutter Trigger-Based Sync

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U18.0	-	E103[1:0]	E102[7:0]	E101[7:0]	SP1's exposure time in units of lines
-	U18.0	-	E106[1:0]	E105[7:0]	E104[7:0]	SP2's exposure time in units of lines

6.9.3.5.12. Analog Gain Information

This information indicates analog gain, set by using the Exposure Control function.

Table 6-51 Front Embedded Data Bit Assignment for the Analog Gain Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U11.0	-	-	E122[2:0]	E121[7:0]	Analog gain for SP1H (in units of 0.1 dB)
-	U11.0	-	-	E124[2:0]	E123[7:0]	Analog gain for SP1L (in units of 0.1 dB)
-	U11.0	-	-	E126[2:0]	E125[7:0]	Analog gain for SP2H (in units of 0.1 dB)
-	U11.0	-	-	E128[2:0]	E127[7:0]	Analog gain for SP2L (in units of 0.1 dB)

6.9.3.5.13. Digital Gain Information

This information indicates digital gain, set by using the Exposure Control function.

Table 6-52 Front Embedded Data Bit Assignment for the Digital Gain Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U9.8	-	E143[0]	E142[7:0]	E141[7:0]	<ul style="list-style-type: none"> In the case of HDR output This register indicates digital gain for HDR output. In the case of non-HDR output This register indicates digital gain for SP1H.
-	U9.8	-	E147[0]	E146[7:0]	E145[7:0]	This register indicates digital gain for SP1L.
-	U9.8	-	E151[0]	E150[7:0]	E149[7:0]	This register indicates digital gain for SP2H.
-	U9.8	-	E155[0]	E154[7:0]	E153[7:0]	This register indicates digital gain for SP2L.

6.9.3.5.14. Optical Center Compensation Information

The Optical Center Compensation Information indicates the compensation level by the Optical Center Compensation function. This compensation level is the sum of the compensation level automatically set by the sensor for each drive mode and the compensation level determined by the Optical Center Compensation function. For details, refer to “[6.2 Optical Center Compensation Function](#).”

Table 6-53 Front Embedded Data Bit Assignment for the Optical Center Compensation Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U12.0	-	-	E166[3:0]	E165[7:0]	This register indicates the horizontal compensation level for optical center.
-	U12.0	-	-	E168[3:0]	E167[7:0]	This register indicates the vertical compensation level for optical center.

6.9.3.5.15. Horizontal/Vertical Image Flip Information

This register indicates the settings of the Horizontal/Vertical Flip function.

Table 6-54 Front Embedded Data Bit Assignment for the Horizontal/Vertical Flip Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U1.0	-	-	-	E169[0]	Horizontal flipping 0: Flipping disabled 1: Flipping enabled
-	U1.0	-	-	-	E170[0]	Vertical flipping 0: Flipping disabled 1: Flipping enabled

6.9.3.5.16. First Pixel Color Information

This register indicates the settings of the First Pixel Color Selection function.

Table 6-55 Front Embedded Data Bit Assignment for the First Pixel Color Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
BID_	U1.0	-	-	-	E171[0]	This register is used to select the first pixel color in the Active Area (Analog Crop) in the combination of the LID. (LID, BID): First pixel color (0, 0): CF0 (0, 1): CF1 (1, 0): CF2 (1, 1): CF3
LID_	U1.0	-	-	-	E171[1]	This register is used to select the first pixel color in the Active Area (Analog Crop) in the combination of the BID. (LID, BID): First pixel color (0, 0): CF0 (0, 1): CF1 (1, 0): CF2 (1, 1): CF3
OBBID_	U1.0	-	-	-	E171[2]	This register indicates the first pixel color in the OB Area. 0: CF0 and CF2 1: CF1 and CF3

6.9.3.5.17. Crop function information

This information indicates the information regarding the output image which has been set by using the Crop function. The Crop Function Information is valid when the DCROP_ON_ register's value is 1. For details, refer to "**6.4 Crop Function**."

Table 6-56 Front Embedded Data Bit Assignment for the Crop Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U12.0	-	-	E182[3:0]	E181[7:0]	This register indicates the horizontal offset value of a crop area.
-	U14.0	-	-	E184[5:0]	E183[7:0]	This register indicates the vertical offset value of a crop area.
-	U12.0	-	-	E186[3:0]	E185[7:0]	This register indicates the horizontal size of a crop area.
-	U14.0	-	-	E188[5:0]	E187[7:0]	This register is used to set the vertical size of a crop area.

6.9.3.5.18. Drive Mode Information

The sensor indicates the drive mode number in operation. Regarding the drive mode number, refer to “[Table 4-2](#).”

Table 6-57 Front Embedded Data Bit Assignment for the Drive Mode Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U8.0	-	-	-	E197[7:0]	Drive mode number

6.9.3.5.19. Sync Mode Information

This information indicates the information about the settings of the Sync function.

Table 6-58 Front Embedded Data Bit Assignment for the Sync Mode Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U2.0	-	-	-	E201[1:0]	This register is used to select the sync method. 0: Internal sync 1: External pulse-based sync 2: Shutter trigger-based sync
-	U2.0	-	-	-	E202[1:0]	This register indicates the settings of the autonomous operating mode. 0: Level detection auto mode disabled 1: Level detection auto mode enabled

6.9.3.5.20. Period of Time Information

The period of time information shows the number of drive clocks in the horizontal period and the number of lines in the vertical period.

Table 6-59 Front Embedded Data Bit Assignment for the Period of Time Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U16.0	-	-	E206[7:0]	E205[7:0]	This register indicates the number of drive clocks in the horizontal period.
-	U18.0	-	E211[1:0]	E210[7:0]	E209[7:0]	This register indicates the number of lines in the vertical period.

6.9.3.5.21. Extended Frame and Extended Line Information

This information shows the number of frames and lines extended by the sensor's Exposure Control function and Sync function.

Table 6-60 Front Embedded Data Bit Assignment for the Extended Frame and Extended Line Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U3.0	-	-	-	E213[2:0]	Number of extended frames
-	U18.0	-	E216[1:0]	E215[7:0]	E214[7:0]	Number of extended lines

6.9.3.5.22. Function Operating State Information

This information indicates whether a function is enabled or disabled.

Table 6-61 Front Embedded Data Bit Assignment for the Function Operating State Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U1.0	-	-	-	E217[0]	This register is used to enable or disable the Crop function. 0: Disabled 1: Enabled
-	U1.0	-	-	-	E218[0]	This register indicates whether the PG Image Output function is enabled or disabled. 0: Disabled 1: Enabled
-	U1.0	-	-	-	E219[0]	This register indicates the setting for enabling or disabling the masking of image data output, performed by the Host Communication Mask function. 0: Disabled 1: Enabled
-	U1.0	-	-	-	E219[1]	This register indicates the setting for enabling or disabling the replacement of the Data Type value with a host-specified value, performed by the Host Communication Mask function. 0: Disabled 1: Enabled
-	U1.0	-	-	-	E223[0]	This register indicates the setting for enabling or disabling the output of the Line Information Pixel to the Front Embedded Data and Rear Embedded Data. 0: Disabled 1: Enabled
-	U1.0	-	-	-	E223[1]	This register indicates the setting for enabling or disabling the output of the Line Information Pixel to the Active Area (Output), Optical Black and Mask Data to the Front Embedded Data and Rear Embedded Data. 0: Disabled 1: Enabled

6.9.3.5.23. White Balance Information

This information indicates white balance gain, set using the White Balance function.

Table 6-62 Front Embedded Data Bit Assignment for the White Balance Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U4.8	-	-	E250[3:0]	E249[7:0]	The white balance gain for CF0
-	U4.8	-	-	E252[3:0]	E251[7:0]	The white balance gain for CF1
-	U4.8	-	-	E254[3:0]	E253[7:0]	The white balance gain for CF2
-	U4.8	-	-	E256[3:0]	E255[7:0]	The white balance gain for CF3

6.9.3.5.24. PWL Information

This information indicates the information about the settings of the PWL function.

Table 6-63 Front Embedded Data Bit Assignment for the PWL Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U12.0	-	-	E259[3:0]	E258[7:0]	This register is used to set the value to increase the pedestal level.
-	U24.0	-	E263[7:0]	E262[7:0]	E261[7:0]	The X coordinate of the PWL Control Point 1
-	U24.0	-	E266[7:0]	E265[7:0]	E264[7:0]	The X coordinate of the PWL Control Point 2
...
-	U24.0	-	E311[7:0]	E310[7:0]	E309[7:0]	The X coordinate of the PWL Control Point 17
-	U24.0	-	E314[7:0]	E313[7:0]	E312[7:0]	The Y coordinate of the PWL Control Point 1
-	U24.0	-	E317[7:0]	E316[7:0]	E315[7:0]	The Y coordinate of the PWL Control Point 2
...
-	U24.0	-	E362[7:0]	E361[7:0]	E360[7:0]	The Y coordinate of the PWL Control Point 17

6.9.3.5.25. Clamp Information

The Clamp Information indicates the black level's offset value to be set by the Digital Clamp function.

Table 6-64 Front Embedded Data Bit Assignment for the Clamp Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	S10.5	-	-	E374[7:0]	E373[7:0]	The black level's offset value for CF0 of SP1_HCG
-	S10.5	-	-	E376[7:0]	E375[7:0]	The black level's offset value for CF1 of SP1_HCG
-	S10.5	-	-	E378[7:0]	E377[7:0]	The black level's offset value for CF2 of SP1_HCG
-	S10.5	-	-	E380[7:0]	E379[7:0]	The black level's offset value for CF3 of SP1_HCG
-	S10.5	-	-	E382[7:0]	E381[7:0]	The black level's offset value for CF0 of SP1_LCG
-	S10.5	-	-	E384[7:0]	E383[7:0]	The black level's offset value for CF1 of SP1_LCG
-	S10.5	-	-	E386[7:0]	E385[7:0]	The black level's offset value for CF2 of SP1_LCG
-	S10.5	-	-	E388[7:0]	E387[7:0]	The black level's offset value for CF3 of SP1_LCG
-	S10.5	-	-	E390[7:0]	E389[7:0]	The black level's offset value for CF0 of SP2H
-	S10.5	-	-	E392[7:0]	E391[7:0]	The black level's offset value for CF1 of SP2H

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	S10.5	-	-	E394[7:0]	E393[7:0]	The black level's offset value for CF2 of SP2H
-	S10.5	-	-	E396[7:0]	E395[7:0]	The black level's offset value for CF3 of SP2H
-	S10.5	-	-	E398[7:0]	E397[7:0]	The black level's offset value for CF0 of SP2L
-	S10.5	-	-	E400[7:0]	E399[7:0]	The black level's offset value for CF1 of SP2L
-	S10.5	-	-	E402[7:0]	E401[7:0]	The black level's offset value for CF2 of SP2L
-	S10.5	-	-	E404[7:0]	E403[7:0]	The black level's offset value for CF3 of SP2L

6.9.3.5.26. OB Information

This information indicates the information about the sensor's OB.

- The average value of pixel levels in the Sensor Clamp Area
- The average value of the absolute values in the Sensor Clamp Area
- The number of pixels of the Sensor Clamp Area excluded from the Clamp function's calculations

For details regarding the OB information, refer to "[5.4.3.2.2 Calculating the Average Value and the Average Absolute Values of the Pixel Levels in the Sensor Clamp Area.](#)"

Table 6-65 Front Embedded Data Bit Assignment for the OB Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	S10.5	-	-	E406[7:0]	E405[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP1_HCG and CF0)
-	S10.5	-	-	E408[7:0]	E407[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP1_HCG and CF1)
-	S10.5	-	-	E410[7:0]	E409[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP1_HCG and CF2)
-	S10.5	-	-	E412[7:0]	E411[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP1_HCG and CF3)
-	S10.5	-	-	E414[7:0]	E413[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP1_LCG and CF0)
-	S10.5	-	-	E416[7:0]	E415[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP1_LCG and CF1)
-	S10.5	-	-	E418[7:0]	E417[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP1_LCG and CF2)
-	S10.5	-	-	E420[7:0]	E419[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP1_LCG and CF3)
-	S10.5	-	-	E422[7:0]	E421[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP2H and CF0)
-	S10.5	-	-	E424[7:0]	E423[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP2H and CF1)
-	S10.5	-	-	E426[7:0]	E425[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP2H and CF2)
-	S10.5	-	-	E428[7:0]	E427[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP2H and CF3)
-	S10.5	-	-	E430[7:0]	E429[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP2L and CF0)
-	S10.5	-	-	E432[7:0]	E431[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP2L and CF1)
-	S10.5	-	-	E434[7:0]	E433[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP2L and CF2)
-	S10.5	-	-	E436[7:0]	E435[7:0]	The average value of pixel levels in the Sensor Clamp Area (SP2L and CF3)
-	U10.5	-	-	E438[7:0]	E437[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_HCG and CF0)
-	U10.5	-	-	E440[7:0]	E439[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_HCG and CF1)
-	U10.5	-	-	E442[7:0]	E441[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_HCG and CF2)
-	U10.5	-	-	E444[7:0]	E443[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_HCG and CF3)
-	U10.5	-	-	E446[7:0]	E445[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_LCG and CF0)
-	U10.5	-	-	E448[7:0]	E447[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_LCG and CF1)
-	U10.5	-	-	E450[7:0]	E449[7:0]	The average value of the absolute values of

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
						the pixel levels in the Sensor Clamp Area (SP1_LCG and CF2)
-	U10.5	-	-	E452[7:0]	E451[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP1_LCG and CF3)
-	U10.5	-	-	E454[7:0]	E453[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2H and CF0)
-	U10.5	-	-	E456[7:0]	E455[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2H and CF1)
-	U10.5	-	-	E458[7:0]	E457[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2H and CF2)
-	U10.5	-	-	E460[7:0]	E459[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2H and CF3)
-	U10.5	-	-	E462[7:0]	E461[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2L and CF0)
-	U10.5	-	-	E464[7:0]	E463[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2L and CF1)
-	U10.5	-	-	E466[7:0]	E465[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2L and CF2)
-	U10.5	-	-	E468[7:0]	E467[7:0]	The average value of the absolute values of the pixel levels in the Sensor Clamp Area (SP2L and CF3)
-	U16.0	-	-	E470[7:0]	E469[7:0]	The number of pixels of the Sensor Clamp Area excluded from the Clamp function's calculations (SP1_HCG)
-	U16.0	-	-	E472[7:0]	E471[7:0]	The number of pixels of the Sensor Clamp Area excluded from the Clamp function's calculations (SP1_LCG)
-	U16.0	-	-	E474[7:0]	E473[7:0]	The number of pixels of the Sensor Clamp Area excluded from the Clamp function's calculations (SP2H)
-	U16.0	-	-	E476[7:0]	E475[7:0]	The number of pixels of the Sensor Clamp Area excluded from the Clamp function's calculations (SP2L)

6.9.3.5.27. Compositing Gain Information

This information indicates the information about compositing gain for the HDR function.

Table 6-66 Front Embedded Data Bit Assignment for the Compositing Gain Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U10.12	-	E479[5:0]	E478[7:0]	E477[7:0]	This register indicates the compositing gain between SP1_HCG and SP1_LCG, which have been calculated by the sensor. (For CF0)
-	U10.12	-	E482[5:0]	E481[7:0]	E480[7:0]	This register indicates the compositing gain between SP1_HCG and SP1_LCG, which have been calculated by the sensor. (For CF1)
-	U10.12	-	E485[5:0]	E484[7:0]	E483[7:0]	This register indicates the compositing gain between SP1_HCG and SP1_LCG, which have been calculated by the sensor. (For CF2)
-	U10.12	-	E488[5:0]	E487[7:0]	E486[7:0]	This register indicates the compositing gain between SP1_HCG and SP1_LCG, which have been calculated by the sensor. (For CF3)

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U8.12	-	E491[3:0]	E490[7:0]	E489[7:0]	This register indicates the compositing gain between SP2H and SP2L, which have been calculated by the sensor. (For CF0)
-	U8.12	-	E494[3:0]	E493[7:0]	E492[7:0]	This register indicates the compositing gain between SP2H and SP2L, which have been calculated by the sensor. (For CF1)
-	U8.12	-	E497[3:0]	E496[7:0]	E495[7:0]	This register indicates the compositing gain between SP2H and SP2L, which have been calculated by the sensor. (For CF2)
-	U8.12	-	E500[3:0]	E499[7:0]	E498[7:0]	This register indicates the compositing gain between SP2H and SP2L, which have been calculated by the sensor. (For CF3)
-	U12.0	-	-	E502[3:0]	E501[7:0]	This register indicates the compositing gain between SP1 and SP2, which have been calculated by the sensor. (For CF0, fractional part)
-	U24.0	-	E505[3:0] E504[7:4]	E504[3:0] E503[7:4]	E503[3:0] E502[7:4]	This register indicates the compositing gain between SP1 and SP2, which have been calculated by the sensor. (For CF0, integer part)
-	U12.0	-	-	E510[3:0]	E509[7:0]	This register indicates the compositing gain between SP1 and SP2, which have been calculated by the sensor. (For CF1, fractional part)
-	U24.0	-	E513[3:0] E512[7:4]	E512[3:0] E511[7:4]	E511[3:0] E510[7:4]	This register indicates the compositing gain between SP1 and SP2, which have been calculated by the sensor. (For CF1, integer part)
-	U12.0	-	-	E518[3:0]	E517[7:0]	This register indicates the compositing gain between SP1 and SP2, which have been calculated by the sensor. (For CF2, fractional part)
-	U24.0	-	E521[3:0] E520[7:4]	E520[3:0] E519[7:4]	E519[3:0] E518[7:4]	This register indicates the compositing gain between SP1 and SP2, which have been calculated by the sensor. (For CF2, integer part)
-	U12.0	-	-	E526[3:0]	E525[7:0]	This register indicates the compositing gain between SP1 and SP2, which have been calculated by the sensor. (For CF3, fractional part)
-	U24.0	-	E529[3:0] E528[7:4]	E528[3:0] E527[7:4]	E527[3:0] E526[7:4]	This register indicates the compositing gain between SP1 and SP2, which have been calculated by the sensor. (For CF3, integer part)

6.9.3.5.28. Sensitivity Ratio Information

This information indicates the information about the sensitivity ratio for the HDR function.

Table 6-67 Front Embedded Data Bit Assignment for the Sensitivity Ratio Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U3.12	-	-	E534[6:0]	E533[7:0]	This register indicates the sensitivity ratio for the CF0 pixels between SP1_HCG and SP1_LCG.
-	U3.12	-	-	E536[6:0]	E535[7:0]	This register indicates the sensitivity ratio for the CF1 pixels between SP1_HCG and SP1_LCG.
-	U3.12	-	-	E538[6:0]	E537[7:0]	This register indicates the sensitivity ratio for the CF2 pixels between SP1_HCG and SP1_LCG.
-	U3.12	-	-	E540[6:0]	E539[7:0]	This register indicates the sensitivity ratio for the CF3 pixels between SP1_HCG and SP1_LCG.

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U3.12	-	-	E542[6:0]	E541[7:0]	This register indicates the sensitivity ratio for the CF0 pixels between SP2H and SP2L.
-	U3.12	-	-	E544[6:0]	E543[7:0]	This register indicates the sensitivity ratio for the CF1 pixels between SP2H and SP2L.
-	U3.12	-	-	E546[6:0]	E545[7:0]	This register indicates the sensitivity ratio for the CF2 pixels between SP2H and SP2L.
-	U3.12	-	-	E548[6:0]	E547[7:0]	This register indicates the sensitivity ratio for the CF3 pixels between SP2H and SP2L.
-	U10.12	-	E551[5:0]	E550[7:0]	E549[7:0]	This register indicates the sensitivity ratio for the CF0 pixels between SP1 and SP2.
-	U10.12	-	E554[5:0]	E553[7:0]	E552[7:0]	Setting of the sensitivity ratio for the CF1 pixels between SP1 and SP2.
-	U10.12	-	E557[5:0]	E556[7:0]	E555[7:0]	Setting of the sensitivity ratio for the CF2 pixels between SP1 and SP2.
-	U10.12	-	E560[5:0]	E559[7:0]	E558[7:0]	Setting of the sensitivity ratio for the CF3 pixels between SP1 and SP2.

6.9.3.6. Rear Embedded Data

The Rear Embedded Data is the information about the image in the frame currently being transmitted by the sensor.

"**Table 6-68**" shows this information to be transmitted as the Rear Embedded Data.

- The information about Embedded IDs not listed in this table is **Reserved**.

Table 6-68 List of the Rear Embedded Data Information

- The output information in the first line of the Rear Embedded Data

Embedded IDs	Name	Remark
E01 - E02	Data Count Information	" 6.9.3.6.1 Data Count Information "
E05 - E08	Header CRC	" 6.9.3.6.7 CRC "
E09 – E11	This register indicates the output state of the Rear Embedded Data.	" 6.9.3.6.2 The Output State of the Rear Embedded Data "
E17 - E128	AWB Information	" 6.9.3.6.3 AWB Information ."
E909 - E912	Footer CRC	" 6.9.3.6.7 CRC "

- The output information in the lines ranging from 2nd to 9th of the Rear Embedded Data

Embedded IDs	Name	Remark
E01 - E02	Data Count Information	" 6.9.3.6.1 Data Count Information "
E05 - E08	Header CRC	" 6.9.3.6.7 CRC "
E09 – E807	Histogram Information	" 6.9.3.6.4 Histogram Information "
E909 - E912	Footer CRC	" 6.9.3.6.7 CRC "

- The output information in the 10th line of the Rear Embedded Data

Embedded IDs	Name	Remark
E01 - E02	Data Count Information	" 6.9.3.6.1 Data Count Information "
E05 - E08	Header CRC	" 6.9.3.6.7 CRC "
E09 – E12	Information about the number of spot pixels	" 6.9.3.6.5 Spot Pixel Information "
E909 - E912	Footer CRC	" 6.9.3.6.7 CRC "

- The output information in the lines ranging from 11th to 20th of the Rear Embedded Data

Embedded IDs	Name	Remark
E01 - E02	Data Count Information	" 6.9.3.6.1 Data Count Information "
E05 - E08	Header CRC	" 6.9.3.6.7 CRC "
E09 – E908	Coordinate information about spot pixels	" 6.9.3.6.5 Spot Pixel Information "
E909 - E912	Footer CRC	" 6.9.3.6.7 CRC "

- The output information in the 21st line of the Rear Embedded Data

Embedded IDs	Name	Remark
E01 - E02	Data Count Information	" 6.9.3.6.1 Data Count Information "
E05 - E08	Header CRC	" 6.9.3.6.7 CRC "
E09 – E28	Frame CRC Information	" 6.9.3.6.6 Frame CRC Information "
E909 - E912	Footer CRC	" 6.9.3.6.7 CRC "

- The output information in the 22nd line of the Rear Embedded Data

Embedded IDs	Name	Remark
E01 - E02	Data Count Information	" 6.9.3.6.1 Data Count Information "
E05 - E08	Header CRC	" 6.9.3.6.7 CRC "

Embedded IDs	Name	Remark
E909 - E912	Footer CRC	"6.9.3.6.7 CRC"

■ Light Metering Information

As shown in "Table 6-69," the sensor can transmit the two types of light metering information to the Rear Embedded Data.

Table 6-69 AWB Information and Histogram Information

Name	Number of Light Metering Windows	The Signal To Be Used	Output Information
AWB Information	1	Luminance signal Signal for each color filter	Integrated values of signals for each color filter and the number of pixels to be integrated
Histogram Information	9 to 25	Luminance signal	Luminance histogram (The luminance range can be set up to 16 segments.)

Signals, which are used to calculate the Light Metering Information, consist of the luminance signal and signals for each color filter. The latter signals have three types: CF0, CF12, and CF3. "Table 6-70" lists the calculation formulas for each signal.

Table 6-70 The Luminance Signal and Calculation Formulas for Each Color Filter

Signal	Symbol	Calculation Formula
Luminance signal	Y	$\frac{2 \times CF0 + 5 \times \frac{CF1 + CF2}{2} + CF3}{8}$
CF0 signal	CF0	CF0
CF12 signal	CF12	$\frac{CF1 + CF2}{2}$
CF3 signal	CF3	CF3

6.9.3.6.1. Data Count Information

The Data Count Information indicates the number of bytes (900) of the Rear Embedded Data from the subsequent data after the header CRC (E09) to the preceding data before the footer CRC (E908).

Table 6-71 Rear Embedded Data Bit Assignment for the Data Count Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U16.0	-	-	E02[7:0]	E01[7:0]	This register indicates the number of bytes of data from the subsequent data after the header CRC to the preceding data before the footer CRC. Fixed at 900

6.9.3.6.2. The Output State of the Rear Embedded Data

Some information output of the Rear Embedded Data can be individually enabled or disabled by the host. For example, when the IR_DR_EBD_AWBINFO_EN register is set to 0, the sensor does not output the AWB information, but transmits a value "Reserved" to the AWB information. The AWB information is obtained from the AWB light metering window. For details, see "Figure 6-32."

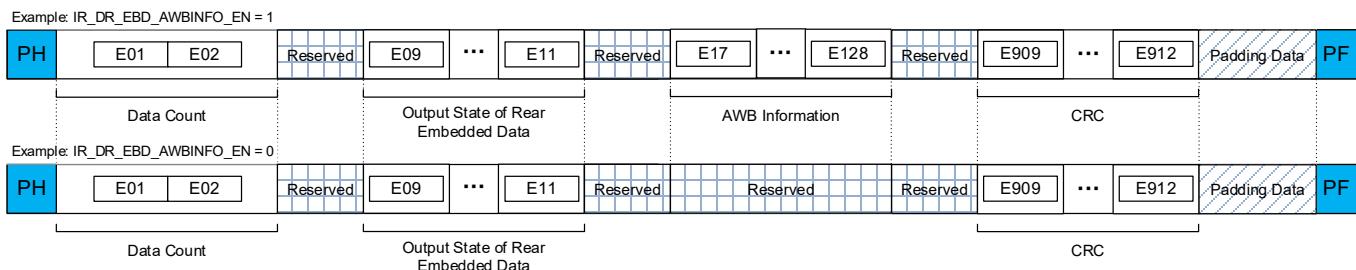


Figure 6-32 Change in Output due to the Output Settings of the Rear Embedded Data

When the REBD_STC_INFO_DISABLE register is set to 1, the output information in the lines ranging from the 10th to 20th of the Rear Embedded Data is not transmitted. In this case, since the subsequent Rear Embedded Data is shifted, the frame blanking period becomes longer. For details, see “**Figure 6-33**.”

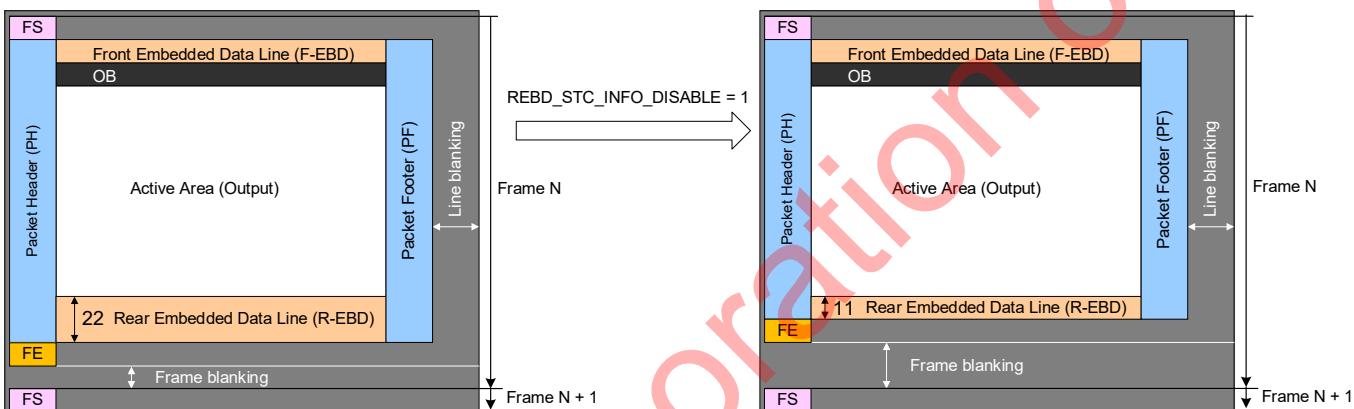


Figure 6-33 A Change in the Number of Output Lines of the Rear Embedded Data

Table 6-72 Rear Embedded Data Bit Assignment for the Output State of the Rear Embedded Data

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
IR_DR_EBD_AWBINFO_EN	U1.0	-	-	-	E09[0]	This register indicates the output state of the AWB information. 0: Output disabled 1: Output enabled
IR_DR_EBD_HISTINFO_EN	U1.0	-	-	-	E10[0]	This register indicates the output state of the histogram information. 0: Output disabled 1: Output enabled
-	U1.0	-	-	-	E11[0]	This register indicates the output state of the spot pixel information. 0: Output disabled 1: Output enabled

6.9.3.6.3. AWB Information

By specifying an area (light metering window) in the Active Area, the sensor can calculate the AWB information.

◇ Memo

If the value of the IR_DR_EBD_AWBINFO_EN register is set to 0, 112 bytes of the data area

(E17 - E128) that indicates the AWB information become unavailable.

■ The light metering window for calculating the AWB information

The host can set the light metering window to calculate the AWB information by using the registers shown in “**Table 6-73**.” The upper left corner of the Active Area (Analog Crop) is the origin’s coordinates (0,0). The entire size of the metering window is determined by the size and the number of cells.

Table 6-73 List of the Registers for Setting the Light Metering Window

Register Name	Description
IR_IS_AWB_HSTART	The horizontal coordinate at the upper left corner of the light metering window. • Set 0 or a value that is a multiple of 4.
IR_IS_AWB_VSTART	The vertical coordinate at the upper left corner of the light metering window. • Set 0 or a value that is a multiple of 4.
IR_IS_AWB_HWIN	The horizontal size of the light metering window (in pixels) • Set a value greater than or equal to 4. • Set a value that is a multiple of 4.
IR_IS_AWB_VWIN	The vertical size of the light metering window (in pixels) • Set a value greater than or equal to 4. • Set a value that is a multiple of 4.

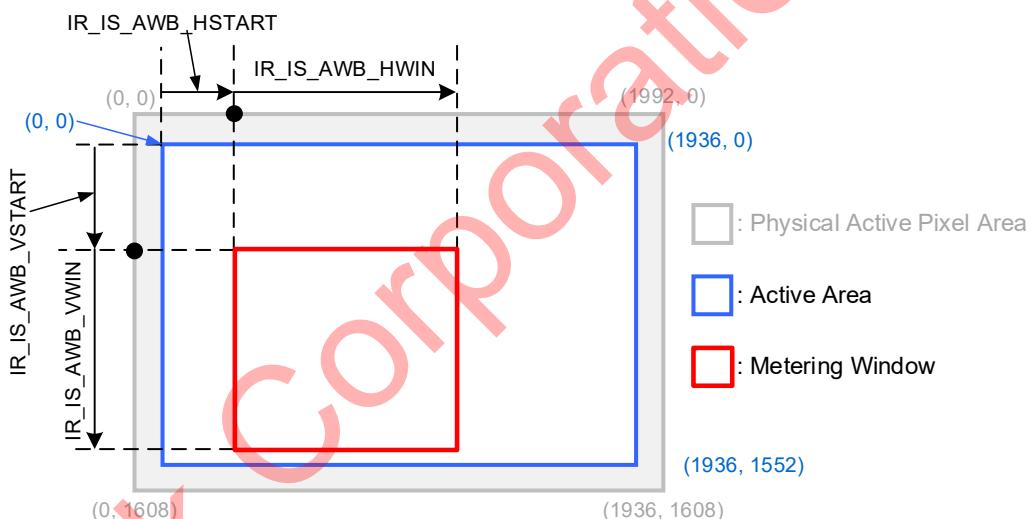


Figure 6-34 Example of Setting the Light Metering Window (AWB)

■ AWB Information Calculation

The sensor calculates the integrated value of the CF0, “CF1 and CF2 (the CF12 signal)” and CF3 signals for the pixels within the light metering window to be used for the AWB information. Although the CF0, CF12 and CF3 signals are in S12.0 precision, the sensor clips the value at the lower limit of 0, if the integration result is negative.

The host can determine whether to integrate each pixel as follows:

- For the luminance signal level, by setting the upper and lower thresholds
- For the CFx (x = 0 to 3) signal levels, by setting the upper threshold

In addition, when determining pixel integration using the CFx (0 to 3) signal, the host can select whether to use the signal level as is or as an absolute value, using the IR_IS_AWB_CF_PEAK_SEL register.

Each value can be set for the SP1_HCG, SP1_LCG, SP2H and SP2L lines. Of the following four conditions, the pixel is excluded from integration, even if one of the conditions cannot be satisfied.

- $\text{IR_IS_AWB_Y_DARK_x} \leq \text{Luminance Signal Level} \leq \text{IR_IS_AWB_Y_PEAK_x}$ ($x = \text{SP1H, SP1L, SP2H, SP2L}$)
- $\text{CF0 Signal Level} \leq \text{IR_IS_AWB_CF0_PEAK_x}$ ($x = \text{SP1H, SP1L, SP2H, SP2L}$)
- $\text{CF12 Signal Level} \leq \text{IR_IS_AWB_CF12_PEAK_x}$ ($x = \text{SP1H, SP1L, SP2H, SP2L}$)
- $\text{CF3 Signal Level} \leq \text{IR_IS_AWB_CF3_PEAK_x}$ ($x = \text{SP1H, SP1L, SP2H, SP2L}$)

The AWB information can be checked using the Rear Embedded Data and specific registers. The AWB information while the sensor continues to transmit invalid frames is the information of the last valid frame. Each integrated value is transmitted in two parts, the low-order 32 bits and the high-order 1 bit.

Integrated Value at the Signal Level in the AWB Light Metering Window = $\text{RO_IS_AWB_INT_x_y_H} \times 2 + \text{RO_IS_AWB_INT_x_y_L}$
 $(x = \text{CF0, CF12, CF3})(y = \text{SP1H, SP1L, SP2H, SP2L})$

The number of pixels to be integrated can be checked using the $\text{RO_IS_AWB_PIXCNT_x}$ ($x = \text{SP1H, SP1L, SP2H, SP2L}$) registers. The number of pixels to be integrated is the same as the CF0, CF12 and CF3 signals. Since the CF0, CF12, and CF3 signals have one value for the 2x2 pixels, the maximum value of the number of pixels to be integrated is the value obtained by dividing the number of pixels within the metering window (width x height) by 4.

Table 6-74 Rear Embedded Data Bit Assignment for the AWB Information

Register Name	Unit	Bit Assignment for Embedded IDs					Description
		[39:32]	[31:24]	[23:16]	[15:8]	[7:0]	
RO_IS_AWB_PIXCNT_SP1H	U21.0	-	-	E19[4:0]	E18[7:0]	E17[7:0]	The count value of AWB pixels (SP1_HCG)
RO_IS_AWB_PIXCNT_SP1L	U21.0	-	-	E23[4:0]	E22[7:0]	E21[7:0]	The count value of AWB pixels (SP1_LCG)
RO_IS_AWB_PIXCNT_SP2H	U21.0	-	-	E27[4:0]	E26[7:0]	E25[7:0]	The count value of AWB pixels (SP2H)
RO_IS_AWB_PIXCNT_SP2L	U21.0	-	-	E31[4:0]	E30[7:0]	E29[7:0]	The count value of AWB pixels (SP1L)
RO_IS_AWB_INT_CF0_SP1H_H x 2 + RO_IS_AWB_INT_CF0_SP1H_L	U33.0	E37[0]	E36[7:0]	E35[7:0]	E34[7:0]	E33[7:0]	AWB integrated value (SP1_HCG, CF0)
RO_IS_AWB_INT_CF12_SP1H_H x 2 + RO_IS_AWB_INT_CF12_SP1H_L	U33.0	E45[0]	E44[7:0]	E43[7:0]	E42[7:0]	E41[7:0]	AWB integrated value (SP1_HCG, CF12)
RO_IS_AWB_INT_CF3_SP1H_H x 2 + RO_IS_AWB_INT_CF3_SP1H_L	U33.0	E53[0]	E52[7:0]	E51[7:0]	E50[7:0]	E49[7:0]	AWB integrated value (SP1_HCG, CF3)
RO_IS_AWB_INT_CF0_SP1L_H x 2 + RO_IS_AWB_INT_CF0_SP1L_L	U33.0	E61[0]	E60[7:0]	E59[7:0]	E58[7:0]	E57[7:0]	AWB integrated value (SP1_LCG, CF0)
RO_IS_AWB_INT_CF12_SP1L_	U33.0	E69[0]	E68[7:0]	E67[7:0]	E66[7:0]	E65[7:0]	AWB integrated value (SP1_LCG,

Register Name	Unit	Bit Assignment for Embedded IDs					Description
		[39:32]	[31:24]	[23:16]	[15:8]	[7:0]	
H x 2 + RO_IS_AWB_INT_CF12_SP1L_L							CF12)
RO_IS_AWB_INT_CF3_SP1L_H x 2 + RO_IS_AWB_INT_CF3_SP1L_L	U33.0	E77[0]	E76[7:0]	E75[7:0]	E74[7:0]	E73[7:0]	AWB integrated value (SP1_LCG, CF3)
RO_IS_AWB_INT_CF0_SP2H_H x 2 + RO_IS_AWB_INT_CF0_SP2H_L	U33.0	E85[0]	E84[7:0]	E83[7:0]	E82[7:0]	E81[7:0]	AWB integrated value (SP2H, CF0)
RO_IS_AWB_INT_CF12_SP2H_H x 2 + RO_IS_AWB_INT_CF12_SP2H_L	U33.0	E93[0]	E92[7:0]	E91[7:0]	E90[7:0]	E89[7:0]	AWB integrated value (SP2H, CF12)
RO_IS_AWB_INT_CF3_SP2H_H x 2 + RO_IS_AWB_INT_CF3_SP2H_L	U33.0	E101[0]	E100[7:0]	E99[7:0]	E98[7:0]	E97[7:0]	AWB integrated value (SP2H, CF3)
RO_IS_AWB_INT_CF0_SP2L_H x 2 + RO_IS_AWB_INT_CF0_SP2L_L	U33.0	E109[0]	E108[7:0]	E107[7:0]	E106[7:0]	E105[7:0]	AWB integrated value (SP2L, CF0)
RO_IS_AWB_INT_CF12_SP2L_H x 2 + RO_IS_AWB_INT_CF12_SP2L_L	U33.0	E117[0]	E116[7:0]	E115[7:0]	E114[7:0]	E113[7:0]	AWB integrated value (SP2L, CF12)
RO_IS_AWB_INT_CF3_SP2L_H x 2 + RO_IS_AWB_INT_CF3_SP2L_L	U33.0	E125[0]	E124[7:0]	E123[7:0]	E122[7:0]	E121[7:0]	AWB integrated value (SP2L, CF3)

6.9.3.6.4. Histogram Information

By specifying an area (light metering window) in the Active Area, the sensor can calculate the luminance histogram information.

◇ **Memo**

If the value of the IR_DR_EBD_HISTINFO_EN register is set to 0, the 8 lines of the Rear Embedded Data that contains the Histogram Information are not transmitted.

■ **The light metering window for calculating the AWB information**

The host can set the light metering window to calculate the luminance histogram information by using the registers shown in “**Table 6-75.**” The upper left corner of the Active Area (Analog Crop) is the origin’s coordinates (0,0). The entire size of the metering window is determined by the size and the number of cells.

Table 6-75 List of the Registers for Setting the Light Metering Window

Register Name	Description
IR_IS_AEB_HSTART	The horizontal coordinate at the upper left corner of the light metering window. • Set 0 or a value that is a multiple of 4.
IR_IS_AEB_VSTART	The vertical coordinate at the upper left corner of the light metering window. • Set 0 or a value that is a multiple of 4.
IR_IS_AEB_HWIN	The horizontal size of each cell (in pixels) • Set a value of 8 or greater.

Register Name	Description
IR_IS_AEB_VWIN	<ul style="list-style-type: none"> Set a value that is a multiple of 4. <p>The vertical size of each cell (in pixels)</p> <ul style="list-style-type: none"> Set a value of 8 or greater. Set a value that is a multiple of 4.
IR_IS_AEB_HNUM	<p>The number of cells in the vertical direction</p> <ul style="list-style-type: none"> Set a value under the following condition: $3 \leq \text{IR_IS_AEB_HNUM} \leq 5$.
IR_IS_AEB_VNUM	<p>The number of light metering windows in the vertical direction</p> <ul style="list-style-type: none"> Set a value under the following condition: $3 \leq \text{IR_IS_AEB_VNUM} \leq 5$.

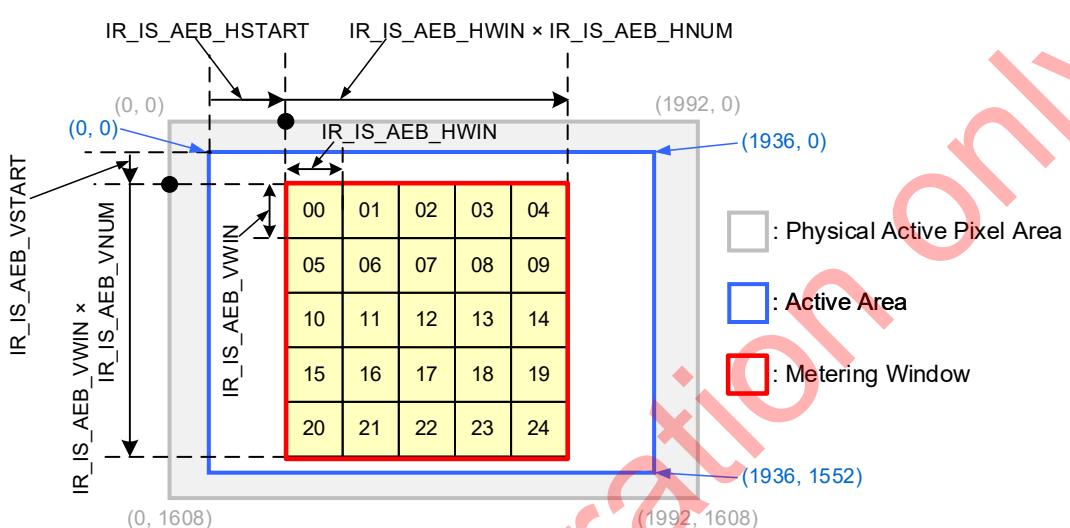


Figure 6-35 Example of Setting the Light Metering Window

■ Checking Histogram Information

The histogram information calculated by the sensor can be checked using the RO_IS_AEB_CNT_x_AREAy_BINz ($x = \text{SP1H}, \text{SP1L}, \text{SP2H}, \text{SP2L}$) ($y = 00$ to 24) ($z = 00$ to 15) registers. The letter **y** in the register name is the frame number. As illustrated in “Figure 6-36,” the cell ID number increases toward the lower right with the upper-left corner set to 00. If the user sets the number of cells to a value less than 25, the value of the registers that do not have the corresponding cell IDs will not be updated. For example, when changing the window from 25 cells (5x5) to 9 cells (3x3) while the sensor is in Streaming State, the sensor retains the same values of the RO_IS_AEB_CNT_x_AREAy_BINz ($x = \text{SP1H}, \text{SP1L}, \text{SP2H}, \text{SP2L}$) ($y = 00$ to 24) ($z = 00$ to 15) registers.

The value of the registers is 0 immediately after a sensor reset.

IR_IS_AEB_HNUM = 5 IR_IS_AEB_VNUM = 5	<table border="1"> <tr><td>00</td><td>01</td><td>02</td><td>03</td><td>04</td></tr> <tr><td>05</td><td>06</td><td>07</td><td>08</td><td>09</td></tr> <tr><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td></tr> <tr><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td></tr> <tr><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td></tr> </table>	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	<table border="1"> <tr><td>00</td><td>01</td><td>02</td></tr> <tr><td>03</td><td>04</td><td>05</td></tr> <tr><td>06</td><td>07</td><td>08</td></tr> </table>	00	01	02	03	04	05	06	07	08
00	01	02	03	04																																
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10	11	12	13	14																																
15	16	17	18	19																																
20	21	22	23	24																																
00	01	02																																		
03	04	05																																		
06	07	08																																		

Figure 6-36 Cell ID Numbers for the Light Metering Window

■ Obtaining the Histogram Information

For the pixels within the light metering window, the sensor compares the luminance signals (U12.0) with the corresponding thresholds that can be set by the host. The sensor individually transmits the number of pixels within each luminance range as the histogram information for the SP1_HCG, SP1_LCG, SP2H and SP2L lines.

◆ Memo

Histogram information output to the Rear Embedded Data while the sensor continues to transmit invalid frames is the information about the last valid frame.

To check the Histogram Information using registers, follow the procedure below: If the WO_I1_CMN_AE_CAPTURE register is set to 1 in an invalid frame, the Histogram Information about the preceding frame is transmitted to the registers.

1. To obtain the Histogram Information within a specific frame, set the WO_I1_CMN_AE_CAPTURE register to 1.
2. Obtain the value of the RO_IS_AEB_CNT_x_AREAy_BINz ($x = \text{SP1H, SP1L, SP2H, SP2L}$ ($y = 00$ to 24) ($z = 00$ to 15)) registers, one frame or later after the frame wherein the WO_I1_CMN_AE_CAPTURE register has been set to 1.

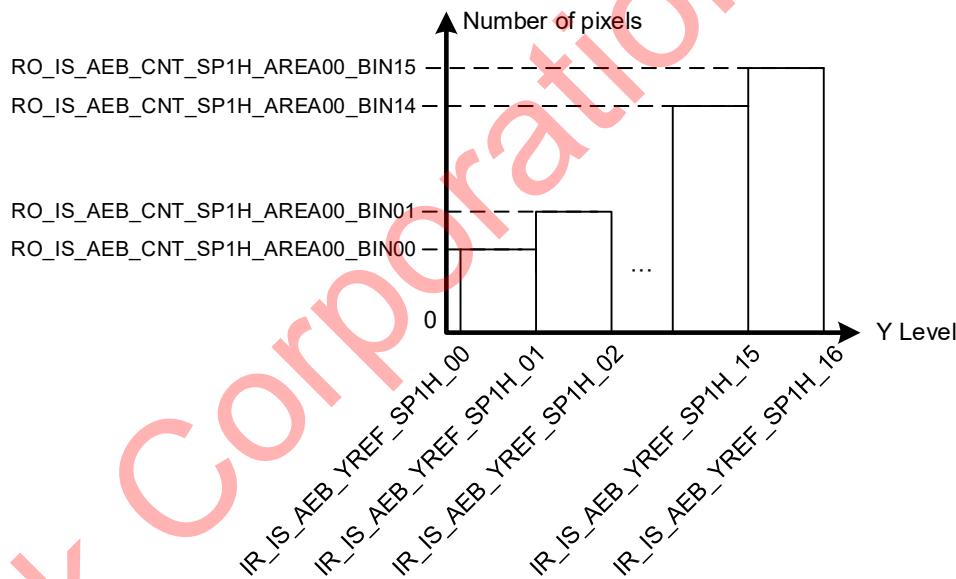


Figure 6-37 Example of Histogram Integration of Cell 00 in the Case of the SP1_HCG

Set the threshold for the luminance range of the histogram using the IR_IS_AEB_YREF_x_y ($x = \text{SP1H, SP1L, SP2H, SP2L}$ ($y = 00$ to 16)) registers. The luminance range for the number of pixels to be counted using the RO_IS_AEB_CNT_x_AREAy_BINz ($x = \text{SP1H, SP1L, SP2H, SP2L}$ ($y = 00$ to 24) ($z = 00$ to 15)) registers is as follows:

$$\text{IR_IS_AEB_YREF_x_}(z) \leq \text{Luminance Signal} < \text{IR_IS_AEB_YREF_x_}(z+1) \\ (x = \text{SP1H, SP1L, SP2H, SP2L}) (z = 0 \text{ to } 15)$$

◆ Note

- Set the histogram threshold as follows so that it monotonically increases:
 $\text{IR_IS_AEB_YREF_x_00} \leq \text{IR_IS_AEB_YREF_x_01} \leq \dots \leq \text{IR_IS_AEB_YREF_x_16}$

(x = SP1H, SP1L, SP2H, SP2L)

- The host cannot read out the value of the RO_IS_AEB_CNT_x_AREAy_BINz (x = SP1H, SP1L, SP2H, SP2L)(y = 00 to 24)(z = 00 to 15) registers while the sensor is in Start-up State.

◇ **Memo**

When the same value is set to the adjacent threshold values, the number of integrated pixels in the target luminance range is 0. For example, when the IR_IS_AEB_YREF_x_03 and IR_IS_AEB_YREF_x_04 registers are set to the same value, the value of the RO_IS_AEB_CNT_x_AREAy_BINz (x = SP1H, SP1L, SP2H, SP2L) (y = 00 to 24) registers is 0.

If the luminance range is set to the number of the segments less than 16, set threshold values to be used in descending order beginning with the IR_IS_AEB_YREF_x_16 (x = SP1H, SP1L, SP2H, SP2L) registers. Regarding unused threshold values, set them to the value equivalent to the minimum threshold value to be used. For example, when using only 8 luminance segments as shown in “**Figure 6-38**,” set all registers from IR_IS_AEB_YREF_x_00 through IR_IS_AEB_YREF_x_08 (x = SP1H, SP1L, SP2H, SP2L) to the same value.

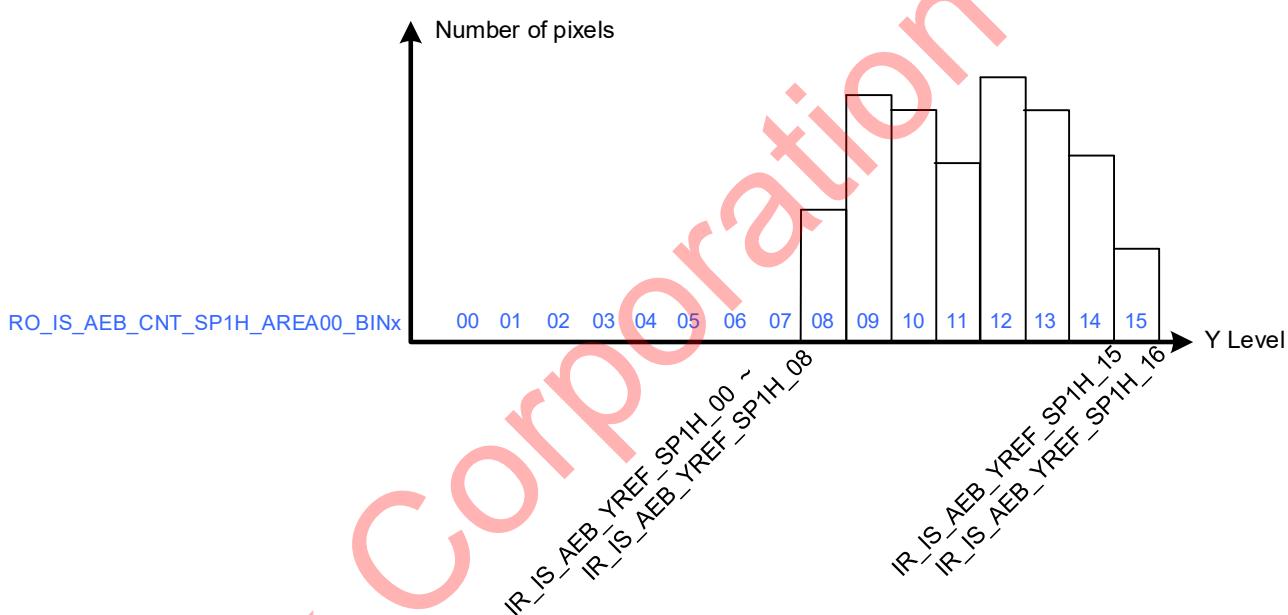


Figure 6-38 When Using Only 8 Luminance Ranges in the Case of the SP1_HCG in Area 00

Since the luminance signal has one value for the 2x2 pixels, the maximum value of the number of pixels to be integrated is the number of pixels (width x height) in the metering window divided by 4.

Table 6-76 Rear Embedded Data Bit Assignment for the Histogram Information

Register Name	Unit	Bit Assignment for Embedded IDs				Line	Description
		[31:24]	[23:16]	[15:8]	[7:0]		
RO_IS_AEB_CNT_SP1H_AREA00_BIN00	U18.0	-	E11 [1:0]	E10 [7:0]	E9 [7:0]	The output information in the 2nd line of the Rear Embedded Data	This register indicates the histogram result of SP1_HCG. BIN00 of Cell #00
RO_IS_AEB_CNT_SP1H_AREA00_BIN01	U18.0	-	E15 [1:0]	E14 [7:0]	E13 [7:0]		This register indicates the histogram result of

Register Name	Unit	Bit Assignment for Embedded IDs				Line	Description
		[31:24]	[23:16]	[15:8]	[7:0]		
							SP1_HCG. BIN00 of AREA00
...
RO_IS_AEB_CNT_SP1H_AREA00_BIN15	U18.0	-	E75 [1:0]	E74 [7:0]	E73 [7:0]		This register indicates the histogram result of SP1_HCG. BIN01 of AREA00
RO_IS_AEB_CNT_SP1H_AREA01_BIN00	U18.0	-	E79 [1:0]	E78 [7:0]	E77 [7:0]		This register indicates the histogram result of SP1_HCG. BIN00 of AREA01
...
RO_IS_AEB_CNT_SP1H_AREA12_BIN07	U18.0	-	E807 [1:0]	E806 [7:0]	E805[7:0]		This register indicates the histogram result of SP1_HCG. BIN07 of AREA12
RO_IS_AEB_CNT_SP1H_AREA12_BIN08	U18.0	-	E11 [1:0]	E10 [7:0]	E9 [7:0]	The output information in the 3rd line of the Rear Embedded Data	This register indicates the histogram result of SP1_HCG. BIN08 of AREA12
RO_IS_AEB_CNT_SP1H_AREA12_BIN09	U18.0	-	E15 [1:0]	E14 [7:0]	E13 [7:0]		This register indicates the histogram result of SP1_HCG. BIN09 of AREA12
...
RO_IS_AEB_CNT_SP1H_AREA24_BIN15	U18.0	-	E807 [1:0]	E806 [7:0]	E805 [7:0]		This register indicates the histogram result of SP1_HCG. BIN15 of AREA24
RO_IS_AEB_CNT_SP1L_AREA00_BIN00	U18.0	-	E11 [1:0]	E10 [7:0]	E9 [7:0]	The output information in the 4th line of the Rear Embedded Data	This register indicates the histogram result of SP1_LCG. BIN00 of AREA00
...
RO_IS_AEB_CNT_SP1L_AREA12_BIN07	U18.0	-	E807 [1:0]	E806 [7:0]	E805 [7:0]		This register indicates the histogram result of SP1_LCG. BIN07 of AREA12
RO_IS_AEB_CNT_SP1L_AREA12_BIN08	U18.0	-	E11 [1:0]	E10 [7:0]	E9 [7:0]	The output information in the 5th line of the Rear Embedded Data	This register indicates the histogram result of SP1_LCG. BIN08 of AREA12
RO_IS_AEB_CNT_SP1L_AREA12_BIN09	U18.0	-	E15 [1:0]	E14 [7:0]	E13 [7:0]		This register indicates the histogram result of SP1_LCG. BIN09 of AREA12
...
RO_IS_AEB_CNT_SP1L_AREA24_BIN15	U18.0	-	E807 [1:0]	E806 [7:0]	E805 [7:0]		This register indicates the histogram result of SP1_LCG. BIN15 of AREA24
RO_IS_AEB_CNT_SP2H_AREA00_BIN00	U18.0	-	E11 [1:0]	E10 [7:0]	E9 [7:0]	The output information in the 6th line of	This register indicates the histogram result of

Register Name	Unit	Bit Assignment for Embedded IDs				Line	Description
		[31:24]	[23:16]	[15:8]	[7:0]		
						the Rear Embedded Data	SP2H. BIN00 of AREA00
RO_IS_AEB_CNT_SP2H_AREA00_BIN01	U18.0	-	E15 [1:0]	E14 [7:0]	E13 [7:0]		This register indicates the histogram result of SP2H. BIN00 of Cell #01
...
RO_IS_AEB_CNT_SP2H_AREA12_BIN07	U18.0	-	E807 [1:0]	E806 [7:0]	E805 [7:0]		This register indicates the histogram result of SP2H. BIN07 of Cell #12
RO_IS_AEB_CNT_SP2H_AREA12_BIN08	U18.0	-	E11 [1:0]	E10 [7:0]	E9 [7:0]		This register indicates the histogram result of SP2H. BIN08 of Cell #12
RO_IS_AEB_CNT_SP2H_AREA12_BIN09	U18.0	-	E15 [1:0]	E14 [7:0]	E13 [7:0]	The output information in the 7th line of the Rear Embedded Data	This register indicates the histogram result of SP2H. BIN09 of Cell #12
...
RO_IS_AEB_CNT_SP2H_AREA24_BIN15	U18.0	-	E807 [1:0]	E806 [7:0]	E805 [7:0]		This register indicates the histogram result of SP2H. BIN15 of Cell #24
RO_IS_AEB_CNT_SP2L_AREA00_BIN00	U18.0	-	E11 [1:0]	E10 [7:0]	E9 [7:0]		This register indicates the histogram result of SP2L. BIN00 of Cell #00
RO_IS_AEB_CNT_SP2L_AREA00_BIN01	U18.0	-	E15 [1:0]	E14 [7:0]	E13 [7:0]	The output information in the 8th line of the Rear Embedded Data	This register indicates the histogram result of SP2L. BIN00 of Cell #01
...
RO_IS_AEB_CNT_SP2L_AREA12_BIN07	U18.0	-	E807 [1:0]	E806 [7:0]	E805 [7:0]		This register indicates the histogram result of SP2L. BIN07 of Cell #12
RO_IS_AEB_CNT_SP2L_AREA12_BIN08	U18.0	-	E11 [1:0]	E10 [7:0]	E9 [7:0]		This register indicates the histogram result of SP2L. BIN08 of Cell #12
RO_IS_AEB_CNT_SP2L_AREA12_BIN09	U18.0	-	E15 [1:0]	E14 [7:0]	E13 [7:0]	The output information in the 9th line of the Rear Embedded Data	This register indicates the histogram result of SP2L. BIN09 of Cell #12
...
RO_S_AEB_CNT_SP2L_AREA24_BIN15	U18.0	-	E807 [1:0]	E806 [7:0]	E805 [7:0]		This register indicates the histogram result of SP2L. BIN15 of Cell #24

6.9.3.6.5. Spot Pixel Information

This information indicates the information about the spot pixels recorded in the sensor. For details, refer to “[5.6 Spot Pixel Compensation Function](#).”

◇ Memo

If the value of the REBD_STC_INFO_DISABLE register is set to 1, the 11 lines of the Rear Embedded Data that contains the spot pixel information is not transmitted.

◆ Note

While the sensor is in Streaming State, the host can stop the output of the Rear Embedded Data using the REBD_STC_INFO_DISABLE register. However, the host cannot resume the output in this state.

To resume the output of the Rear Embedded Data, set the REBD_STC_INFO_DISABLE register to 0 while the sensor is in Start-up State.

■ Information about the number of spot pixels

This information indicates the number of spot pixels regarding SP1 and SP2, recorded in the sensor.

Table 6-77 Rear Embedded Data Bit Assignment for the Pixel Count Information About Spot Pixels

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U11.0	-	-	E10[2:0]	E09[7:0]	Information about the number of spot pixels of SP1
-	U11.0	-	-	E12[2:0]	E11[7:0]	Information about the number of spot pixels of SP2

◇ Memo

The number of spot pixels indicated by the Rear Embedded Data is the sum of spot pixels recorded in the following two areas:

- PICT_STC_PIX category (Up to 100 points)
- OTP (Up to 1024 points)

■ Coordinate information about spot pixels

This information indicates the coordinates of spot pixels regarding SP1 and SP2, recorded in the sensor.

The sensor transmits the coordinate information about spot pixels in 8 lines. The first four lines and the second four lines indicate the coordinate information about the spot pixels of SP1 and SP2 respectively.

Each line contains coordinates for up to 225 points. This information indicates 0xFF for the coordinates for spot pixels that exceed the number of spot pixels recorded in the sensor.

The order of spot pixel coordinates transmitted by the Rear Embedded Data is sorted in ascending order with the vertical coordinates first and then the horizontal coordinates.

Table 6-78 Rear Embedded Data Bit Assignment for the Spot Pixel Coordinate Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U11.0	-	-	E10[2:0]	E09[7:0]	Vertical coordinate of a spot pixel
-	U11.0	-	-	E12[2:0]	E11[7:0]	Horizontal coordinate of a spot pixel

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
...
-	U11.0	-	-	E906[2:0]	E905[7:0]	Vertical coordinate of a spot pixel
-	U11.0	-	-	E908[2:0]	E907[7:0]	Horizontal coordinate of a spot pixel

6.9.3.6.6. Frame CRC Information

This information indicates a CRC calculated by the sensor from one frame of output data.

Regarding the Frame CRC Information, the bit assignment position and the amount of information vary corresponding to the drive mode and the RAW data format.

- Normal, HDR (UC) or HDR (PWL) mode: E09 - E12
- HDR (Line/Line) mode
 - RAW12 x 2: E13 - E20
 - RAW12 x 4: E13 - E28

Table 6-79 Rear Embedded Data Bit Assignment for the Frame CRC Information

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U32.0	E12[7:0]	E11[7:0]	E10[7:0]	E09[7:0]	The Frame CRC Information in Normal, HDR (UC) or HDR (PWL) drive mode
-	U32.0	E16[7:0]	E15[7:0]	E14[7:0]	E13[7:0]	The Frame CRC Information of the first image in HDR (Line/Line) drive mode <ul style="list-style-type: none"> In Normal, HDR (UC) or HDR (PWL) drive mode, the sensor transmits 0xFFFFFFFF.
-	U32.0	E20[7:0]	E19[7:0]	E18[7:0]	E17[7:0]	The Frame CRC Information of the second image in HDR (Line/Line) drive mode <ul style="list-style-type: none"> In Normal, HDR (UC) or HDR (PWL) drive mode, the sensor transmits 0xFFFFFFFF.
-	U32.0	E24[7:0]	E23[7:0]	E22[7:0]	E21[7:0]	The Frame CRC Information of the third image in HDR (Line/Line) drive mode and in RAW12x4 output format <ul style="list-style-type: none"> In Normal, HDR (UC), HDR (PWL) or HDR (Line/Line) drive mode and in RAW12x2 output format, the sensor transmits 0xFFFFFFFF.
-	U32.0	E28[7:0]	E27[7:0]	E26[7:0]	E25[7:0]	The Frame CRC Information of the fourth image in HDR (Line/Line) drive mode and in RAW12x4 output format <ul style="list-style-type: none"> In Normal, HDR (UC), HDR (PWL) or HDR (Line/Line) drive mode and in RAW12x2 output format, the sensor transmits 0xFFFFFFFF.

6.9.3.6.7. CRC Information

This information indicates the following two CRC-32 values:

- Header CRC: A CRC-32 value calculated from the header (E01 to E04)
- Footer CRC: A CRC-32 value calculated from the values from the data ^{*1} immediately after the header CRC to the preceding data ^{*2} before the footer CRC.
 - E09
 - For the Front Embedded Data, E596. For the Rear Embedded Data, E908

The CRC-32 calculation method used by the sensor complies with IEEE802.3.

The following list contains the information to be used for the CRC-32 calculation:

- CRC generator polynomial: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$

- Initial value: 0xFFFFFFFF
- Shift direction: Right
- Output reversal: Enabled
- Bit swapping: Enabled

◆ Note

When four pixels of the Line Information have been assigned, the sensor calculates this information for the header CRC. For details, refer to “[2.4.5 Line Information](#).”

Table 6-80 Front Embedded Data Bit Assignment for CRCs

● Front Embedded Data

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U32.0	E08[7:0]	E07[7:0]	E06[7:0]	E05[7:0]	Header CRC
-	U32.0	E600[7:0]	E599[7:0]	E598[7:0]	E597[7:0]	Footer CRC

● Rear Embedded Data

Register Name	Unit	Bit Assignment for Embedded IDs				Description
		[31:24]	[23:16]	[15:8]	[7:0]	
-	U32.0	E08[7:0]	E07[7:0]	E06[7:0]	E05[7:0]	Header CRC
-	U32.0	E912[7:0]	E911[7:0]	E910[7:0]	E909[7:0]	Footer CRC

6.9.4. Interface

The following shows the registers to which data is written only by the Information Output function. For other information sent out from the Information Output function and corresponding registers, refer to the description of each function.

6.9.4.1. Input Registers

Table 6-81 Input Registers for the Information Output Function

[CONFIG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A64	1	0	REBD_STC_INFO_DISABLE	R/W	U1.0	This register is used to stop the output of the spot pixel information. 0: The sensor does not stop the output of the spot pixel information. 1: The sensor stops the output of the spot pixel information. • While the sensor is in Streaming State, only the processing for image output is enabled.

[VIF]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBDB8	1	0	FEBD_REG_INFO_EN_0	R/W	U1.0	This register is used to enable or disable the output of the Information 0 regarding host-selected register(s). 0: Disabled 1: Enabled
0xBDB9	1	7:0	FEBD_REG_INFO_CAT_0	R/W	U8.0	This register is used to set the category number of a register transmitted by the Information 0 regarding host-selected register(s).
0xBDBA	2	15:0	FEBD_REG_INFO_OFFSET_0	R/W	U16.0	This register is used to set the offset address of a register transmitted by the Information 0 regarding host-selected register(s).
0xBDBC	1	0	FEBD_REG_INFO_EN_1	R/W	U1.0	This register is used to enable or disable the output of the Information 1 regarding host-selected register(s). 0: Disabled 1: Enabled
0xBDBD	1	7:0	FEBD_REG_INFO_CAT_1	R/W	U8.0	This register is used to set the category number of a register transmitted by the Information 1 regarding host-selected register(s).
0xBDBE	2	15:0	FEBD_REG_INFO_OFFSET_1	R/W	U16.0	This register is used to set the offset address of a register transmitted by the Information 1 regarding host-selected register(s).
...		
0xBDDC	1	0	FEBD_REG_INFO_EN_9	R/W	U1.0	This register is used to enable or disable the output of the Information 9 regarding host-selected register(s). 0: Disabled 1: Enabled
0xBDDD	1	7:0	FEBD_REG_INFO_CAT_9	R/W	U8.0	This register is used to set the category number of a register transmitted by the Information 9 regarding host-selected register(s).
0xBDDE	2	15:0	FEBD_REG_INFO_OFFSET_9	R/W	U16.0	This register is used to set the offset address of a register transmitted by the Information 9 regarding host-selected register(s).

[CTRL1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1ADC	4	31:0	IR_DR_I2I_FEBD_FRMCNT_MAX	R/W	U32.0	This register is used to set the maximum value of the Frame Count which is added to the Front Embedded Data. * When this value is set to 0, the Frame Count value is fixed at 0.
0x1AE5	1	0	WO_DR_I2I_FEB_D_FRMCNT_CLR	W	U1.0	This register is used to select whether to reset the Frame Count in the Embedded Data to 1. 0: Reset disabled 1: Reset enabled
0x1AEC	1	0	WO_I1_CMN_AE_CAPTURE	W	U1.0	This register is used to obtain the histogram information. When reading out the RO_IS_AEB_CNT_x_AREAy_BINz (x = SP1H, SP1L, SP2H, SP2L)(y = 00 to 24)(z = 0 to 15) registers, set these registers to 1 for the frame where light metering is performed.
0x1B86	2	11:0	IR_IS_AEB_HSTA_RT	R/W	U12.0	The horizontal coordinate at the upper left corner of the AE light metering window • Set 0 or a value that is a multiple of 4.
0x1B88	2	11:0	IR_IS_AEB_VSTA_RT	R/W	U12.0	The vertical coordinate at the upper left corner of the AE light metering window. • Set 0 or a value that is a multiple of 4.
0x1B8A	2	9:0	IR_IS_AEB_HWIN	R/W	U10.0	The horizontal size of each cell of the AE light metering window (in pixels) • Set a value of 8 or greater. • Set a value that is a multiple of 4.
0x1B8C	2	9:0	IR_IS_AEB_VWIN	R/W	U10.0	The vertical size of each cell of the AE light metering window (in pixels) • Set a value of 8 or greater. • Set a value that is a multiple of 4.
0x1B8E	1	2:0	IR_IS_AEB_HNUM	R/W	U3.0	The number of cells of the AE light metering window in the horizontal direction • Set a value under the following condition: $3 \leq \text{IR_IS_AEB_VNUM} \leq 5$.
0x1B8F	1	2:0	IR_IS_AEB_VNUM	R/W	U3.0	The number of cells of the AE light metering window in the vertical direction • Set a value under the following condition: $3 \leq \text{IR_IS_AEB_VNUM} \leq 5$.
0x1B90	2	11:0	IR_IS_AEB_YREF_SP1H_00	R/W	U12.0	The threshold (00) for the SP1_HCG histogram
0x1B92	2	11:0	IR_IS_AEB_YREF_SP1H_01	R/W	U12.0	The threshold (01) for the SP1_HCG histogram
...	
0x1BB0	2	11:0	IR_IS_AEB_YREF_SP1H_16	R/W	U12.0	The threshold (16) for the SP1_HCG histogram
0x1BB2	2	11:0	IR_IS_AEB_YREF_SP1L_00	R/W	U12.0	The threshold (00) for the SP1_LCG histogram
0x1BB4	2	11:0	IR_IS_AEB_YREF_SP1L_01	R/W	U12.0	The threshold (01) for the SP1_LCG histogram
...	
0x1BD2	2	11:0	IR_IS_AEB_YREF_SP1L_16	R/W	U12.0	The threshold (16) of the SP1_LCG histogram
0x1BD4	2	11:0	IR_IS_AEB_YREF_SP2H_00	R/W	U12.0	The threshold (00) for the SP2_HCG histogram
0x1BD6	2	11:0	IR_IS_AEB_YREF_SP2H_01	R/W	U12.0	The threshold (01) for the SP2_HCG histogram.
...	
0x1BF4	2	11:0	IR_IS_AEB_YREF_	R/W	U12.0	The threshold (16) of the histogram for the SP2_HCG.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
			SP2H_16			
0x1BF6	2	11:0	IR_IS_AEB_YREF_SP2L_00	R/W	U12.0	The threshold (00) of the histogram for the SP2_LCG.
0x1BF8	2	11:0	IR_IS_AEB_YREF_SP2L_01	R/W	U12.0	The threshold (01) of the histogram for the SP2_LCG.
...		
0x1C16	2	11:0	IR_IS_AEB_YREF_SP2L_16	R/W	U12.0	The threshold (16) of the histogram for the SP2_LCG.
0x1C1A	2	11:0	IR_IS_AWB_HSTA_RT	R/W	U12.0	The horizontal coordinate at the upper left corner of the AWB light metering window Set 0 or a value that is a multiple of 4.
0x1C1C	2	11:0	IR_IS_AWB_VSTA_RT	R/W	U12.0	The vertical coordinate at the upper left corner of the AWB light metering window. Set 0 or a value that is a multiple of 4.
0x1C1E	2	11:0	IR_IS_AWB_HWI_N	R/W	U12.0	The horizontal size of the AWB light metering window (in pixels) <ul style="list-style-type: none"> Set a value greater than or equal to 4. Set a value that is a multiple of 4.
0x1C20	2	11:0	IR_IS_AWB_VWI_N	R/W	U12.0	The vertical size of the AWB light metering window (in pixels) <ul style="list-style-type: none"> Set a value greater than or equal to 4. Set a value that is a multiple of 4.
0x1C22	1	0	IR_IS_AWB_CF_P_EAK_SEL	R/W	U1.0	Selection of the signal level for the integration method for the CF signal of the AWB information. <ul style="list-style-type: none"> 0: The signal level is used as is. 1: The absolute value of the signal level is used.
0x1C24	2	11:0	IR_IS_AWB_Y_PEAK_SP1H	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of luminance) for determining whether to integrate the pixel for the AWB information calculation. (SP1_HCG)
0x1C26	2	11:0	IR_IS_AWB_Y_DA_RK_SP1H	R/W	U12.0	This register is used to set the threshold (i.e., the lower limit of luminance) for determining whether to integrate the pixel for the AWB information calculation. (SP1_HCG)
0x1C28	2	11:0	IR_IS_AWB_CF0_PEAK_SP1H	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF0 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP1_HCG)
0x1C2A	2	11:0	IR_IS_AWB_CF12_PEAK_SP1H	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF12 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP1_HCG)
0x1C2C	2	11:0	IR_IS_AWB_CF3_PEAK_SP1H	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF3 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP1_HCG)
0x1C2E	2	11:0	IR_IS_AWB_Y_PEAK_SP1L	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of luminance) for determining whether to integrate the pixel for the AWB information calculation. (SP1_LCG)
0x1C30	2	11:0	IR_IS_AWB_Y_DA_RK_SP1L	R/W	U12.0	This register is used to set the threshold (i.e., the lower limit of luminance) for determining whether to integrate the pixel for the AWB information calculation. (SP1_LCG)
0x1C32	2	11:0	IR_IS_AWB_CF0_PEAK_SP1L	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF0 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP1_LCG)
0x1C34	2	11:0	IR_IS_AWB_CF12_PEAK_SP1L	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF12 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP1_LCG)
0x1C36	2	11:0	IR_IS_AWB_CF3_	R/W	U12.0	This register is used to set the threshold (i.e.,

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
			PEAK_SP1L			the upper limit of the CF3 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP1_LCG)
0x1C38	2	11:0	IR_IS_AWB_Y_PEAK_SP2H	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of luminance) for determining whether to integrate the pixel for the AWB information calculation. (SP2_HCG)
0x1C3A	2	11:0	IR_IS_AWB_Y_DARKEK_SP2H	R/W	U12.0	This register is used to set the threshold (i.e., the lower limit of luminance) for determining whether to integrate the pixel for the AWB information calculation. (SP2_HCG)
0x1C3C	2	11:0	IR_IS_AWB_CF0_PEAK_SP2H	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF0 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP2_HCG)
0x1C3E	2	11:0	IR_IS_AWB_CF12_PEAK_SP2H	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF12 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP2_HCG)
0x1C40	2	11:0	IR_IS_AWB_CF3_PEAK_SP2H	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF3 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP2_HCG)
0x1C42	2	11:0	IR_IS_AWB_Y_PEAK_SP2L	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of luminance) for determining whether to integrate the pixel for the AWB information calculation. (SP2_LCG)
0x1C44	2	11:0	IR_IS_AWB_Y_DARKEK_SP2L	R/W	U12.0	This register is used to set the threshold (i.e., the lower limit of luminance) for determining whether to integrate the pixel for the AWB information calculation. (SP2_LCG)
0x1C46	2	11:0	IR_IS_AWB_CF0_PEAK_SP2L	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF0 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP2_LCG)
0x1C48	2	11:0	IR_IS_AWB_CF12_PEAK_SP2L	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF12 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP2_LCG)
0x1C4A	2	11:0	IR_IS_AWB_CF3_PEAK_SP2L	R/W	U12.0	This register is used to set the threshold (i.e., the upper limit of the CF3 signal level) for determining whether to integrate the pixel for the AWB information calculation. (SP2_LCG)

[CONST1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x0171	1	0	IR_DR_I2I_FEBD_EN	R/W	U1.0	This register is used to enable or disable the output of the Front Embedded Data. 0: Output disabled 1: Output enabled
0x0172	1	0	IR_DR_I2I_REBD_EN	R/W	U1.0	This register is used to enable or disable the output of the Rear Embedded Data. 0: Output disabled 1: Output enabled
0x0173	1	0	IR_DR_EBD_AWB_INFO_EN	R/W	U1.0	This register indicates the output state of the AWB information. 0: Output disabled 1: Output enabled
0x0174	1	0	IR_DR_EBD_HIST_INFO_EN	R/W	U1.0	This register indicates the output state of the histogram information. 0: Output disabled 1: Output enabled
0x01B9	1	0	IR_DR_I2I_FEBD_FRMCNT_MAX_RESET	R/W	U1.0	This register is used to forcibly reset the Frame Count when the maximum value (i.e., IR_DR_I2I_FEBD_FRMCNT_MAX) of the Frame

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
						Count in the Front Embedded Data is dynamically changed. 0: Forcible reset disabled 1: Forcible reset enabled

6.9.4.2. Output Register

Table 6-82 Output Registers for the Information Output Function

[VIF_COM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x7DC8	4	31:0	DIF_FRMINFO_FRAME_COUNT	R	U32.0	This register indicates the Frame Count value added to the Front Embedded Data.

[STATE]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1F40	2	11:0	RO_CD_DU_TEMP_SENSOR_OUT	R	U8.4	This register indicates the temperature information of Temperature Sensor 1. The sensor's temperature [°C] = the sensor's temperature information / 16 – 50
0x1F42	2	11:0	RO_CD_DU_TEMP_SENSOR1_OUT	R	U8.4	This register indicates the temperature information of Temperature Sensor 2. The sensor's temperature [°C] = the sensor's temperature information / 16 – 50
0x1FA8	1	0	RO_IS_AWB_INT_CF0_SP1H_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF0 of the SP1_HCG line.
0x1FA9	1	0	RO_IS_AWB_INT_CF12_SP1H_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF12 of the SP1_HCG line.
0x1FAA	1	0	RO_IS_AWB_INT_CF3_SP1H_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF3 of the SP1_HCG line.
0x1FAB	1	0	RO_IS_AWB_INT_CF0_SP1L_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF0 of the SP1_LCG line.
0x1FAC	1	0	RO_IS_AWB_INT_CF12_SP1L_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF12 of the SP1_LCG line.
0x1FAD	1	0	RO_IS_AWB_INT_CF3_SP1L_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF3 of the SP1_LCG line.
0x1FAE	1	0	RO_IS_AWB_INT_CF0_SP2H_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF0 of the SP2_HCG line.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1FAF	1	0	RO_IS_AWB_INT_CF12_SP2H_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF12 of the SP2_HCG line.
0x1FB0	1	0	RO_IS_AWB_INT_CF3_SP2H_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF3 of the SP2_HCG line.
0x1FB1	1	0	RO_IS_AWB_INT_CF0_SP2L_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF0 of the SP2_LCG line.
0x1FB2	1	0	RO_IS_AWB_INT_CF12_SP2L_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF12 of the SP2_LCG line.
0x1FB3	1	0	RO_IS_AWB_INT_CF3_SP2L_L	R	U1.0	This register indicates the integrated value (LSB) of the signal level in the light metering window to be used for the AWB Information for the CF3 of the SP2_LCG line.
0x1FB4	4	31:0	RO_IS_AWB_INT_CF0_SP1H_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF0 of the SP1_HCG line.
0x1FB8	4	31:0	RO_IS_AWB_INT_CF12_SP1H_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF12 of the SP1_HCG line.
0x1FBC	4	31:0	RO_IS_AWB_INT_CF3_SP1H_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF3 of the SP1_HCG line.
0x1FC0	4	31:0	RO_IS_AWB_INT_CF0_SP1L_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF0 of the SP1_LCG line.
0x1FC4	4	31:0	RO_IS_AWB_INT_CF12_SP1L_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF12 of the SP1_LCG line.
0x1FC8	4	31:0	RO_IS_AWB_INT_CF3_SP1L_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF3 of the SP1_LCG line.
0x1FCC	4	31:0	RO_IS_AWB_INT_CF0_SP2H_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF0 of the SP2_HCG line.
0x1FD0	4	31:0	RO_IS_AWB_INT_CF12_SP2H_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF12 of the SP2_HCG line.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1FD4	4	31:0	RO_IS_AWB_INT_CF3_SP2H_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF3 of the SP2_HCG line.
0x1FD8	4	31:0	RO_IS_AWB_INT_CF0_SP2L_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF0 of the SP2_LCG line.
0x1FDC	4	31:0	RO_IS_AWB_INT_CF12_SP2L_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF12 of the SP2_LCG line.
0x1FE0	4	31:0	RO_IS_AWB_INT_CF3_SP2L_H	R	U32.0	This register indicates the integrated value (MSB) of the signal level in the light metering window to be used for the AWB Information for the CF3 of the SP2_LCG line.
0x1FE4	3	20:0	RO_IS_AWB_PIXCNT_SP1H	R	U21.0	The number of Integrated pixels of the AWB information for SP1_HCG
0x1FE8	3	20:0	RO_IS_AWB_PIXCNT_SP1L	R	U21.0	The number of Integrated pixels of the AWB information for SP1_LCG
0x1FEC	3	20:0	RO_IS_AWB_PIXCNT_SP2H	R	U21.0	The number of Integrated pixels of the AWB information for SP2H
0x1FF0	3	20:0	RO_IS_AWB_PIXCNT_SP2L	R	U21.0	The number of Integrated pixels of the AWB information for SP2L
0x6000	3	17:0	RO_IS_AEB_CNT_SP1H_AREA00_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA00
0x6004	3	17:0	RO_IS_AEB_CNT_SP1H_AREA00_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA00
...		
0x603C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA00_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA00
0x6040	3	17:0	RO_IS_AEB_CNT_SP1H_AREA01_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA01
0x6044	3	17:0	RO_IS_AEB_CNT_SP1H_AREA01_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA01
...		
0x607C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA01_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA01
0x6080	3	17:0	RO_IS_AEB_CNT_SP1H_AREA02_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA02
0x6084	3	17:0	RO_IS_AEB_CNT_SP1H_AREA02_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA02
...		
0x60BC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA02_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA02
0x60C0	3	17:0	RO_IS_AEB_CNT_SP1H_AREA03_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA03
0x60C4	3	17:0	RO_IS_AEB_CNT_SP1H_	R	U18.0	This register indicates the histogram result of SP1_HCG.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
			AREA03_BIN01			BIN01 of AREA03
...		
0x60FC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA03_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA03
0x6100	3	17:0	RO_IS_AEB_CNT_SP1H_AREA04_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA04
0x6104	3	17:0	RO_IS_AEB_CNT_SP1H_AREA04_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA04
...		
0x613C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA04_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA04
0x6140	3	17:0	RO_IS_AEB_CNT_SP1H_AREA05_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA05
0x6144	3	17:0	RO_IS_AEB_CNT_SP1H_AREA05_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA05
...		
0x617C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA05_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA05
0x6180	3	17:0	RO_IS_AEB_CNT_SP1H_AREA06_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA06
0x6184	3	17:0	RO_IS_AEB_CNT_SP1H_AREA06_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA06
...		
0x61BC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA06_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA06
0x61C0	3	17:0	RO_IS_AEB_CNT_SP1H_AREA07_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA07
0x61C4	3	17:0	RO_IS_AEB_CNT_SP1H_AREA07_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA07
...		
0x61FC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA07_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA07
0x6200	3	17:0	RO_IS_AEB_CNT_SP1H_AREA08_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA08
0x6204	3	17:0	RO_IS_AEB_CNT_SP1H_AREA08_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA08
...		
0x623C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA08_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA08
0x6240	3	17:0	RO_IS_AEB_CNT_SP1H_AREA09_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA09
0x6244	3	17:0	RO_IS_AEB_CNT_SP1H_AREA09_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA09
...		
0x627C	3	17:0	RO_IS_AEB_CNT_SP1H_	R	U18.0	This register indicates the histogram result of SP1_HCG.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
			AREA09_BIN15			BIN15 of AREA09
0x6280	3	17:0	RO_IS_AEB_CNT_SP1H_AREA10_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA10
0x6284	3	17:0	RO_IS_AEB_CNT_SP1H_AREA10_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA10
...		
0x62BC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA10_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA10
0x62C0	3	17:0	RO_IS_AEB_CNT_SP1H_AREA11_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA11
0x62C4	3	17:0	RO_IS_AEB_CNT_SP1H_AREA11_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA11
...		
0x62FC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA11_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA11
0x6300	3	17:0	RO_IS_AEB_CNT_SP1H_AREA12_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA12
0x6304	3	17:0	RO_IS_AEB_CNT_SP1H_AREA12_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA12
...		
0x633C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA12_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA12
0x6340	3	17:0	RO_IS_AEB_CNT_SP1H_AREA13_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA13
0x6344	3	17:0	RO_IS_AEB_CNT_SP1H_AREA13_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA13
...		
0x637C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA13_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA13
0x6380	3	17:0	RO_IS_AEB_CNT_SP1H_AREA14_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA14
0x6384	3	17:0	RO_IS_AEB_CNT_SP1H_AREA14_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA14
...		
0x63BC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA14_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA14
0x63C0	3	17:0	RO_IS_AEB_CNT_SP1H_AREA15_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA15
0x63C4	3	17:0	RO_IS_AEB_CNT_SP1H_AREA15_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA15
...		
0x63FC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA15_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA15
0x6400	3	17:0	RO_IS_AEB_CNT_SP1H_AREA16_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA16

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x6404	3	17:0	RO_IS_AEB_CNT_SP1H_AREA16_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA16
...		
0x643C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA16_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA16
0x6440	3	17:0	RO_IS_AEB_CNT_SP1H_AREA17_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA17
0x6444	3	17:0	RO_IS_AEB_CNT_SP1H_AREA17_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA17
...		
0x647C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA17_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA17
0x6480	3	17:0	RO_IS_AEB_CNT_SP1H_AREA18_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA18
0x6484	3	17:0	RO_IS_AEB_CNT_SP1H_AREA18_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA18
...		
0x64BC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA18_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA18
0x64C0	3	17:0	RO_IS_AEB_CNT_SP1H_AREA19_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA19
0x64C4	3	17:0	RO_IS_AEB_CNT_SP1H_AREA19_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA19
...		
0x64FC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA19_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA19
0x6500	3	17:0	RO_IS_AEB_CNT_SP1H_AREA20_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA20
0x6504	3	17:0	RO_IS_AEB_CNT_SP1H_AREA20_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA20
...		
0x653C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA20_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA20
0x6540	3	17:0	RO_IS_AEB_CNT_SP1H_AREA21_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA21
0x6544	3	17:0	RO_IS_AEB_CNT_SP1H_AREA21_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA21
...		
0x657C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA21_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA21
0x6580	3	17:0	RO_IS_AEB_CNT_SP1H_AREA22_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA22
0x6584	3	17:0	RO_IS_AEB_CNT_SP1H_AREA22_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA22
...		

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x65BC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA22_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA22
0x65C0	3	17:0	RO_IS_AEB_CNT_SP1H_AREA23_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA23
0x65C4	3	17:0	RO_IS_AEB_CNT_SP1H_AREA23_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA23
...		
0x65FC	3	17:0	RO_IS_AEB_CNT_SP1H_AREA23_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA23
0x6600	3	17:0	RO_IS_AEB_CNT_SP1H_AREA24_BIN00	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN00 of AREA24
0x6604	3	17:0	RO_IS_AEB_CNT_SP1H_AREA24_BIN01	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN01 of AREA24
...		
0x663C	3	17:0	RO_IS_AEB_CNT_SP1H_AREA24_BIN15	R	U18.0	This register indicates the histogram result of SP1_HCG. BIN15 of AREA24
0x6800	3	17:0	RO_IS_AEB_CNT_SP1L_AREA00_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA00
0x6804	3	17:0	RO_IS_AEB_CNT_SP1L_AREA00_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA00
...		
0x683C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA00_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA00
0x6840	3	17:0	RO_IS_AEB_CNT_SP1L_AREA01_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA01
0x6844	3	17:0	RO_IS_AEB_CNT_SP1L_AREA01_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA01
...		
0x687C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA01_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA01
0x6880	3	17:0	RO_IS_AEB_CNT_SP1L_AREA02_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA02
0x6884	3	17:0	RO_IS_AEB_CNT_SP1L_AREA02_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA02
...		
0x68BC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA02_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA02
0x68C0	3	17:0	RO_IS_AEB_CNT_SP1L_AREA03_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA03
0x68C4	3	17:0	RO_IS_AEB_CNT_SP1L_AREA03_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA03
...		
0x68FC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA03_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA03
0x6900	3	17:0	RO_IS_AEB_CNT_SP1L_	R	U18.0	This register indicates the histogram

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
			AREA04_BIN00			result of SP1_LCG. BIN00 of AREA04
0x6904	3	17:0	RO_IS_AEB_CNT_SP1L_AREA04_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA04
...		
0x693C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA04_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA04
0x6940	3	17:0	RO_IS_AEB_CNT_SP1L_AREA05_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA05
0x6944	3	17:0	RO_IS_AEB_CNT_SP1L_AREA05_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA05
...		
0x697C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA05_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA05
0x6980	3	17:0	RO_IS_AEB_CNT_SP1L_AREA06_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA06
0x6984	3	17:0	RO_IS_AEB_CNT_SP1L_AREA06_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA06
...		
0x69BC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA06_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA06
0x69C0	3	17:0	RO_IS_AEB_CNT_SP1L_AREA07_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA07
0x69C4	3	17:0	RO_IS_AEB_CNT_SP1L_AREA07_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA07
...		
0x69FC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA07_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA07
0x6A00	3	17:0	RO_IS_AEB_CNT_SP1L_AREA08_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA08
0x6A04	3	17:0	RO_IS_AEB_CNT_SP1L_AREA08_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA08
...		
0x6A3C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA08_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA08
0x6A40	3	17:0	RO_IS_AEB_CNT_SP1L_AREA09_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA09
0x6A44	3	17:0	RO_IS_AEB_CNT_SP1L_AREA09_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA09
...		
0x6A7C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA09_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA09
0x6A80	3	17:0	RO_IS_AEB_CNT_SP1L_AREA10_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA10
0x6A84	3	17:0	RO_IS_AEB_CNT_SP1L_AREA10_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
						BIN01 of AREA10
...		
0x6ABC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA10_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA10
0x6AC0	3	17:0	RO_IS_AEB_CNT_SP1L_AREA11_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA11
0x6AC4	3	17:0	RO_IS_AEB_CNT_SP1L_AREA11_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA11
...		
0x6AFC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA11_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA11
0x6B00	3	17:0	RO_IS_AEB_CNT_SP1L_AREA12_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA12
0x6B04	3	17:0	RO_IS_AEB_CNT_SP1L_AREA12_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA12
...		
0x6B3C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA12_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA12
0x6B40	3	17:0	RO_IS_AEB_CNT_SP1L_AREA13_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA13
0x6B44	3	17:0	RO_IS_AEB_CNT_SP1L_AREA13_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA13
...		
0x6B7C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA13_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA13
0x6B80	3	17:0	RO_IS_AEB_CNT_SP1L_AREA14_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA14
0x6B84	3	17:0	RO_IS_AEB_CNT_SP1L_AREA14_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA14
...		
0x6BBC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA14_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA14
0x6BC0	3	17:0	RO_IS_AEB_CNT_SP1L_AREA15_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA15
0x6BC4	3	17:0	RO_IS_AEB_CNT_SP1L_AREA15_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA15
...		
0x6BFC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA15_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA15
0x6C00	3	17:0	RO_IS_AEB_CNT_SP1L_AREA16_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA16
0x6C04	3	17:0	RO_IS_AEB_CNT_SP1L_AREA16_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA16
...		
0x6C3C	3	17:0	RO_IS_AEB_CNT_SP1L_	R	U18.0	This register indicates the histogram result of SP1_LCG.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
			AREA16_BIN15			BIN15 of AREA16
0x6C40	3	17:0	RO_IS_AEB_CNT_SP1L_AREA17_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA17
0x6C44	3	17:0	RO_IS_AEB_CNT_SP1L_AREA17_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA17
...		
0x6C7C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA17_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA17
0x6C80	3	17:0	RO_IS_AEB_CNT_SP1L_AREA18_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA18
0x6C84	3	17:0	RO_IS_AEB_CNT_SP1L_AREA18_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA18
...		
0x6CBC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA18_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA18
0x6CC0	3	17:0	RO_IS_AEB_CNT_SP1L_AREA19_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA19
0x6CC4	3	17:0	RO_IS_AEB_CNT_SP1L_AREA19_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA19
...		
0x6CF0	3	17:0	RO_IS_AEB_CNT_SP1L_AREA19_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA19
0x6D00	3	17:0	RO_IS_AEB_CNT_SP1L_AREA20_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA20
0x6D04	3	17:0	RO_IS_AEB_CNT_SP1L_AREA20_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA20
...		
0x6D3C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA20_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA20
0x6D40	3	17:0	RO_IS_AEB_CNT_SP1L_AREA21_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA21
0x6D44	3	17:0	RO_IS_AEB_CNT_SP1L_AREA21_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA21
...		
0x6D7C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA21_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA21
0x6D80	3	17:0	RO_IS_AEB_CNT_SP1L_AREA22_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA22
0x6D84	3	17:0	RO_IS_AEB_CNT_SP1L_AREA22_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA22
...		
0x6DBC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA22_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA22
0x6DC0	3	17:0	RO_IS_AEB_CNT_SP1L_AREA23_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA23

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x6DC4	3	17:0	RO_IS_AEB_CNT_SP1L_AREA23_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA23
...		
0x6DFC	3	17:0	RO_IS_AEB_CNT_SP1L_AREA23_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA23
0x6E00	3	17:0	RO_IS_AEB_CNT_SP1L_AREA24_BIN00	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN00 of AREA24
0x6E04	3	17:0	RO_IS_AEB_CNT_SP1L_AREA24_BIN01	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN01 of AREA24
...		
0x6E3C	3	17:0	RO_IS_AEB_CNT_SP1L_AREA24_BIN15	R	U18.0	This register indicates the histogram result of SP1_LCG. BIN15 of AREA24
0x7000	3	17:0	RO_IS_AEB_CNT_SP2H_AREA00_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA00
0x7004	3	17:0	RO_IS_AEB_CNT_SP2H_AREA00_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA00
...		
0x703C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA00_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA00
0x7040	3	17:0	RO_IS_AEB_CNT_SP2H_AREA01_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA01
0x7044	3	17:0	RO_IS_AEB_CNT_SP2H_AREA01_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA01
...		
0x707C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA01_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA01
0x7080	3	17:0	RO_IS_AEB_CNT_SP2H_AREA02_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA02
0x7084	3	17:0	RO_IS_AEB_CNT_SP2H_AREA02_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA02
...		
0x70BC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA02_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA02
0x70C0	3	17:0	RO_IS_AEB_CNT_SP2H_AREA03_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA03
0x70C4	3	17:0	RO_IS_AEB_CNT_SP2H_AREA03_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA03
...		
0x70FC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA03_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA03
0x7100	3	17:0	RO_IS_AEB_CNT_SP2H_AREA04_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA04
0x7104	3	17:0	RO_IS_AEB_CNT_SP2H_AREA04_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA04
...		

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x713C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA04_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA04
0x7140	3	17:0	RO_IS_AEB_CNT_SP2H_AREA05_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA05
0x7144	3	17:0	RO_IS_AEB_CNT_SP2H_AREA05_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA05
...		
0x717C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA05_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA05
0x7180	3	17:0	RO_IS_AEB_CNT_SP2H_AREA06_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA06
0x7184	3	17:0	RO_IS_AEB_CNT_SP2H_AREA06_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA06
...		
0x71BC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA06_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA06
0x71C0	3	17:0	RO_IS_AEB_CNT_SP2H_AREA07_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA07
0x71C4	3	17:0	RO_IS_AEB_CNT_SP2H_AREA07_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA07
...		
0x71FC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA07_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA07
0x7200	3	17:0	RO_IS_AEB_CNT_SP2H_AREA08_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA08
0x7204	3	17:0	RO_IS_AEB_CNT_SP2H_AREA08_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA08
...		
0x723C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA08_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA08
0x7240	3	17:0	RO_IS_AEB_CNT_SP2H_AREA09_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA09
0x7244	3	17:0	RO_IS_AEB_CNT_SP2H_AREA09_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA09
...		
0x727C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA09_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA09
0x7280	3	17:0	RO_IS_AEB_CNT_SP2H_AREA10_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA10
0x7284	3	17:0	RO_IS_AEB_CNT_SP2H_AREA10_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA10
...		
0x72BC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA10_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA10
0x72C0	3	17:0	RO_IS_AEB_CNT_SP2H_	R	U18.0	This register indicates the histogram

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
			AREA11_BIN00			result of SP2_HCG. BIN00 of AREA11
0x72C4	3	17:0	RO_IS_AEB_CNT_SP2H_AREA11_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA11
...		
0x72FC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA11_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA11
0x7300	3	17:0	RO_IS_AEB_CNT_SP2H_AREA12_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA12
0x7304	3	17:0	RO_IS_AEB_CNT_SP2H_AREA12_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA12
...		
0x733C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA12_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA12
0x7340	3	17:0	RO_IS_AEB_CNT_SP2H_AREA13_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA13
0x7344	3	17:0	RO_IS_AEB_CNT_SP2H_AREA13_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA13
...		
0x737C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA13_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA13
0x7380	3	17:0	RO_IS_AEB_CNT_SP2H_AREA14_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA14
0x7384	3	17:0	RO_IS_AEB_CNT_SP2H_AREA14_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA14
...		
0x73BC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA14_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA14
0x73C0	3	17:0	RO_IS_AEB_CNT_SP2H_AREA15_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA15
0x73C4	3	17:0	RO_IS_AEB_CNT_SP2H_AREA15_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA15
...		
0x73FC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA15_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA15
0x7400	3	17:0	RO_IS_AEB_CNT_SP2H_AREA16_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA16
0x7404	3	17:0	RO_IS_AEB_CNT_SP2H_AREA16_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA16
...		
0x743C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA16_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA16
0x7440	3	17:0	RO_IS_AEB_CNT_SP2H_AREA17_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA17
0x7444	3	17:0	RO_IS_AEB_CNT_SP2H_AREA17_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
						BIN01 of AREA17
...		
0x747C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA17_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA17
0x7480	3	17:0	RO_IS_AEB_CNT_SP2H_AREA18_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA18
0x7484	3	17:0	RO_IS_AEB_CNT_SP2H_AREA18_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA18
...		
0x74BC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA18_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA18
0x74C0	3	17:0	RO_IS_AEB_CNT_SP2H_AREA19_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA19
0x74C4	3	17:0	RO_IS_AEB_CNT_SP2H_AREA19_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA19
...		
0x74FC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA19_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA19
0x7500	3	17:0	RO_IS_AEB_CNT_SP2H_AREA20_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA20
0x7504	3	17:0	RO_IS_AEB_CNT_SP2H_AREA20_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA20
...		
0x753C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA20_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA20
0x7540	3	17:0	RO_IS_AEB_CNT_SP2H_AREA21_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA21
0x7544	3	17:0	RO_IS_AEB_CNT_SP2H_AREA21_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA21
...		
0x757C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA21_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA21
0x7580	3	17:0	RO_IS_AEB_CNT_SP2H_AREA22_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA22
0x7584	3	17:0	RO_IS_AEB_CNT_SP2H_AREA22_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA22
...		
0x75BC	3	17:0	RO_IS_AEB_CNT_SP2H_AREA22_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA22
0x75C0	3	17:0	RO_IS_AEB_CNT_SP2H_AREA23_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA23
0x75C4	3	17:0	RO_IS_AEB_CNT_SP2H_AREA23_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA23
...		
0x75FC	3	17:0	RO_IS_AEB_CNT_SP2H_	R	U18.0	This register indicates the histogram result of SP2_HCG.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
			AREA23_BIN15			BIN15 of AREA23
0x7600	3	17:0	RO_IS_AEB_CNT_SP2H_AREA24_BIN00	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN00 of AREA24
0x7604	3	17:0	RO_IS_AEB_CNT_SP2H_AREA24_BIN01	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN01 of AREA24
...		
0x763C	3	17:0	RO_IS_AEB_CNT_SP2H_AREA24_BIN15	R	U18.0	This register indicates the histogram result of SP2_HCG. BIN15 of AREA24
0x7800	3	17:0	RO_IS_AEB_CNT_SP2L_AREA00_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA00
0x7804	3	17:0	RO_IS_AEB_CNT_SP2L_AREA00_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA00
...		
0x783C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA00_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA00
0x7840	3	17:0	RO_IS_AEB_CNT_SP2L_AREA01_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA01
0x7844	3	17:0	RO_IS_AEB_CNT_SP2L_AREA01_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA01
...		
0x787C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA01_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA01
0x7880	3	17:0	RO_IS_AEB_CNT_SP2L_AREA02_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA02
0x7884	3	17:0	RO_IS_AEB_CNT_SP2L_AREA02_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA02
...		
0x78BC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA02_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA02
0x78C0	3	17:0	RO_IS_AEB_CNT_SP2L_AREA03_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA03
0x78C4	3	17:0	RO_IS_AEB_CNT_SP2L_AREA03_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA03
...		
0x78FC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA03_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA03
0x7900	3	17:0	RO_IS_AEB_CNT_SP2L_AREA04_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA04
0x7904	3	17:0	RO_IS_AEB_CNT_SP2L_AREA04_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA04
...		
0x793C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA04_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA04
0x7940	3	17:0	RO_IS_AEB_CNT_SP2L_AREA05_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA05

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x7944	3	17:0	RO_IS_AEB_CNT_SP2L_AREA05_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA05
...		
0x797C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA05_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA05
0x7980	3	17:0	RO_IS_AEB_CNT_SP2L_AREA06_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA06
0x7984	3	17:0	RO_IS_AEB_CNT_SP2L_AREA06_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA06
...		
0x79BC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA06_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA06
0x79C0	3	17:0	RO_IS_AEB_CNT_SP2L_AREA07_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA07
0x79C4	3	17:0	RO_IS_AEB_CNT_SP2L_AREA07_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA07
...		
0x79FC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA07_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA07
0x7A00	3	17:0	RO_IS_AEB_CNT_SP2L_AREA08_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA08
0x7A04	3	17:0	RO_IS_AEB_CNT_SP2L_AREA08_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA08
...		
0x7A3C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA08_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA08
0x7A40	3	17:0	RO_IS_AEB_CNT_SP2L_AREA09_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA09
0x7A44	3	17:0	RO_IS_AEB_CNT_SP2L_AREA09_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA09
...		
0x7A7C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA09_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA09
0x7A80	3	17:0	RO_IS_AEB_CNT_SP2L_AREA10_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA10
0x7A84	3	17:0	RO_IS_AEB_CNT_SP2L_AREA10_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA10
...		
0x7ABC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA10_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA10
0x7AC0	3	17:0	RO_IS_AEB_CNT_SP2L_AREA11_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA11
0x7AC4	3	17:0	RO_IS_AEB_CNT_SP2L_AREA11_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA11
...		

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x7AFC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA11_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA11
0x7B00	3	17:0	RO_IS_AEB_CNT_SP2L_AREA12_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA12
0x7B04	3	17:0	RO_IS_AEB_CNT_SP2L_AREA12_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA12
...		
0x7B3C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA12_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA12
0x7B40	3	17:0	RO_IS_AEB_CNT_SP2L_AREA13_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA13
0x7B44	3	17:0	RO_IS_AEB_CNT_SP2L_AREA13_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA13
...		
0x7B7C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA13_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA13
0x7B80	3	17:0	RO_IS_AEB_CNT_SP2L_AREA14_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA14
0x7B84	3	17:0	RO_IS_AEB_CNT_SP2L_AREA14_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA14
...		
0x7BBC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA14_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA14
0x7BC0	3	17:0	RO_IS_AEB_CNT_SP2L_AREA15_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA15
0x7BC4	3	17:0	RO_IS_AEB_CNT_SP2L_AREA15_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA15
...		
0x7BFC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA15_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA15
0x7C00	3	17:0	RO_IS_AEB_CNT_SP2L_AREA16_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA16
0x7C04	3	17:0	RO_IS_AEB_CNT_SP2L_AREA16_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA16
...		
0x7C3C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA16_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA16
0x7C40	3	17:0	RO_IS_AEB_CNT_SP2L_AREA17_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA17
0x7C44	3	17:0	RO_IS_AEB_CNT_SP2L_AREA17_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA17
...		
0x7C7C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA17_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA17
0x7C80	3	17:0	RO_IS_AEB_CNT_SP2L_	R	U18.0	This register indicates the histogram

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
			AREA18_BIN00			result of SP2_LCG. BIN00 of AREA18
0x7C84	3	17:0	RO_IS_AEB_CNT_SP2L_AREA18_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA18
...		
0x7CBC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA18_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA18
0x7CC0	3	17:0	RO_IS_AEB_CNT_SP2L_AREA19_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA19
0x7CC4	3	17:0	RO_IS_AEB_CNT_SP2L_AREA19_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA19
...		
0x7CFC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA19_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA19
0x7D00	3	17:0	RO_IS_AEB_CNT_SP2L_AREA20_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA20
0x7D04	3	17:0	RO_IS_AEB_CNT_SP2L_AREA20_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA20
...		
0x7D3C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA20_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA20
0x7D40	3	17:0	RO_IS_AEB_CNT_SP2L_AREA21_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA21
0x7D44	3	17:0	RO_IS_AEB_CNT_SP2L_AREA21_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA21
...		
0x7D7C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA21_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA21
0x7D80	3	17:0	RO_IS_AEB_CNT_SP2L_AREA22_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA22
0x7D84	3	17:0	RO_IS_AEB_CNT_SP2L_AREA22_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA22
...		
0x7DBC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA22_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA22
0x7DC0	3	17:0	RO_IS_AEB_CNT_SP2L_AREA23_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA23
0x7DC4	3	17:0	RO_IS_AEB_CNT_SP2L_AREA23_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN01 of AREA23
...		
0x7DFC	3	17:0	RO_IS_AEB_CNT_SP2L_AREA23_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA23
0x7E00	3	17:0	RO_IS_AEB_CNT_SP2L_AREA24_BIN00	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN00 of AREA24
0x7E04	3	17:0	RO_IS_AEB_CNT_SP2L_AREA24_BIN01	R	U18.0	This register indicates the histogram result of SP2_LCG.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
						BIN01 of AREA24
...		
0x7E3C	3	17:0	RO_IS_AEB_CNT_SP2L_AREA24_BIN15	R	U18.0	This register indicates the histogram result of SP2_LCG. BIN15 of AREA24

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6.10. OTP Function

6.10.1. Functional Purpose

The user can write any desired data to the OTP Areas.

6.10.2. Functional Overview

"Table 6-83," shows the structure of the sensor's OTP ROM.

The reserved region is where SSS stores its own data at the factory. Therefore, please do not overwrite each bit in this region with 1s.

Table 6-83 The Sensor's OTP Structure

Page	Row	Description
0 - 145	0 - 583	Reserved region
146 - 147	584 - 589	Region for the Safety Mechanism function Refer to the IMX623-AA** "Safety Application Note."
147	590	This register is used to configure the I ² C communication-related settings.
147	590 - 591	Reserved region
148 - 149	592 - 599	User Area
150 - 151	600 - 607	Reserved region

Read or write operations to the OTP ROM are performed in segments of 512 bits, referred to as "Pages." One Page consists of another unit of 128 bits, which is referred to as "Row." The OTP ROM consists of 152 Pages as illustrated in "**Figure 6-39.**" For example, Page 148, where the user area is present, consists of four Rows, ranging from Rows 592 to 595.

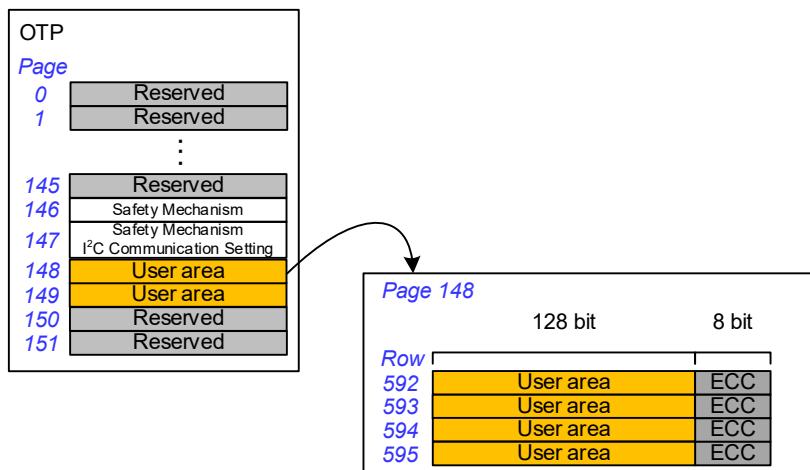


Figure 6-39 The OTP Structure

◇ Memo

- Each Row has an 8-bit ECC region that is used for error correction in addition to a 128-bit region that retains the values written to the OTP ROM.
- When writing to the OTP ROM, the sensor calculates an ECC for each Row and writes it to the OTP ROM together with the 128-bit region.
- The host cannot read or write data to 8-bit ECC regions.

6.10.3. Functional Specifications

6.10.3.1. OTP Writeable Area

"Table 6-84" shows an overview of Pages from 147 to 149, which are the part of the OTP ROM, where the host can write data.

The "OTP Interface Register" column lists the registers to be used for a write operation to the OTP ROM.

The "Register" column lists the registers which are set to the values stored on the OTP ROM. During the sensor's startup, the sensor reads out the data written to the OTP ROM and then transmits the data to the registers in the Register column.

◆ Note

If valid values are stored in both, the values in the Serial NOR Flash device have priority.

Table 6-84 An Overview of the Writable Area on the OTP ROM

- Page 147

Page	Row	OTP Interface Register	Register	Description
147	588	OTP_W_USERDATA0 to OTP_W_USERDATA7	-	Reserved User-set value: 0 • When using the sensor's safety mechanisms, refer to the IMX623-AA** "Safety Application Note."
	589	OTP_W_USERDATA8	-	Reserved User-set value: 0
	590	OTP_W_USERDATA9 [7:0]	OTP_I2C_SLAVE_ADDRESS_EN	Selection of a slave address 0: 0x1B

Page	Row	OTP Interface Register	Register	Description
				1: 0x1A
		OTP_W_USERDATA9 [15:8]	OTP_INCK_FREQ_LL	This register is used to set the master clock frequency in Hz and bits [7:0] of the frequency value. Available range for setting: 18 MHz to 30 MHz
		OTP_W_USERDATA9 [23:16]	OTP_INCK_FREQ_LH	This register is used to set the master clock frequency in Hz and bits [15:8] of the frequency value. Available range for setting: 18 MHz to 30 MHz
		OTP_W_USERDATA9 [31:24]	OTP_INCK_FREQ_HL	This register is used to set the master clock frequency in Hz and bits [23:16] of the frequency value. Available range for setting: 18 MHz to 30 MHz
		OTP_W_USERDATA10 [7:0]	OTP_INCK_FREQ_HH	This register is used to set the master clock frequency in Hz and bits [31:24] of the frequency value. Available range for setting: 18 MHz to 30 MHz
		OTP_W_USERDATA10 [31:8] to OTP_W_USERDATA11	-	Reserved User-set value: 0 • When using the sensor's safety mechanisms, refer to the IMX623-AA** "Safety Application Note."
591	591	OTP_W_USERDATA12 to OTP_W_USERDATA15	-	Reserved User-set value: 0

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Page	Row	OTP Interface Register	Register	Description
148	592	OTP_W_USERDATA0	OTP_COM_USER_00	User Area • The area where the host can write desired values.
		OTP_W_USERDATA1	OTP_COM_USER_01	
		OTP_W_USERDATA2	OTP_COM_USER_02	
		OTP_W_USERDATA3	OTP_COM_USER_03	
	593	OTP_W_USERDATA4	OTP_COM_USER_04	
		OTP_W_USERDATA5	OTP_COM_USER_05	
		OTP_W_USERDATA6	OTP_COM_USER_06	
		OTP_W_USERDATA7	OTP_COM_USER_07	
	594	OTP_W_USERDATA8	OTP_COM_USER_08	
		OTP_W_USERDATA9	OTP_COM_USER_09	
		OTP_W_USERDATA10	OTP_COM_USER_10	
		OTP_W_USERDATA11	OTP_COM_USER_11	
	595	OTP_W_USERDATA12	OTP_COM_USER_12	
		OTP_W_USERDATA13	OTP_COM_USER_13	
		OTP_W_USERDATA14	OTP_COM_USER_14	
		OTP_W_USERDATA15	OTP_COM_USER_15	

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Page	Row	OTP Interface Register	Register	Description
149	596	OTP_W_USERDATA0	OTP_COM_USER_16	User Area • The area where the host can write desired values.
		OTP_W_USERDATA1	OTP_COM_USER_17	
		OTP_W_USERDATA2	OTP_COM_USER_18	
		OTP_W_USERDATA3	OTP_COM_USER_19	

Page	Row	OTP Interface Register	Register	Description
	597	OTP_W_USERDATA4	OTP_COM_USER_20	
		OTP_W_USERDATA5	OTP_COM_USER_21	
		OTP_W_USERDATA6	OTP_COM_USER_22	
		OTP_W_USERDATA7	OTP_COM_USER_23	
	598	OTP_W_USERDATA8	OTP_COM_USER_24	
		OTP_W_USERDATA9	OTP_COM_USER_25	
		OTP_W_USERDATA10	OTP_COM_USER_26	
		OTP_W_USERDATA11	OTP_COM_USER_27	
	599	OTP_W_USERDATA12	OTP_COM_USER_28	
		OTP_W_USERDATA13	OTP_COM_USER_29	
		OTP_W_USERDATA14	OTP_COM_USER_30	
		OTP_W_USERDATA15	OTP_COM_USER_31	

◇ **Memo**

When no data has been written to the User Area, the sensor reads out 0 from the OTP_COM_USER_x (x = 0 to 31) registers.

6.10.3.2. The Method for Writing a Value to the OTP ROM

Writes a value to the OTP ROM using the OTP_W_USERDATAx (x = 0 to 15) registers. For details regarding how to write data to the OTP ROM, see “[Figure 6-40](#).”

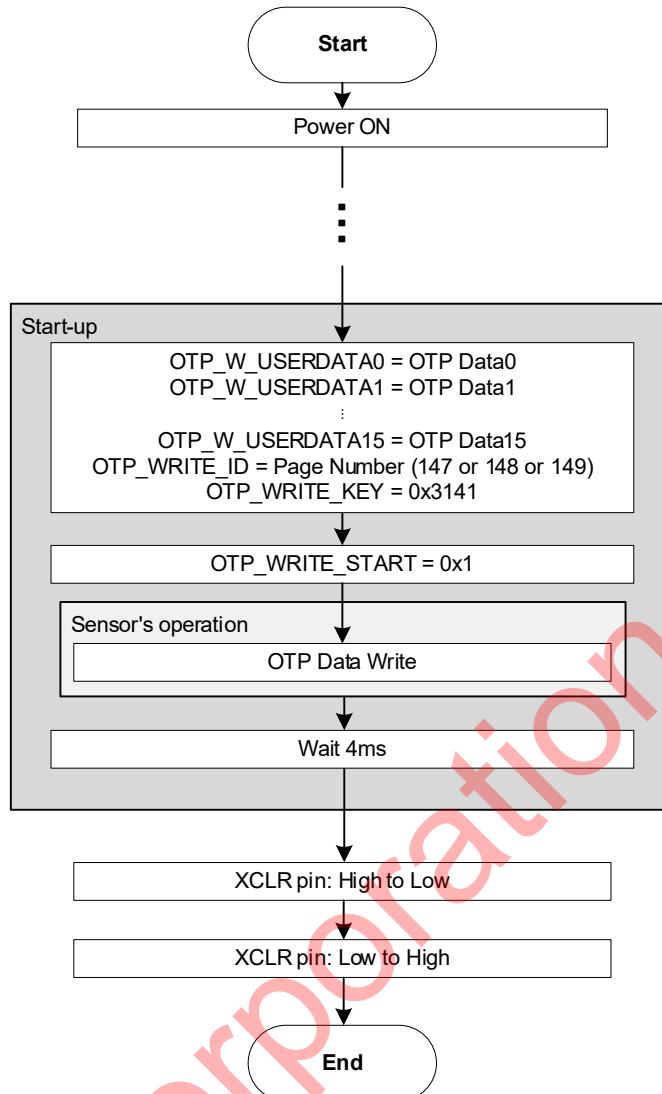


Figure 6-40 OTP Write Flow

◆ Note

- Be sure to write to the OTP ROM while the sensor is in Start-up State.
- When writing to the OTP ROM, ensure that the value to be written is correct before setting the OTP_WRITE_START register to 1.
- Upon completion of writing to the OTP ROM, be sure to reset the sensor.

◆ Memo

When loading data stored on the OTP ROM, load the data while the sensor is in Initial1 State. For this reason, the value of each register cannot be updated by just writing to the OTP ROM. To update these registers with the written data, drive the XCLR pin low and reset the sensor.

6.10.4. Conditions

■ Writing to the OTP ROM

The OTP ROM can be written only once. Rewriting any value to an already-written area, the value of that area will become indeterminate.

6.10.5. Interface

6.10.5.1. Input Registers

Table 6-85 Input Registers for the OTP Function

[CMD_TRG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8A10	1	0	OTP_WRITE_START	W	U1.0	<p>This register is used to start an OTP write operation.</p> <p>1. Beginning of an OTP write operation</p> <ul style="list-style-type: none"> • Be sure to set the OTP_WRITE_KEY register to the "key" before beginning a write operation. • If the OTP_WRITE_KEY register is invalid, the sensor does not begin a write operation to the OTP area.

[OTP_WRITE]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xD8AC	1	7:0	OTP_WRITE_ID	R/W	U8.0	This register is used to set the OTP Page number for a write operation. Available range: 147 (0x93) to 149 (0x95)
0xD8AE	2	15:0	OTP_WRITE_KEY	R/W	U16.0	The OTP write key. Setting this register to the valid value (0x3141) and then setting the OTP_WRITE_START register to 1 initiate writing to the OTP ROM.
0xD8BC	4	31:0	OTP_W_USERDATA0	R/W	U32.0	The data 0 to be written to the OTP ROM
0xD8C0	4	31:0	OTP_W_USERDATA1	R/W	U32.0	The data 1 to be written to the OTP ROM
...	
0xD8F8	4	31:0	OTP_W_USERDATA15	R/W	U32.0	The data 15 to be written to the OTP ROM

6.10.5.2. Output Register

Table 6-86 Output Registers for the OTP Function

[OTP_COM]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x8200	4	31:0	OTP_COM_USER_00	R	U32.0	Data #00 in the OTP user area
0x8204	4	31:0	OTP_COM_USER_01	R	U32.0	Data #01 in the OTP user area
...		
0x827C	4	31:0	OTP_COM_USER_31	R	U32.0	Data #31 in the OTP user area

Chapter 7 Test Function

This chapter describes functions used for testing in the development stage and manufacturing process.

Table 7-1 List of Test Functions

Function Name	Applications
PG Image Output Function	Produces output of test patterns from the sensor
Light Metering Window Overlay Function	Overlays the light metering window and light metering masking region(s) to be used by the sensor.

7.1. PG Image Output Function

7.1.1. Functional Purpose

The sensor transmits pattern generator images (PG images) to the host, enabling the user to confirm the sensor's image processing without preparing any subjects such as color charts or gray scale charts.

7.1.2. Functional Overview

The PG Image Output function is positioned in the Output I/F block as illustrated in “**Figure 1-2**.” Therefore, the sensor is not affected by any functions which are in the preceding stages of the PG Image Output function. Please note that any functions which are performed after PG Image Output function affect the output of the PG image.

As illustrated in “**Figure 7-1**,” the PG Image Output function outputs the horizontal ramp image.

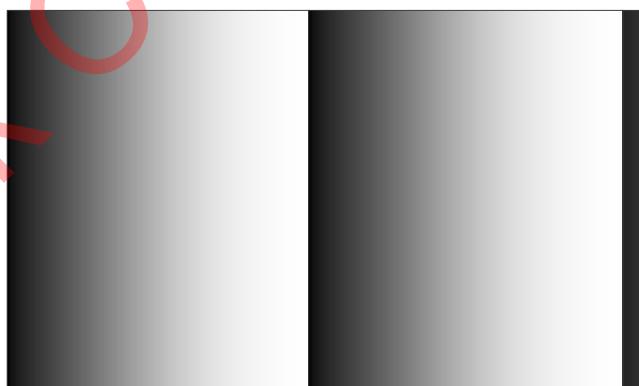


Figure 7-1 Horizontal Ramp Image

7.1.3. Functional Specifications

7.1.3.1. Enabling or Disabling the PG Image Output Function

To enable or disable the PG Image Output function, set the DIF_PG_EN register to 1 or 0 respectively. The DIF_PG_EN register is compatible with the Application Lock Safety Mechanism. For details, refer to “[3.1.5 Application Lock Function](#).”

7.1.3.2. Configuring Output Settings of the Horizontal Ramp Image

Regarding the output of the horizontal ramp image produced by the PG Image Output function, the host can set without any restrictions the pixel level at the left edge of the output image and the amount of pixel level increment for each pixel.

“[Figure 7-2](#)” illustrates an example of the Horizontal Ramp Image.

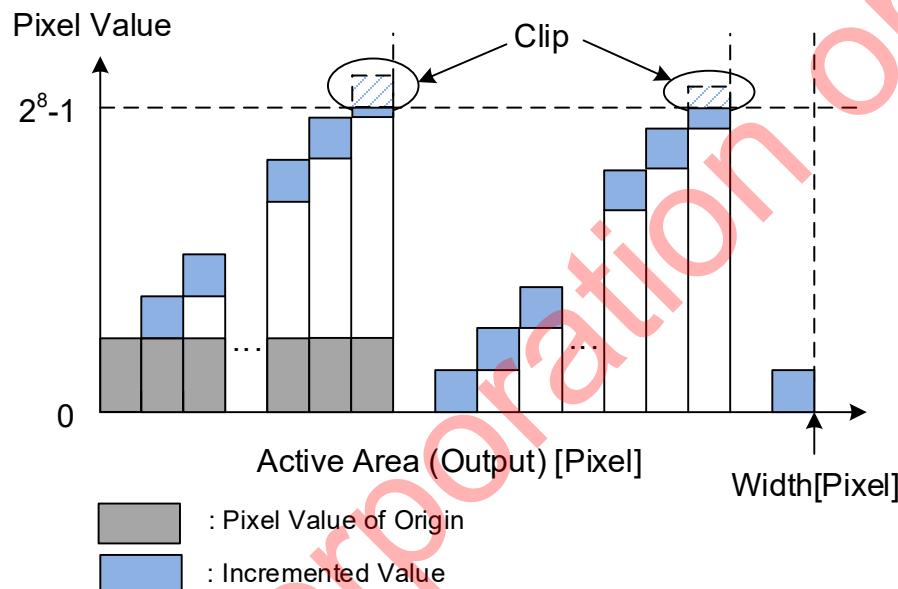


Figure 7-2 Example of the Pixel Value Output of the Horizontal Ramp Image

■ Clipping

As a result of incrementing the pixel level, if the pixel level exceeds the maximum bit precision that has been set in the IR_DR_I2I_PG_PIX_BW_x (x = S0, S1, S2, S3) registers, the level is clipped to the maximum value. The next pixel level reverts to 0 and the sensor resumes incrementing the level. Set the IR_DR_I2I_PG_PIX_BW_x (x = S0, S1, S2, S3) registers to the value corresponding to the RAW output format.

■ Setting the pixel level at the left edge of the output image

The pixel level at the left edge of the output image can be calculated from the following base value and an amount of shift for the base value:

- IR_DR_I2I_PG_RAMP_STA_VAL register (Base value)
- IR_DR_I2I_PG_RAMP_STA_SHIFT register (Amount of shift for the base value)

The sensor performs bit shifting to the MSB side by the number of bits specified by the IR_DR_I2I_PG_RAMP_STA_SHIFT registers in relation to the base value. The resultant value is the pixel level at the left edge.

■ Setting the amount of incremented pixel level

In the same way as "the pixel level at the left edge of the output image," the amount of incremented pixel level is calculated from the following base value and an amount of shift for the base value:

- IR_DR_I2I_PG_RAMP_HSTEP_VAL register (Base value)
- IR_DR_I2I_PG_RAMP_HSTEP_SHIFT register (Amount of shift for the base value)

◆ **Note**

The host can select the amount of bit shifting from 0, 1, 2, 3, 4, 6, 8, or 12 by using the IR_DR_I2I_PG_RAMP_x_SHIFT (x = STA, HSTEP) registers. As shown in "**Table 7-2**," a register's value does not necessarily match the amount of bit shifting.

Table 7-2 The Relationship Between the Register Values and the Amount of Bit Shifting

IR_DR_I2I_PG_RAMP_x_SHIFT (x = STA, HSTEP)	Amount of Bit Shifting
0	No bit shift
1	A 1-bit shift
2	A 2-bit shift
3	A 3-bit shift
4	A 4-bit shift
5	A 6-bit shift
6	An 8-bit shift
7	A 12-bit shift

7.1.4. Conditions

Set the IR_DR_I2I_PG_RAMP_HSTEP_VAL register to any value other than 0. (The base value for the amount of incremented value.)

7.1.5. Interface

7.1.5.1. Input Registers

Table 7-3 Input Registers for the PG Image Output Function

[VIF]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBE14	1	0	DIF_PG_EN_	R/W	U1.0	This register is used to enable or disable the output of the PG image. 0: PG image output disabled 1: PG image output enabled

[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBF60	1	0	DIF_PG_EN_APL	R/W	U1.0	This register is used to be compared with the DIF_PG_EN_ register for the Application Lock function.

[CTRL1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1AC4	1	2:0	IR_DR_I2I_PG_PIX_BW_S0	R/W	U3.0	This register is used to set the maximum bit precision for the 1st line for the PG Image Output function. 0: 8 bits 1: 10 bits 2: 12 bits 3: 14 bits 4: 16 bits 5: 20 bits 6: 24 bits 7: Setting prohibited
0x1AC5	1	1:0	IR_DR_I2I_PG_PIX_BW_S1	R/W	U2.0	This register is used to set the maximum bit precision for the 2nd line for the PG Image Output function. 0: 8 bits 1: 10 bits 2: 12 bits 3: 14 bits
0x1AC6	1	1:0	IR_DR_I2I_PG_PIX_BW_S2	R/W	U2.0	This register is used to set the maximum bit precision for the 3rd line for the PG Image Output function. 0: 8 bits 1: 10 bits 2: 12 bits 3: 14 bits
0x1AC7	1	1:0	IR_DR_I2I_PG_PIX_BW_S3	R/W	U2.0	This register is used to set the maximum bit precision for the 4th line for the PG Image Output function. 0: 8 bits 1: 10 bits 2: 12 bits 3: 14 bits
0x1AC8	2	11:0	IR_DR_I2I_PG_RAMP_STA_VAL	R/W	U12.0	This register is used to set the base value for the pixel level (Y) at the left edge of the output image in the case of PG image output.

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1ACC	1	2:0	IR_DR_I2I_PG_RAMP_S TA_SHIFT	R/W	U3.0	This register is used to set the amount of shift for the base value for the pixel level at the left edge of the output image in the case of PG image output. 0: No bit shift 1: A 1-bit shift 2: A 2-bit shift 3: A 3-bit shift 4: A 4-bit shift 5: A 6-bit shift 6: An 8-bit shift 7: A 12-bit shift
0x1ACE	2	11:0	IR_DR_I2I_PG_RAMP_H STEP_VAL	R/W	U12.0	This register is used to set the base value of the incremental pixel level in PG image output.
0x1AD0	1	2:0	IR_DR_I2I_PG_RAMP_H STEP_SHIFT	R/W	U3.0	This register is used to set the amount of shift in relation to the base value of the incremental pixel level in PG image output. 0: No bit shift 1: A 1-bit shift 2: A 2-bit shift 3: A 3-bit shift 4: A 4-bit shift 5: A 6-bit shift 6: An 8-bit shift 7: A 12-bit shift

7.2. Light Metering Window Overlay Function

7.2.1. Functional Purpose

Overlaying the light metering window on the captured image enables the user to visually adjust the metering window and masking area.

7.2.2. Functional Overview

As an auxiliary function for image quality adjustments, this function can overlay the light metering window, which is set by the Exposure Control and White Balance functions, and masking for the light metering window and then can output the resultant image. "Figure 7-3" illustrates an image output by this function.

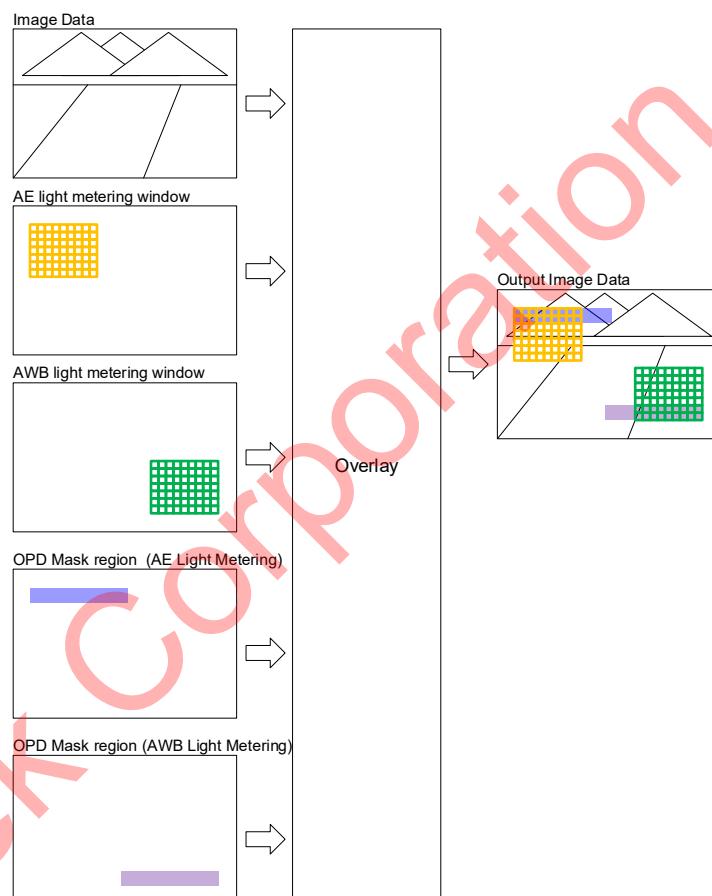


Figure 7-3 Example of an Overlaid Light Metering Window

◇ **Memo**

Set the light metering window and light metering region mask for overlaying, corresponding to the settings of each function. To change the light metering window settings, refer to "**5.2 Exposure Control Function**" and "**5.3 White Balance Function**".

7.2.3. Functional Specifications

7.2.3.1. Enabling or disabling the Light Metering Window Overlay Function

The Light Metering Window Overlay function is implemented as an auxiliary function to visually adjust the image quality. To enable or disable this function, set the OPO_BYPASS_ register to 0 or 1, respectively. The OPO_BYPASS_ register is compatible with the Application Lock function. For details, refer to “[3.1.5 Application Lock Function](#).”

◆ Note

Since this function is a test function, do not use it for any purposes other than adjusting the light metering window.

7.2.3.2. Setting the Light Metering Window Overlay Function

When the sensor overlays the light metering window and the light metering region mask on an image captured by the sensor, the host can display or hide the light metering window or add a color to it for easier identification. “[Table 7-4](#)” shows the registers for displaying the light metering window.

Table 7-4 Registers Used to Set the Light Metering Window Overlay Function

Register				Description
Display	Color	Transmittance	Display Width	
OPO_AE_WIN_DISP_ON	IR_YC_OPO_AE_WIN_DISP_COLOR	-	IR_YC_OPO_AE_WIN_DISP_LINEWIDTH	This register is used to enable or disable the overlay of the light metering window to be used for AE.
AWB_OPD_WIN_DISP_ON	IR_YC_OPO_AWB_WIN_DISP_COLOR	-	IR_YC_OPO_AWB_WIN_DISP_LINEWIDTH	This register is used to enable or disable the overlay of the light metering window to be used for AWB.
OPO_AE_SQMSK_DISP_ON	IR_YC_OPO_AE_SQMSK_DISP_COLOR	IR_YC_OPO_AE_SQMSK_DISP_BLEND	-	This register is used to enable or disable the overlay settings of rectangular masking for AE.
AWB_OPD_SQMSK_DISP_ON	IR_YC_OPO_AWB_SQMSK_DISP_COOLOR	IR_YC_OPO_AWB_SQMSK_DISP_BLEND	-	This register is used to set a rectangular mask to be used for AWB.
OPO_ELMSK_DISP_ON	IR_YC_OPO_ELMSK_DISP_COLOR	IR_YC_OPO_ELMSK_DISP_BLEND	-	This register is used to enable or disable the overlay settings of elliptical masking for AE and AWB.

- The user can select the color for the overlaid metering window from black (0), blue (1), green (2), cyan (3), red (4), magenta (5), yellow (6) and white (7).
- Regarding the light metering region mask, setting the transmittance from 0.0 (100% transmittance) to 1.0 (0% transmittance) enables the user to adjust the position while

- checking the mask target.
- The width of the light metering window can be selected from four types: 4, 8, 16 and 32 pixels.
- The light metering region mask is overlaid under the metering window.

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7.2.4. Interface

7.2.4.1. Input Registers

Table 7-5 Input Registers for the Light Metering Window Overlay Function

[CTRL1]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1CD0	1	3:0	IR_YC_OPO_ELMSK_DISP_BLEND	R/W	U1.3	This register is used to set the transmittance for AE and AWB in the case of elliptical masking. 0.0: 100% to 1.0: 0%
0x1CD1	1	2:0	IR_YC_OPO_ELMSK_DISP_COLOR	R/W	U3.0	This register is used to set the color for the elliptical mask to be overlaid for AE and AWB. 0: Black 1: Blue 2: Green 3: Cyan 4: Red 5: Magenta 6: Yellow 7: White
0x1CD2	1	3:0	IR_YC_OPO_AE_SQMSK_DISP_BLEND	R/W	U1.3	This register is used to set the transmittance for a rectangular mask to be used for AE. 0.0: 100% to 1.0: 0%
0x1CD3	1	2:0	IR_YC_OPO_AE_SQMSK_DISP_COLOR	R/W	U3.0	This register is used to set the color for a rectangular mask to be used for AE. 0: Black 1: Blue 2: Green 3: Cyan 4: Red 5: Magenta 6: Yellow 7: White
0x1CD4	1	3:0	IR_YC_OPO_AWB_SQMSK_DISP_BLEND	R/W	U1.3	This register is used to set the transmittance for a rectangular mask to be used for AWB. 0.0: 100% to 1.0: 0%
0x1CD5	1	2:0	IR_YC_OPO_AWB_SQMSK_DISP_COLOR	R/W	U3.0	This register is used to set the color for a rectangular mask to be used for AWB. 0: Black 1: Blue 2: Green 3: Cyan 4: Red 5: Magenta 6: Yellow 7: White
0x1CD6	1	2:0	IR_YC_OPO_AE_WIN_DISP_COLOR	R/W	U3.0	This register is used to set the color for the light metering window for AE. 0: Black 1: Blue 2: Green 3: Cyan 4: Red 5: Magenta 6: Yellow 7: White

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0x1CD7	1	1:0	IR_YC_OPO_AE_WIN_DISP_LINEWIDTH	R/W	U2.0	This register is used to set the display width of the light metering window for AE. 0: 4 pixels 1: 8 pixels 2: 16 pixels 3: 32 pixels
0x1CD8	1	2:0	IR_YC_OPO_AWB_WIN_DISP_COLOR	R/W	U3.0	This register is used to set the color for the light metering window for AWB. 0: Black 1: Blue 2: Green 3: Cyan 4: Red 5: Magenta 6: Yellow 7: White
0x1CD9	1	1:0	IR_YC_OPO_AWB_WIN_DISP_LINEWIDTH	R/W	U2.0	This register is used to set the display width of the light metering window for AWB. 0: 4 pixels 1: 8 pixels 2: 16 pixels 3: 32 pixels

[AE_OPD]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xAE33	1	0	OPO_BYPASS_	R/W	U1.0	This register is used to enable or disable the Light Metering Window Overlay function 0: Enabled 1: Disabled
0xAE34	1	0	OPO_ELMASK_DISP_ON	R/W	U1.0	This register is used to enable or disable the overlay settings of elliptical masking for AE and AWB. 0: Overlay disabled 1: Overlay enabled
0xAE35	1	0	OPO_AE_SQMSK_DISP_ON	R/W	U1.0	This register is used to enable or disable the overlay settings of rectangular masking for AE. 0: Overlay disabled 1: Overlay enabled
0xAE36	1	0	OPO_AE_WIN_DISP_ON	R/W	U1.0	This register is used to enable or disable the overlay of the light metering window to be used for AE. 0: Overlay disabled 1: Overlay enabled

[AWB_OPD]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xB28F	1	0	AWB_OPD_SQMSK_DISP_ON	R/W	U1.0	This register is used to set a rectangular mask to be used for AWB. 0: Overlay disabled 1: Overlay enabled
0xB290	1	0	AWB_OPD_WIN_DISP_ON	R/W	U1.0	This register is used to enable or disable the overlay of the light metering window to be used for AWB. 0: Overlay disabled 1: Overlay enabled

[SM_CFG]

Address	Register Unit	Bit	Register Name	R/W	Unit	Description
0xBF29	1	0	OPO_BYPASS_APL	R/W	U1.0	This register is used to be compared with the OPO_BYPASS_ register for the Application Lock function.

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