## Description of the 7-stage MIPS pipeline in Problem 3

In the 7-stage pipeline described below, the program counter (PC) stores the *virtual* address of the instruction currently in the IT stage. The pipeline implements *full forwarding*. The details for each stage are described below:

**Stage 1: IT** The Instruction Translate (IT) stage uses the TLB to translate the (virtual) PC address into a physical instruction address. We can occasionally have a TLB miss, but you can safely ignore this possibility for this problem.

**Stage 2: IF** The Instruction Fetch (IF) stage uses the physical instruction address computed in the IT stage to access the cache, and fetches the 32-bit instruction stored at that address. You can safely ignore the possibility of a cache miss.

**Stage 3: ID** The Instruction Decode (ID) stage first decodes the 32-bit instruction (e.g., identifying the opcode field, the rs, rt, and rd fields, etc.). In the second half of the clock cycle, it reads the register file. It also computes the (virtual) *target address*, if the instruction is a jump (`j`) or a branch (`beq/bne`).

**Stage 4: EX** The Execute (EX) stage does the necessary ALU operations for the instruction. For branches, this includes resolving the branch *decision* (taken or not-taken). For `lw/sw` instructions, the ALU computes the (virtual) data address from/to which data is to be read/written.

**Stage 5: MT** The Memory Translate (MT) stage translates the virtual data address into a physical data address using the TLB, if the instruction is a `lw` or `sw`. As in the IT stage, you can safely ignore the possibility of a TLB miss.

**Stage 6: MM** The Memory (MM) stage uses the physical data address computed in the MT stage to access the cache if the instruction is a `lw` (data is read from the cache into the rt register) or a `sw` (data in the rt register is written to the cache). You can safely ignore the possibility of a cache miss.

**Stage 7: WB** The Write Back (WB) stage updates the register file (if necessary) in the first half of the clock cycle.