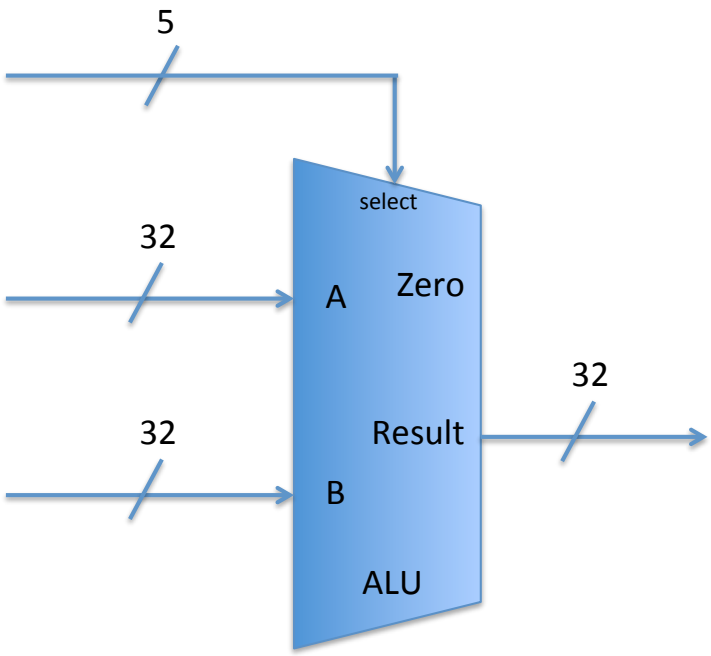
The ALU

In the first project the Register File was designed (which will require a little modification later. In this project we are going to design the ALU for our MIPS processor. The architecture of the design is as follows:



There are two operands to the ALU. They will be connected to the Read Data ports of the register file (with some more logic later). The select will come from the ALU control logic which will direct the ALU which operation to perform.

The instructions you are to include are itemized below (with an “X” in the ALU column).

You should also create a test bench to verify that the ALU behaves as expected. Please note that there are no clocks in this circuit, it is strictly a combinational array.