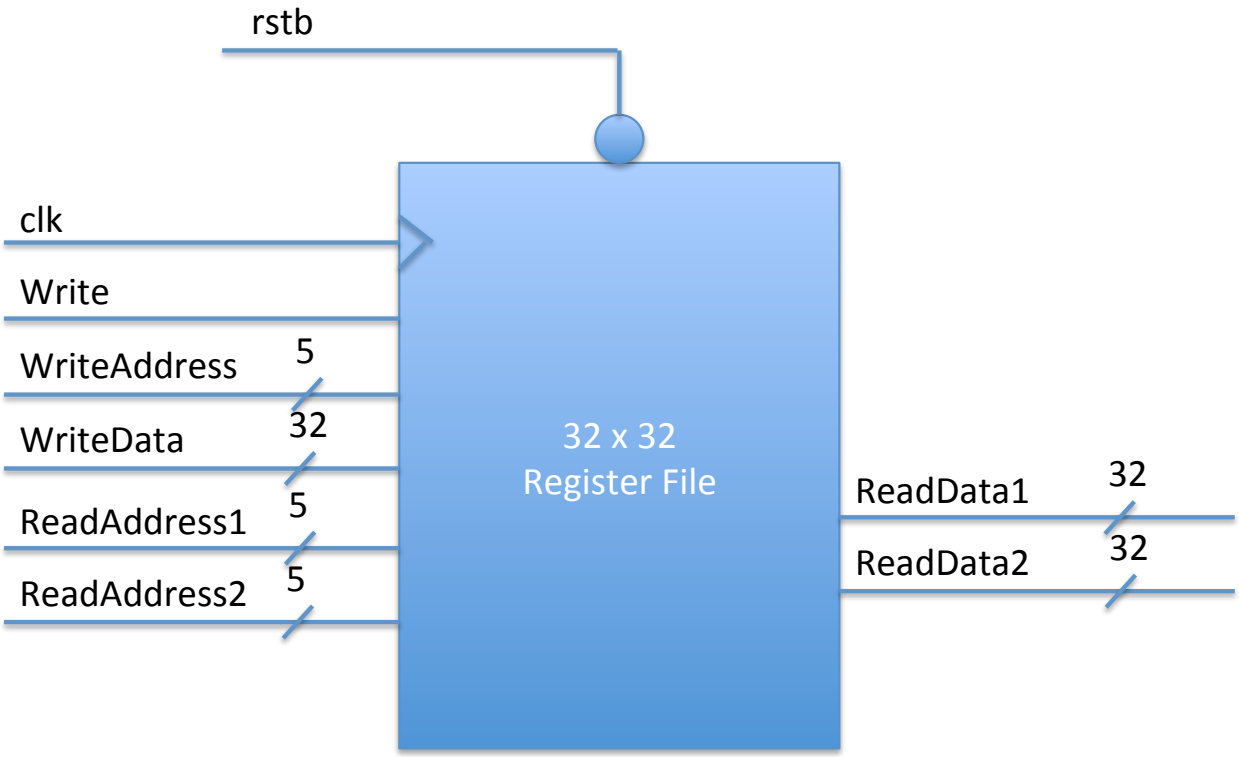
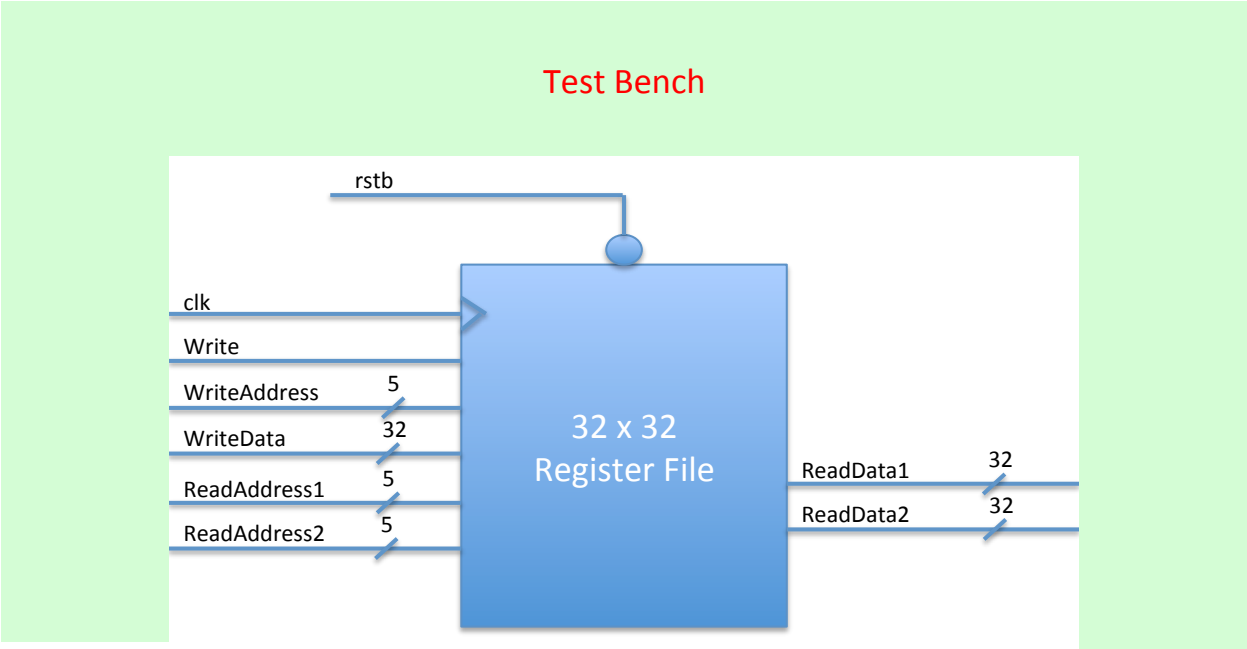
This project will serve to set the standard for project development this semester. Please perform the project and document according to this description.

DESCRIPTION

Using the techniques taught in class regarding HDL design create a register file that has 32 registers 32-bits wide (32 x 32). The register file will have a synchronous write port and two asynchronous read ports. On the active edge of the clock, if write=1, then the 16 bits on WriteData will be written into the register referenced by WriteAddress. REG[WriteAddress] <— WriteData. The contents of the register referenced by each ReadAddress will immediately be presented on the read data port. ReadData <— REG[ReadAddress].

BLOCK DIAGRAM





VERIFICATION

1. Create the design using the Verilog style taught in class
2. Organize your code so that it is intuitive with respect to its functionality
3. Add a header at the beginning to document the design - name, data, purpose
4. Create a test bench using the same module name with "_tb"
5. Verify the design using simulation
6. Write a report describing the assignment and your work
7. Include a description of the verification
8. Include your source code with the report
9. Demonstrate to instructor
10. Hand in report and upload it to BeachBoard dropbox