CECS 440 Spring 2015 Project 4 - Single Cycle MIPS with Sorting Code

This project takes the design of the single cycle MIPS processor and generates executable code (machine) to implement the algorithm. The instruction will supply the control.v file and the data file to be loaded into the data memory at the beginning of the program.

The program will be loaded into the 1024 x 32 data memory starting at address 0x200 and will fill the memory through address 0x3FF. To clarify these addresses are memory addresses, the MIPS address range will be 0x800 through 0xFFC.

Program Tasks

1. Add the 32 largest values and place the sum in data memory address (0x100 [memory] 0x400 [MIPS]).

2. Add the 32 smallest values and place the sum in data memory address (0x101 [memory] 0x404 [MIPS]).

3. AND every location together (entire table) and place the result in data memory address (0x102 [memory] 0x408 [MIPS]).

4. OR every location together (entire table) and place the result in data memory address (0x103 [memory] 0x40C [MIPS]).

5. ADD every location together (entire table) and place the result in data memory address (0x104 [memory] 0x410 [MIPS]).

Details

1. The addition performed for numbers 1 & 2 should be signed.

2. The addition performed for number 5 should be unsigned.

3. The 'seed' (start value) for ANDING should be 0xFFFFFFFF. i.e. The first location read should be ANDED with 0xFFFFFFFF and then every other is ANDED with the cumulative result.

4. The 'seed' (start value) for ORING should be 0x00000000. i.e. The first location read should be ORED with 0x00000000and then every other is ORED with the cumulative result.

Comments

This is not the easiest of assignments. It requires great attention to details. Use of the supplied Excel spreadsheet for creating the code should prove invaluable. It is highly recommended to break the problem up into discrete functions and combine the results once verified.

Due Date: Project Due on April 7