CECS 460

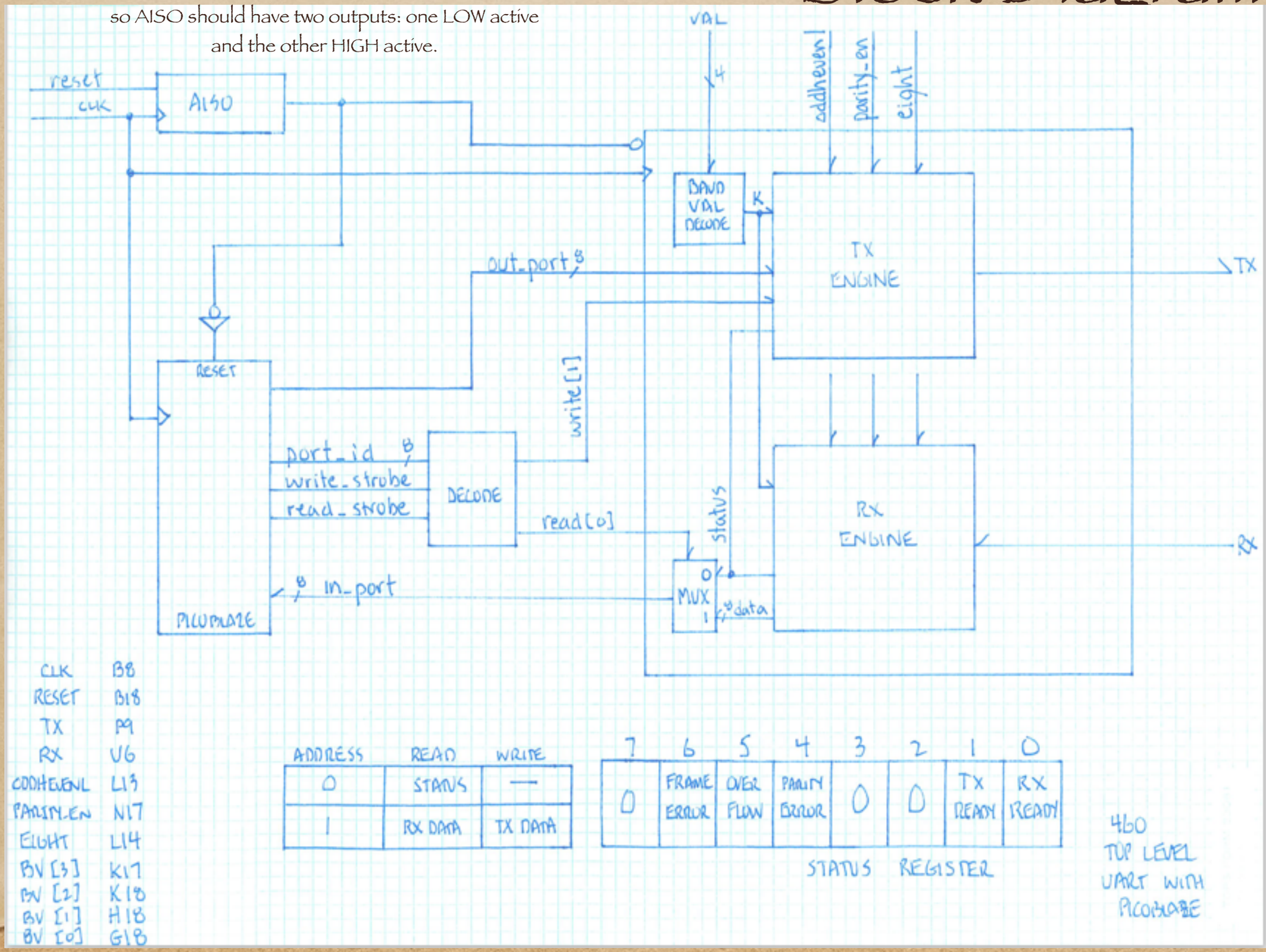
Project 3

Transmit Engine

plus Picoblaze

Block Diagram

Remember AISO has a HIGH active reset
on the input and a LOW active reset on output.
Also remember the Picoblaze has a HIGH active reset -
so AISO should have two outputs: one LOW active
and the other HIGH active.



CLK	B8
RESET	B18
TX	P9
RX	U6
CODHEVENL	L13
PARITY_EN	N17
EIGHT	L14
BV [3]	K17
BV [2]	K18
BV [1]	H18
BV [0]	G18

ADDRESS	READ	WRITE
0	STATUS	—
1	RX DATA	TX DATA

7	6	5	4	3	2	1	0
0	FRAME ERROR	OVER FLOW	PARITY ERROR	0	0	TX READY	RX READY

STATUS REGISTER

460
TOP LEVEL
UART WITH
PICOBLAZE

Block Diagram Discussion

- This is meant to convey the TRANSMIT function but by looking ahead we can save ourselves time when we construct our design
- Please use recommended pinouts (Nexys2), for Nexys3 please choose the equivalent pins

Project Discussion

- Make sure you simulate your design before you program your board. This allows you to see how the inward parts of your design are operating - you might be surprised
- The software to be written is simple, monitor the TXRDY bit in the status register (see below)
- When you see the TXRDY bit you should continuously transmit the sequence "CSULB CECS 460 <CR><LF>"

Deliverables

- Due October 20
- Complete the documentation using the recommended style from the chip specification presentation
- Please include: Technical discussion, source code (leave out the detailed Picoblaze files), the psm and ucf files
- Please upload to Dropbox
- Please demonstrate to instructor with hard copy of deliverables