# Project Two
# UART Transmit Block

CSULB

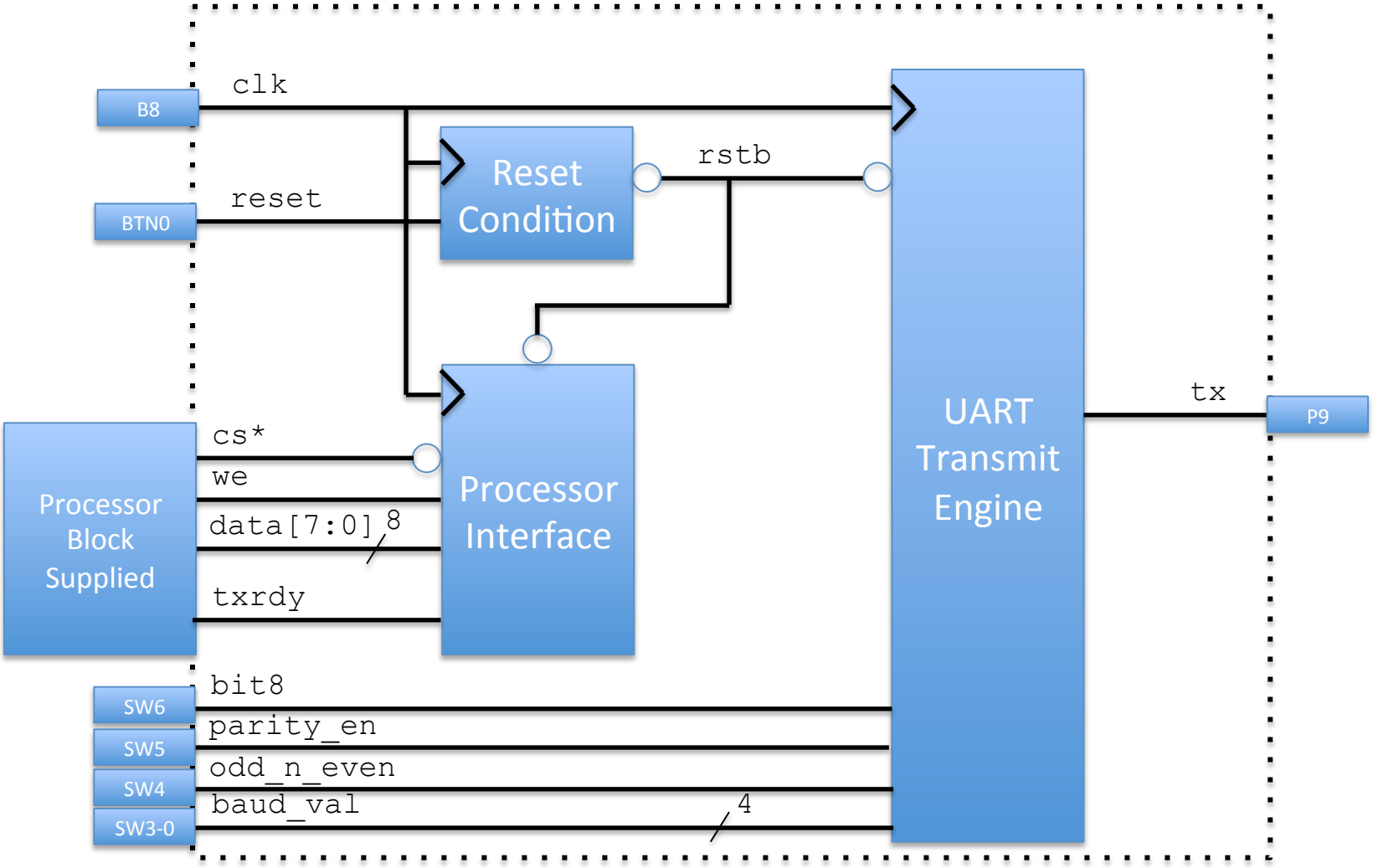
CECS460

Due October 4, 2012

# Explanation

- This presentation is meant to be combined with the discussion given in class regarding the operation of the UART transmit block
- Notice that there will be a block supplied by the instructor for the processor interface that you will include in your design (both simulation and implementation)

# Top Level Diagram



# Pinout Explanation

- (I) bit8 (1: 8 bits, 0: 7 bits)
- (I) parity_en (1: parity enabled, 0: no parity)
- (I) odd_n_even: (1: odd parity, 0: even parity)
- (I) baud_val: (see table next page)
- (I) cs*: Low active chip select
- (I) we: High active write enable
- (O) txrdy: High active signal telling processor that it may write another byte
- (I) data[7:0]: data from processor to be transmitted
- Some I/O identified by device on Nexsys2 and others identified by pinout on FPGA

# BAUD Rate Definition

| baud[3:0] | BAUD Rate | Bit Time | Engineering Notation |
|---|---|---|---|
| 0000 | 300 | 3.3333E-03 | 3.3333 ms |
| 0001 | 1200 | 8.3333E-04 | 833.33 us |
| 0010 | 2400 | 4.1667E-04 | 416.66 us |
| 0011 | 4800 | 2.0833E-04 | 208.33 us |
| 0100 | 9600 | 1.0417E-04 | 104.16 us |
| 0101 | 19200 | 5.2083E-05 | 52.083 us |
| 0110 | 38400 | 2.6042E-05 | 26.041 us |
| 0111 | 57600 | 1.7361E-05 | 17.361 us |
| 1000 | 115200 | 8.6806E-06 | 8.6806 us |
| 1001 | 230400 | 4.3403E-06 | 4.3403 us |
| 1010 | 460800 | 2.1701E-06 | 2.1701 us |
| 1011 | 921600 | 1.0851E-06 | 1.0851 us |

# Processor Interface Emulation of Pico Blaze

cs* will be formed by combining the PORT_ID (ADDRESS) with the WRITE_STROBE. What you need to keep in mind is that the WRITE_STROBE is only active for one clock.

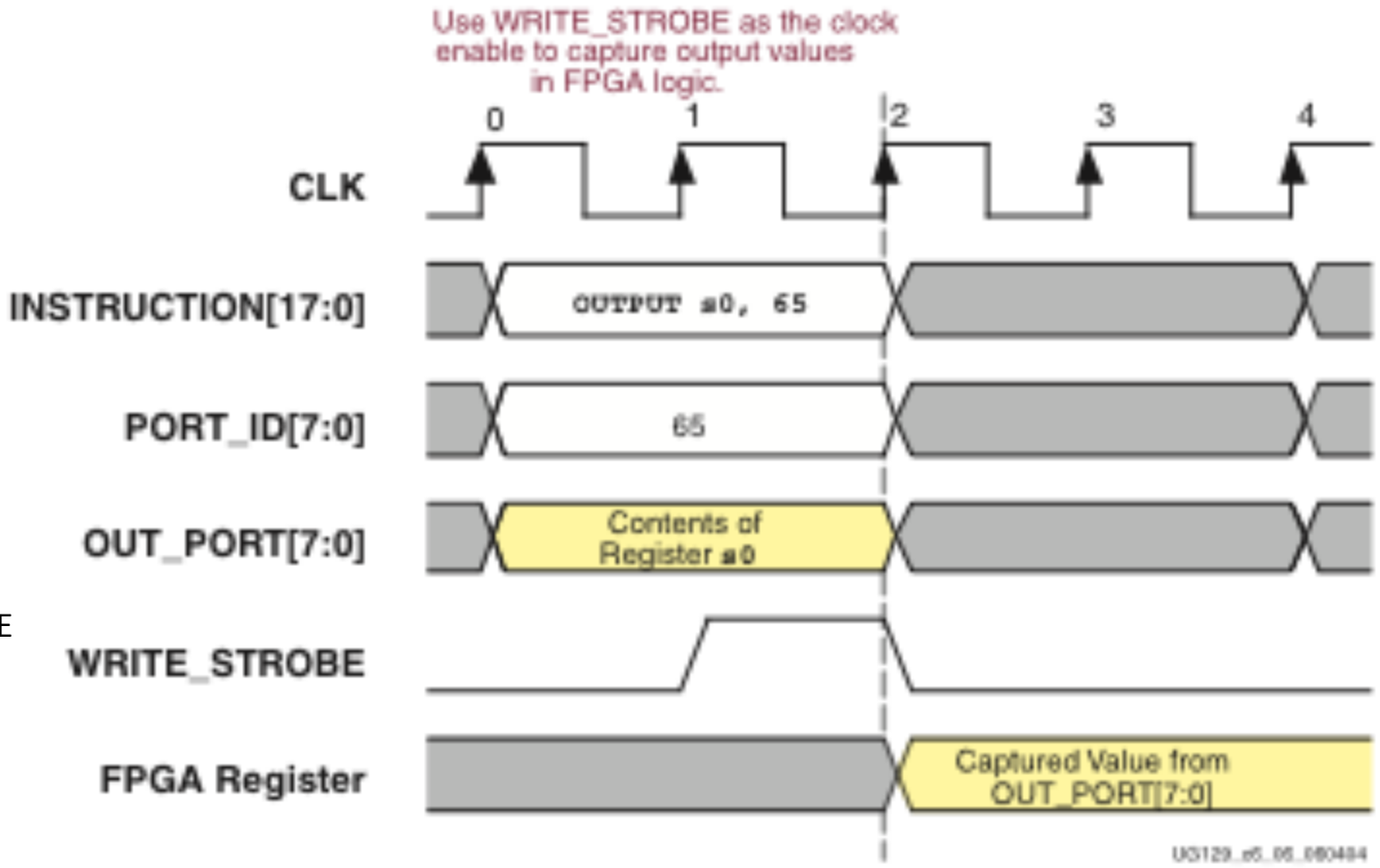



*Figure 6-6:* **Port Timing for OUTPUT Instruction**