

KCU116 GTY IBERT Design Creation

May 2019



Revision History

Date	Version	Description
05/29/19	8.0	Updated for 2019.1. Some screenshots not updated.
12/10/18	7.0	Updated for 2018.3. Some screenshots not updated.
06/18/18	6.0	Updated for 2018.2.
04/09/18	5.0	Updated for 2018.1.
12/20/17	4.0	Updated for 2017.4.
10/26/17	3.0	Updated for 2017.3.1.
06/20/17	2.0	Updated for 2017.2.
04/19/17	1.0	Initial version.

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KCU116 IBERT Overview

- > Xilinx KCU116 Board
- > KCU116 Software Install and Board Setup
- > Setup for the KCU116 IBERT Design
- > IBERT Testing
 - » FMC (Bank 227)
 - » zSFP (Bank 226)
 - » PCIe (Bank 224 & 225)
- > Create IBERT Design for All Banks
 - » Testing All Banks with Optional User Provided Hardware
- > References

KCU116 IBERT Overview

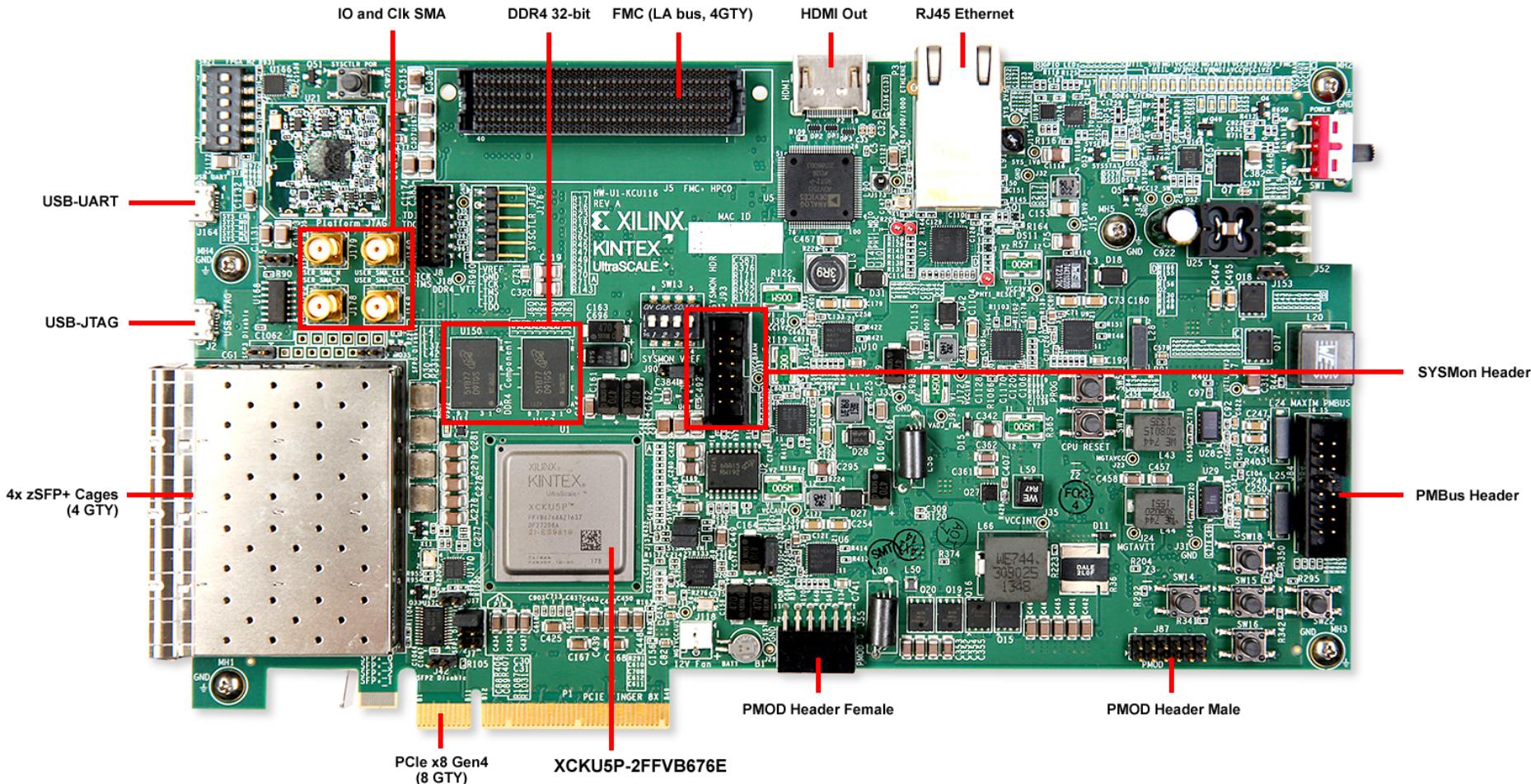
> Description

- » The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the UltraScale Kintex GTY transceivers. A graphical user interface is provided through the Vivado Hardware Manager.

> Reference Design IP

- » LogiCORE UltraScale IBERT GTY Example Designs

Xilinx KCU116 Board



Note: Presentation applies to the KCU116

KCU116 Software Install and Board Setup

- > Refer to XTP464 – KCU116 Software Install and Board Setup for details on:
 - » Software Requirements
 - » KCU116 Board Setup
 - » Clock Setup
 - » Optional Hardware Setup



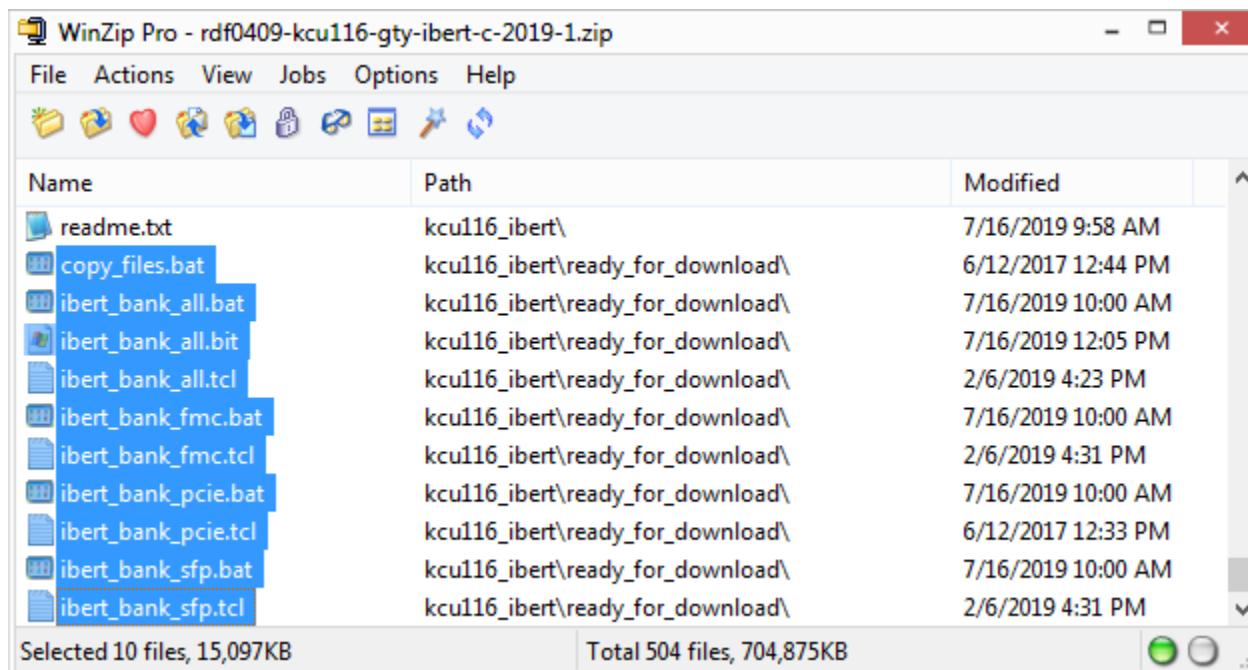
Note: The Clock Setup is required for this tutorial

Setup for the KCU116 IBERT Design



Setup for the KCU116 IBERT Design

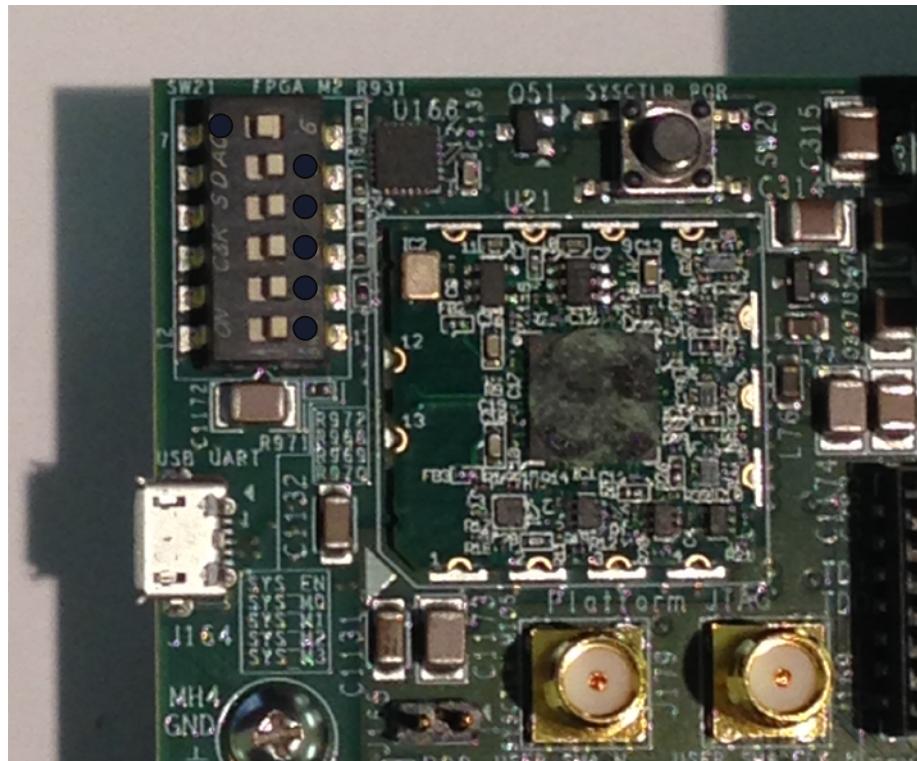
- > Open the RDF0409 - KCU116 GTY IBERT Design Files (2019.1 C) ZIP file, and extract these files to your C:\ drive:
 - » kcu116_ibert\ready_for_download*



Setup for the KCU116 IBERT Design

- > Set S21 to 000001 (1 = on, Position 1 → Position 6)

» This disables Master SPI configuration

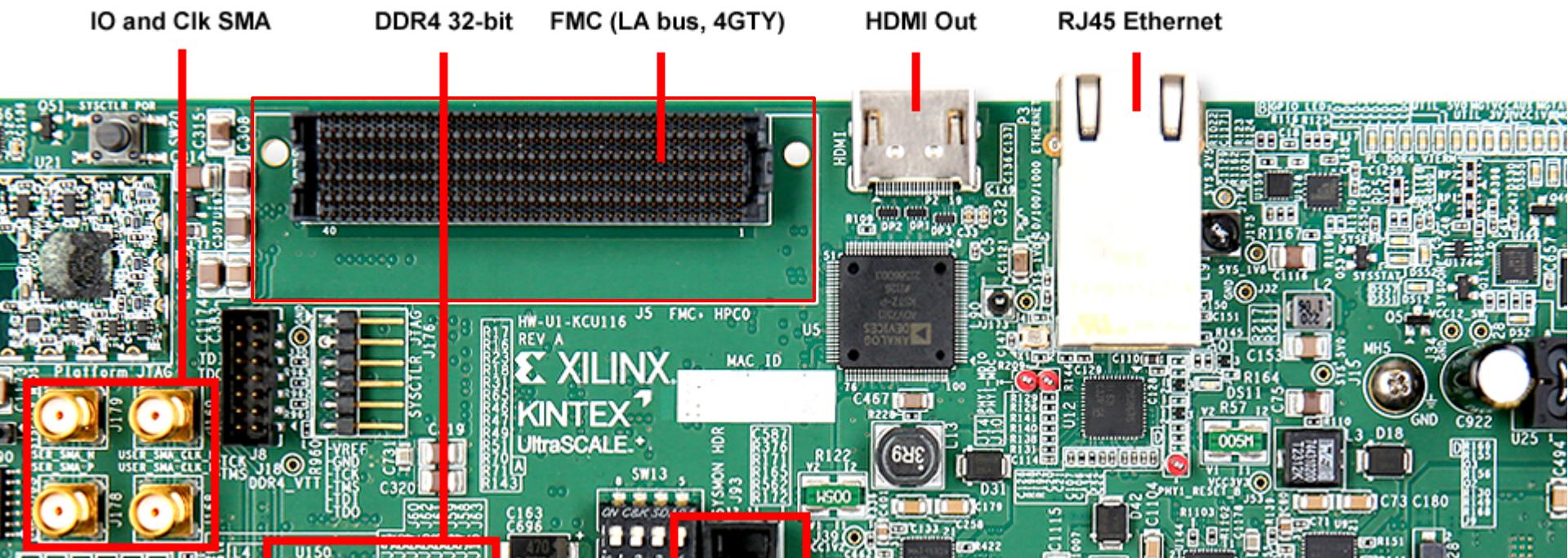


Testing FMC IBERT



Testing FMC IBERT

- > As noted in the Setup Guide, XTP464, attach the optional FMC XM107 board to the FMC HPC connector

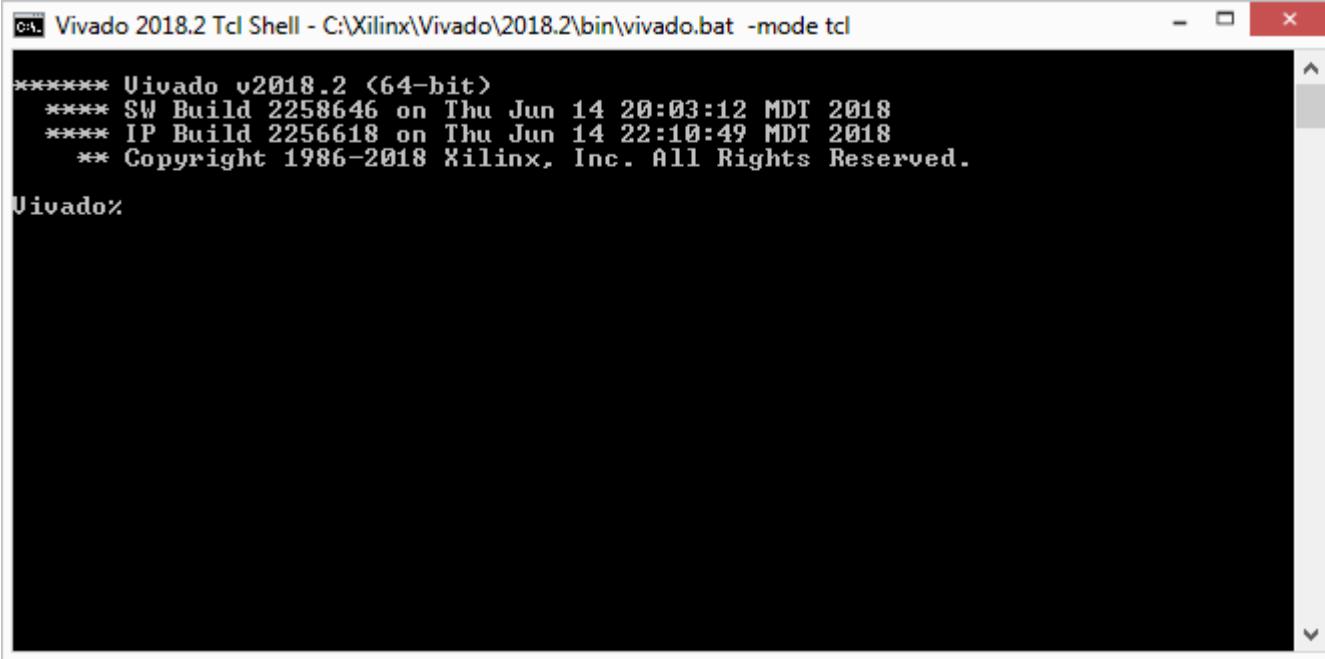


Note: Presentation applies to the KCU116

Testing FMC IBERT

> Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 →
Vivado 2019.1 Tcl Shell



Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl

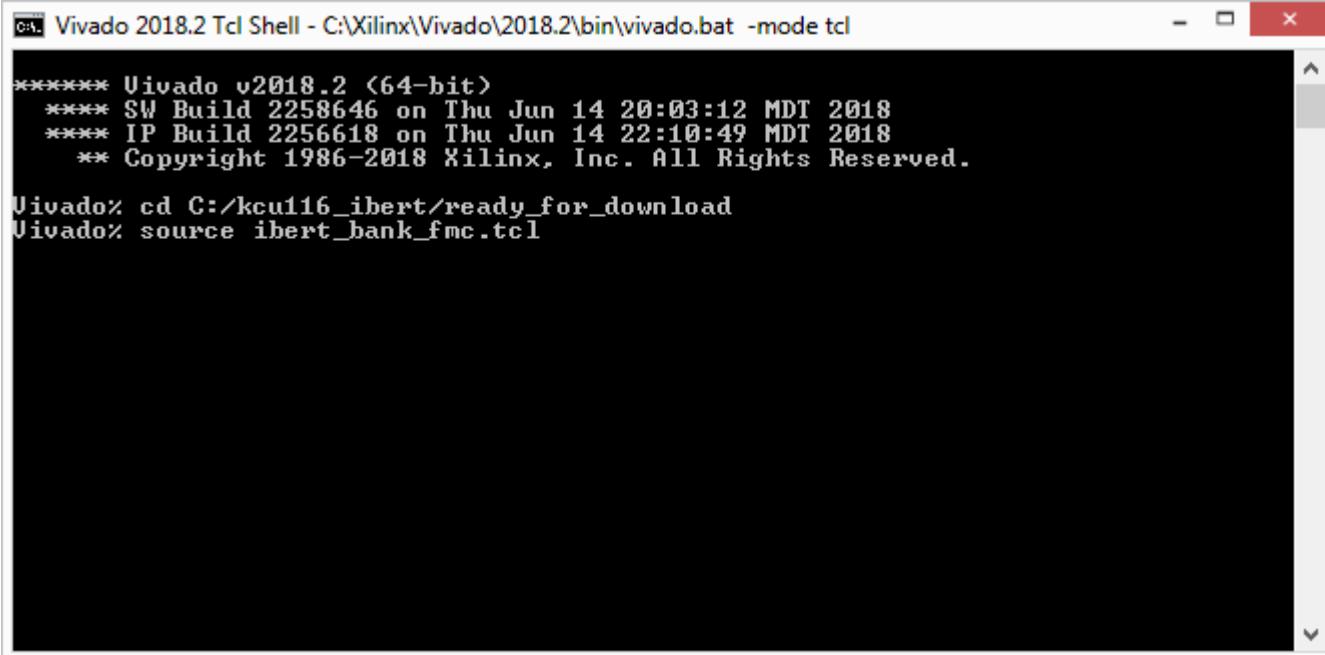
```
***** Vivado v2018.2 (64-bit)
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
```

Vivado>

Testing FMC IBERT

- > In a Vivado Tcl Shell type:

```
cd C:/kcu116_ibert/ready_for_download  
source ibert_bank_fmc.tcl
```

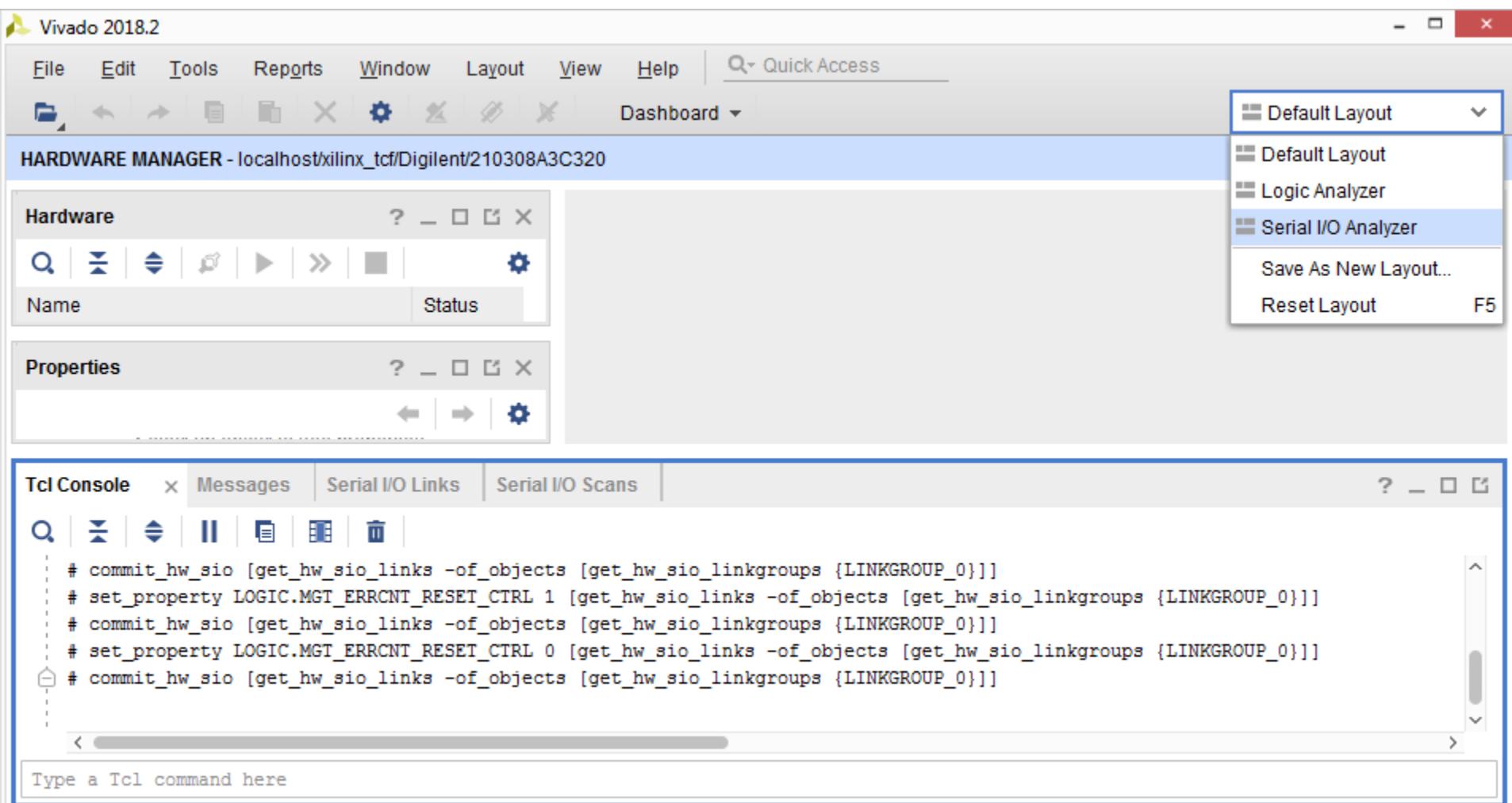


The screenshot shows a Windows command-line interface window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2018.2 (64-bit)  
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018  
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/kcu116_ibert/ready_for_download  
Vivado> source ibert_bank_fmc.tcl
```

Testing FMC IBERT

- > If needed, set Vivado GUI layout to Serial I/O Analyzer



Testing FMC IBERT

- > FMC HPC line rate is 28.125 Gbps
- > Close Vivado GUI after finished viewing

The screenshot shows the Vivado 2019.1 Hardware Manager interface. The title bar reads "Vivado 2019.1". The menu bar includes File, Edit, Tools, Reports, Window, Layout, View, Help, and Quick Access. The toolbar contains icons for file operations like Open, Save, and Close, along with a gear icon for settings. A "Dashboard" button is also present. On the right, a tab labeled "Serial I/O Analyzer" is visible. The main window is titled "HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210308A65F35". Below the title bar, there are tabs for "Tcl Console", "Messages", "Serial I/O Links" (which is selected), and "Serial I/O Scans". The "Serial I/O Links" tab displays a table with the following columns: Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, and RX Pattern. The table lists four FMC links:

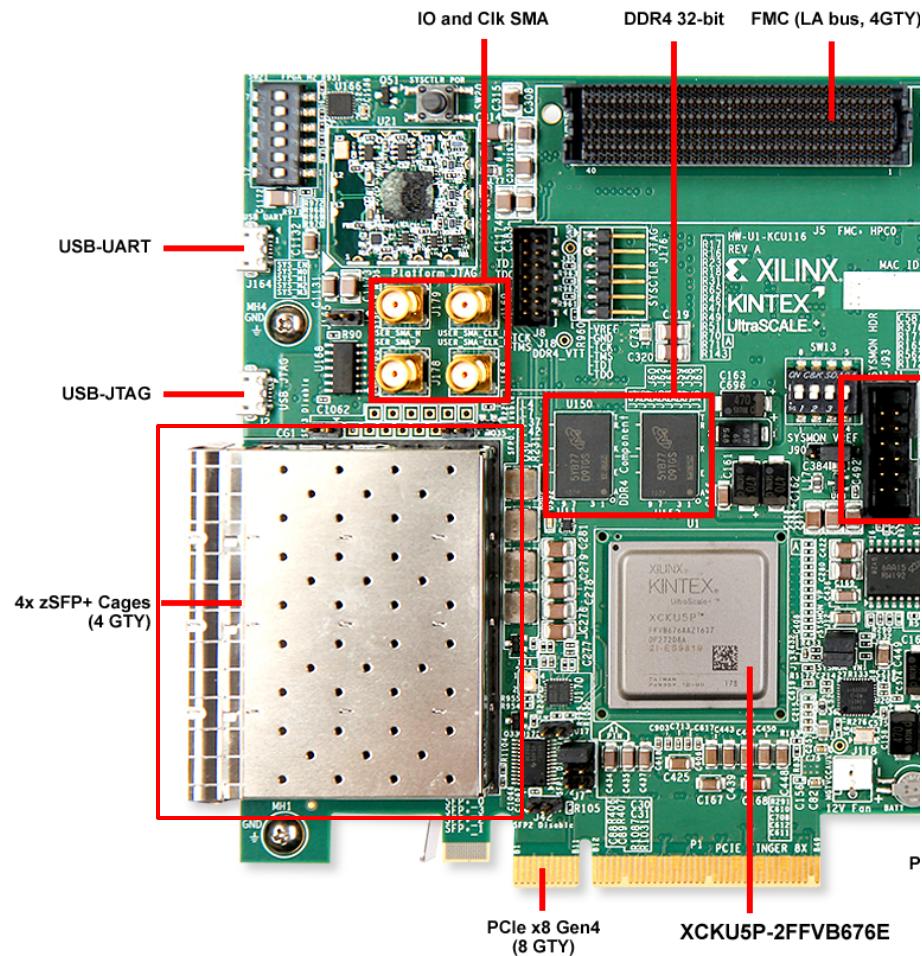
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
FMC (4)							Reset	PRBS 15-bit	PRBS 15-bit
Link 0	MGT_X0Y12/TX	MGT_X0Y12/RX	28.125 Gbps	4.847E12	0E0	2.063E-13	Reset	PRBS 15-bit	PRBS 15-bit
Link 1	MGT_X0Y13/TX	MGT_X0Y13/RX	28.131 Gbps	4.847E12	0E0	2.063E-13	Reset	PRBS 15-bit	PRBS 15-bit
Link 2	MGT_X0Y14/TX	MGT_X0Y14/RX	28.125 Gbps	4.847E12	0E0	2.063E-13	Reset	PRBS 15-bit	PRBS 15-bit
Link 3	MGT_X0Y15/TX	MGT_X0Y15/RX	28.125 Gbps	4.848E12	0E0	2.063E-13	Reset	PRBS 15-bit	PRBS 15-bit

Testing zSFP IBERT



Testing zSFP IBERT

- > This test requires four zSFP 28 Gbps Loopbacks

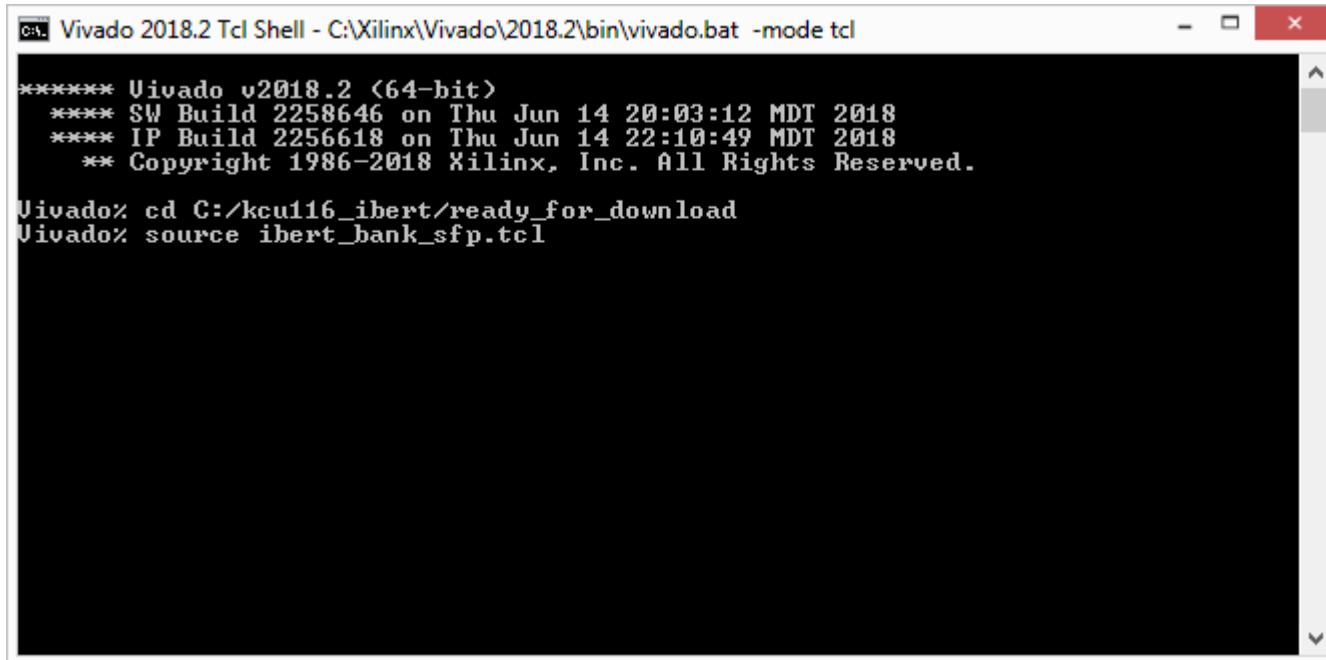


Note: Test requires the Si5328 set to 156.25 MHz

Testing zSFP IBERT

- > In the Vivado Tcl Shell type:

```
cd C:/kcu116_ibert/ready_for_download  
source ibert_bank_sfp.tcl
```



The screenshot shows a Windows command-line interface window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2018.2 (64-bit)  
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018  
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/kcu116_ibert/ready_for_download  
Vivado> source ibert_bank_sfp.tcl
```

Testing zSFP IBERT

- > zSFP line rate is 28.125 Gbps
- > Close Vivado GUI after finished viewing

Vivado 2019.1

File Edit Tools Reports Window Layout View Help Quick Access

Dashboard Serial I/O Analyzer

HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210308A65F35

Tcl Console Messages Serial I/O Links Serial I/O Scans ? _ □ □

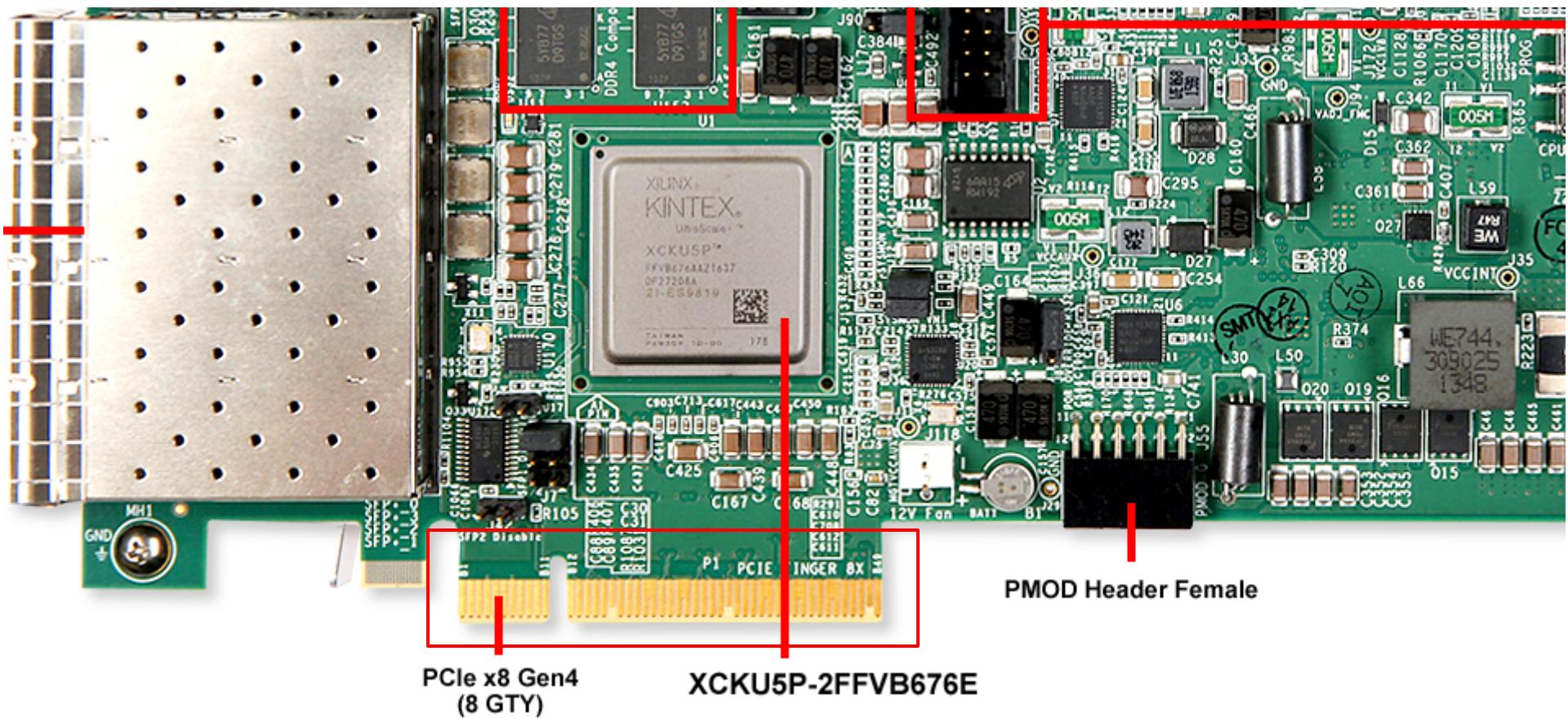
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
SFP (4)							Reset	PRBS 9-bit	PRBS 9-bit
Link 0	MGT_X0Y8/TX	MGT_X0Y8/RX	28.168 Gbps	6.006E12	0E0	1.665E-13	Reset	PRBS 9-bit	PRBS 9-bit
Link 1	MGT_X0Y9/TX	MGT_X0Y9/RX	28.125 Gbps	6.006E12	0E0	1.665E-13	Reset	PRBS 9-bit	PRBS 9-bit
Link 2	MGT_X0Y10/TX	MGT_X0Y10/RX	28.125 Gbps	6.006E12	0E0	1.665E-13	Reset	PRBS 9-bit	PRBS 9-bit
Link 3	MGT_X0Y11/TX	MGT_X0Y11/RX	28.125 Gbps	6.006E12	0E0	1.665E-13	Reset	PRBS 9-bit	PRBS 9-bit

Testing PCIe IBERT



Testing PCIe IBERT

- > Requires [Whizz PCIe Loopback connector](#)
- > Connect a micro USB cable to the PCIe Loopback card for power
 - » Connect this cable to your PC
- > Attach to the PCIe connector (P1) on the KCU116

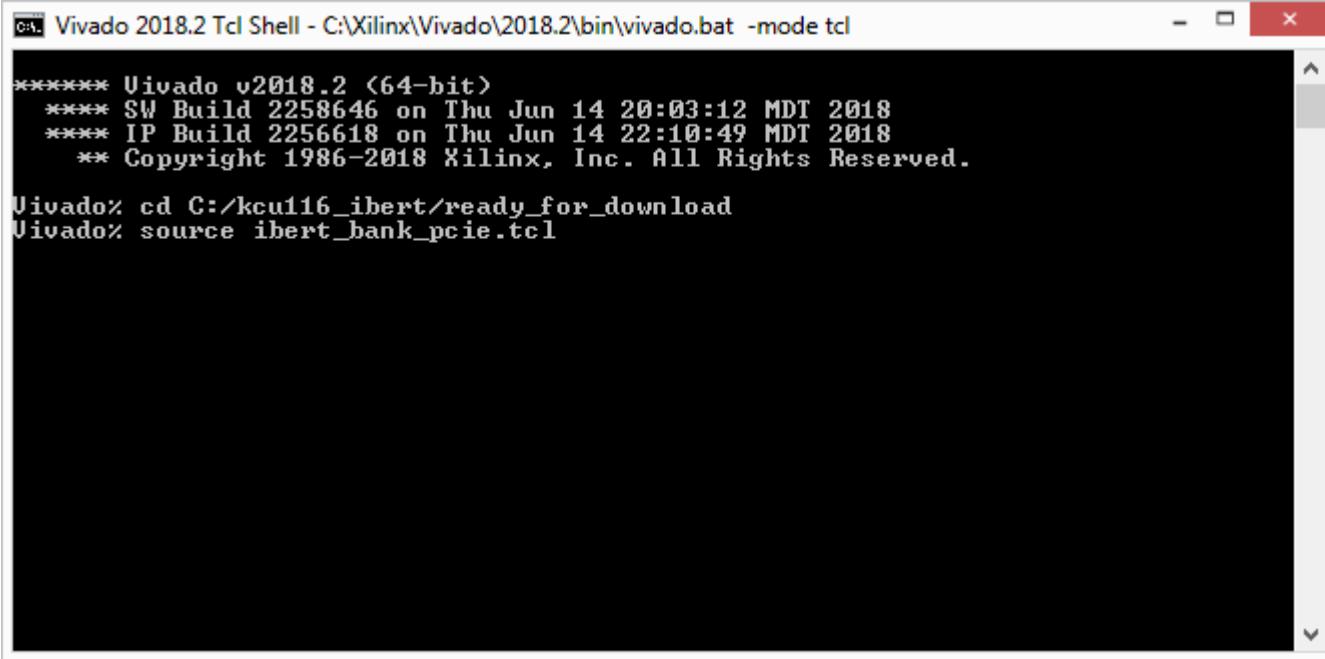


Note: Presentation applies to the KCU116

Testing PCIe IBERT

- > In a Vivado Tcl Shell type:

```
cd C:/kcu116_ibert/ready_for_download  
source ibert_bank_pcie.tcl
```



The screenshot shows a Windows command-line interface window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2018.2 (64-bit)  
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018  
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/kcu116_ibert/ready_for_download  
Vivado> source ibert_bank_pcie.tcl
```

Testing PCIe IBERT

- > PCIe line rate is 8 Gbps
- > Close Vivado GUI after finished viewing

The screenshot shows the Vivado 2019.1 Hardware Manager interface. The title bar reads "Vivado 2019.1". The menu bar includes File, Edit, Tools, Reports, Window, Layout, View, Help, and Quick Access. The toolbar contains icons for file operations like Open, Save, and Close, along with a gear icon for settings. A "Dashboard" dropdown is also present. On the right, a tab labeled "Serial I/O Analyzer" is visible. The main window is titled "HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210308A65F35". The "Serial I/O Links" tab is selected, showing a table with the following columns: Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, and RX Pattern. The table lists 8 PCIe links under the "PCIe" category:

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
PCIe (8)							Reset	PRBS 31-bit	PRBS 31-bit
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	8.000 Gbps	1.179E12	0E0	8.481E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	8.000 Gbps	1.179E12	0E0	8.481E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	7.990 Gbps	1.179E12	0E0	8.481E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	7.995 Gbps	1.179E12	0E0	8.481E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	8.000 Gbps	1.179E12	0E0	8.481E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	7.992 Gbps	1.179E12	0E0	8.481E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	8.000 Gbps	1.179E12	0E0	8.481E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	1.179E12	0E0	8.481E-13	Reset	PRBS 31-bit	PRBS 31-bit

Create IBERT Design for All Banks

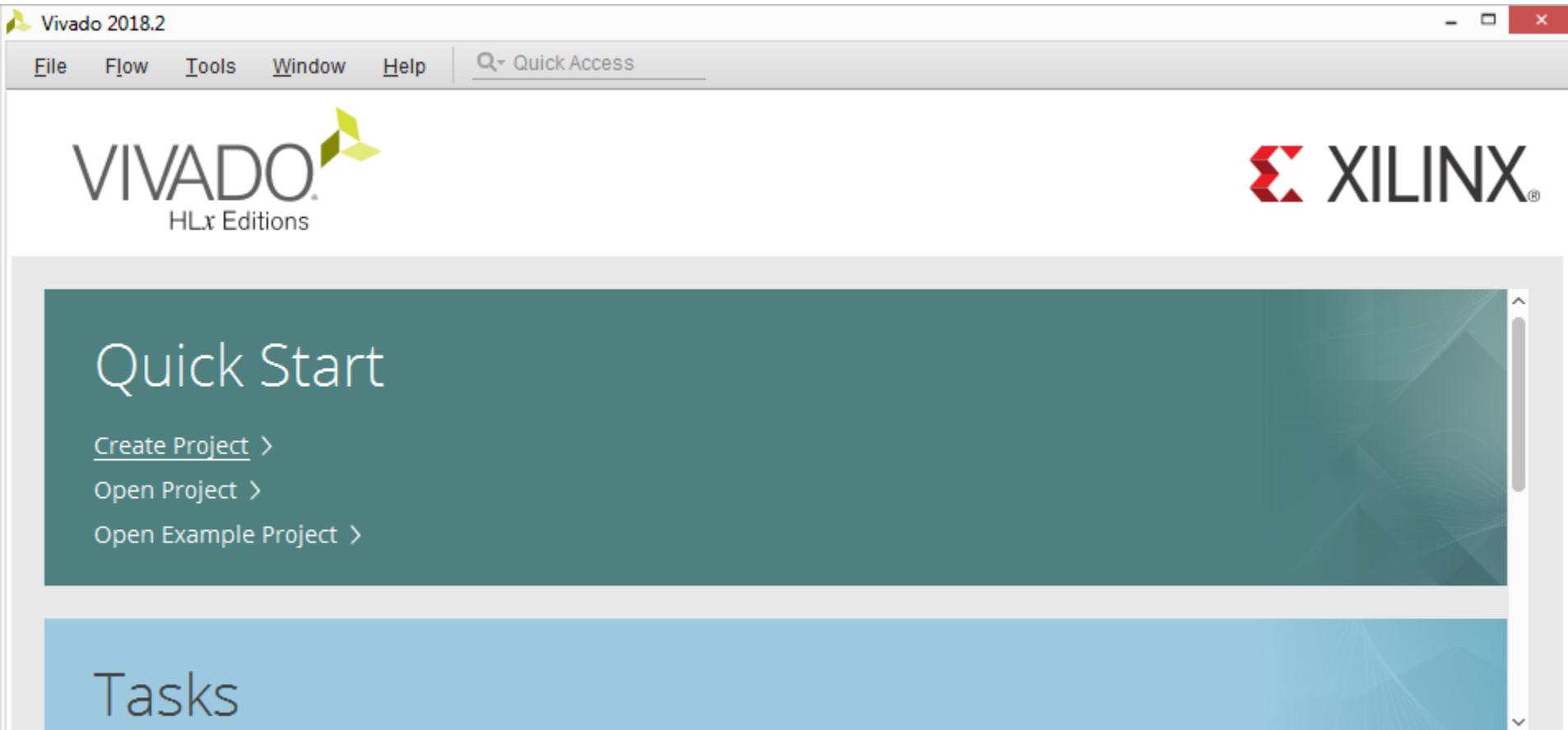


Create IBERT Design for All Banks

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 → Vivado

> Select Create Project



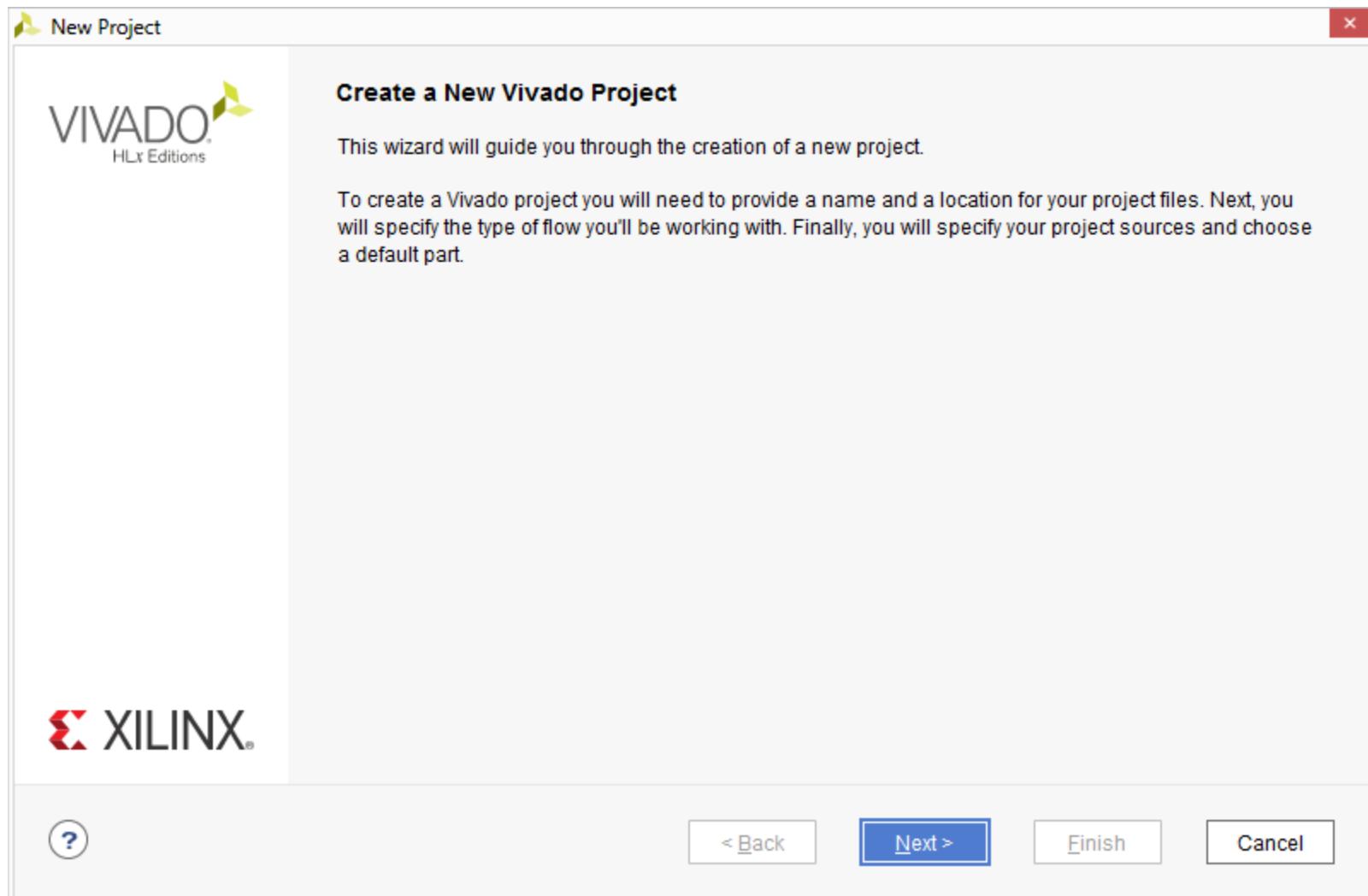
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the KCU116

XILINX

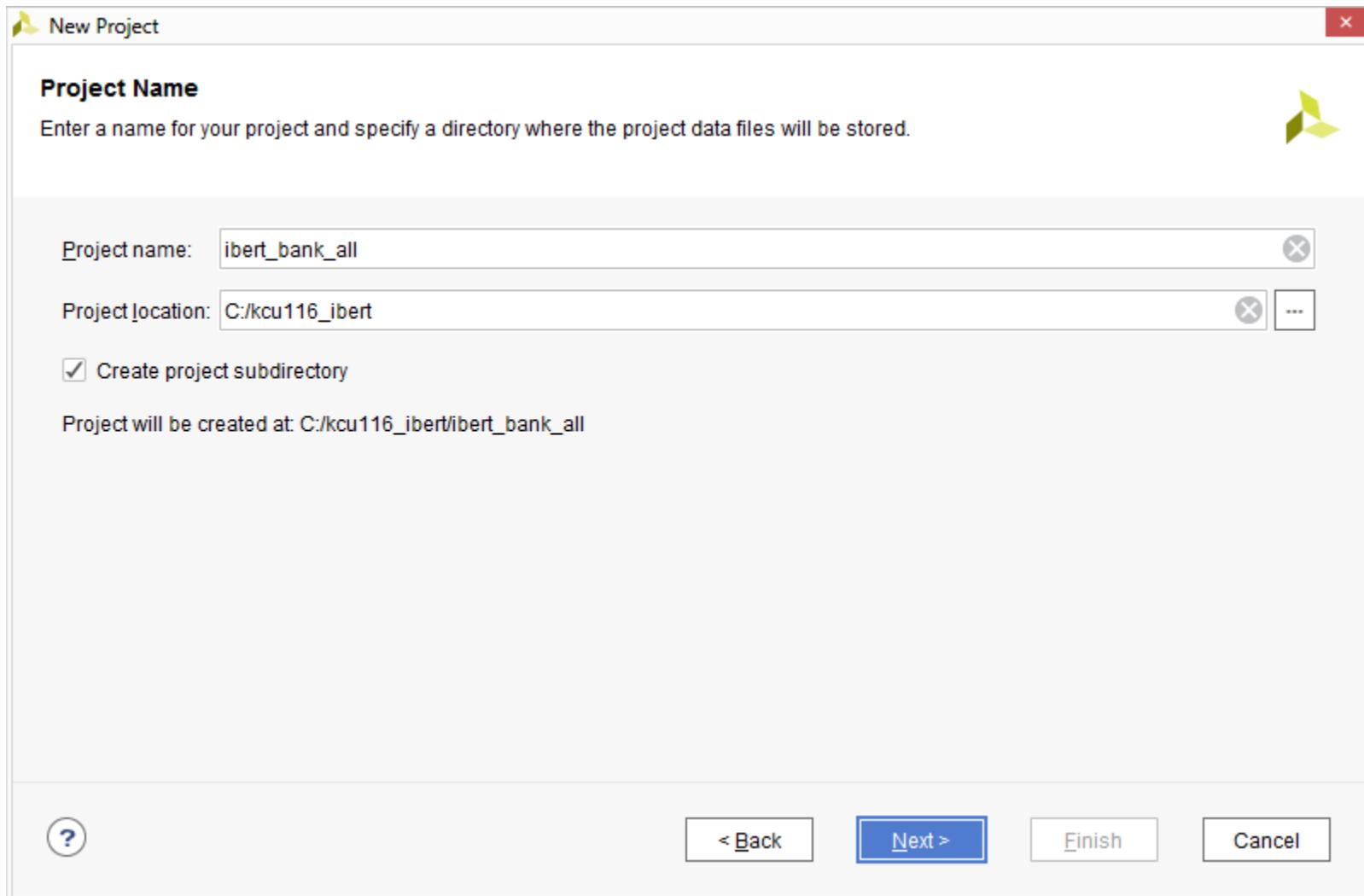
Create IBERT Design for All Banks

> Click Next



Create IBERT Design for All Banks

- > Set the Project name and location to ibert_bank_all and C:/kcu116_ibert; check Create project subdirectory

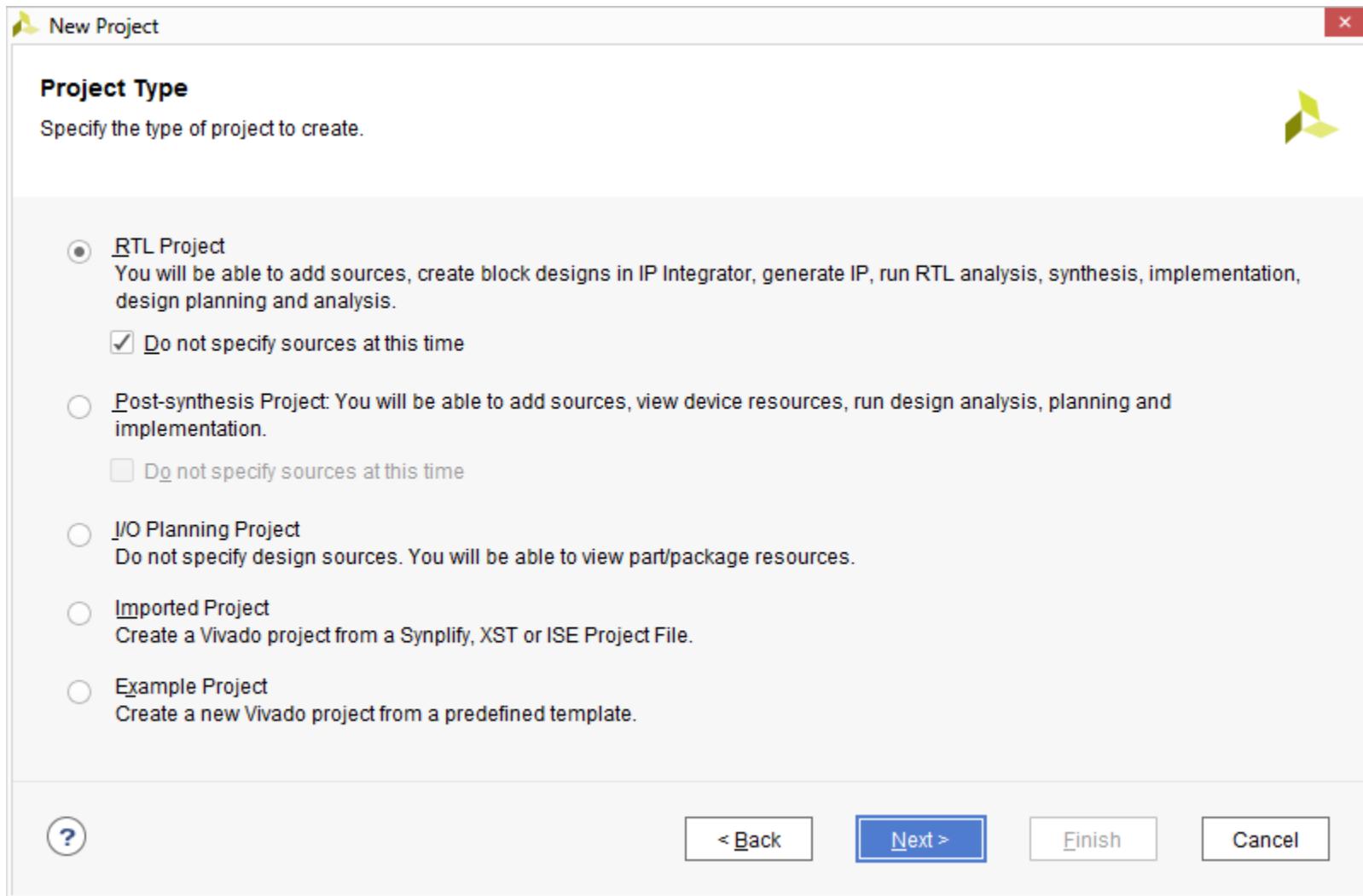


Note: Vivado generally requires forward slashes in paths

Create IBERT Design for All Banks

> Select RTL Project

» Select Do not specify sources at this time



Create IBERT Design for All Banks

- > Under Boards, select the KCU116 Evaluation Platform

New Project

Default Part
Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

Reset All Filters

Vendor: All Name: All

Search:

Display Name	Preview	Vendor	F
Kintex UltraScale+ KCU116 Evaluation Platform Add Daughter Card Connections		xilinx.com	1
Kintex UltraScale KCU1500 Acceleration Development Board		xilinx.com	1

< >

?

< Back

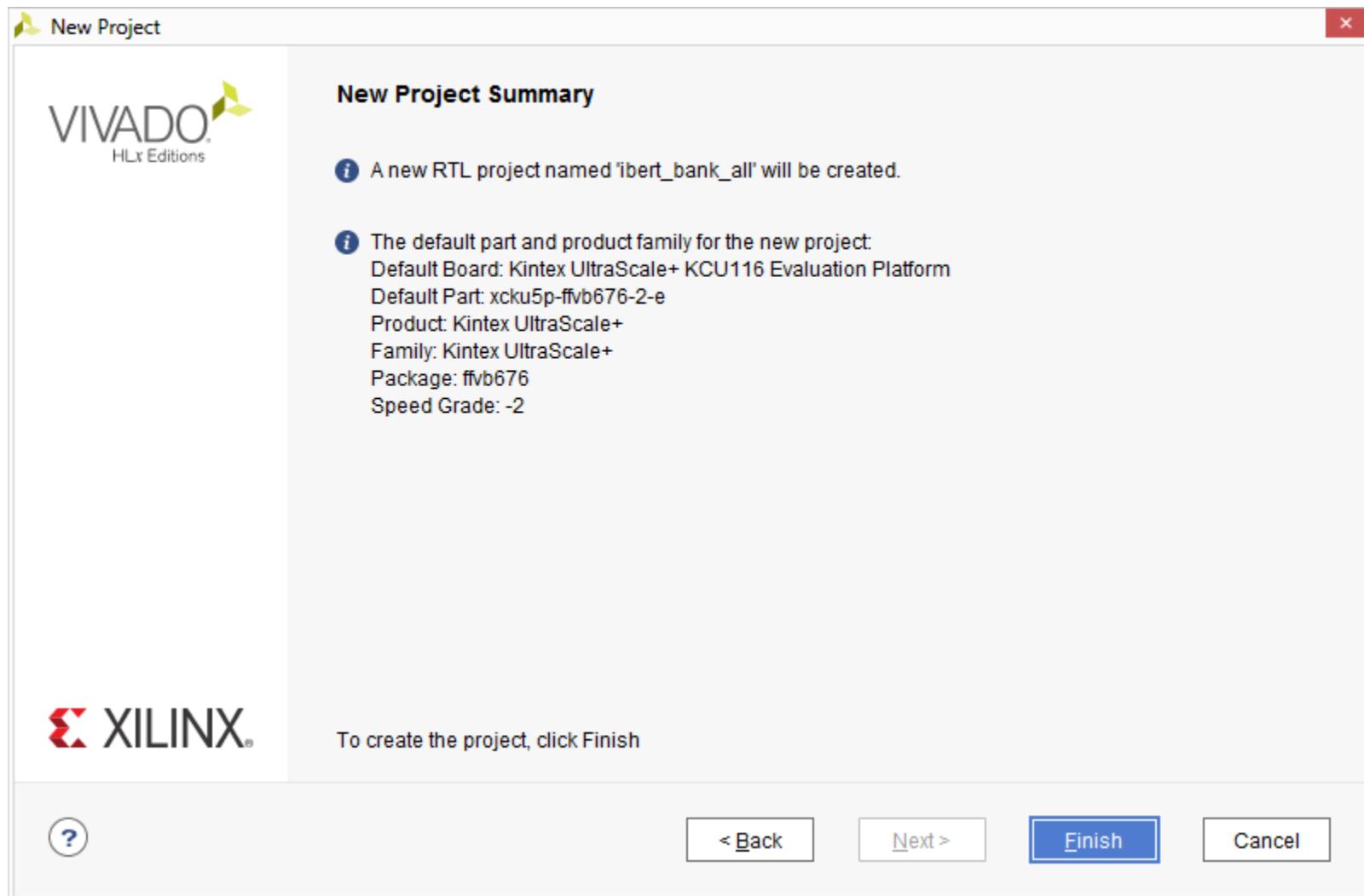
Next >

Finish

Cancel

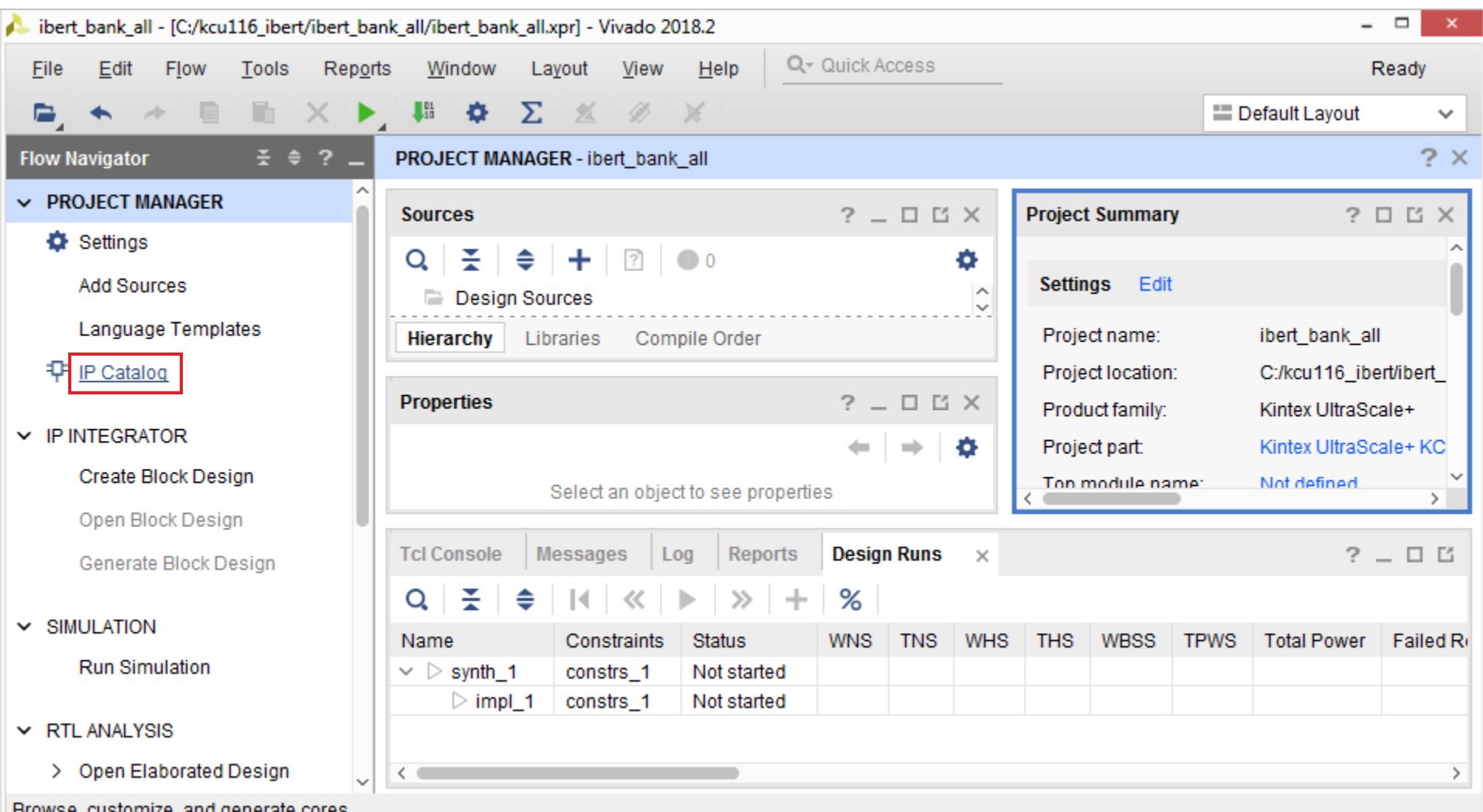
Create IBERT Design for All Banks

> Click Finish



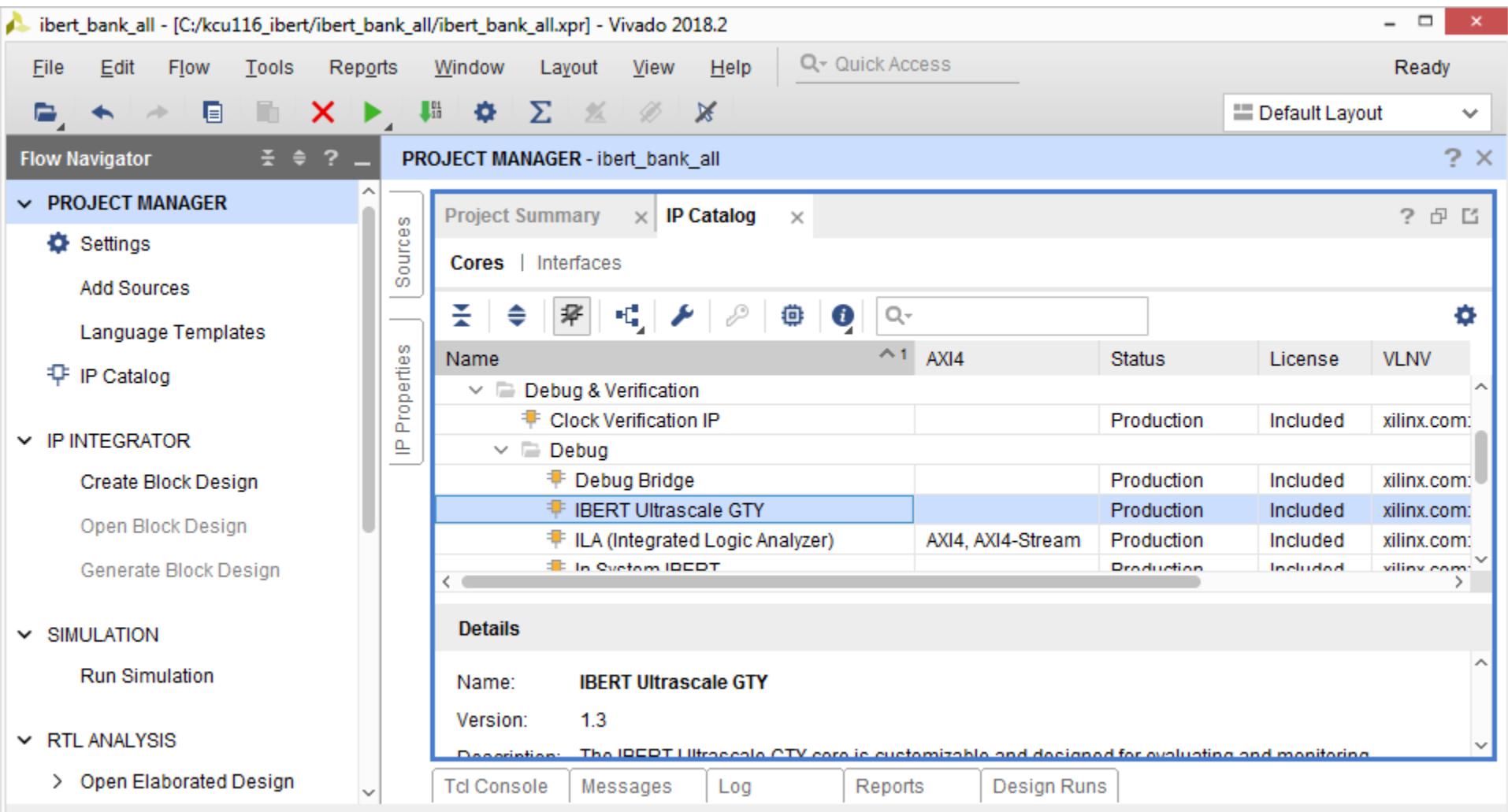
Create IBERT Design for All Banks

> Click on IP Catalog



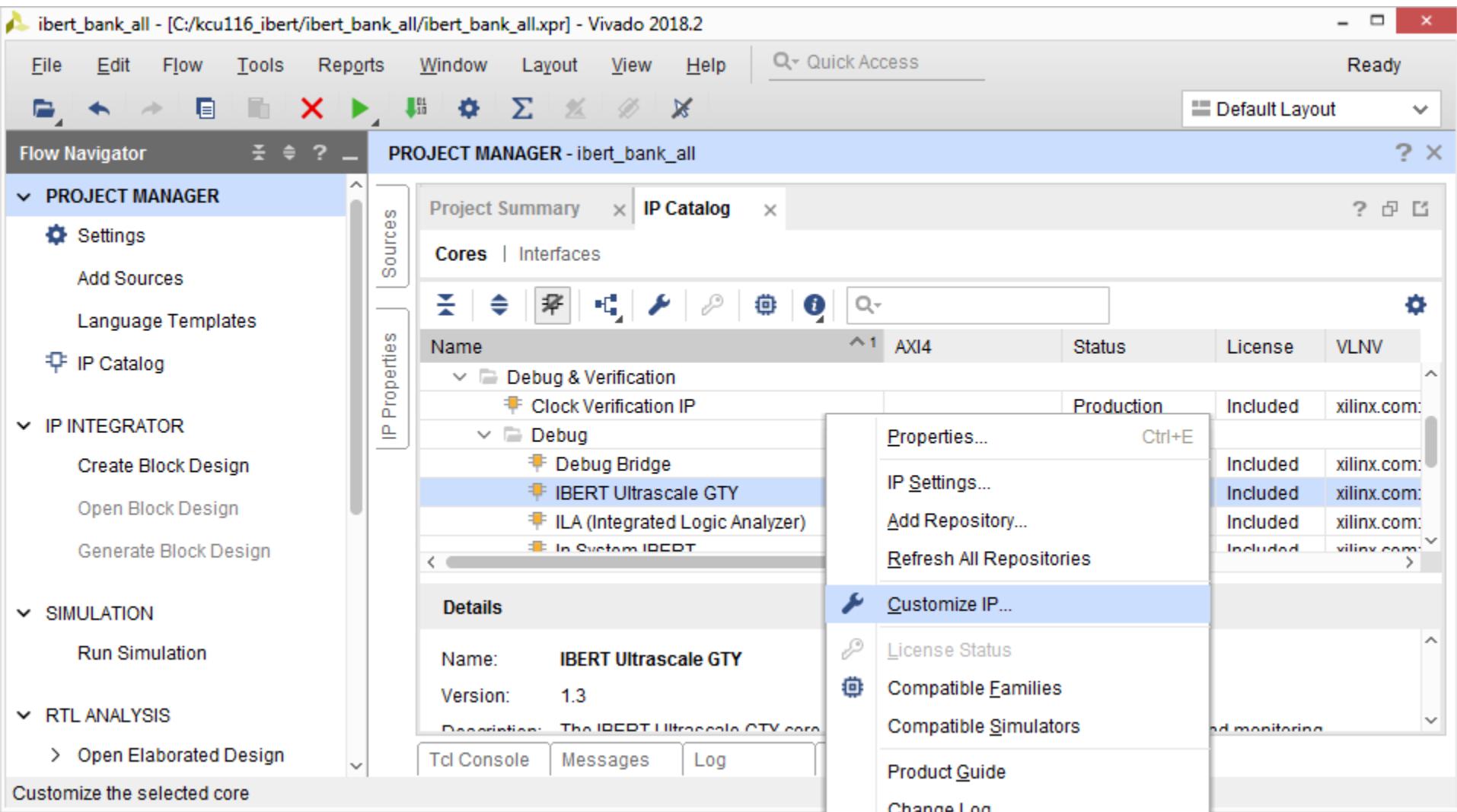
Create IBERT Design for All Banks

- > Select IBERT UltraScale GTY, v1.3 under Debug & Verification



Create IBERT Design for All Banks

- > Right click on IBERT UltraScale GTY and select Customize IP...

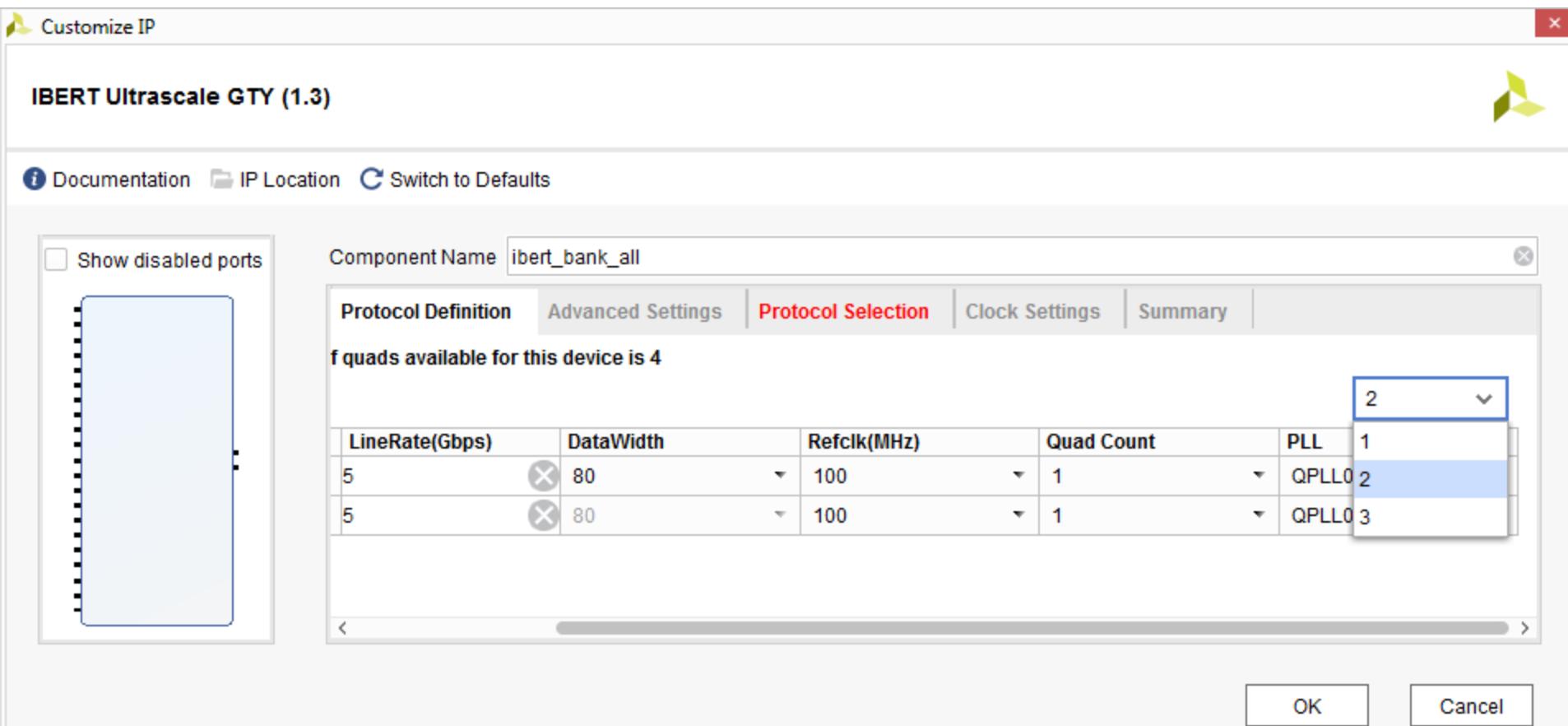


Note: Presentation applies to the KCU116

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Create IBERT Design for All Banks

- > Set the Component name: `ibert_bank_all`
- > Under the Protocol Definition tab
 - » Select 2 Protocols



Create IBERT Design for All Banks

> Under the Protocol Definition tab

- » Protocol Custom 1: LineRate: 8.0, Refclk: 100 Quad Count: 2
- » Protocol Custom 2: LineRate: 28.125, Refclk: 156.25 Quad Count: 2

Customize IP

IBERT Ultrascale GTY (1.3)

Documentation IP Location Switch to Defaults

Show disabled ports

Component Name: ibert_bank_all

Protocol Definition Advanced Settings Protocol Selection Clock Settings Summary

The maximum number of quads available for this device is 4

Number of Protocols

Protocol	LineRate(Gbps)	DataWidth	Refclk(MHz)	Quad Count
Custom 1	8.0	80	100	2
Custom 2	28.125	80	156.25	2

OK Cancel

Create IBERT Design for All Banks

- > Under the Protocol Selection tab
- > Set QUAD_224 and QUAD_225 to
 - » Custom 1 / 8.0 Gbps, and MGTREFCLK0 225

Customize IP

IBERT Ultrascale GTY (1.3)

Documentation IP Location Switch to Defaults

Show disabled ports

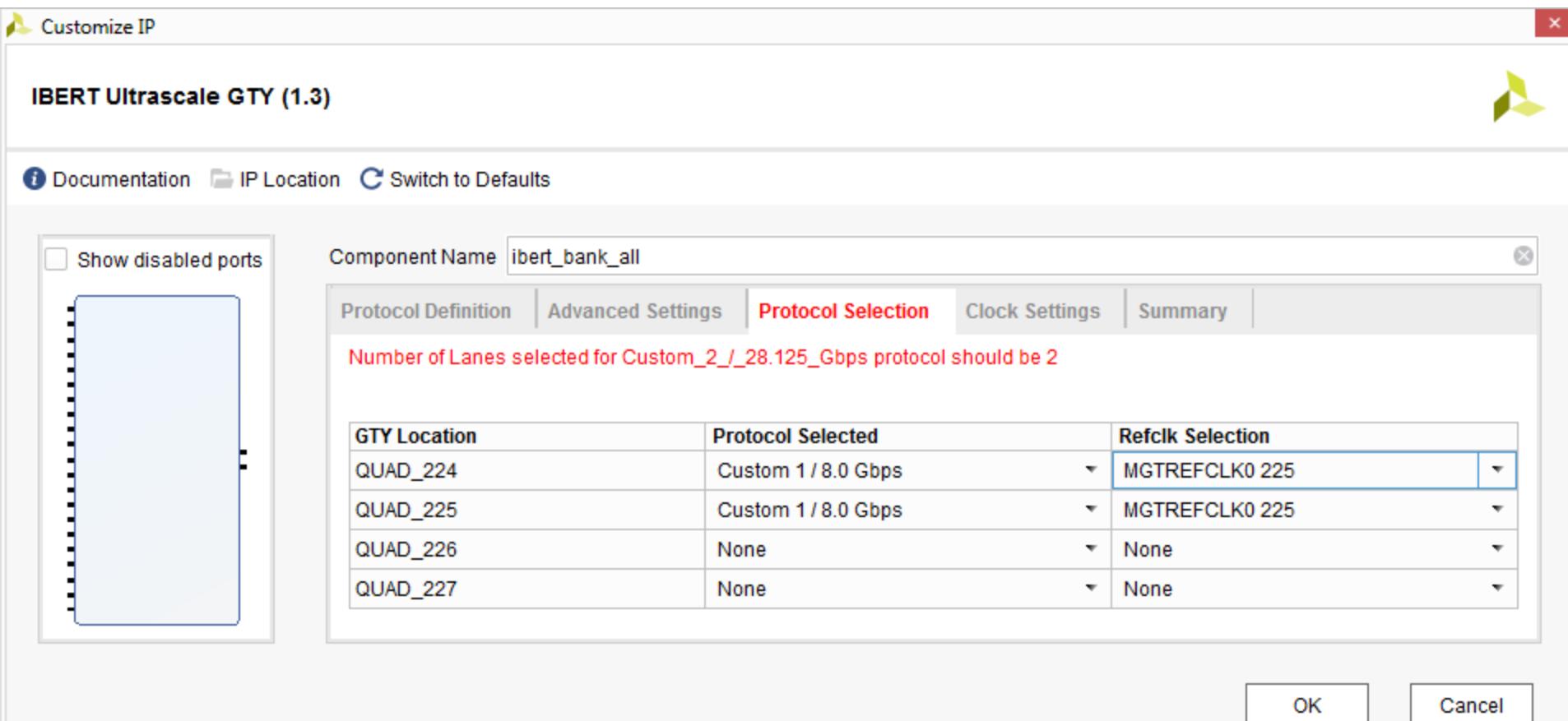
Component Name: ibert_bank_all

Protocol Definition Advanced Settings **Protocol Selection** Clock Settings Summary

Number of Lanes selected for Custom_2/_28.125_Gbps protocol should be 2

GTY Location	Protocol Selected	Refclk Selection
QUAD_224	Custom 1 / 8.0 Gbps	MGTREFCLK0 225
QUAD_225	Custom 1 / 8.0 Gbps	MGTREFCLK0 225
QUAD_226	None	None
QUAD_227	None	None

OK Cancel



Create IBERT Design for All Banks

- > Set QUAD_226 to
 - » Custom 2 / 28.125 Gbps, and MGTREFCLK0 226
- > Set QUAD_227 to
 - » Custom 1 / 28.125 Gbps, and MGTREFCLK0 227

Customize IP

IBERT Ultrascale GTY (1.3)

Documentation IP Location Switch to Defaults

Show disabled ports

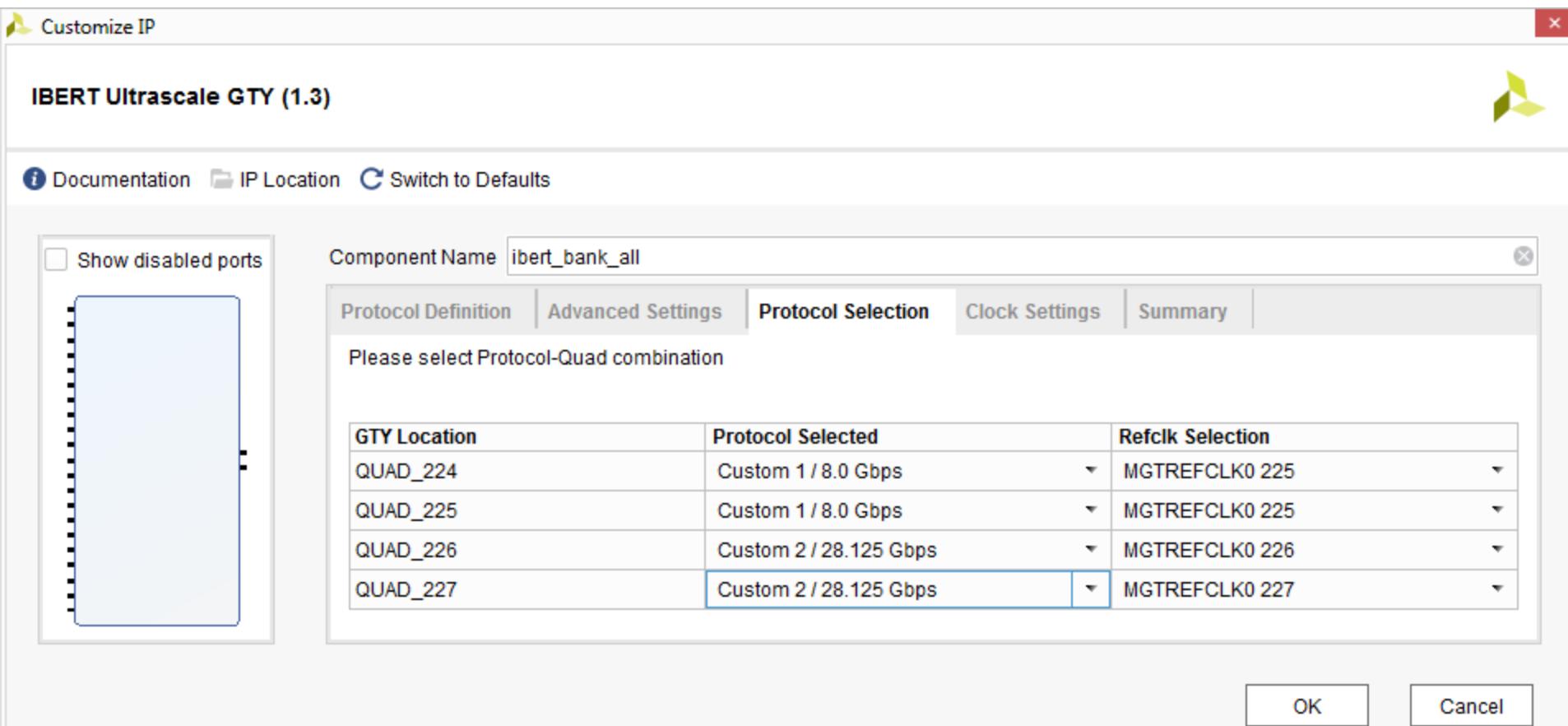
Component Name: ibert_bank_all

Protocol Selection

Please select Protocol-Quad combination

GTY Location	Protocol Selected	Refclk Selection
QUAD_224	Custom 1 / 8.0 Gbps	MGTREFCLK0 225
QUAD_225	Custom 1 / 8.0 Gbps	MGTREFCLK0 225
QUAD_226	Custom 2 / 28.125 Gbps	MGTREFCLK0 226
QUAD_227	Custom 2 / 28.125 Gbps	MGTREFCLK0 227

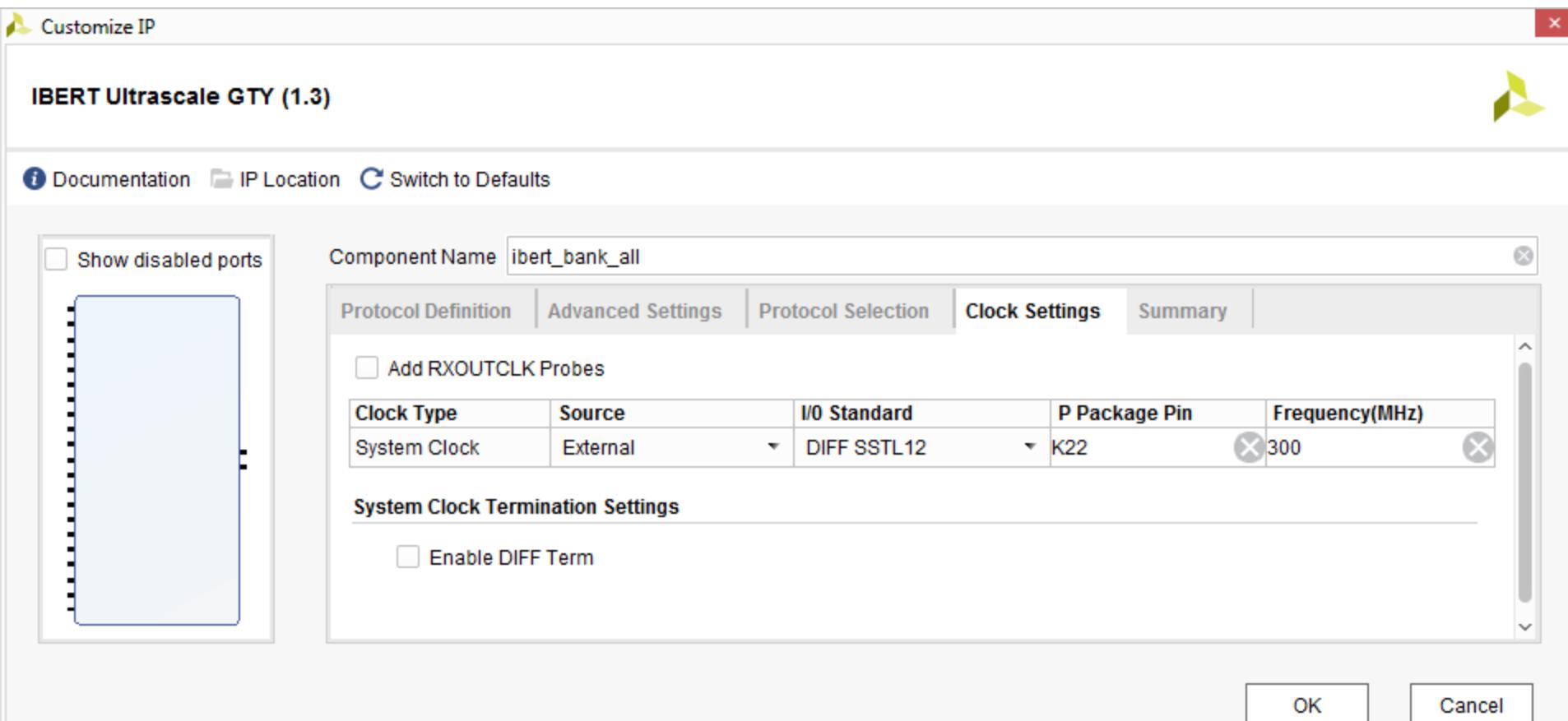
OK Cancel



Create IBERT Design for All Banks

> Under the Clock Settings tab, set the System Clock:

- » DIFF SSTL12, P Package Pin: K22, Frequency: 300
- » Deselect Enable DIFF Term



Create IBERT Design for All Banks

- > Review the summary and click OK

Screenshot of the "Customize IP" dialog for the "IBERT Ultrascale GTY (1.3)" component.

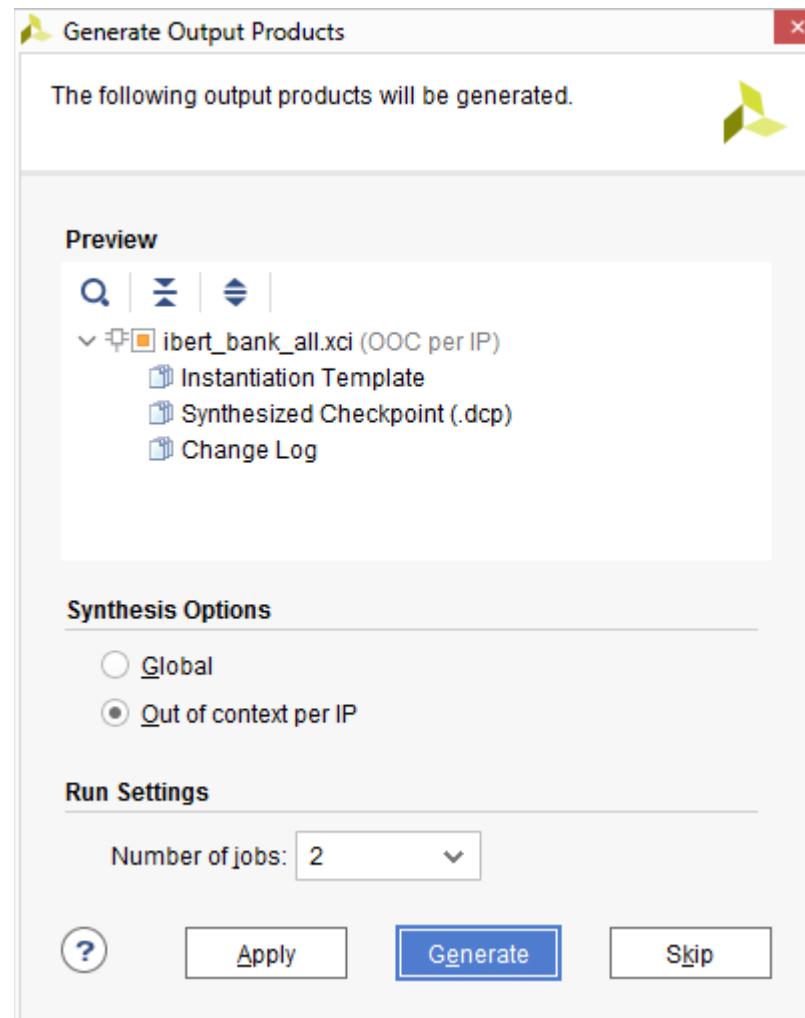
The dialog shows the following details:

- Component Name:** ibert_bank_all
- Protocol Definition:** Summary tab selected.
- IBERT Design Summary:** Table showing configuration details:

Number of Protocols	2
System Clock Source	External (P Pin : K22)
System Clock Frequency	300
RefClk Sources	3
- Buttons:** OK and Cancel.

Create IBERT Design for All Banks

- > Click Generate

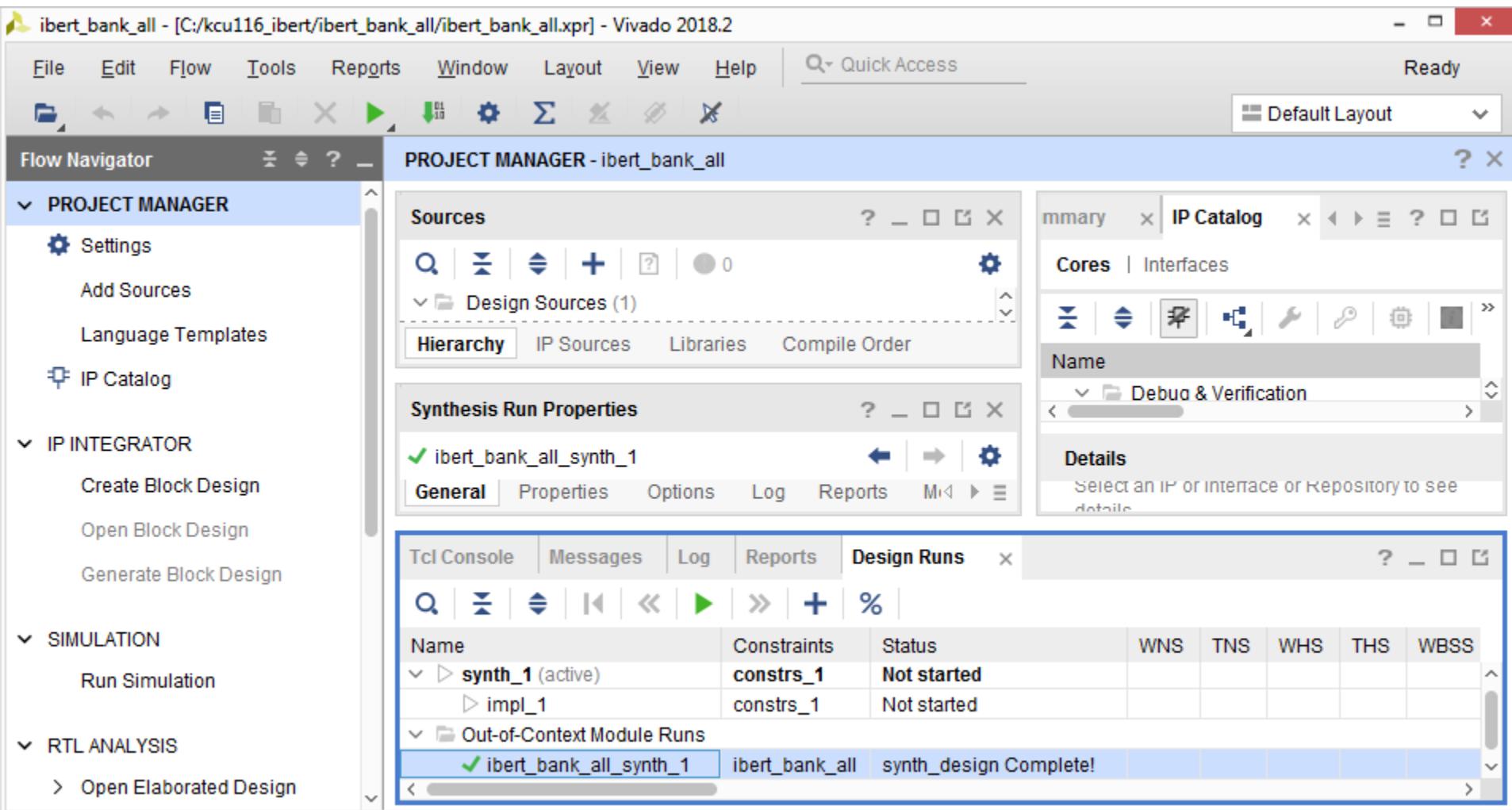


Note: This step will take about 10 minutes

Create IBERT Design for All Banks

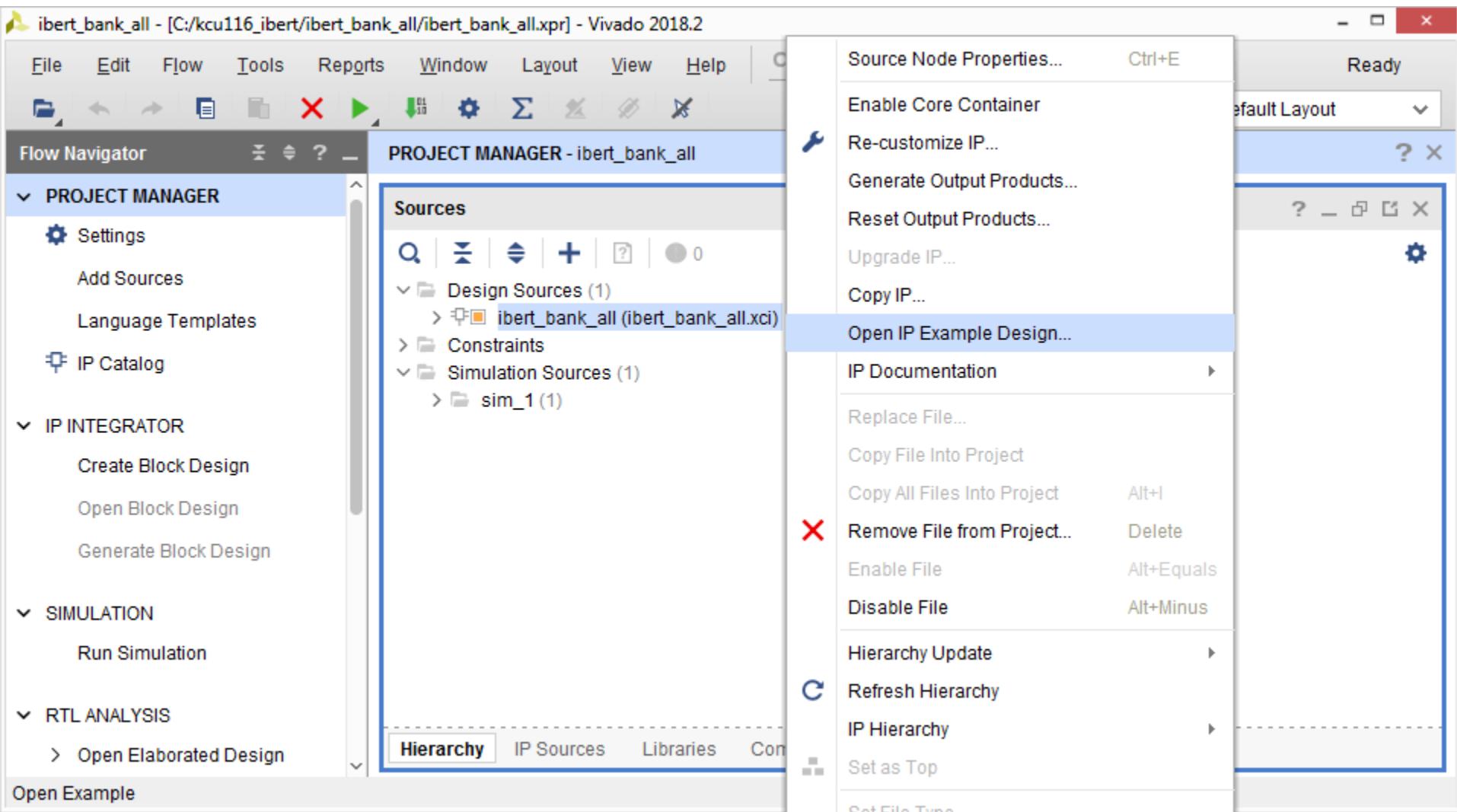
> The Generated IBERT IP appears in Design Sources

» Wait until checkmark appears on ibert_bank_all_synth_1



Compile Example Design

- > Right click on ibert_bank_all and select Open IP Example Design...

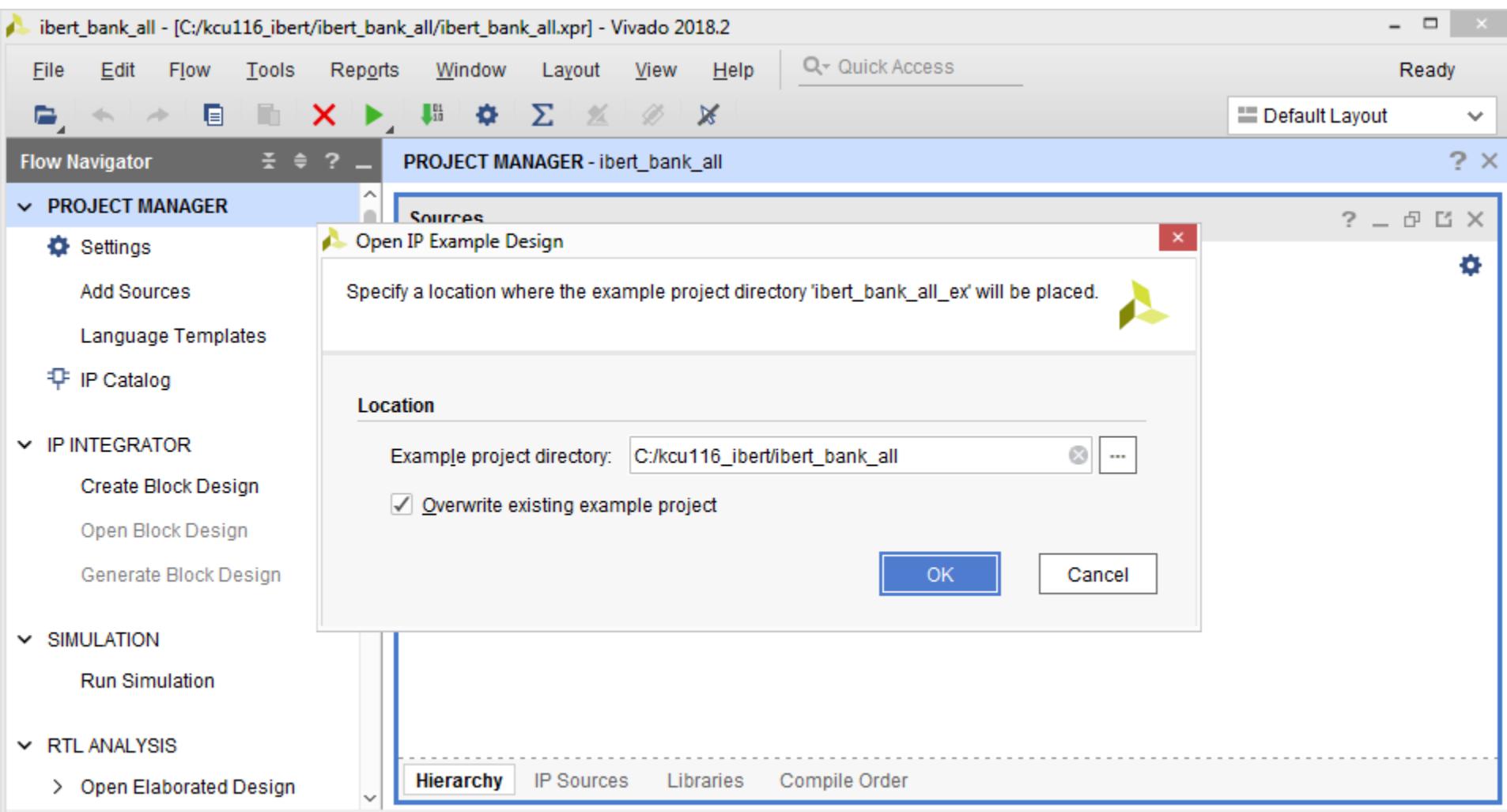


Note: Presentation applies to the KCU116

XILINX

Compile Example Design

- > Set the location to C:/kcu116_ibert/ibert_bank_all and click OK



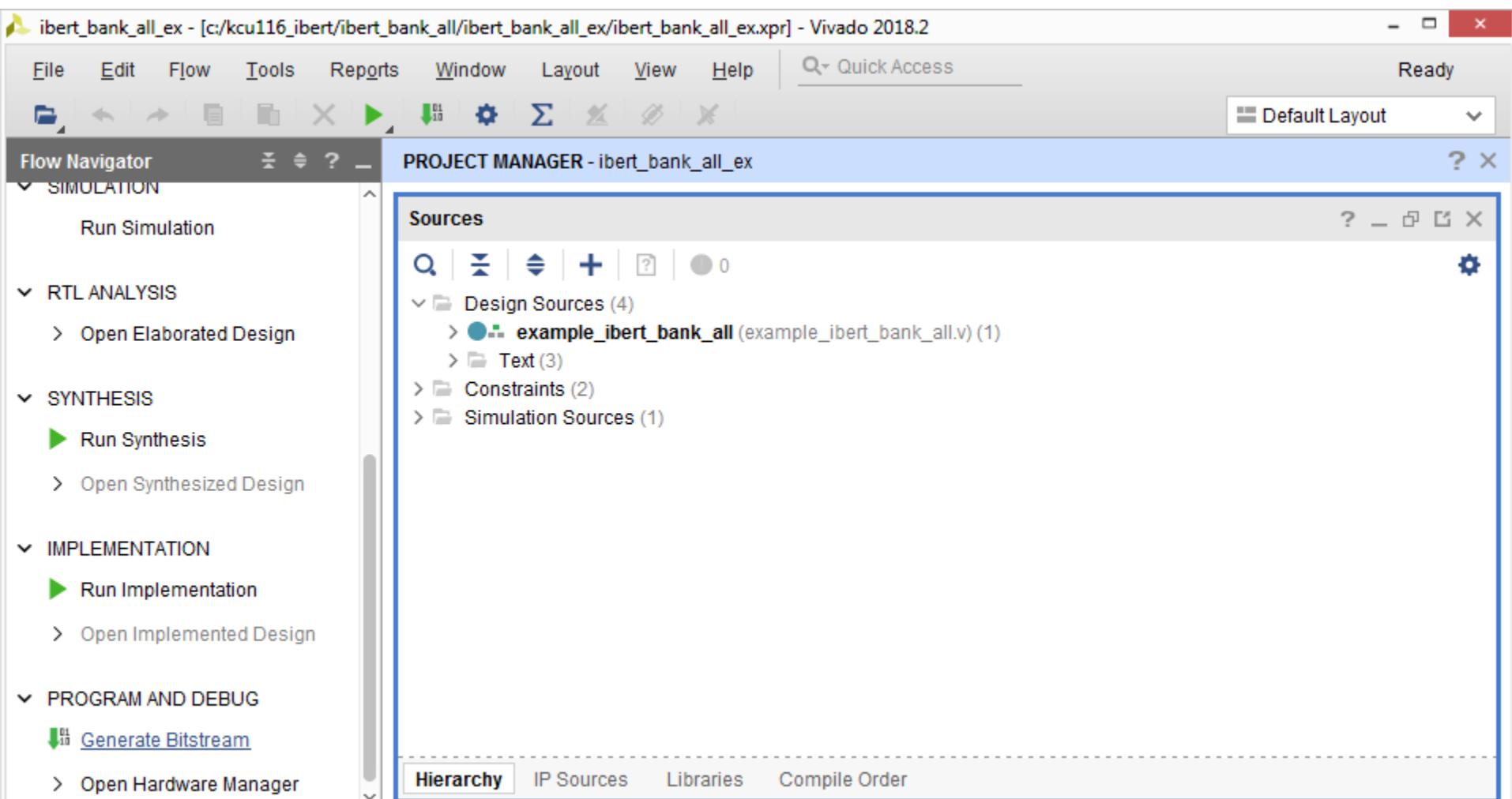
Open Example

Note: Presentation applies to the KCU116

 XILINX

Compile Example Design

- > A new project is created
- > Click Generate Bitstream

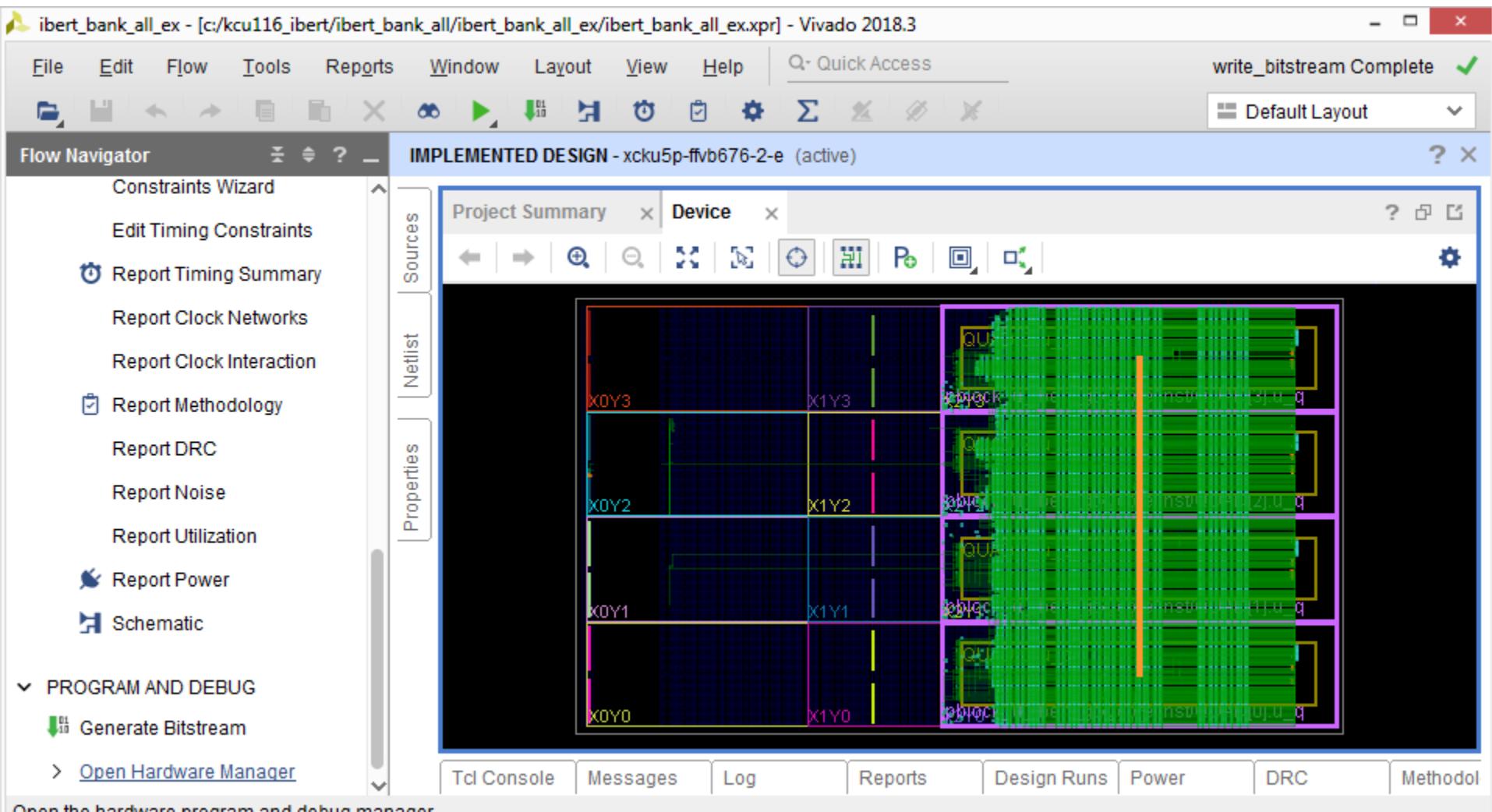


Generate a programming file after implementation

Note: The original project window can be closed

Compile Example Design

- > Open and view the Implemented Design
- > Click Open Hardware Manager



Note: Presentation applies to the KCU116

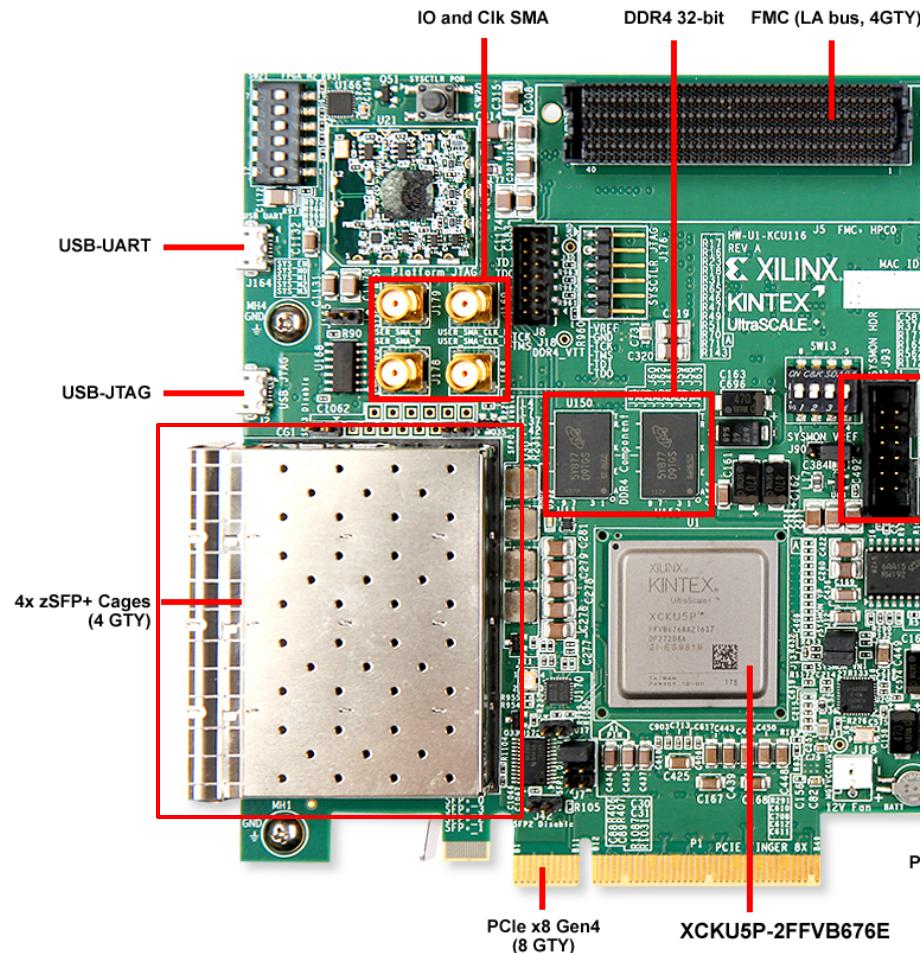
 XILINX

Testing All Banks with Optional User Provided Hardware



Hardware Setup with User Provided Hardware

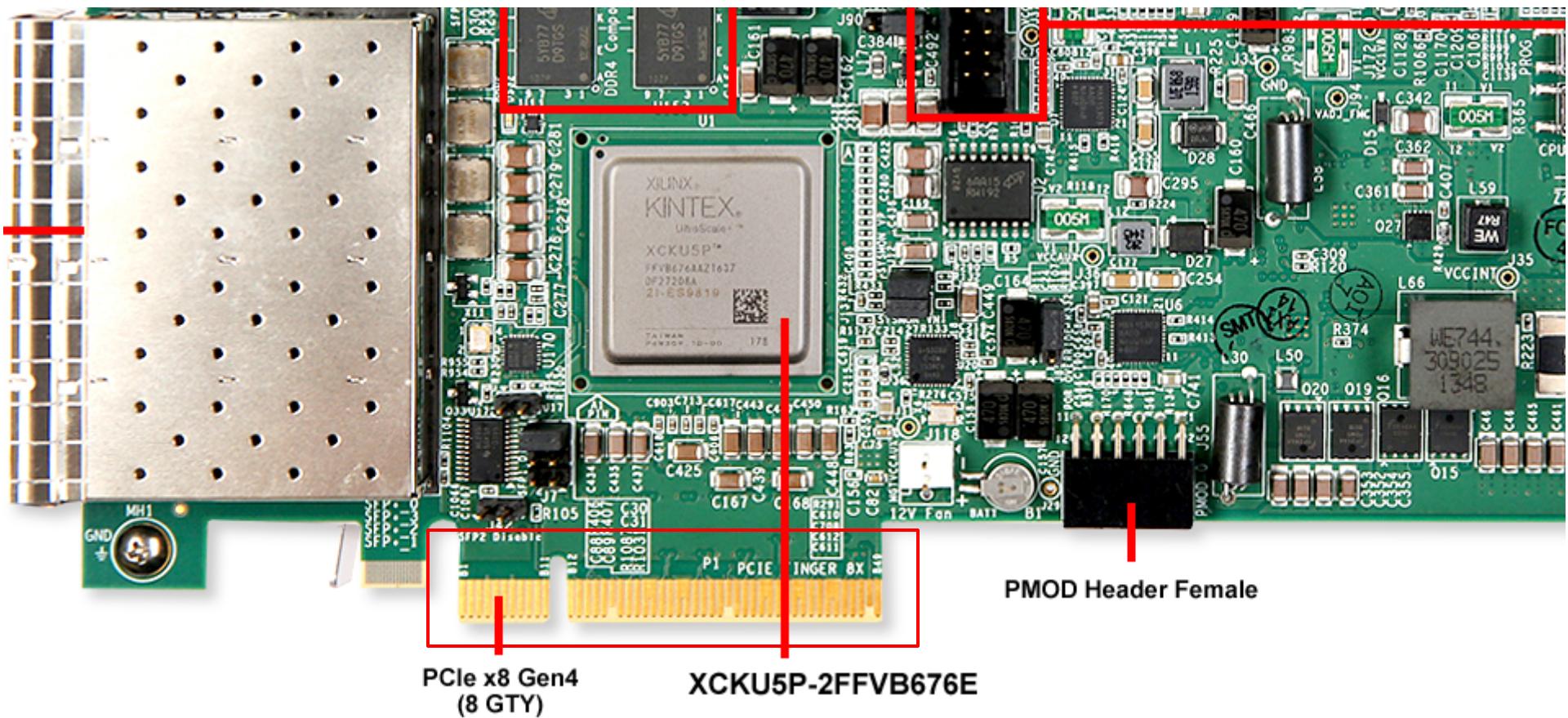
- > Insert 4 zSFP Loopback adapters



Note: Test requires the Si5328 set to 156.25 MHz

Hardware Setup with User Provided Hardware

- > Attach Whizz PCIe Loopback connector
- > Connect a micro USB cable to the PCIe Loopback card for power
 - » Connect this cable to your PC



Hardware Setup with User Provided Hardware

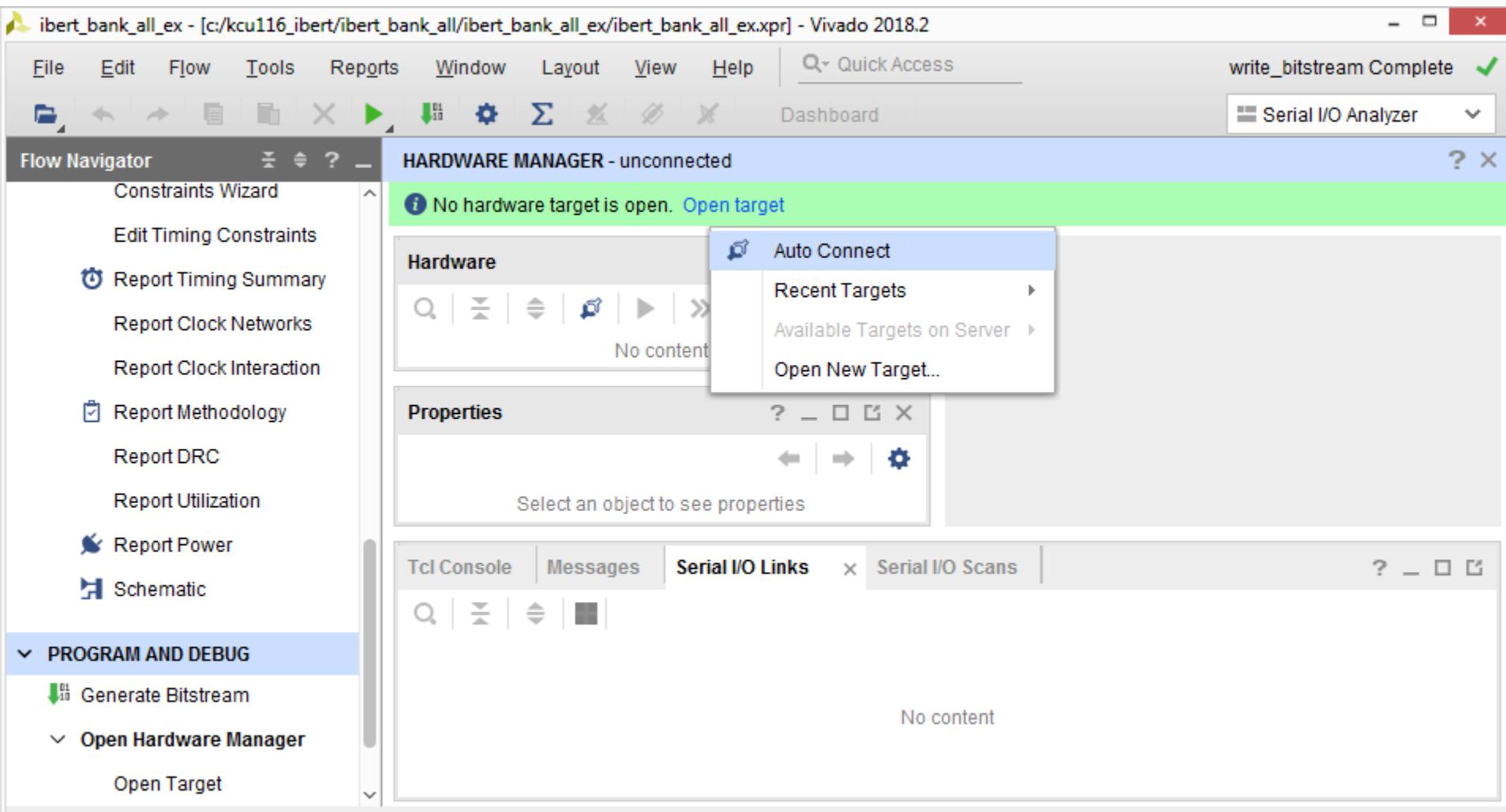
- > Attach an XM107 to the HPC0 connector

- » XM107 boards available through [Whizz Systems](#)



Run IBERT Example Design

- > Click Open target and select Auto Connect



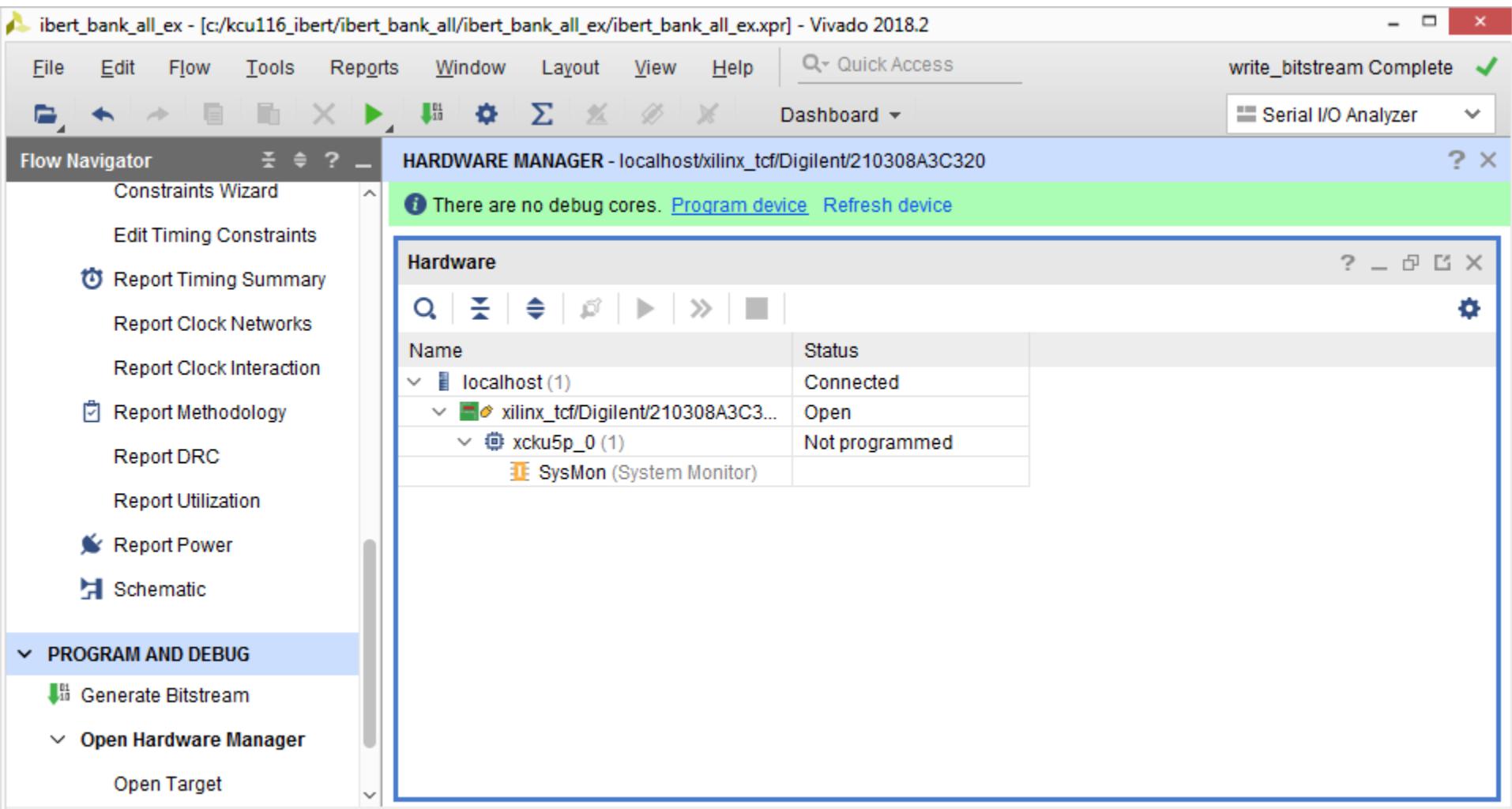
Automatically connect to local hardware target

Note: Presentation applies to the KCU116

 XILINX

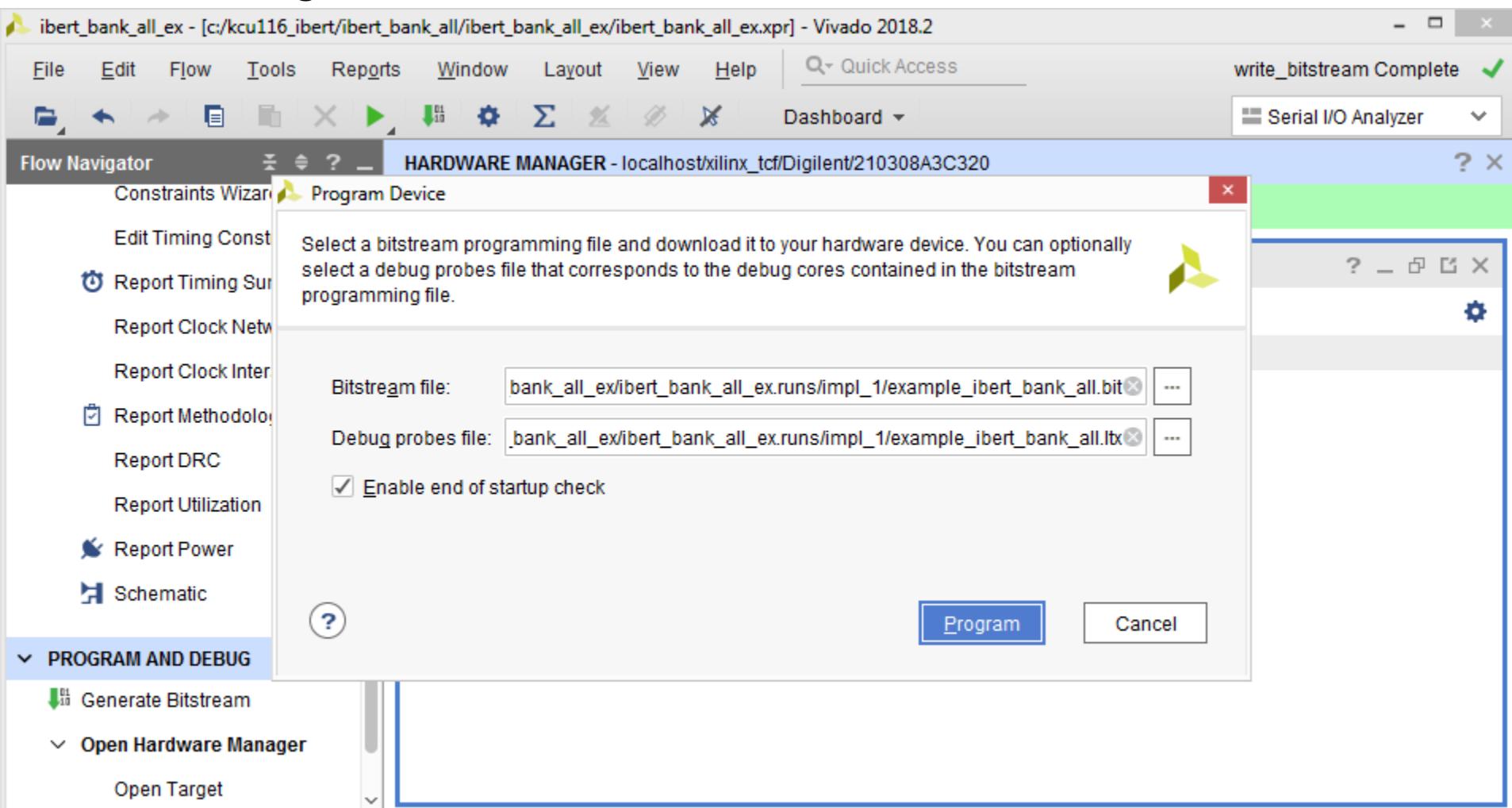
Run IBERT Example Design

> Click Program device



Run IBERT Example Design

- > The newly created bitstream and LTX files are set to the default
- > Click Program



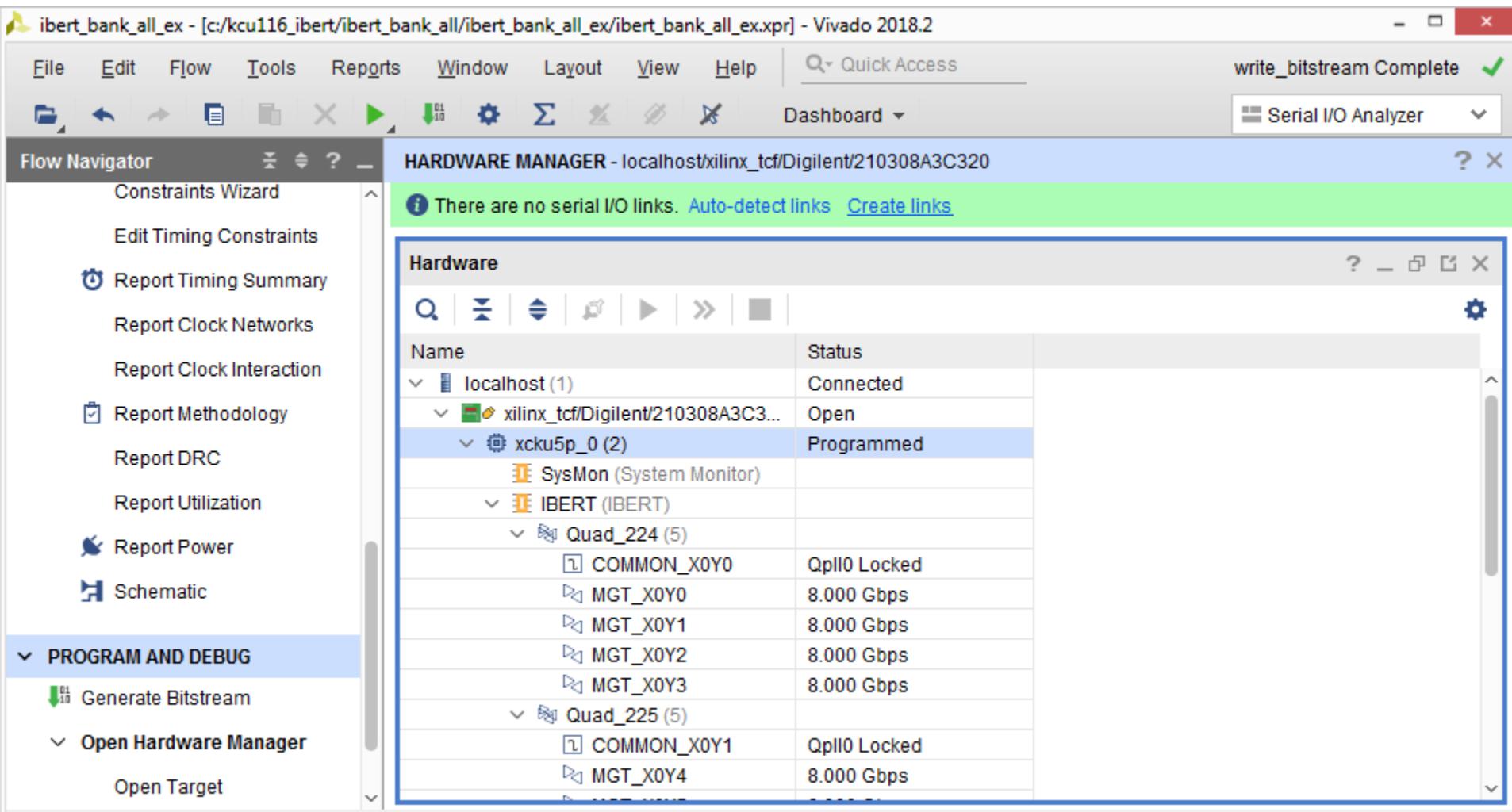
Hardware Device: xcku5p_0

Note: Presentation applies to the KCU116

 XILINX

Run IBERT Example Design

> Click Create links

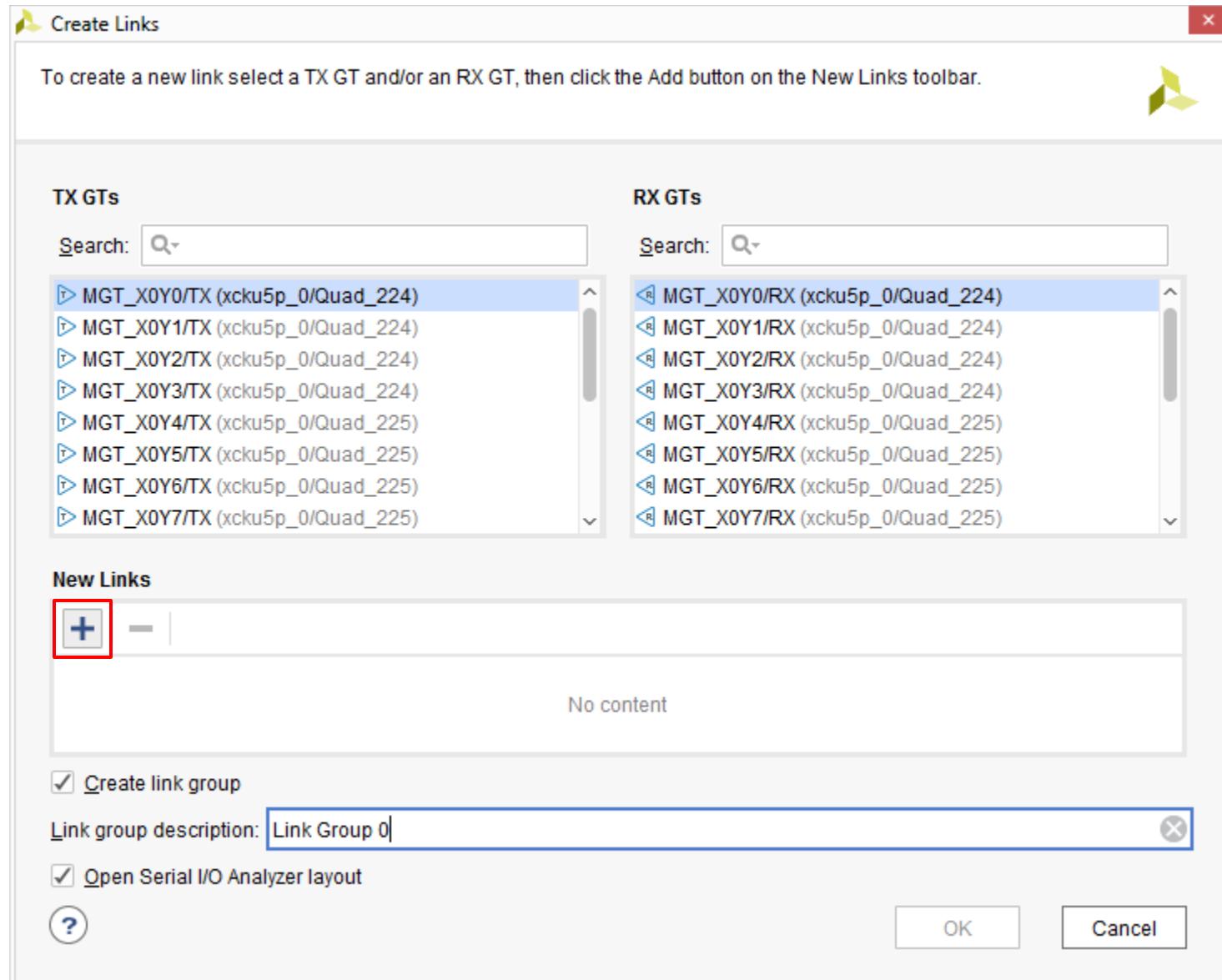


Note: Si5328 clock must be set as per XTP464

XILINX

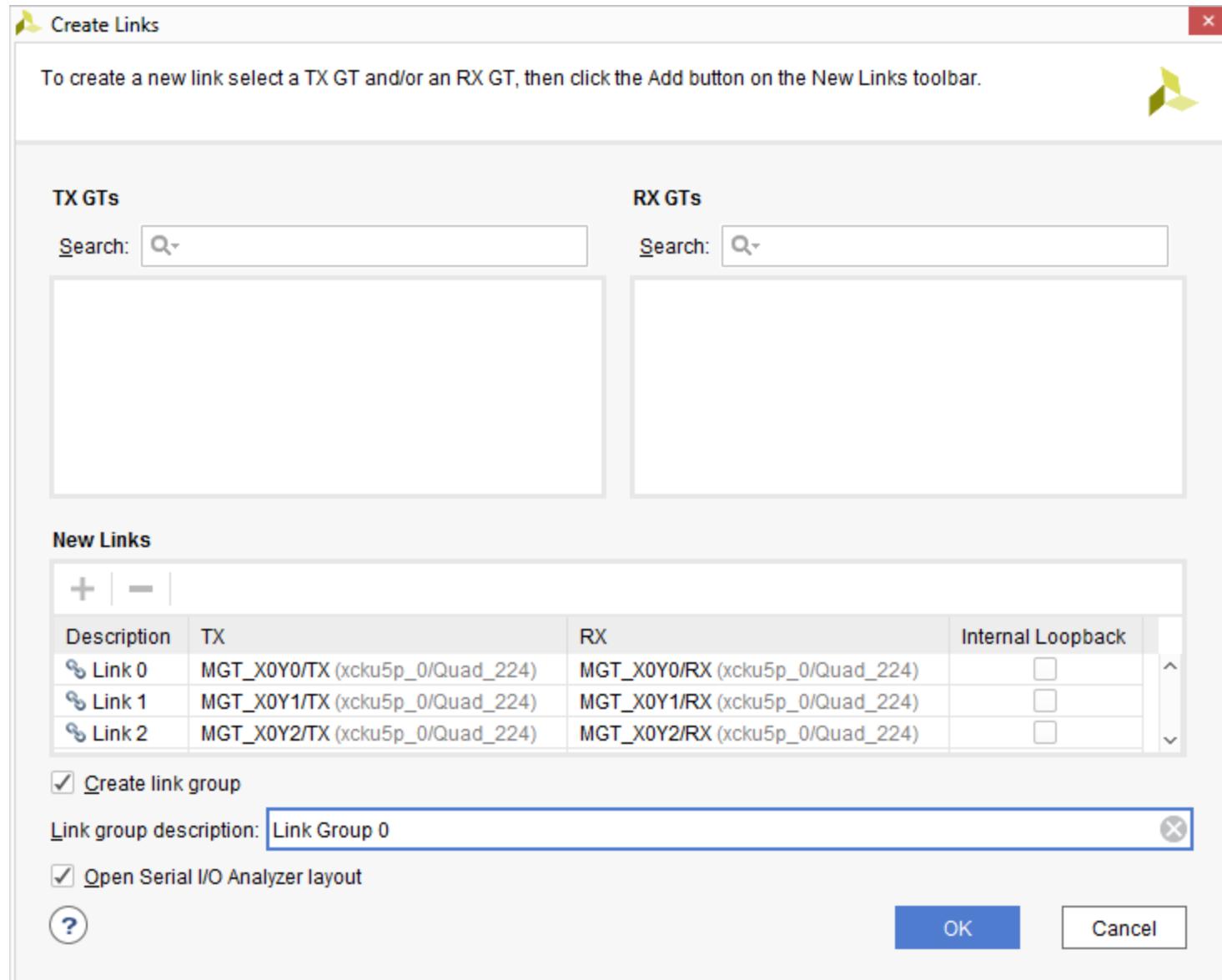
Run IBERT Example Design

- > Click on the Add Link button



Run IBERT Example Design

- > Add all the links and click OK



Run IBERT Example Design

> The links appear under the Serial I/O Links tab

The screenshot shows the Vivado 2018.2 Hardware Manager interface. The title bar indicates the project is "ibert_bank_all_ex" and the bitstream has been completed ("write_bitstream Complete"). The menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, Help, and Quick Access. The toolbar contains icons for file operations like Open, Save, and Run. A dashboard section is visible. The main window is titled "HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210308A3C320". On the left, a "Flow Navigator" pane is partially visible. The central area features a table titled "Serial I/O Links". The table has columns: Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, and RX Pattern. It lists 16 links under "Link Group 0": Link 0 to Link 15. Each link entry includes a "Reset" button. The "TX" and "RX" columns show MGT_X0Yx/TX and MGT_X0Yx/RX respectively. The "Status" column shows various speeds: 8.000 Gbps, 8.013 Gbps, 8.000 Gbps, etc. The "Bits" column shows values like 8.187E11. The "Errors" column shows error counts like 2.38E2. The "BER" column shows BER values like 2.907E-6. The "TX Pattern" and "RX Pattern" columns both show "PRBS 7-bit".

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
Link Group 0 (16)							Reset	PRBS 7-bit	PRBS 7-bit
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	8.000 Gbps	8.187E11	2.38E2	2.907E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	8.000 Gbps	8.187E11	2.34E2	2.858E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	8.013 Gbps	8.187E11	2.37E2	2.895E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	8.187E11	1.94E2	2.37E-10	Reset	PRBS 7-bit	PRBS 7-bit
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	8.000 Gbps	8.187E11	2.36E2	2.882E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	7.990 Gbps	8.188E11	2.04E2	2.492E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	8.010 Gbps	8.188E11	2.37E2	2.894E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	7.991 Gbps	8.188E11	1.96E2	2.394E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 8	MGT_X0Y8/TX	MGT_X0Y8/RX	28.070 Gbps	2.879E12	1.695E7	5.89E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 9	MGT_X0Y9/TX	MGT_X0Y9/RX	28.128 Gbps	2.879E12	1.141E7	3.963E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 10	MGT_X0Y10/TX	MGT_X0Y10/RX	28.150 Gbps	2.879E12	7.696E6	2.673E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 11	MGT_X0Y11/TX	MGT_X0Y11/RX	28.125 Gbps	2.879E12	4.495E6	1.561E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 12	MGT_X0Y12/TX	MGT_X0Y12/RX	28.128 Gbps	2.879E12	1.557E7	5.41E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 13	MGT_X0Y13/TX	MGT_X0Y13/RX	28.125 Gbps	2.879E12	7.011E6	2.435E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 14	MGT_X0Y14/TX	MGT_X0Y14/RX	28.125 Gbps	2.879E12	1.209E7	4.2E-6	Reset	PRBS 7-bit	PRBS 7-bit
Link 15	MGT_X0Y15/TX	MGT_X0Y15/RX	28.125 Gbps	2.879E12	1.526E7	5.299E-6	Reset	PRBS 7-bit	PRBS 7-bit

Run IBERT Example Design

- > Set all TX and RX Patterns to PRBS 31-bit

Screenshot of Vivado 2018.3 Hardware Manager showing the Serial I/O Links configuration for an IBERT example design.

The window title is "ibert_bank_all_ex - [c:/kcu116_ibert/ibert_bank_all/ibert_bank_all_ex/ibert_bank_all_ex.xpr] - Vivado 2018.3".

The "Serial I/O Analyzer" tab is selected in the top right.

The "Hardware Manager" pane shows the "Serial I/O Links" tab. The table lists 16 links under "Link Group 0".

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
Link Group 0 (16)								PRBS 7-bit	PRBS 7-bit
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	8.001 Gbps	1.047E13	1.734E10	1.657E-3	Reset	PRBS 7-bit	PRBS 7-bit
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	8.000 Gbps	1.047E13	1.734E10	1.657E-3	Reset	PRBS 9-bit	PRBS 7-bit
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	8.000 Gbps	1.047E13	1.731E10	1.654E-3	Reset	PRBS 15-bit	PRBS 7-bit
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	7.998 Gbps	1.047E13	1.731E10	1.654E-3	Reset	PRBS 23-bit	PRBS 7-bit
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	8.000 Gbps	1.047E13	1.73E10	1.653E-3	Reset	PRBS 7-bit	PRBS 7-bit
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	7.993 Gbps	1.047E13	1.73E10	1.653E-3	Reset	Fast Clk	PRBS 7-bit
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	7.991 Gbps	1.047E13	1.729E10	1.652E-3	Reset	Slow Clk	PRBS 7-bit
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	1.047E13	1.729E10	1.652E-3	Reset	PRBS 7-bit	PRBS 7-bit
Link 8	MGT_X0Y8/TX	MGT_X0Y8/RX	28.125 Gbps	3.68E13	2.267E11	6.161E-3	Reset	PRBS 7-bit	PRBS 7-bit
Link 9	MGT_X0Y9/TX	MGT_X0Y9/RX	28.095 Gbps	3.68E13	5.196E11	1.412E-2	Reset	PRBS 7-bit	PRBS 7-bit
Link 10	MGT_X0Y10/TX	MGT_X0Y10/RX	28.125 Gbps	3.68E13	5.157E11	1.401E-2	Reset	PRBS 7-bit	PRBS 7-bit
Link 11	MGT_X0Y11/TX	MGT_X0Y11/RX	28.127 Gbps	3.68E13	5.245E11	1.425E-2	Reset	PRBS 7-bit	PRBS 7-bit
Link 12	MGT_X0Y12/TX	MGT_X0Y12/RX	28.125 Gbps	3.68E13	3.086E11	8.388E-3	Reset	PRBS 7-bit	PRBS 7-bit
Link 13	MGT_X0Y13/TX	MGT_X0Y13/RX	28.125 Gbps	3.68E13	3.181E11	8.645E-3	Reset	PRBS 7-bit	PRBS 7-bit
Link 14	MGT_X0Y14/TX	MGT_X0Y14/RX	28.125 Gbps	3.68E13	2.583E11	7.02E-3	Reset	PRBS 7-bit	PRBS 7-bit
Link 15	MGT_X0Y15/TX	MGT_X0Y15/RX	28.125 Gbps	3.68E13	2.381E11	6.469E-3	Reset	PRBS 7-bit	PRBS 7-bit

The "TX Pattern" column for Link 15 is currently set to "PRBS 7-bit". A dropdown menu is open over this cell, showing the option "PRBS 31-bit" highlighted.

Run IBERT Example Design

> Set TX/RX Patterns to PRBS 9-bit for Links 8-11 (zSFP)

Screenshot of Vivado 2018.3 Hardware Manager showing Serial I/O Links configuration.

The TX Pattern column for links 8-11 has been set to PRBS 9-bit, highlighted by a red box.

TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset
Multiple	Multiple	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 9-bit	PRBS 9-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 9-bit	PRBS 9-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 9-bit	PRBS 9-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 9-bit	PRBS 9-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset

Run IBERT Example Design

> Set TX/RX Patterns to PRBS 15-bit for Links 12-15 (FMC)

Screenshot of Vivado 2018.3 Hardware Manager showing the Serial I/O Links configuration table.

The table lists 16 serial I/O links, each with the following columns:

TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset
Multiple	Multiple	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 9-bit	PRBS 9-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 9-bit	PRBS 9-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 9-bit	PRBS 9-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 15-bit	PRBS 15-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 15-bit	PRBS 15-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 15-bit	PRBS 15-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset
PRBS 15-bit	PRBS 15-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	<input checked="" type="checkbox"/>	Inject	Reset

The last four rows, corresponding to Links 12-15, have their TX Pattern and RX Pattern set to PRBS 15-bit, and are highlighted with a red border.

Run IBERT Example Design

- > Set TX Pre to 3.74 dB and TX Post to 0.45 dB for Links 8-15

Screenshot of Vivado 2018.3 Hardware Manager showing Serial I/O Links configuration.

The table displays settings for 16 Serial I/O Links. The columns represent:

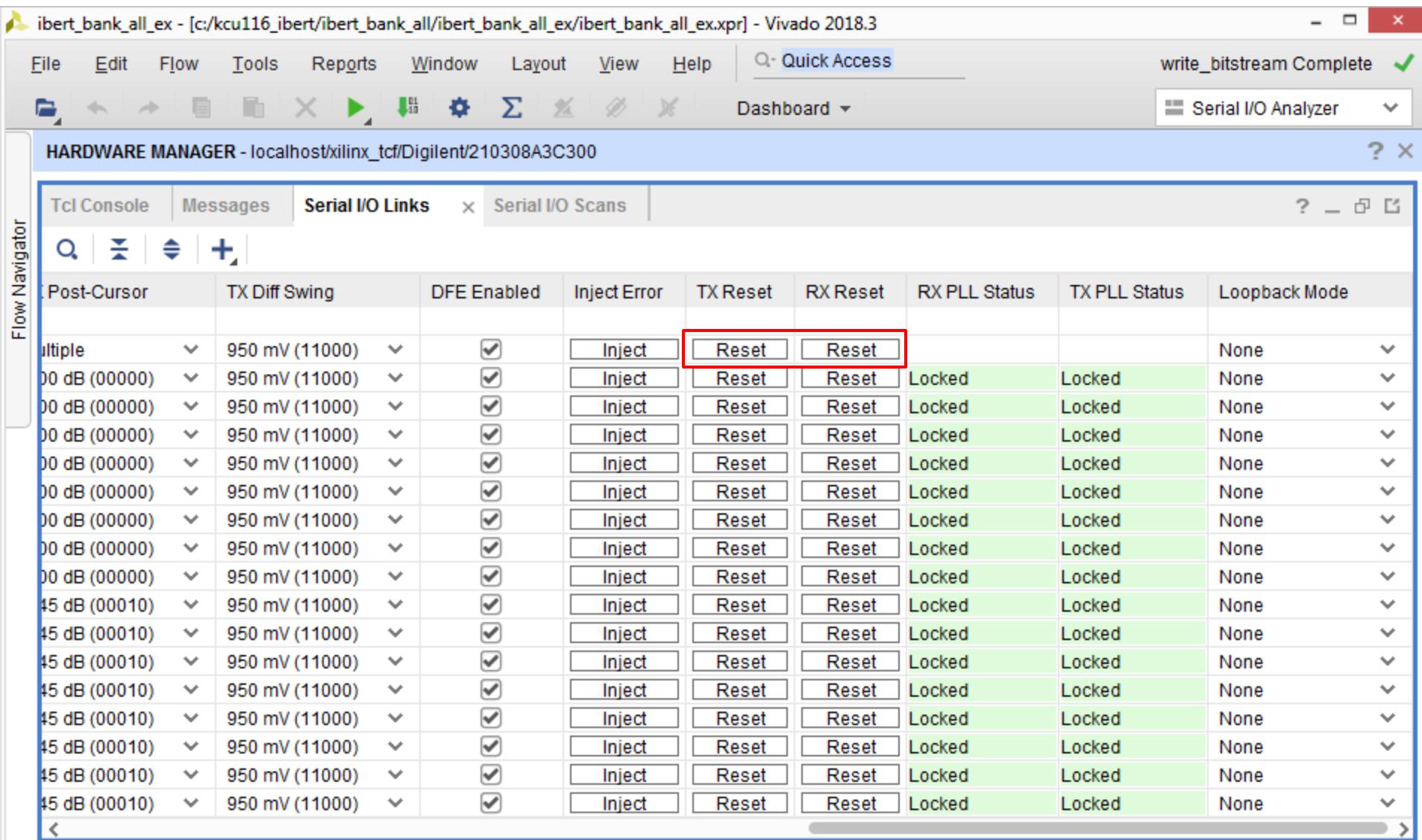
- TX Pattern
- RX Pattern
- TX Pre-Cursor
- TX Post-Cursor
- TX Diff Swing
- DFE Enabled
- Inject Error
- TX Reset

The TX Pre-Cursor and TX Post-Cursor values for Links 8-15 are highlighted with a red border:

Link	TX Pre-Cursor	TX Post-Cursor
8	3.74 dB (01110)	0.45 dB (00010)
9	3.74 dB (01110)	0.45 dB (00010)
10	3.74 dB (01110)	0.45 dB (00010)
11	3.74 dB (01110)	0.45 dB (00010)
12	3.74 dB (01110)	0.45 dB (00010)
13	3.74 dB (01110)	0.45 dB (00010)
14	3.74 dB (01110)	0.45 dB (00010)
15	3.74 dB (01110)	0.45 dB (00010)
16	3.74 dB (01110)	0.45 dB (00010)

Run IBERT Example Design

› Click TX Reset, followed by RX Reset



Run IBERT Example Design

- > Click the BERT Reset button to reset the link error counts

Screenshot of Vivado 2018.3 Hardware Manager showing Serial I/O Links for the ibert_bank_all_ex design.

The "BERT Reset" column for Link 0 is highlighted with a red box.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
Link Group 0 (16)							Reset	Multiple	Multiple
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	8.000 Gbps	6.058E10	9.7E1	1.601E-9	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	8.000 Gbps	6.061E10	9.4E1	1.551E-9	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	8.000 Gbps	6.064E10	1.01E2	1.666E-9	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	6.066E10	9.9E1	1.632E-9	Reset	PRBS 31-bit	PRBS 31-bit
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	7.997 Gbps	6.071E10	8.6E1	1.417E-9	Reset	PRBS 31-bit	PRBS 31-bit
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	8.000 Gbps	6.074E10	9.7E1	1.597E-9	Reset	PRBS 31-bit	PRBS 31-bit
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	8.000 Gbps	6.075E10	9.6E1	1.58E-9	Reset	PRBS 31-bit	PRBS 31-bit
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	7.996 Gbps	6.077E10	9E1	1.481E-9	Reset	PRBS 31-bit	PRBS 31-bit
Link 8	MGT_X0Y8/TX	MGT_X0Y8/RX	28.125 Gbps	2.137E11	3.126E6	1.463E-5	Reset	PRBS 9-bit	PRBS 9-bit
Link 9	MGT_X0Y9/TX	MGT_X0Y9/RX	28.125 Gbps	2.137E11	3.635E6	1.7E-5	Reset	PRBS 9-bit	PRBS 9-bit
Link 10	MGT_X0Y10/TX	MGT_X0Y10/RX	28.125 Gbps	2.138E11	1.24E6	5.803E-6	Reset	PRBS 9-bit	PRBS 9-bit
Link 11	MGT_X0Y11/TX	MGT_X0Y11/RX	28.102 Gbps	2.142E11	2.371E6	1.107E-5	Reset	PRBS 9-bit	PRBS 9-bit
Link 12	MGT_X0Y12/TX	MGT_X0Y12/RX	28.125 Gbps	2.142E11	1.174E6	5.48E-6	Reset	PRBS 15-bit	PRBS 15-bit
Link 13	MGT_X0Y13/TX	MGT_X0Y13/RX	28.113 Gbps	2.142E11	1.241E6	5.793E-6	Reset	PRBS 15-bit	PRBS 15-bit
Link 14	MGT_X0Y14/TX	MGT_X0Y14/RX	28.123 Gbps	2.142E11	8.362E5	3.903E-6	Reset	PRBS 15-bit	PRBS 15-bit
Link 15	MGT_X0Y15/TX	MGT_X0Y15/RX	28.125 Gbps	2.143E11	2.037E6	9.507E-6	Reset	PRBS 15-bit	PRBS 15-bit

Run IBERT Example Design

- > All links are showing no errors

Screenshot of the Vivado 2018.3 Hardware Manager showing the Serial I/O Links tab.

The title bar shows: ibert_bank_all_ex - [c:/kcu116_ibert/ibert_bank_all/ibert_bank_all_ex/ibert_bank_all_ex.xpr] - Vivado 2018.3

The menu bar includes: File, Edit, Flow, Tools, Reports, Window, Layout, View, Help, Quick Access, write_bitstream Complete, and a checkmark icon.

The toolbar includes: File, Edit, Flow, Tools, Reports, Window, Layout, View, Help, Quick Access, Dashboard, and a Serial I/O Analyzer tab.

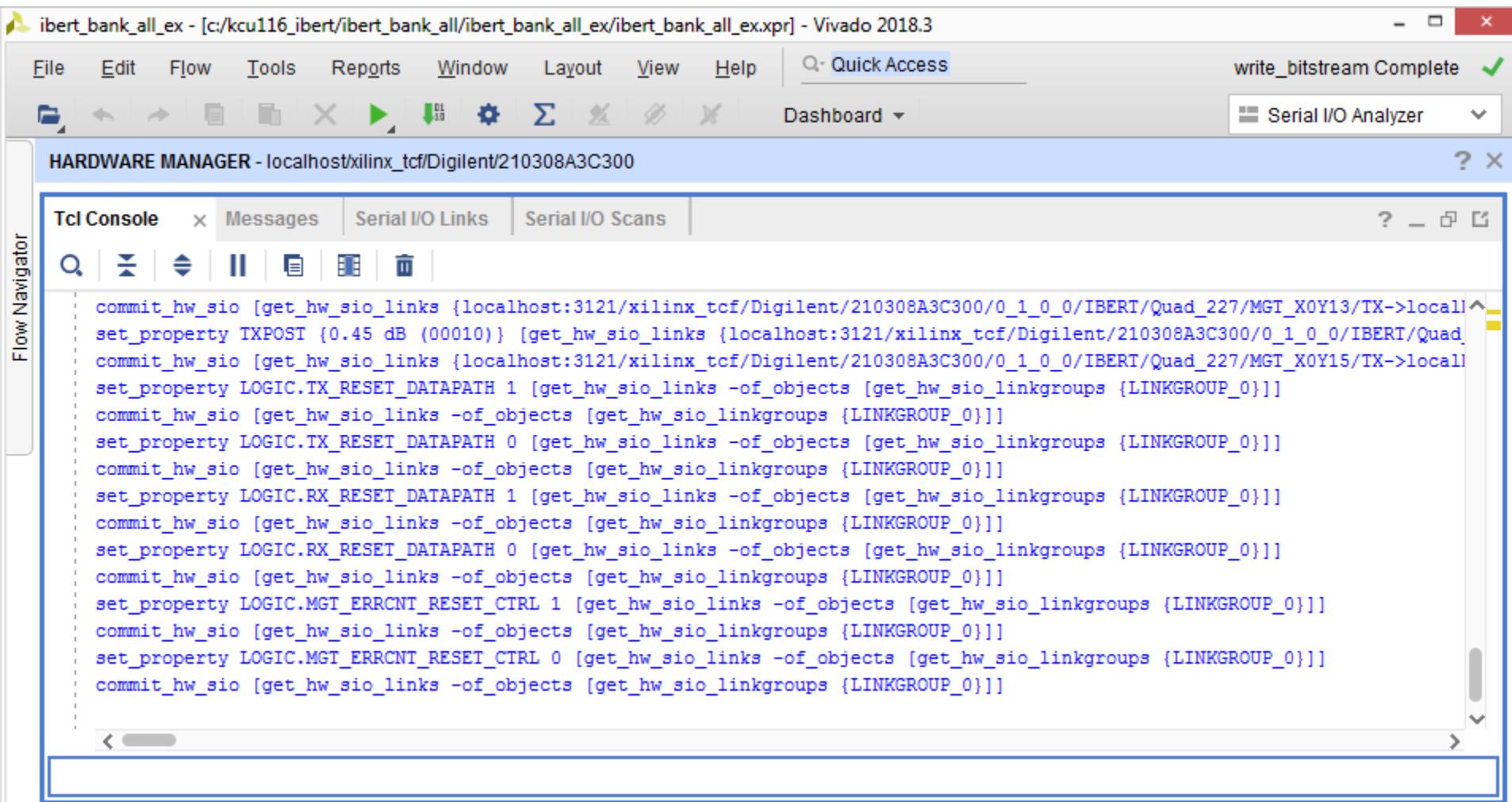
The main window displays the HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210308A3C300 interface.

The Serial I/O Links tab is selected, showing the following table:

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Patt
Ungrouped Links (0)									
Link Group 0 (16)							Reset	Multiple	Multiple
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	8.000 Gbps	1.214E13	0E0	8.236E-14	Reset	PRBS 31-bit	PRBS 3
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	8.000 Gbps	1.214E13	0E0	8.236E-14	Reset	PRBS 31-bit	PRBS 3
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	8.000 Gbps	1.214E13	0E0	8.236E-14	Reset	PRBS 31-bit	PRBS 3
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	1.214E13	0E0	8.236E-14	Reset	PRBS 31-bit	PRBS 3
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	7.999 Gbps	1.214E13	0E0	8.236E-14	Reset	PRBS 31-bit	PRBS 3
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	8.000 Gbps	1.214E13	0E0	8.236E-14	Reset	PRBS 31-bit	PRBS 3
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	7.991 Gbps	1.214E13	0E0	8.236E-14	Reset	PRBS 31-bit	PRBS 3
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	1.214E13	0E0	8.236E-14	Reset	PRBS 31-bit	PRBS 3
Link 8	MGT_X0Y8/TX	MGT_X0Y8/RX	28.125 Gbps	4.269E13	0E0	2.343E-14	Reset	PRBS 9-bit	PRBS 9
Link 9	MGT_X0Y9/TX	MGT_X0Y9/RX	28.113 Gbps	4.269E13	0E0	2.343E-14	Reset	PRBS 9-bit	PRBS 9
Link 10	MGT_X0Y10/TX	MGT_X0Y10/RX	28.135 Gbps	4.269E13	0E0	2.343E-14	Reset	PRBS 9-bit	PRBS 9
Link 11	MGT_X0Y11/TX	MGT_X0Y11/RX	28.125 Gbps	4.269E13	0E0	2.343E-14	Reset	PRBS 9-bit	PRBS 9
Link 12	MGT_X0Y12/TX	MGT_X0Y12/RX	28.125 Gbps	4.269E13	0E0	2.343E-14	Reset	PRBS 15-bit	PRBS 1
Link 13	MGT_X0Y13/TX	MGT_X0Y13/RX	28.089 Gbps	4.269E13	0E0	2.343E-14	Reset	PRBS 15-bit	PRBS 1
Link 14	MGT_X0Y14/TX	MGT_X0Y14/RX	28.125 Gbps	4.269E13	0E0	2.343E-14	Reset	PRBS 15-bit	PRBS 1
Link 15	MGT_X0Y15/TX	MGT_X0Y15/RX	28.125 Gbps	4.269E13	0E0	2.343E-14	Reset	PRBS 15-bit	PRBS 1

Run IBERT Example Design

- **Tcl console commands can be saved as TCL file for later playback**



References



References

> IBERT IP

- » LogiCORE IP Integrated Bit Error Ratio Tester for UltraScale GTY – PG196
 - https://www.xilinx.com/support/documentation/ip_documentation/ibert_ultrascale_gty/v1_3/pg196-ibert-ultrascale-gty.pdf

> Vivado Release Notes

- » Vivado Design Suite User Guide - Release Notes – UG973
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug973-vivado-release-notes-install-license.pdf
- » Vivado Design Suite 2019 - Vivado Known Issues
 - <https://www.xilinx.com/support/answers/72162.html>

> Vivado Programming and Debugging

- » Vivado Design Suite Programming and Debugging User Guide – UG908
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug908-vivado-programming-debugging.pdf

Documentation



Documentation

> Kintex UltraScale+

- » Kintex UltraScale+ FPGA Family
 - <https://www.xilinx.com/products/silicon-devices/fpga/kintex-ultrascale-plus.html>

> KCU116 Documentation

- » Kintex UltraScale FPGA KCU116 Evaluation Kit
 - <https://www.xilinx.com/products/boards-and-kits/ek-u1-kcu116-g.html>
- » KCU116 Board User Guide – UG1239
 - https://www.xilinx.com/support/documentation/boards_and_kits/kcu116/ug1239-kcu116-eval-bd.pdf
- » KCU116 Evaluation Kit Quick Start Guide User Guide – XTP471
 - https://www.xilinx.com/support/documentation/boards_and_kits/kcu116/xtp471-kcu116-quickstart.pdf
- » KCU116 - Known Issues Master Answer Record
 - <https://www.xilinx.com/support/answers/68360.html>