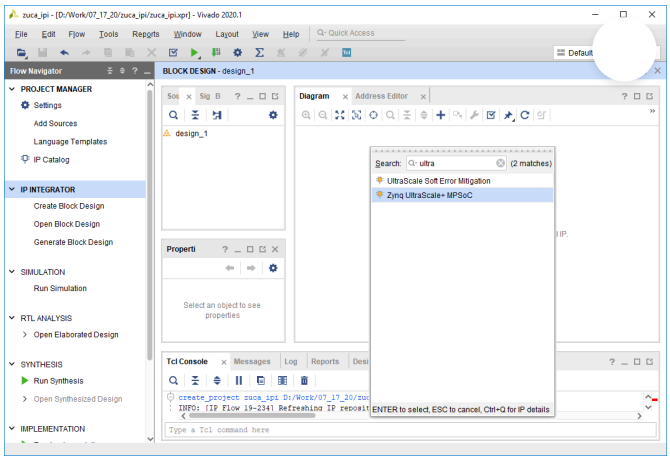
Add a Zynq UltraScale Processor to a Block Design

The Zynq UltraScale+ MPSoC IP represents the non-FPGA components of a Zynq UltraScale chip, referred to as the Processing System, or PS. It must be used in a block design that wants to connect anything to the processor, and to configure PS-side peripherals, clocks, and other settings.

Note: *This section only applies to boards with a Zynq UltraScale+ chip.*

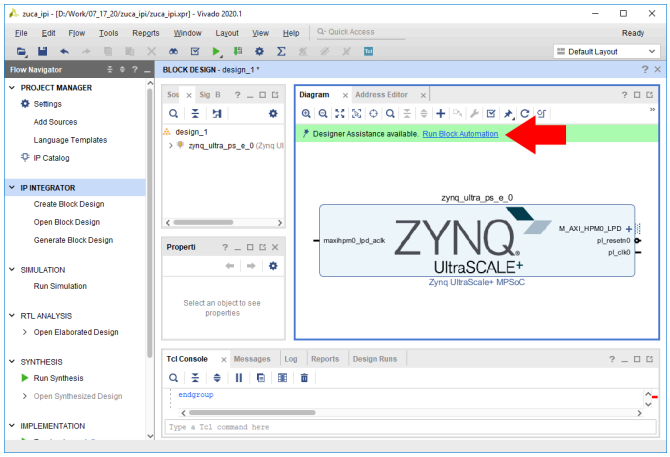
In the block diagram pane's toolbar, click the **Add IP** button (➕).

In the pop up, search for and double click on **Zynq UltraScale+ MPSoC**.



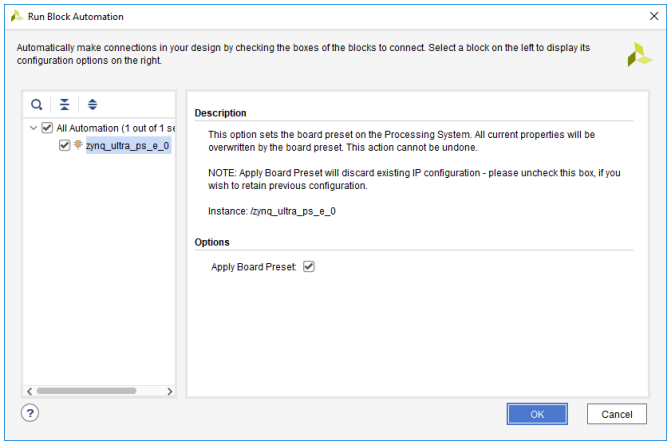
(https://digilent.com/reference/_detail/learn/programmable-logic/tutorials/2020.1/add-ultrascale-zynq-processor/add-zynq-ultra.png?id=programmable-logic%3Aguides%3Avivado-add-zynq-ultrascale)

Click **Run Block Automation** in the Design Assistance banner (the green bar).



(https://digilent.com/reference/_detail/learn/programmable-logic/tutorials/2020.1/add-ultrascale-zynq-processor/run-block-automation-1.png?id=programmable-logic%3Aguides%3Avivado-add-zynq-ultrascale)

In the dialog that pops up make sure *Apply Board Preset* is checked. This will apply the preset configuration from the board files to the IP, which saves a lot of time and prevents potential issues with doing the configuration entirely manually. Click **OK** to continue.



(https://digilent.com/reference/_detail/learn/programmable-logic/tutorials/2020.1/add-ultrascale-zynq-processor/run-block-automation-2.png?id=programmable-logic%3Aguides%3Avivado-add-zynq-ultrascale)

The needs of your project may require that you change some of the default settings of the PS. To edit its settings, double click on it to open the configuration wizard.

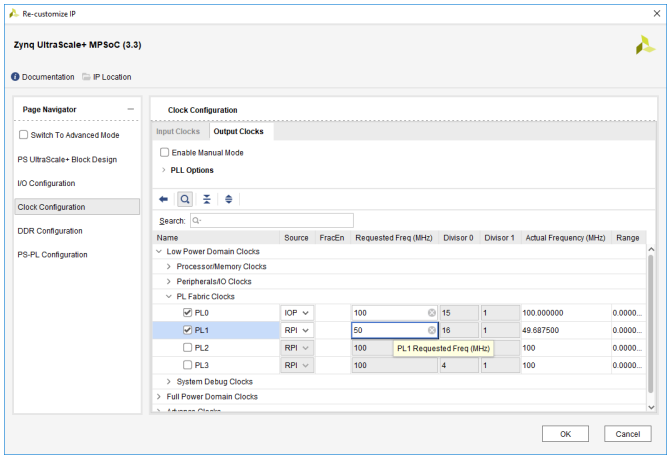
Two specific cases are highlighted below:

The PS can generate multiple clocks that are then provided to the FPGA fabric. These clocks are referred to as PL clocks, and can be found in the **Clock Configuration** tab of the MPSoC configuration wizard. They are located under the *Low Power Domain Clocks → PL Fabric Clocks* dropdowns. They can be enabled (or disabled) with a checkbox, the hardware source used to drive the clock can be changed, and the frequency can be modified.

Board files for Digilent Zynq UltraScale boards enable at least one low power domain PL clock by default, which is intended to be used with peripherals connected to the MPSoC's M_AXI_HPM0_LPD port.

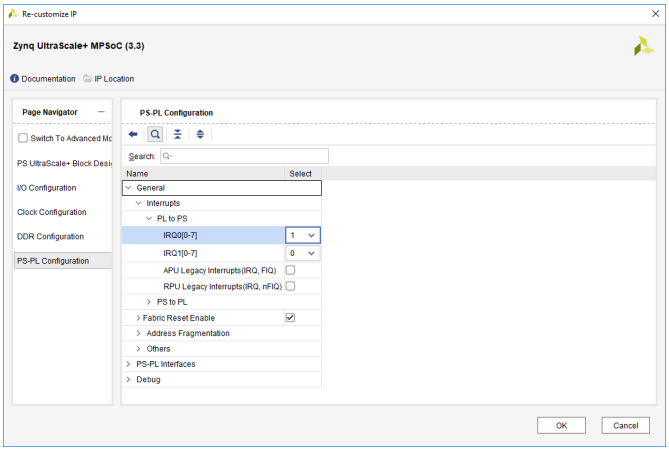
Some designs may require additional clocks of specific frequencies be added to your design. In these cases, enable a second clock and specify the needed frequency, as seen in the image to the right.

Note: *This section can always be returned to later, as the addition of an additional clock can be performed any time before the hardware is built.*



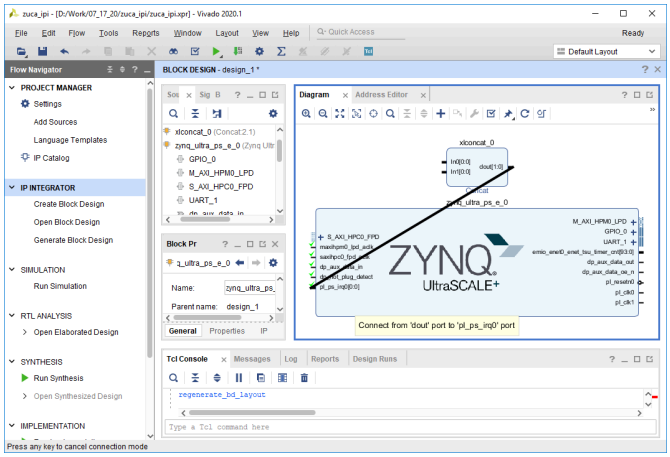
(https://digilent.com/reference/_detail/learn/programmable-logic/tutorials/2020.1/add-ultrascale-zynq-processor/add-additional-clock.png?id=programmable-logic%3Aguides%3Avivado-add-zynq-ultrascale)

UltraScale devices can also use interrupts generated in FPGA fabric to trigger interrupts within the Processing System. Interrupt-related settings can be changed within the configuration wizard's **PS-PL Configuration** tab. These interrupts can use the IRQ0 port, which can be found under the *General → Interrupts → PL to PS* dropdowns. To enable this port, the IRQ0 dropdown should be set to “1”.



(https://digilent.com/reference/_detail/learn/programmable-logic/tutorials/2020.1/add-ultrascale-zynq-processor/add-interrupt.png?id=programmable-logic%3Aguides%3Avivado-add-zynq-ultrascale)

While interrupts can be directly connected to the pl_ps_irq0 (IRQ0) port by clicking and dragging from one port to another, some designs may require multiple interrupt sources. In these cases, add a **Concat** IP to your block design, and manually connect it to the pl_ps_irq0 port. Additional input ports can be added to a Concat block through its configuration wizard (opened by double clicking on the IP).



(https://digilent.com/reference/_detail/learn/programmable-logic/tutorials/2020.1/add-ultrascale-zynq-processor/add-interrupt-concat.png?id=programmable-logic%3Aguides%3Avivado-add-zynq-ultrascale)

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