There are four seven-segment LED displays on the prototyping board. To save the number of FPGA chip's 110 pins, a time-multiplexing scheme is used. The block diagram of the time-multiplexing module, dispaux, is shown in Figure 3.7(a). The inputs are inO, inl, in2, and in3, which correspond to four 8-bit seven-segment LED patterns, and the outputs are an, which is a 4-bit signal that enables the four displays individually, and seg, which is the shared 8-bit signal that controls the eight LED segments. The circuit generates a properly timed enable signal and routes the four input patterns to the output alternatively. The design of this module is discussed in Chapter 4. For now, we just treat it as a black box that takes four seven-segment LED patterns, and instantiates it in the code. Testing circuit We use a simple 8-bit increment circuit to verify operation of the decoder. The sketch is shown in Figure 3.7(b). The sw input is the 8-bit switch of the prototyping board. It is fed to an incrementer to obtain sw+l. The original and incremented sw signals are then passed to four decoders to display the four hexadecimal digits on seven-segment LED displays.