HDL Example: Magnetars and Topological Qubits

For HDL (using **Verilog**), you could model a qubit's state as a finite state machine (FSM):

```
module topological_qubit (
    input wire clk,
    input wire reset,
    input wire entangle,
    output reg [1:0] state
);

    always @(posedge clk or posedge reset) begin
        if (reset)
            state <= 2'b00;  // Ground state
        else if (entangle)
            state <= 2'b11;  // Entangled state
        else
            state <= state;  // Hold current state
    end
endmodule
```