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SAN JOSE STATE UNIVERSITY

ELECTRICAL ENGINEERING DEPARTMENT

EE122 LAB MANUAL

SAN JOSE STATE UNIVERSITY

ELECTRICAL ENGINEERING DEPARTMENT

Getting started with the practical design fabrication and testing of analog circuits and systems

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Welcome to EE 122 Laboratory

Lab Attendance:

You are required to attend every lab meeting, for the full length of the lab meeting, unless you have a personal emergency. Midterms and work for example, are not considered emergencies. While it is true that many things can be done outside of the lab time, you need to work during the lab time, so that if you run into trouble the TA's can mentor you. If you leave early and then have questions that were covered in lab meetings, the TA's might not be able to help you in a timely manner. If you have a true emergency, contact the TA and you can get help during office hours. There is a grade for active participation that can be lowered significantly if you do not attend the lab meetings or leave early. Of course, if you have finished your work, you may leave.

Teams:

You need to work alone since the labs are online now. You can take help from others but cannot share the lab reports. The work should not plagiarize.

Preparing for lab is important:

Lab exercises from the heart of our EE program, and can be quite challenging to complete in a timely manner. There are many things that you can do to make sure that you are ready for the short time we are together in lab. Not only is time is limited in lab, access to the TA can be limited (There is a minimum of 16 students per TA.) Before every lab meeting gets under way, you will be expected to prove that you have prepared.

What can you do to plan for a successful lab experience?

Derive mathematical models for the circuit/systems that you are going to implement. Calculate how device tolerances will affect the performance or your circuit/system Show up to lab meetings on time with the proper mental and physical preparation to succeed. Discuss lab exercises with your fellow teammates before lab.

Learn/review concepts from previous courses that you need to complete the lab. Have a list of the materials you will need to conduct the exercise.

If required/possible, build circuit and measure DC operating points.

Answer quiz questions on Canvas.

There are some tools that every EE student has to know how to use properly to be a successful analog/system engineer:

Spice: There are many versions of spice but the one that will be supported in lab is LTspice from linear technology. LTspice is a fully functional spice program that is even used by Linear's competitors. It can be downloaded for free:

http://www.linear.com/designtools/software/#LTspice A getting started guide can be found here : http://ltspice.linear.com/software/LTspiceGettingStartedGuide.pdf

The user guide can be found here: http://ltspice.linear.com/software/scad3.pdf

Multi-meters (Fluke 45)

http://dl.dropbox.com/u/35091424/fluke_45_user_manual.pdf

Power Supply (Agilent E3631A)

http://dl.dropbox.com/u/35091424/E3631A_triple_output_power_supply_user_manual.pdf

Oscilloscope (Agilent 54621A)

http://dl.dropbox.com/u/35091424/54621A_oscilloscope_manual.pdf

PC Board Layout (Diptrace): In order to create a system that can be reliable used, or sold, it has to be implemented on a PCB. Diptrace has a free "lite" version capable of 500pins and two layers. The software can be downloaded and tutorials can be from:

http://www.diptrace.com/

PCB in box:

http://www.pcbfx.com/

Proto board Layout, board layout, Arduino Interface:

http://fritzing.org/

Chapter 1:
Introduction to Printed Circuit Board Design

Week 1

Introduction

This lab serves as an introduction to PCB design. There are a variety of EDA (Electronic Design Automation) software packages (such as Eagle, OrCAD). We will be using DipTrace for this lab.

Objective

The purpose of this lab is for students to become familiar with EDA software, the design and manufacturing of PCBs. Students will be implementing an Astable flip flop via schematics and then convert it into a PCB layout. This lab will be simulation only.

Pre-Lab

Read: http://en.wikipedia.org/wiki/Printed_circuit_board View: http://www.youtube.com/watch?v=bgBjub85TT4&feature=related View tutorial: http://www.diptrace.com/tour/

View: http://www.youtube.com/watch?v=EdExkuvGySE&NR=1

Tips

Resistors, Capacitors, Inductors are under the Spice tab. PMOSFET AND NMOSFET are under the spice tab. BJTS/MOSFETS are under the transistors tab.

LED's are under the discrete tab. Battery is under the Disc_Sch tab. Use R key to flip components.

Lab Exercise

- Create a layout for an astable flip flop as shown in the following tutorial, but create it using a single layer board:
  http://www.diptrace.com/books/tutorial.pdf or here.

- Print out the schematics and PCB board layout.

Post-Lab

- Design a 2-input NAND gate using 2 PMOS (your choice) transistors and 2 NMOS (your choice) transistors. Use a double layer board with through hole parts.

Questions to be answered in lab report

1. Discuss some of the advantages and disadvantages of PCBs.
2. What is design for manufacturability (DFM) for PCB's?
3. What is the difference between auto placement and auto routing? Is there a tradeoff when you do one or the other?
4. What is the point of having multiple layers on the PCB board?
5. What is the difference between surface mounted and through-hole mounted components?

Lab report:

For this assignment, turn in individual reports in electronic form (PDF only please) to Canvas containing:

- Screen grabs (Properly labeled) of the astable flip-flop (schematic and pcb layout) and the 2-input NAND (schematic and pcb layout) gate that show you have completed the tutorial and created your design. Only include the finished designs, do not include a picture of every step.
- Screen grabs of the “clean” ERC reports.
- Answers to the questions.
- Here is a link to a word template: Report Template

Chapter 2:
Introduction to Circuit Simulation (LTspice)

Week 2

Introduction

This lab serves as an introduction to an industry standard circuit simulation tool LTspice.

Objective

After successfully completing the work outlined in this lab, students should be able to use LTspice to perform virtual experiments, verify designs before fabrication, and explore circuit topologies rapidly. Students should also know when in the design flow to use a spice tool.

Pre-Lab

Download the software onto your computer. It is PC based but runs on Macs and linux OS's under wine.

Watch these videos on setting the environment for LTspice to create readable plots:

How to document your designs in LTspice PPT tutorial

How to document your designs in LTspice "Live"

If you do not like to watch videos, read these notes: How to document your designs in LTspice.

Read/Watch the following material http://www.linear.com/designtools/software/#LTspice

Read through the getting started guide can be found here : http://ltspice.linear.com/software/LTspiceGettingStartedGuide.pdf

Familiarize yourself with the user guide: http://ltspice.linear.com/software/scad3.pdf

Getting started with circuit simulation

Finding DC bias points:

Sometimes EE's want to calculate the DC bias points of a circuit before doing other analysis steps. It is helpful to know that one's circuit is at least correct at DC before applying a time varying signal. While it is true that for networks comprised of linear circuit elements one can mathematically solve for each node voltage and branch current, often EE's use non-linear elements when designing practical systems. Furthermore, it is an independent way to check one's math. This also works for building and testing ones analog circuit. Check the DC voltages at each node before trying to test the systems transient response.

Start LTspice and create a new schematic by clicking on the new schematic button as shown in Figure 1.

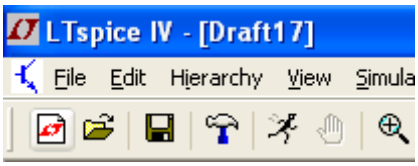

Figure 1: Creating a new schematic.

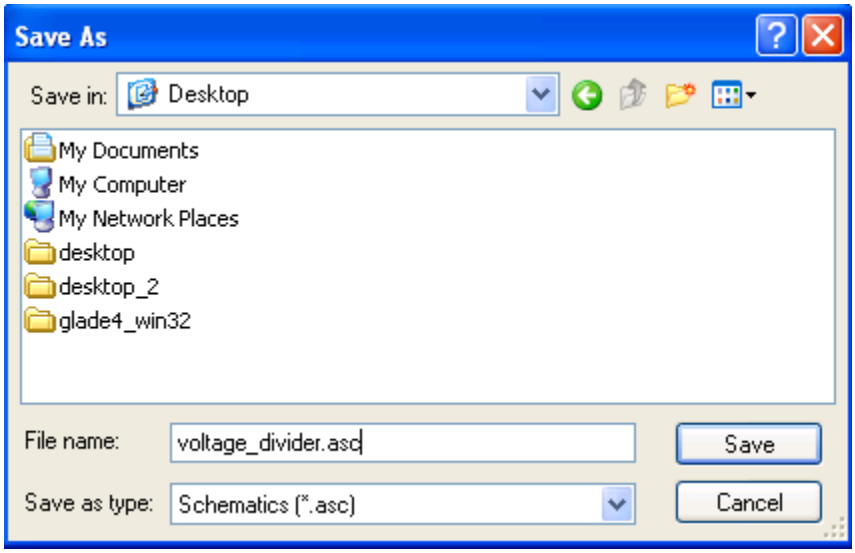

Figure 2: Saving a schematic.

Save the file by clicking on file…save as in Figure 2.

Place the voltage source, two resistors and grounds for a voltage divider circuit as shown in Figure 3. (See the getting started tutorial form Linear Tech if you need to know how to place parts: http://ltspice.linear.com/software/LTspiceGettingStartedGuide.pdf)

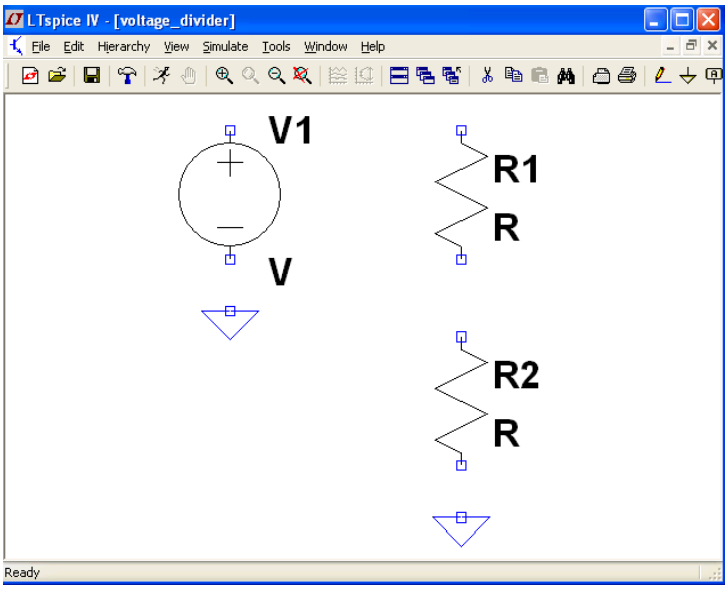

Figure 3: Place parts in a schematic.

Right click on the voltage source to change the DC voltage to 10V as in Figure 4.

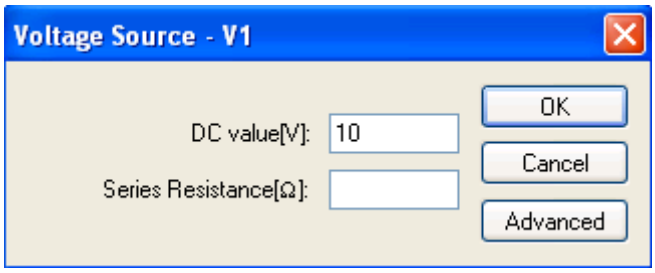

Figure 4: Change the DC voltage.

Follow the same procedure to change the resistances to 10k each (Figure 5).

Use the wire tool to connect the circuit as in Figure 6.

Add the net names as in Figure 7.

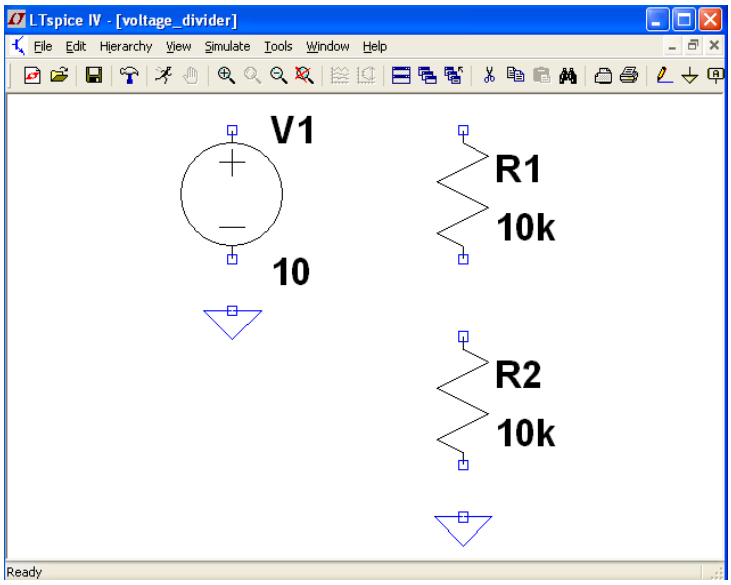

Figure 5: Setting Resistances in a schematic.

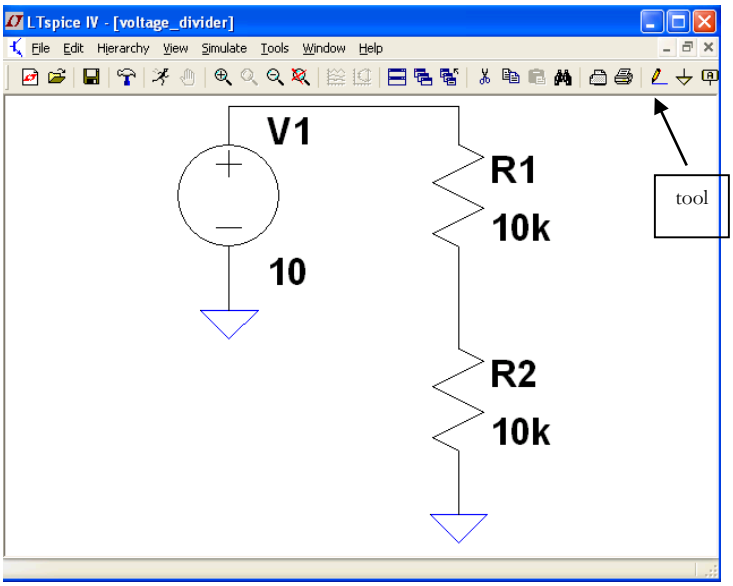

Figure 6: Adding wires to a schematic.

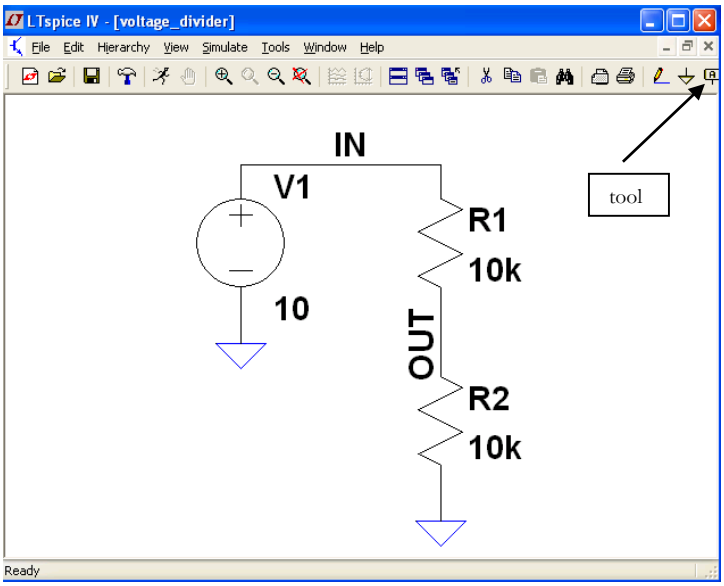

Figure 7: Adding net names to a schematic.

Add a .op simulation command to solve for the DC operating conditions by go to Simulation… Edit simulation command (Figure 8), clicking on the tab DC op pnt (Figure 9), clicking OK, and then placing on the schematic (Figure 10).

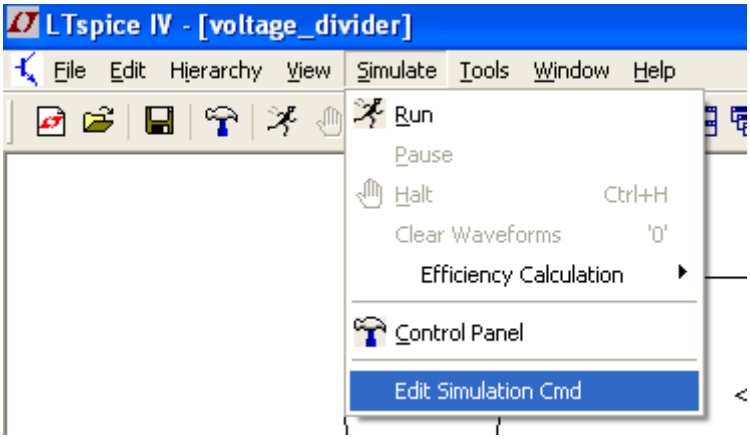

Figure 8: Edit Simulation command.

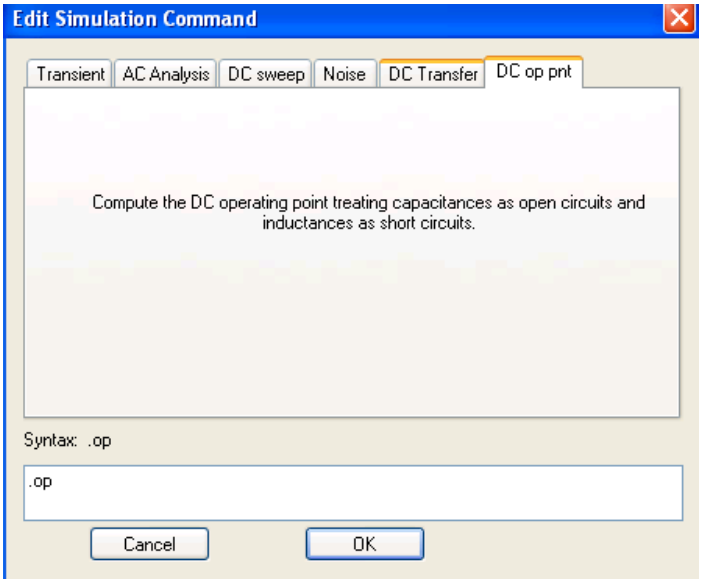

Figure 9: Choosing a .op simulation.

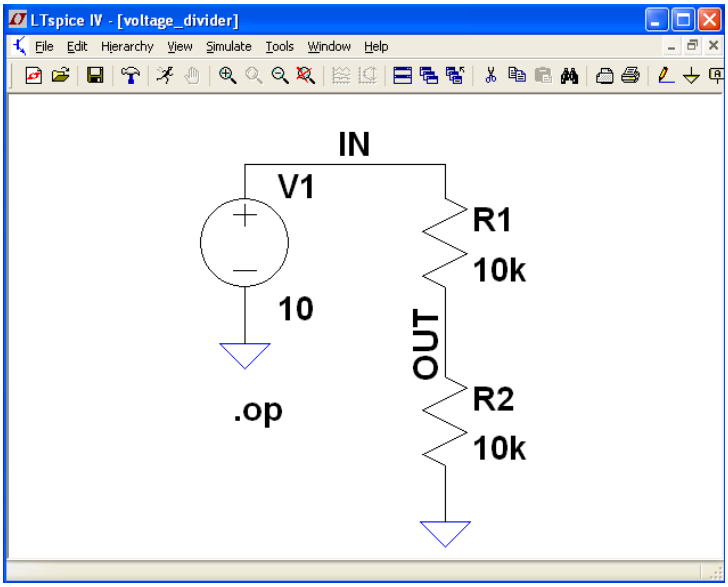

Figure 10: Schematic ready for simulation.

Run the simulation by clicking on the running figure in the toolbar. You should see the results as in Figure 11. Notice that the voltages and currents match the numerical voltages a "hand analysis" would have predicted. Notice also that the program did not produce an equation describing the relationship between the voltages and currents for any voltage or resistor combinations.

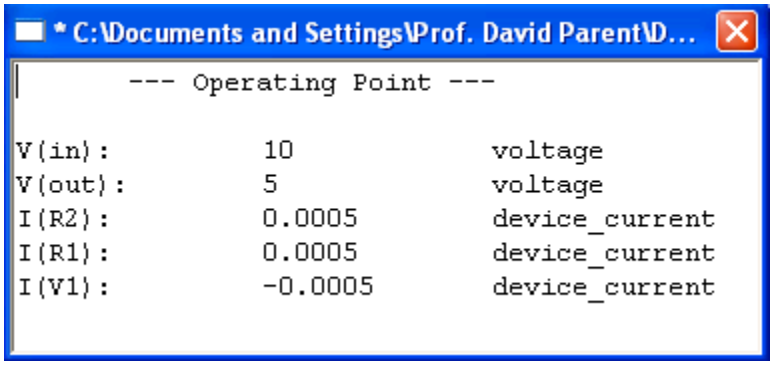

Figure 11: DC voltages and currents.

Stepping a device's value:

Sometimes EE's want to see how a system responds to a changing parameter. In spice, we can program a parameter to vary linearly or logarithmically.

To change a resistor's value to a variable, right click the R2 and change the value to {R2} as shown in Figure 12.

To vary the R2 value logarithmically add a spice directive: step dec param R2 1 100k (Figure 13).

Your schematic should look like Figure 14.

Run your simulation and you should get Figure 15.

Left click on the x-axis in the plot (around the 60K value) to change the x-axis to a logarithmic display. Fill out the pop-up as in Figure 16. Your figure should look like Figure 17.

Plot V(out) and I(R1). Your figure should look like Figure 18.

Figure 12: Changing a device's parameter to a variable.

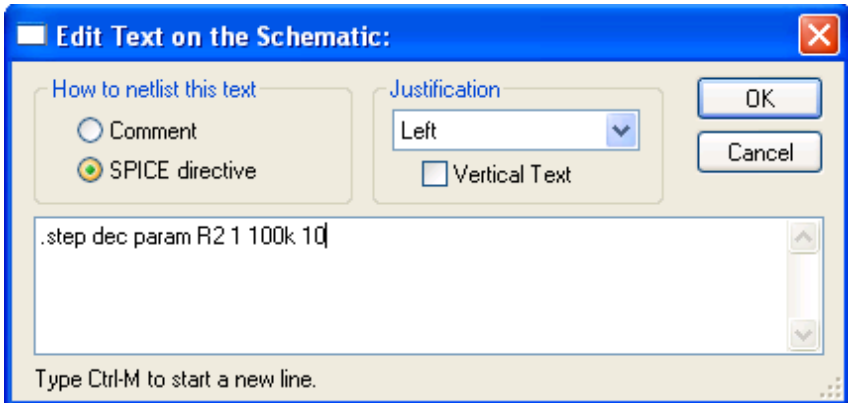

Figure 13: Stepping R2 logarithmically from 1 to 100k with 10 steps per decade.

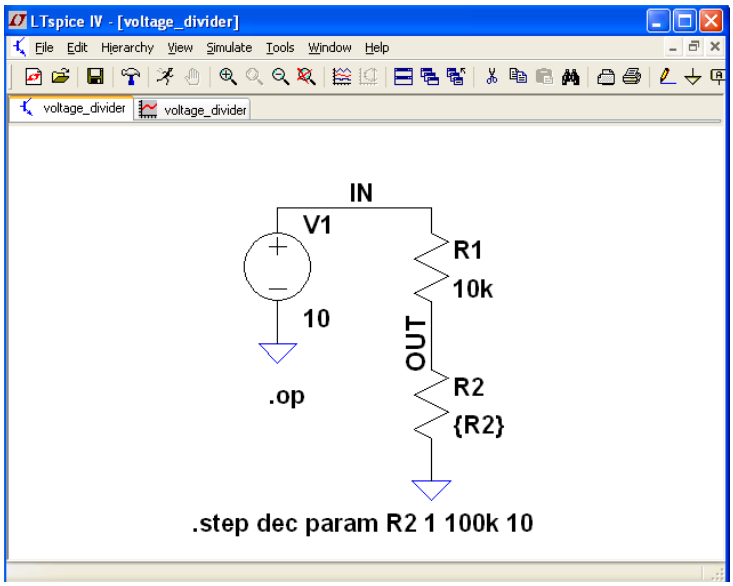

Figure 14: Schematic that shows stepping R2 logarithmically from 1 to 100k with 10 steps per decade.

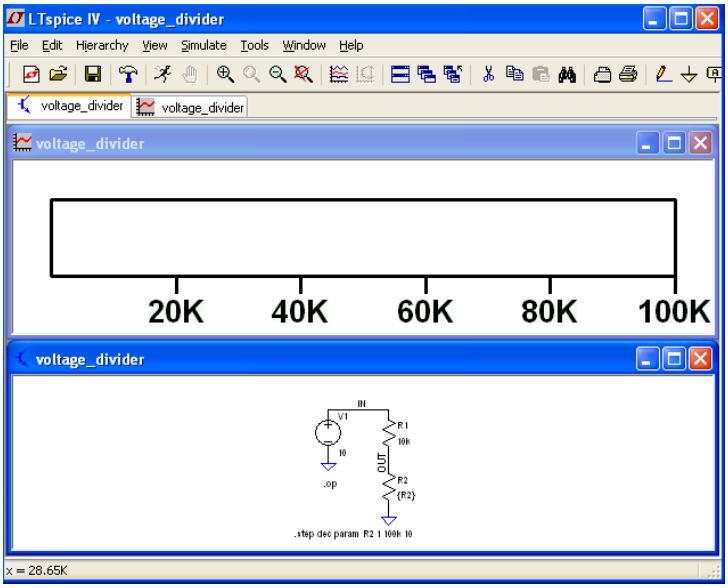

Figure 15: Plot window.

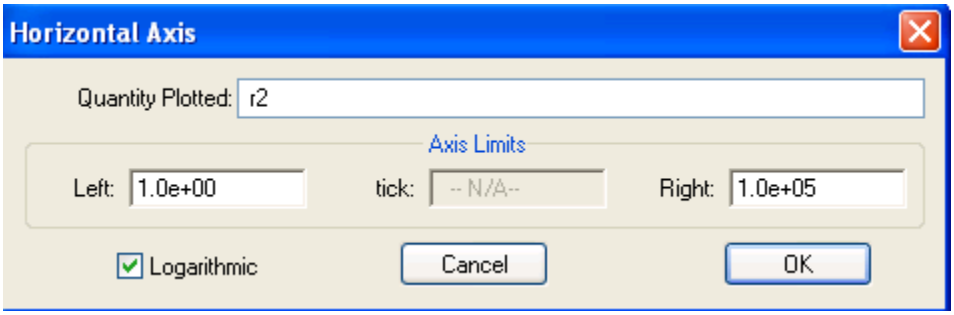

Figure 16: Change X axis to show logarithmic plotting of R2.

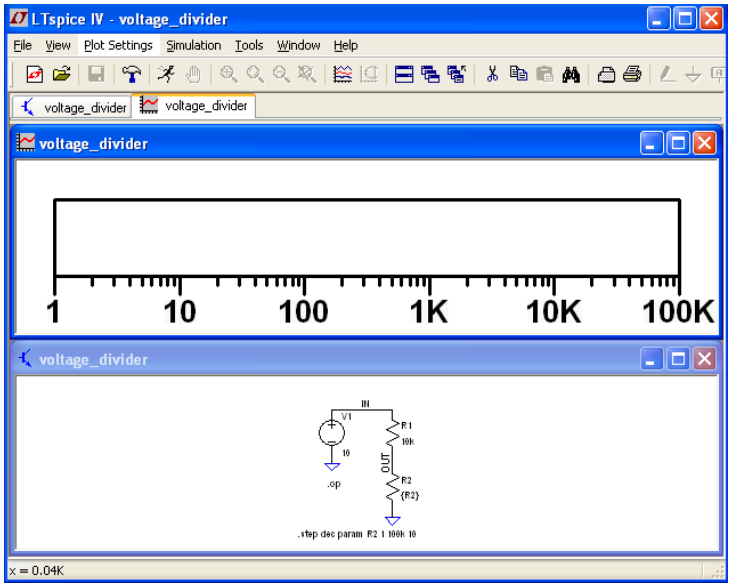

Figure 17: Results of changing X axis to show logarithmic plotting of R2.

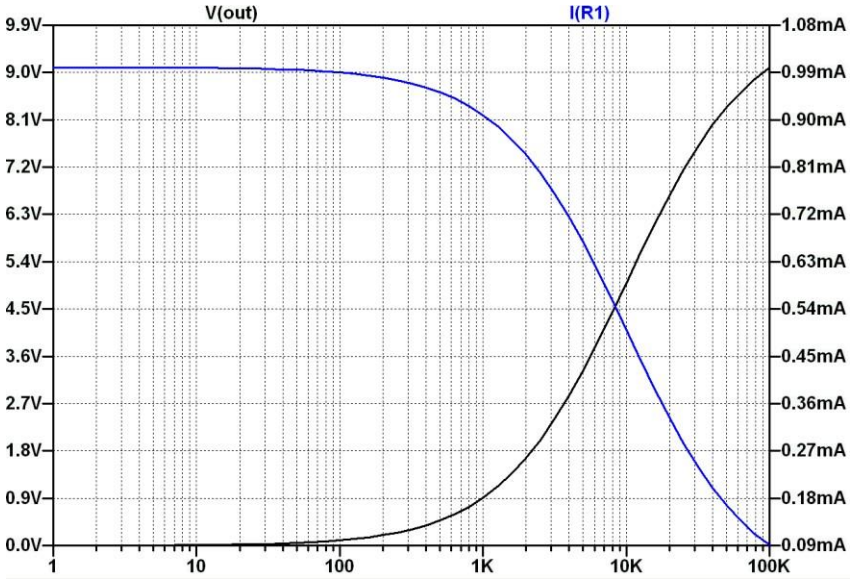

Figure 18: Results of changing R2.

Using a behavioral voltage source to check hand calculations against a spice simulation:

Sometimes EE's want to use a behavioral source to mimic an ideal device or check hand calculations. In this example you will add a behavioral voltage source that is the equations for

Vout in terms Vin, R1 and R2.

Add a behavioral voltage source BV to your schematic (Figure 19).

Right click on the behavioral voltage source and fill out the form as in (Figure 20), V={R2}*10/(10k+{R2}) .

Add a net name to the top of the behavioral voltage source called Check (Figure 21)

Run the simulation and plot V(out) and V(Check) (Figure 22). Note that they match perfectly.

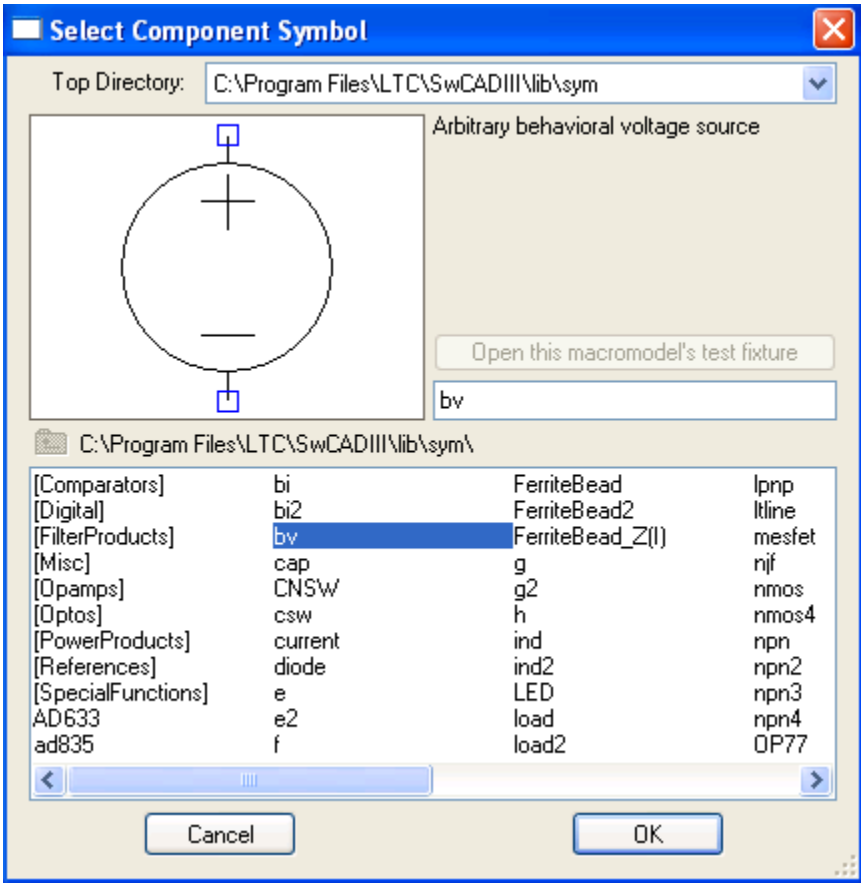

Figure 19: Adding a behavioral voltage source.

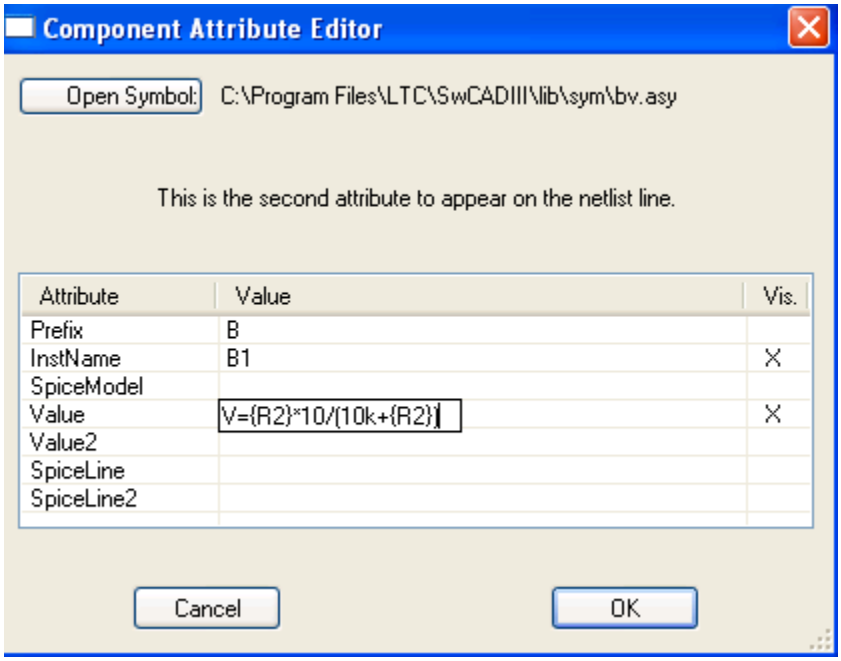

Figure 20: Adding the equation for Vout.

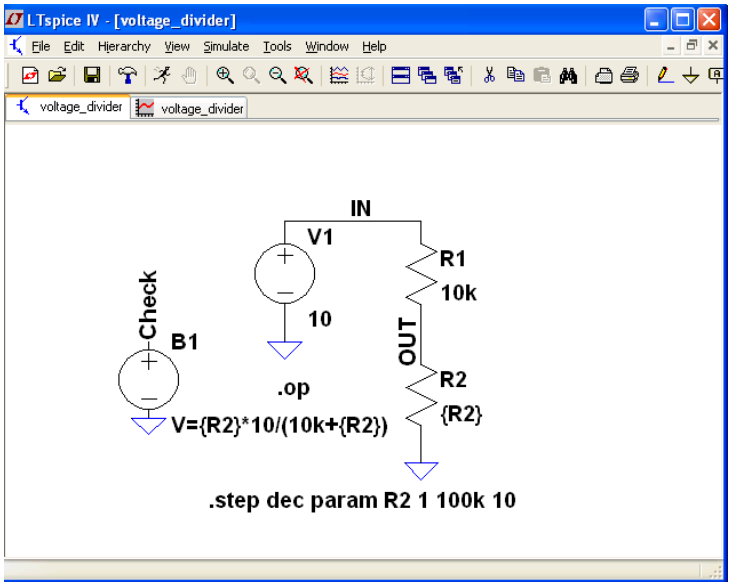

Figure 21: Completed Schematic.

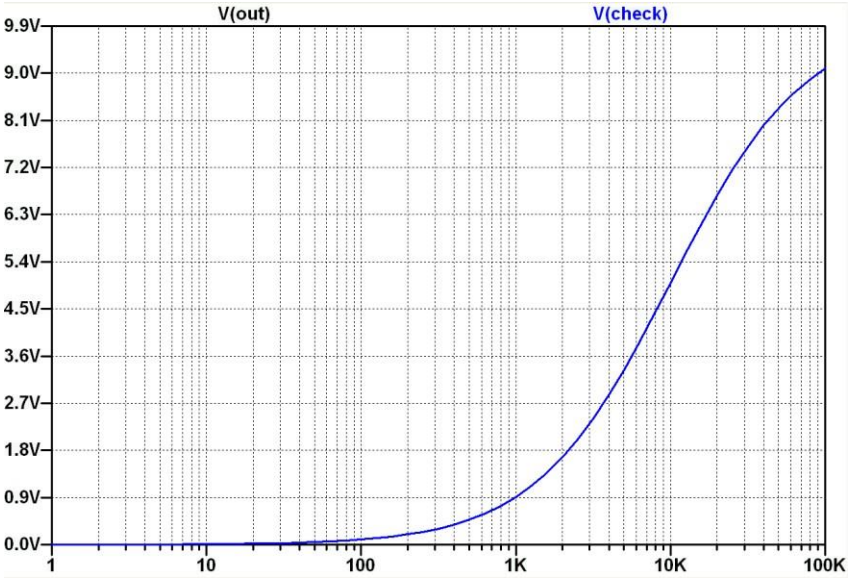

Figure 22: Vout and Vcheck match!

Using a spice to simulate frequency response of a system:

A frequency analysis of a circuit is quite easy to do in spice. To have a meaningful simulation, you will delete R1 and add a capacitor in its place.

To change the parameters of the voltage source, right click V1 and click on advanced in the pop-up (Figure 23).

Enter in 1 for AC voltage (Figure 24). This will make it so you can read the gain directly from Vout.

Change the spice directive for R2 to a list of R values 10k and 20k.

Change the simulation to AC (Figure 25).

Delete R1 and add a capacitor of 10uF. (Figure 26)

The completed schematic is shown in Figure 26, and V(out) in Db (assuming input of 1V) vs. frequency (Hz) Notice Vcheck and Vout do not match (Figure 27).

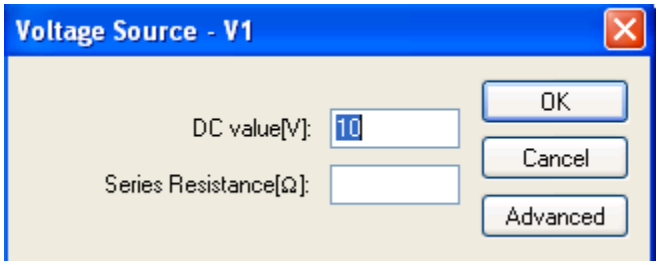

Figure 23: Editing a voltage sources advanced parameter.

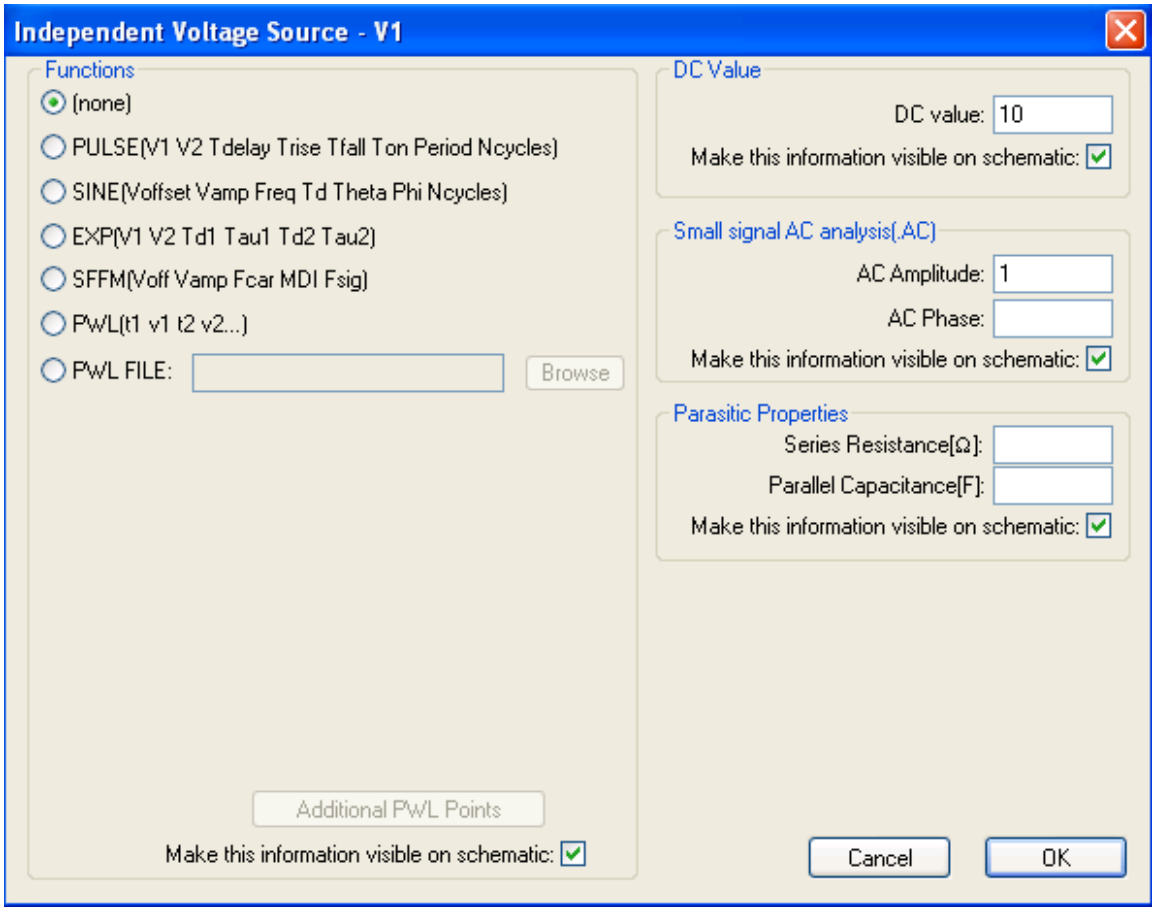

Figure 24: Adding an AC source of 1V.

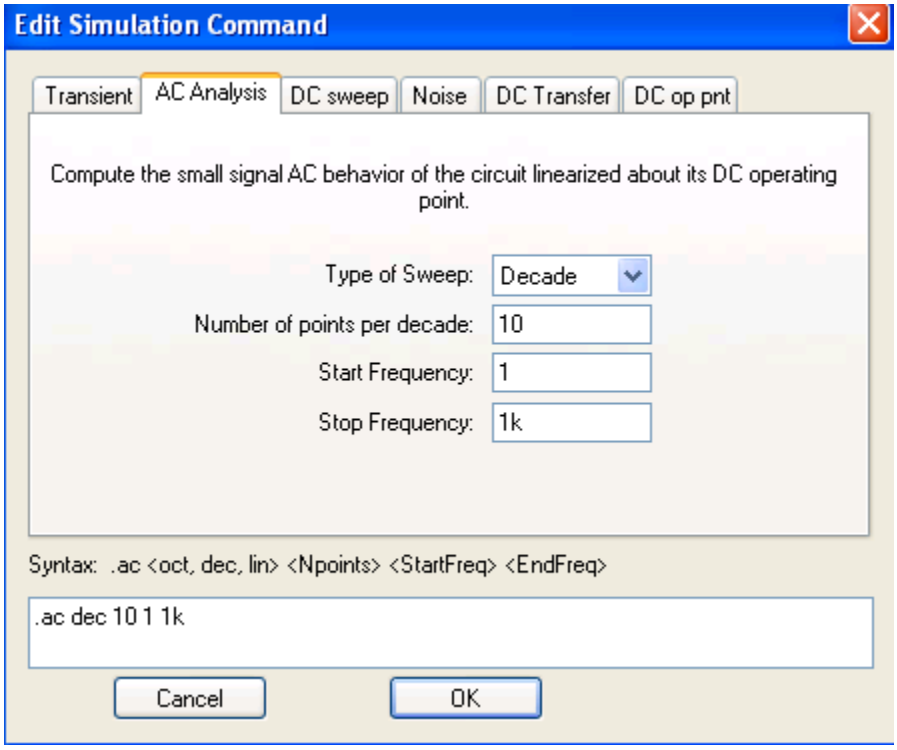

Figure 25: Changing the simulation to an AC analysis.

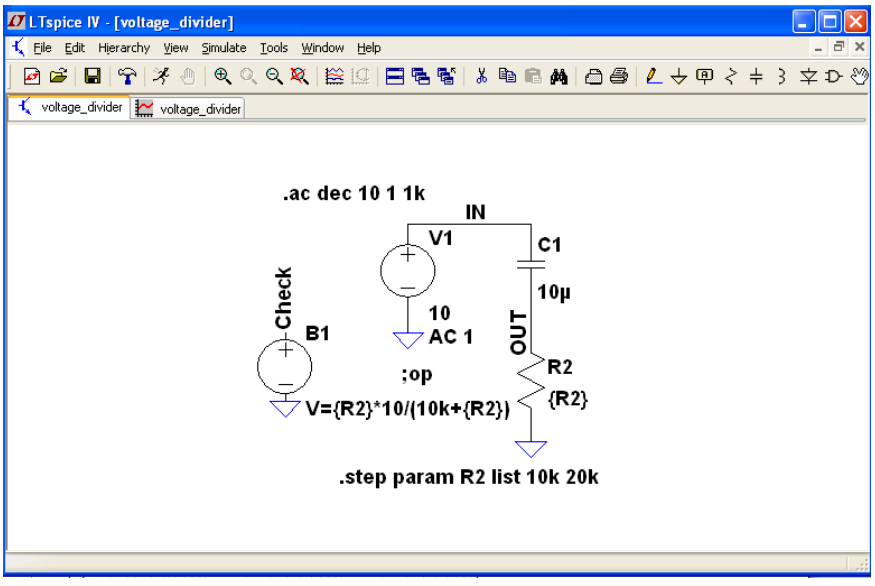

Figure 26: Completed Schematic.

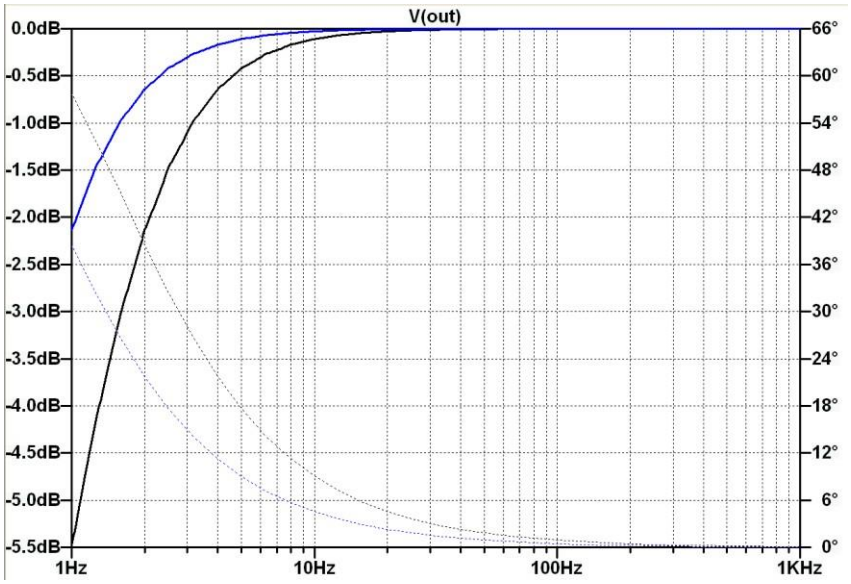

Figure 27: Bode Plot of High Pass Filter.

Using a spice to simulate frequency the time response of a system:

Change the voltage source to have a sin wave output of 1-volt amplitude, 1kHz frequency and 0 DC offset voltage (Figure 28).

Change the simulation to a transient simulation of 2ms (Figure 29).

The completed schematic is shown in Figure 30, and the simulation results are shown in Figure 31.

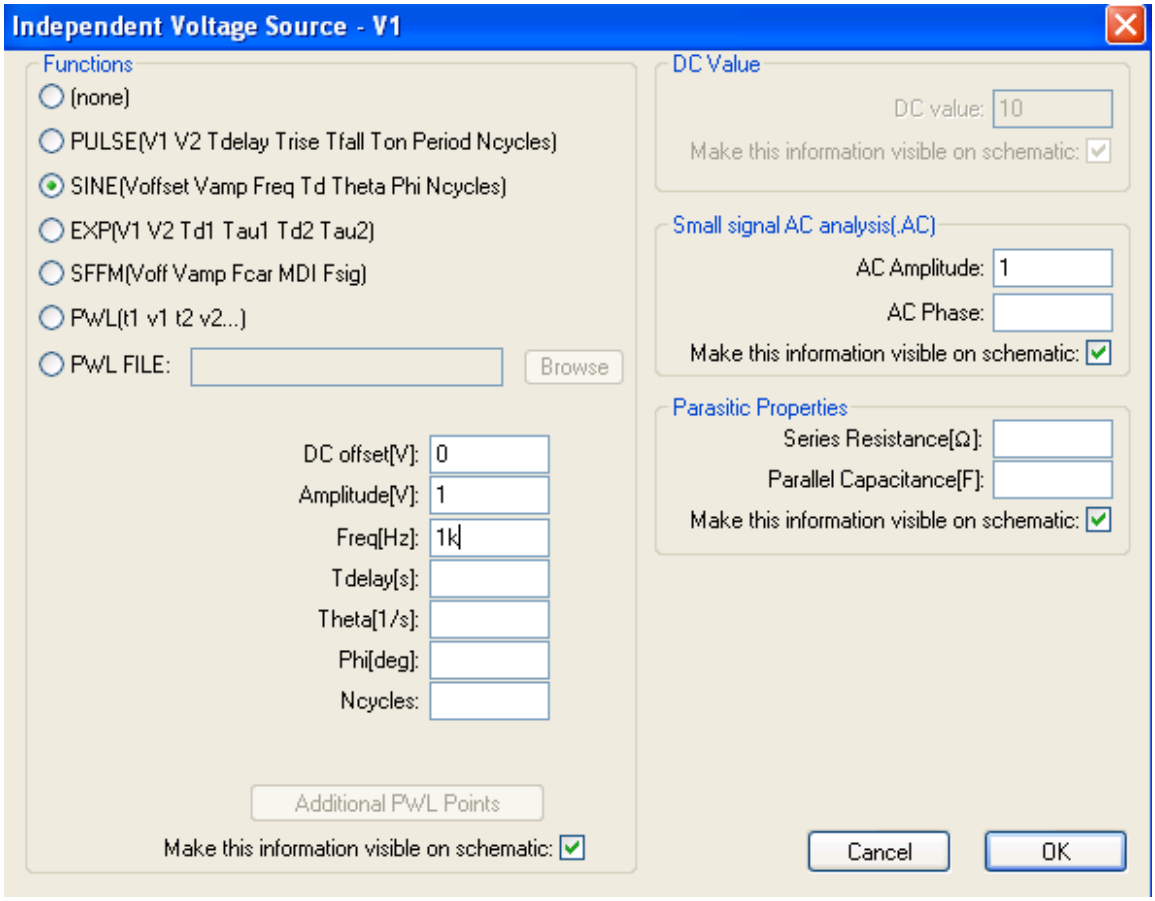

Figure 28: Setting a voltage signal to have a 1volt amplitude, 0V DC offset, and a1kHz frequency.

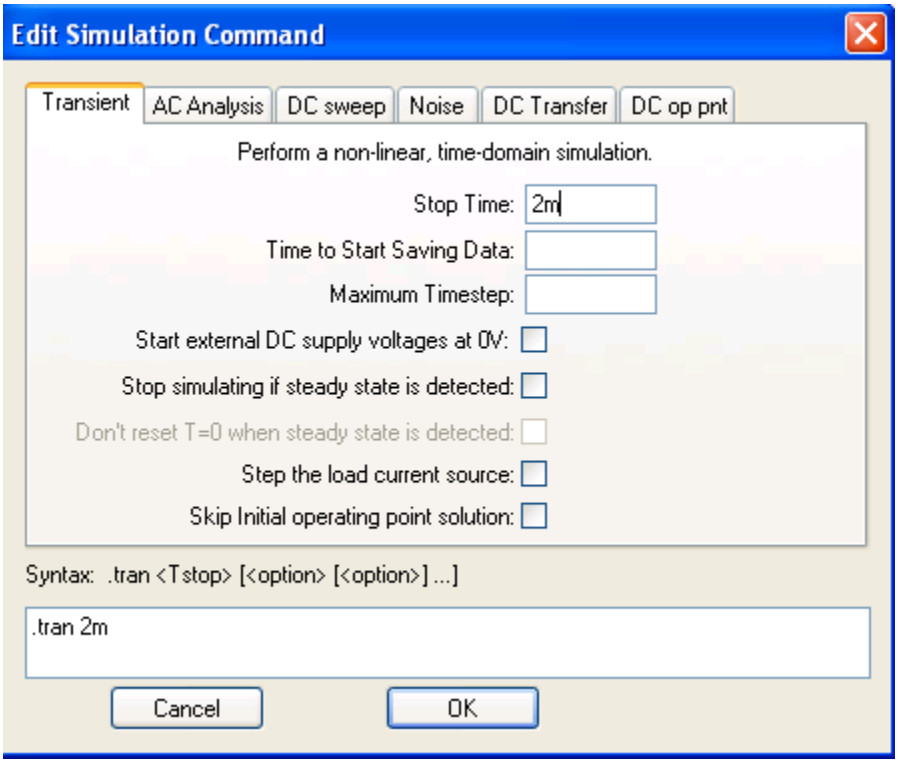

Figure 29: Setting a transient simulation of 2mS.

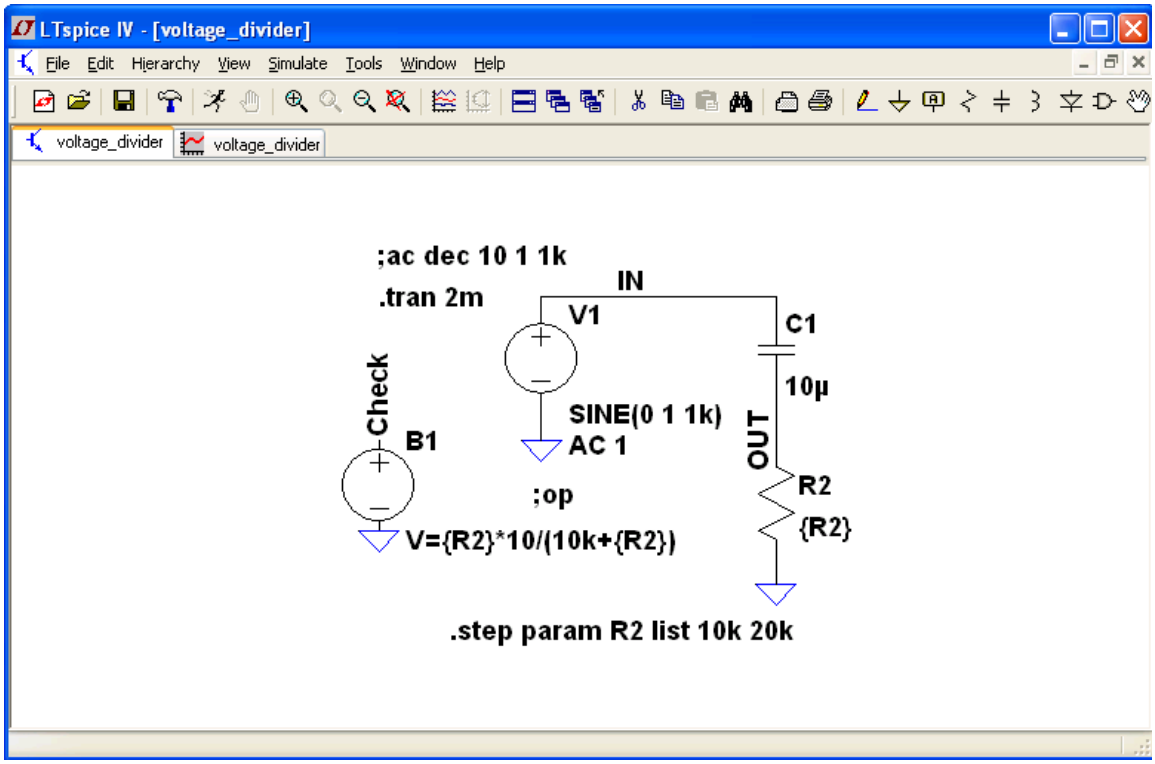

Figure 30: Completed Schematic.

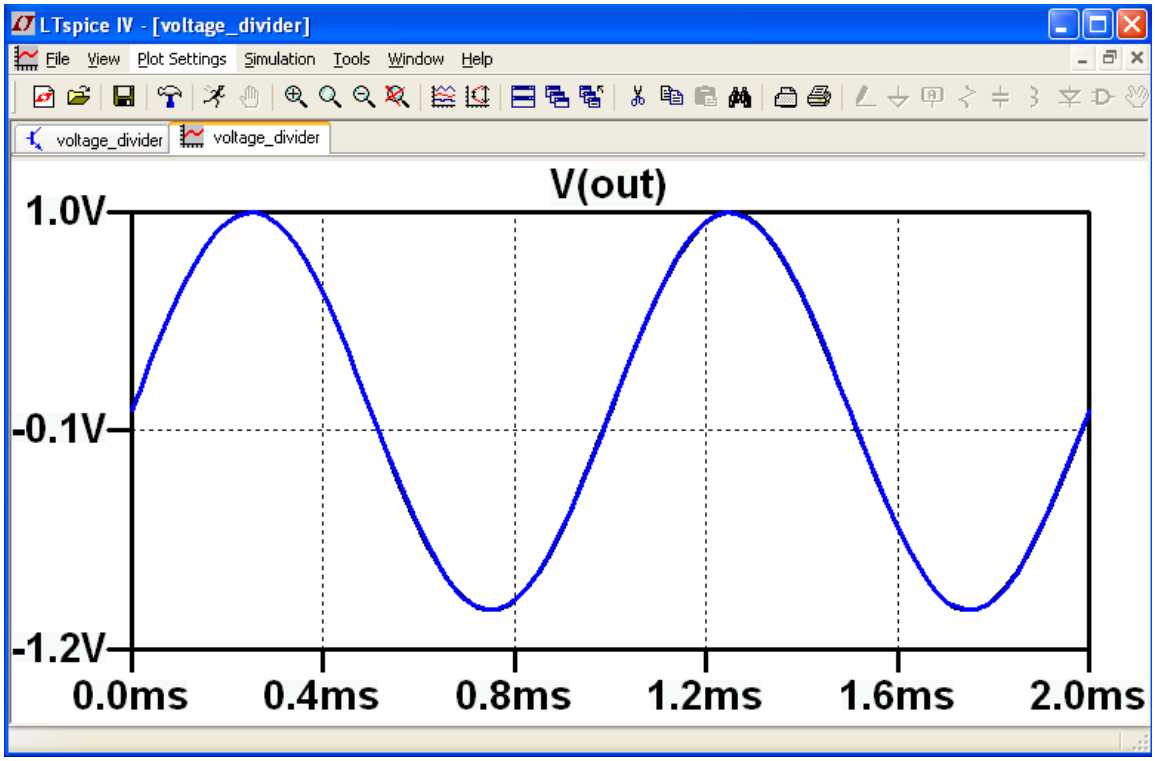

Figure 31: Transient response.

Using a LTspice to explore Linear Technology's Products:

One great thing about LTspice is that you can explore their product line easily. To see this:

- Go to add a component and click on opamps.. and then on the LT1001 (Figure 32)
- Click on Open this macro-model's test fixture (Figure 32).
- A precision absolute value circuit appears (Figure 33). Run the simulation and you should get (Figure 34).
- To see the data sheet online, right click on the opamp (Figure 35). The datasheet should appear (Figure 36).

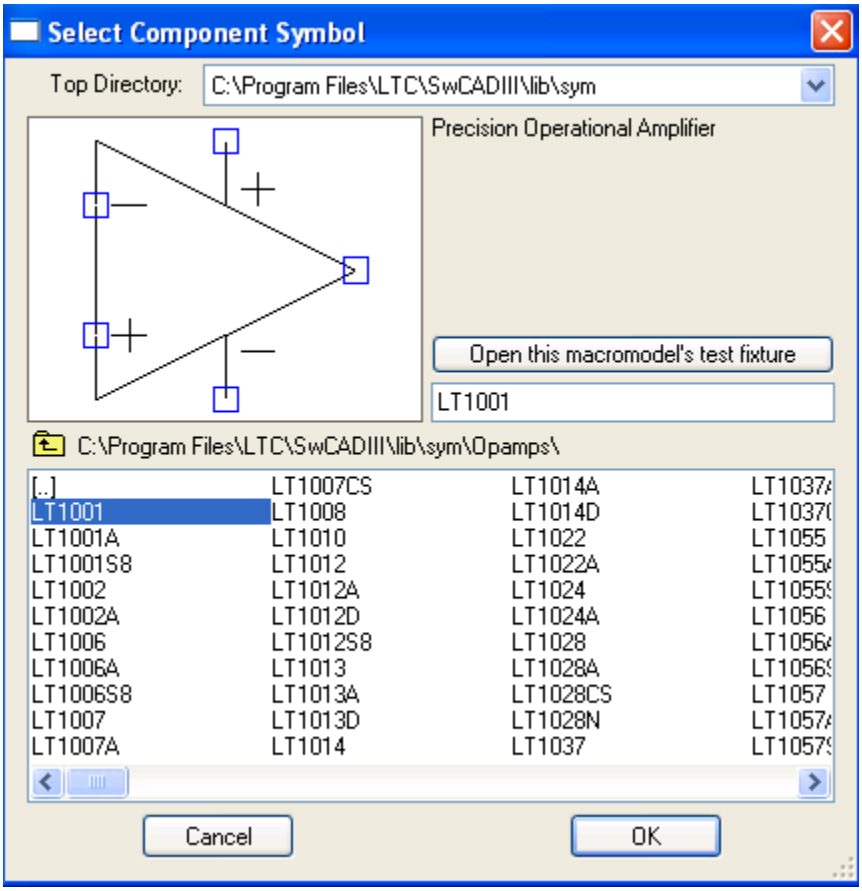

Figure 32: Exploring an OPAMP's test Jig.

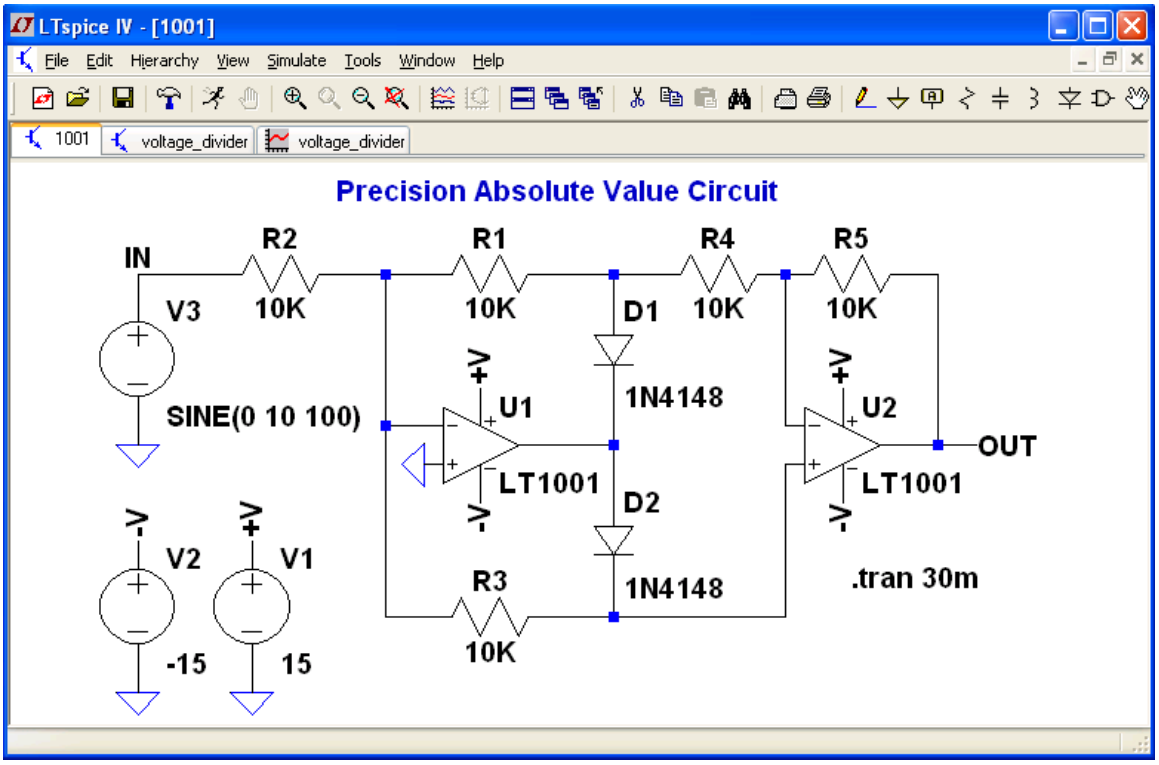

Figure 33: Precision Absolute Value Circuit.

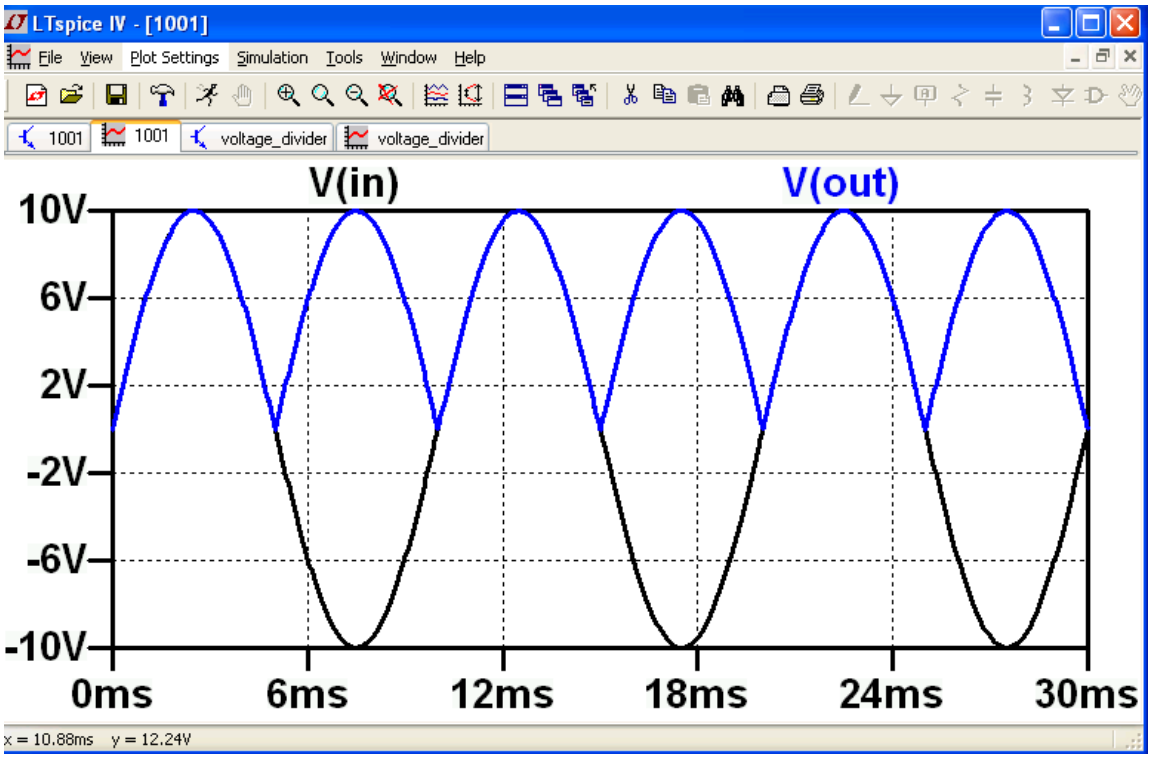

Figure 34: Transient Results.

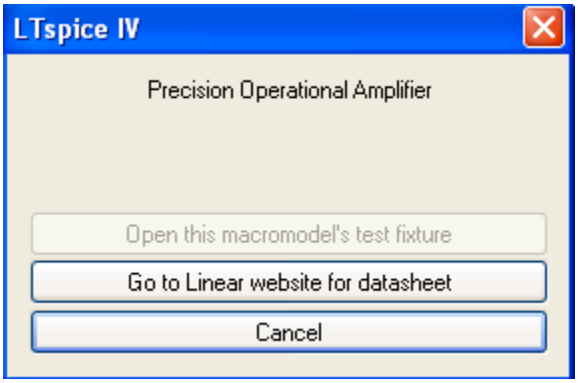

Figure 35: Finding the data sheet online.

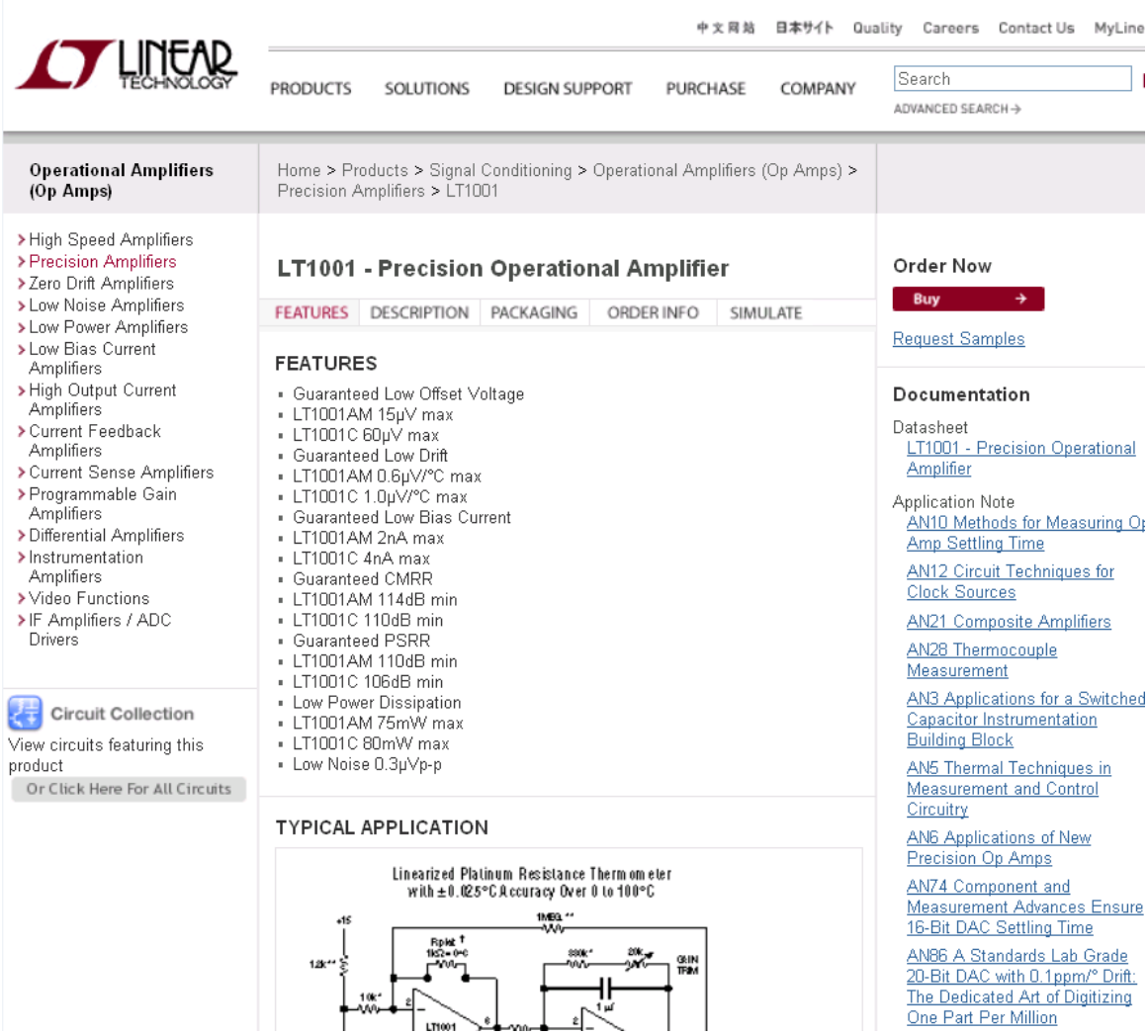

Figure 36: LT1001 datasheet.

Simulating a circuit with an .op, transient and AC simulation:

In this section you will run all three types of simulation of an OPAMP. You should be able to see how all three relate to each other.

- Save the precision absolute value circuit as EE122_lab1.asc

- Modify the circuit to be a non-inverting amplifier with R1=9kΩ, and R2=9kΩ (Figure 37).
- Run a DC (.op) simulation with Vin=1V (Figure 38).

- Run an AC simulation with Vin AC=1V from 1 to 10MHz (Figure 39), 10 step per decade.

- Run a 2ms transient simulation with VIN a sine wave with zero DC offset, 1kHz frequency and 1V amplitude. Plot Vin and vout. (Figure 40).

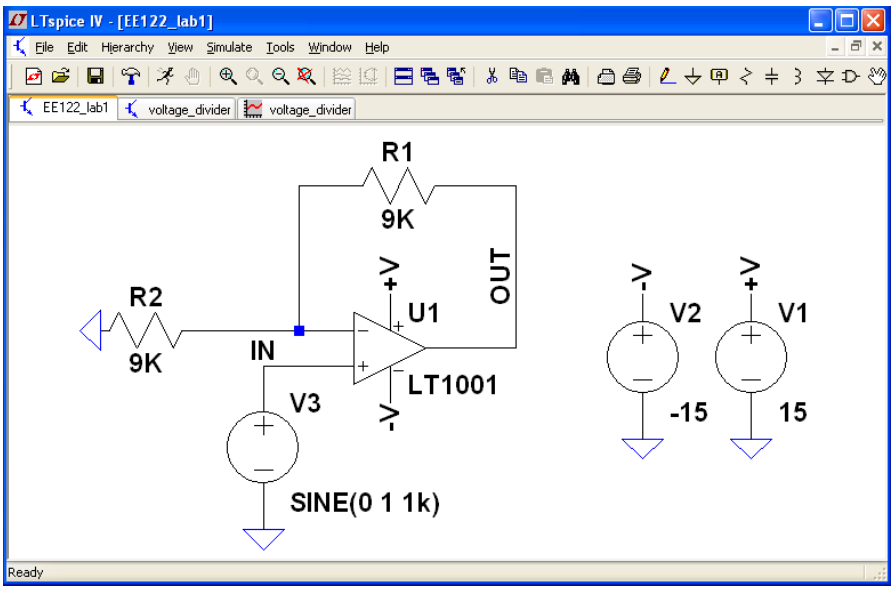

Figure 37: Non-inverting amplifier.

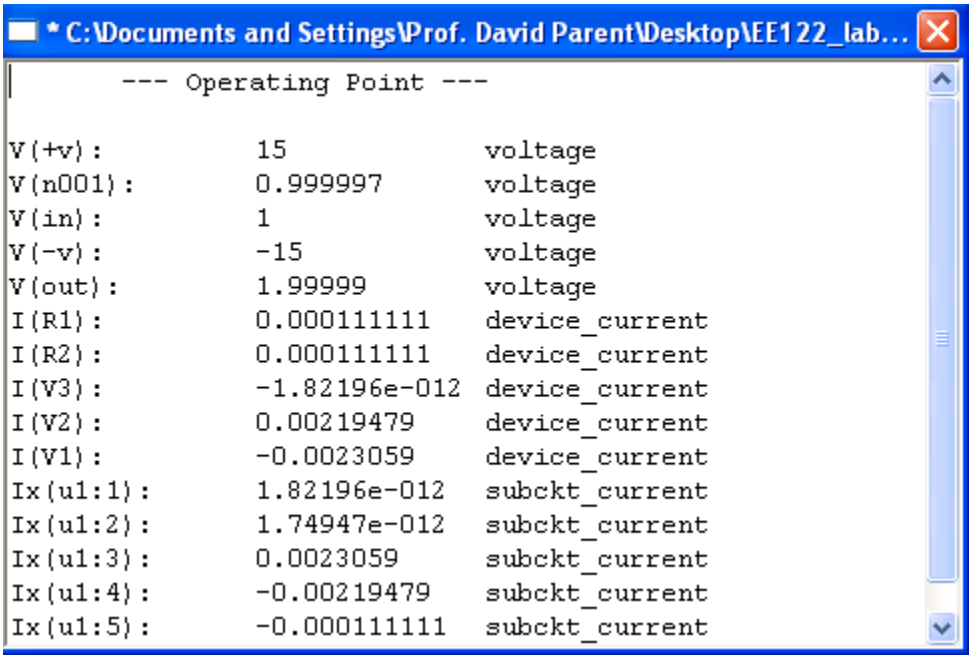

Figure 38: DC simulation of noninverting amplifier.

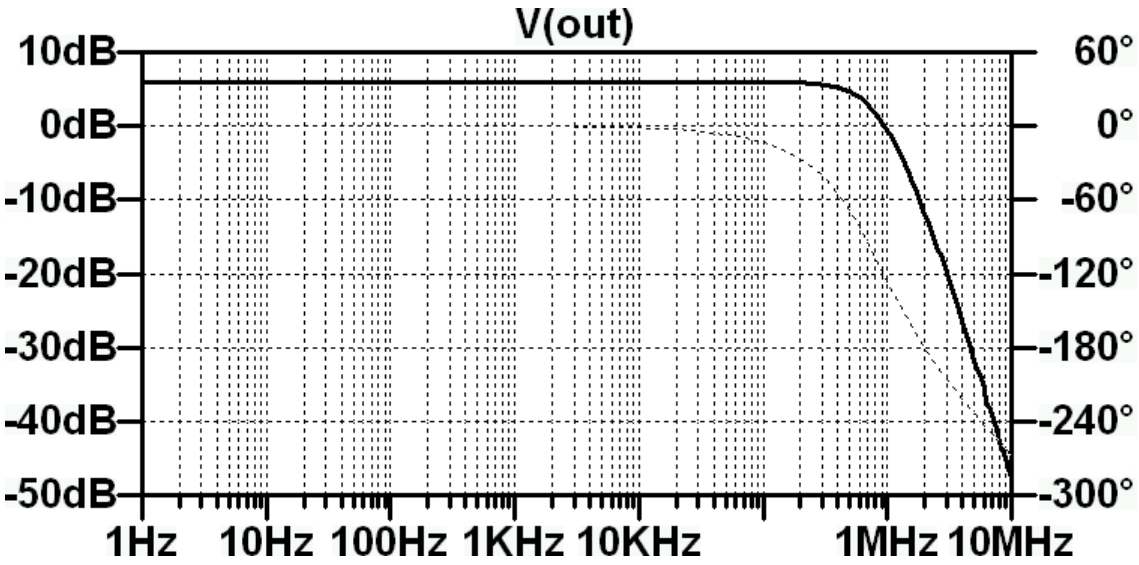

Figure 39: Bode Plot of Noninverting amplifier.

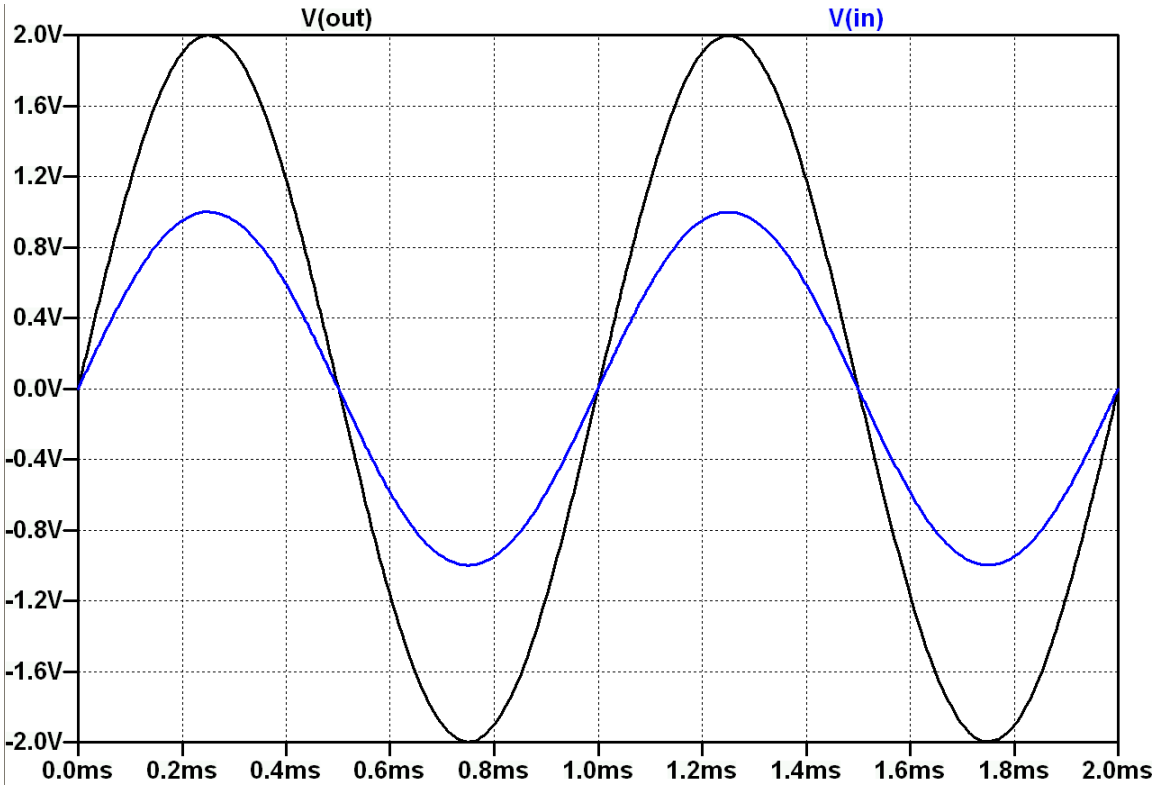

Figure 40: Transient results of non-inverting amplifier.

Input a LTspice file from a dropbox link:

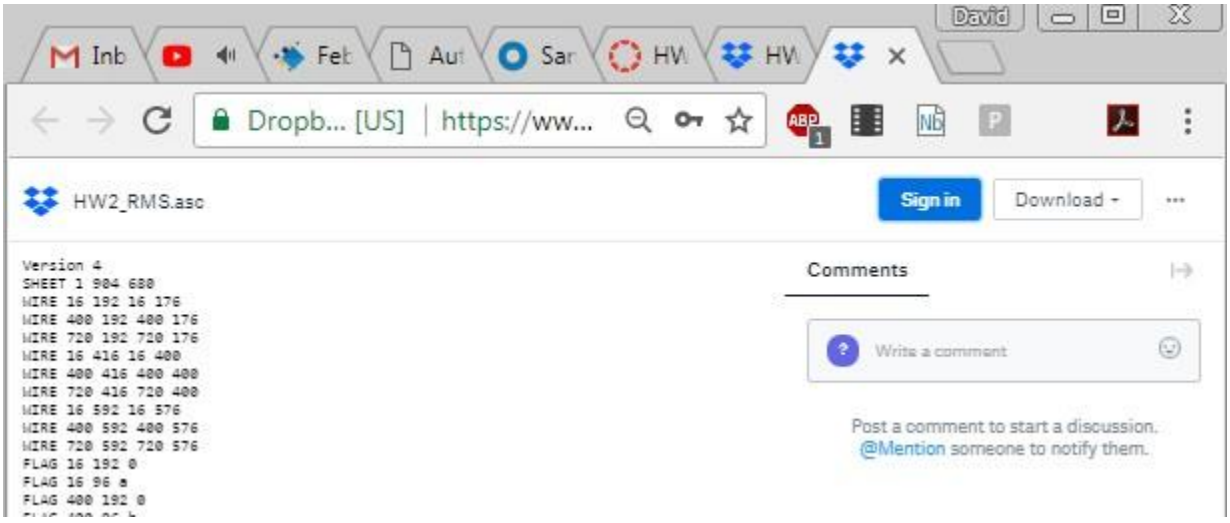

Figure 41: Download file from dropbox.

- Click on the link and you should get a screen that looks like Figure 41.
- Left click on the Download button in the upper right corner of your browser as in Figure 42, and then select Direct download.
- Open file.

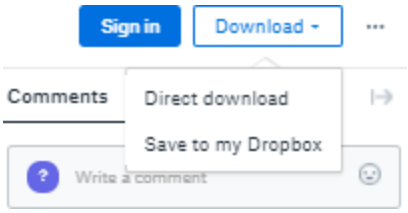

Figure 42: Click on Direct download.

Try it with this link:

Post-Lab

Repeat the previous section but for an inverting amplifier using the same R values.

Questions to be answered in lab report

1. What is the theoretical gain (Assume an Ideal OPAMP) of the non-inverting amplifier from "Simulating a circuit with an .op, transient and AC simulation""?
2. What was the simulated gain from each simulation? You will have to use a marker to read the Bode plot and peak to peak values of the transient.
3. Why don't the two values match? Support your answer with hand calculations. Notes to help with this question can be found here, but from EE110 we have:
4. The Model for the OPAMP can be non-ideal ($AV(s) = A\ vol$) for example.
5. The DC gain in finite. (See data sheet.)

Lab Report:

For this assignment, turn in individual reports in electronic form (PDF only please) to Canvas containing at minimum:

- Screen grabs from putting it all together.
- Answers to the questions.

Chapter 3:
Solar Cell Modeling and Applications

Week 3

There is no lab report due for this chapter. There are five check points that the TA will mark off as you go along.

Solar Cell Modeling

A great introduction to solar cells can be found here:

Terms

- I_{load} is the photo generated current.
- I_{sc} is the current the cell produces at zero bias.
- R_s is the series resistance of the solar cell.
- I_s is reverse saturation current of a diode.
- n is the ideality factor of a diode usually between 1-2.
- V_{oc} is open circuit voltage of a solar cell.
- V_{th} is the thermal voltage (KT/q = 26mV) at room temperature.

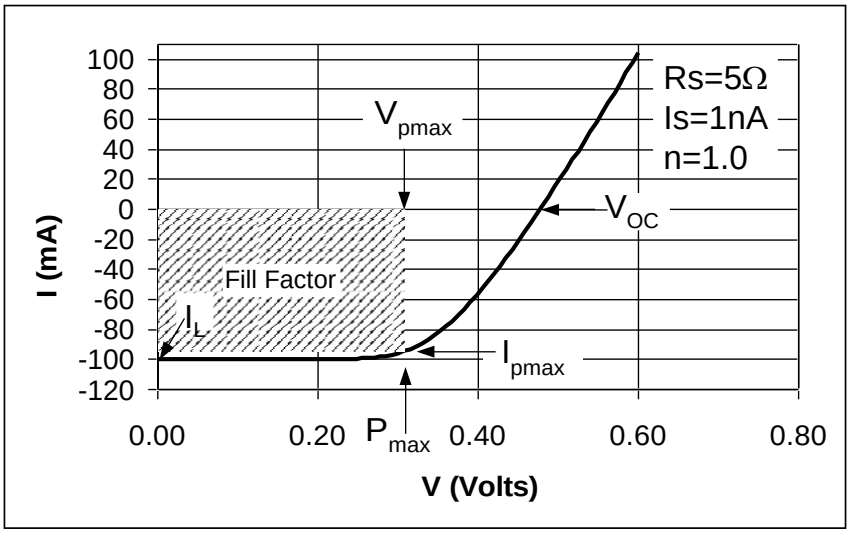

Figure 43: IV response of a solar cell with series resistance showing IL, Voc, Pmax, and FF generated from equation 1 after [5].

Solar Cell Modeling

Looking at the I-V equation for a solar cell under illumination (equation 1.) [5], it can be seen that the only optical parameter that needs to be measured is I_L and that the diode parameters could be extracted from a purely electrical simulation. I_s is the reverse saturation current, n is the ideality factor, V_{th} is the thermal voltage, and Rs is the series resistance of the diode (solar cell). Equation (1) assumes that there is no shunt conductance across the solar cell.

$$I = I_s\left(\exp\left[\frac{V - IR_s}{nV_{th}}\right] - 1\right) - I_L \qquad (1)$$

The load current (I_L), otherwise known as the short circuit current can be found by setting the voltage to zero (short circuit) and then measuring the current under illumination. I_s, n, and R_s can then be found by a purely electrical simulation.

Once I_L, I_s, n, and R_s have been determined, the open circuit voltage (V_{oc}), maximum power (P_{max}), and fill factor (FF) can be found.

V_{oc} is found be setting I from equation 1 to zero and solving for the resulting voltage.

$$V_{oc} = nV_{th} \ln\left(\frac{I_L}{I_s}\right) \qquad (2)$$

Equation (3) represents the power extracted from a solar cell. To find the maximum point, the derivative of the power is taken with respect to current and the current that satisfies equation (4) is the current at the maxim power point (Figure 43).

$$P = IV = I\left[nV_{th}\ln\left(\frac{I + I_L}{I_s} + 1\right) + IR_s\right] \qquad (3)$$

$$nV_{th}\ln\left(\frac{I_{pmax} + I_L}{I_s} + 1\right) + \frac{nV_{th}I_{pmax}}{I_{pmax} + I_L + I_o} + 2R_s = 0 \qquad (4)$$

The maximum power is then easily calculated by substituting Imax into equation (3). The fill factor is then calculated according to equation (6).

$$P_{max} = I_{pmax}\left[nV_{th} \ln\left(\frac{I_{pmax} + I_L}{I_s} + 1 \right) + I_{pmax} R_s \right] \quad (5)$$

$$FF = \frac{P_{max}}{I_L V_{oc}} \quad (6)$$

While equations (1-6) show that it is possible to decouple the optical and electrical simulation of a solar cell, the extraction of n, I_s, n, and R_s needs to be accurate and automated for this technique to be useful in the characterization of solar cells.

To extract n and I_s using the simple method the natural log of the current is plotted vs. the applied voltage (Figure 44). A linear range is selected, and a linear regression is performed. The results are of the form y=Ax+B. The ideality factor n is given by equation (7), while the reverse saturation current is given by equation (8).

$$n = \frac{1}{V_{th} A} \quad (7)$$

$$I_s = \exp(B) \quad (8)$$

R_s is found by finding the linear range of the current vs. voltage plot (Figure 44) and performing a linear regression to extract the slope. Rs is given by:

$$R_s = 1/A \quad (9)$$

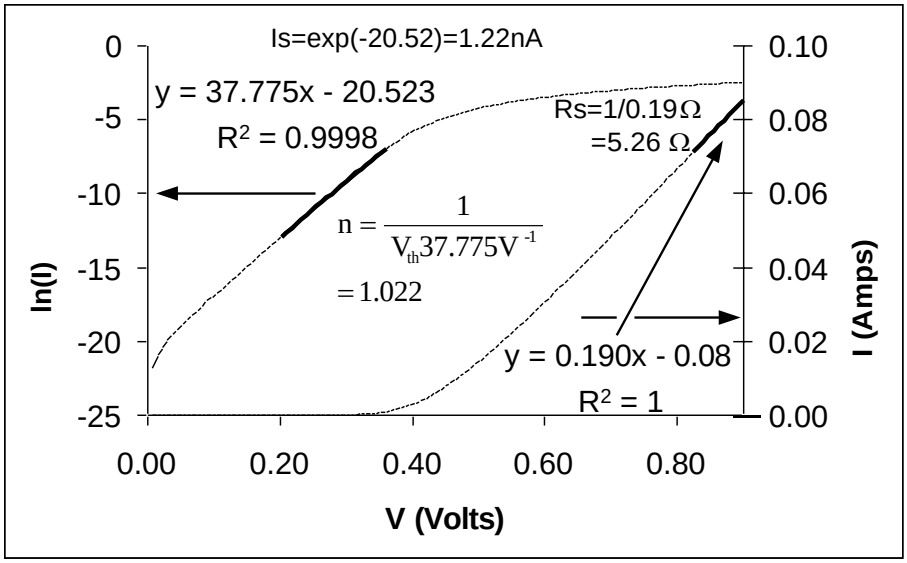

Figure 44: Simple extraction methodology plot for a diode with an IV characteristic generated from equation 1.

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16. *Kaminski, J. J. Marchand, A. Laugier, "I-V methods to extract junction parameters with special emphasis on low series resistance," Solid State Electronics, Vol 43, pp. 741-745, 1999.*
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Energy Harvesting

A great article on energy harvesting can be found here. If this link does not work then use this link.

Lab Activities

Modeling a solar cell in LTspice:

- Build the solar cell model shown in Figure 45. It can be downloaded from here:

- Run the file. You should see a blank area open up as is Figure 46.

- Plot V(out) and I(R_s). You should see Figure 47.

- Change the X-axis to V(out). You should see Figure 48.

- Plot the power as V(out)× I(rs) (Figure 49).

******TA Checkpoint A******

- Stepping R_{load} is a method to measure the IV characteristics of solar cell, but it is extremely time consuming to do and it does not lend itself to automation. It can also be hard to extract R_s. It a real test lab an SMU voltage source measurement unit is used. The voltage is swept and the current measured. This is modeled in LTspice as in Figure 50.

- Change your model to match Figure 50, and rerun the simulation, and re-extract V_{oc}, I_{sc} and maximum power (Figure 51, Figure 52).

******TA Checkpoint B******

- Create a solar cell model in LTspice with R_s=0.5 ohm, R_{shunt}=50k ohm, I_s=10nA, I_{load}=-400mA, and n=1.2, at room temperature.

- What is the V_{oc} and maximum power?

- If R_s=2ohm, what is the V_{oc} and maximum power?

******TA Checkpoint C******

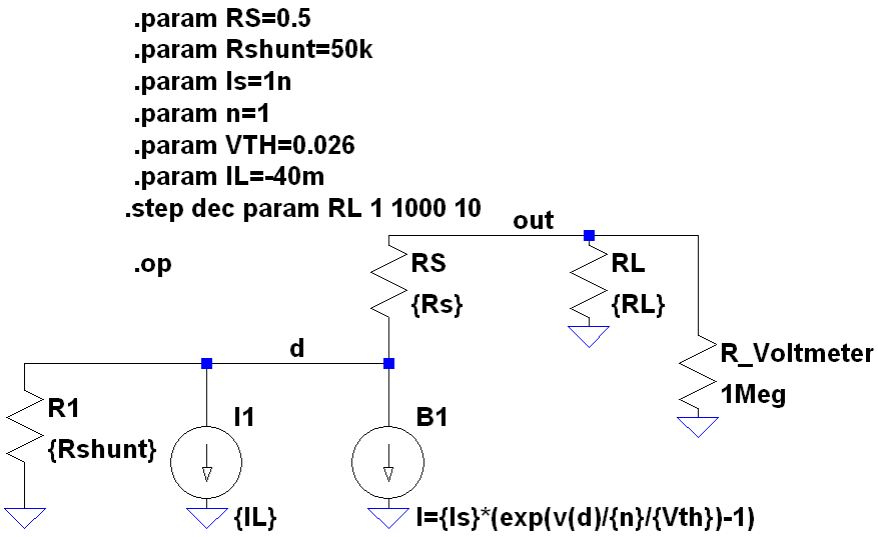


Figure 45: Solar Cell Model with programmable parameters.

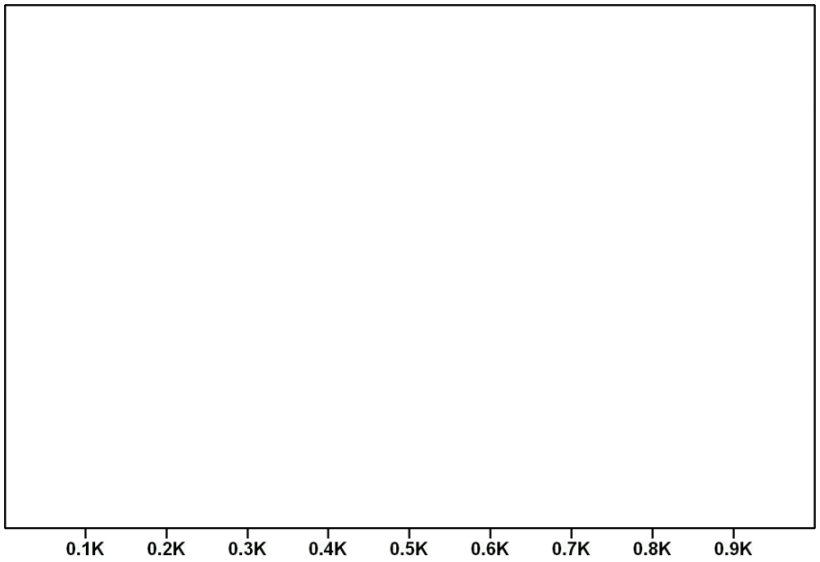


Figure 46: Simulation results without data.

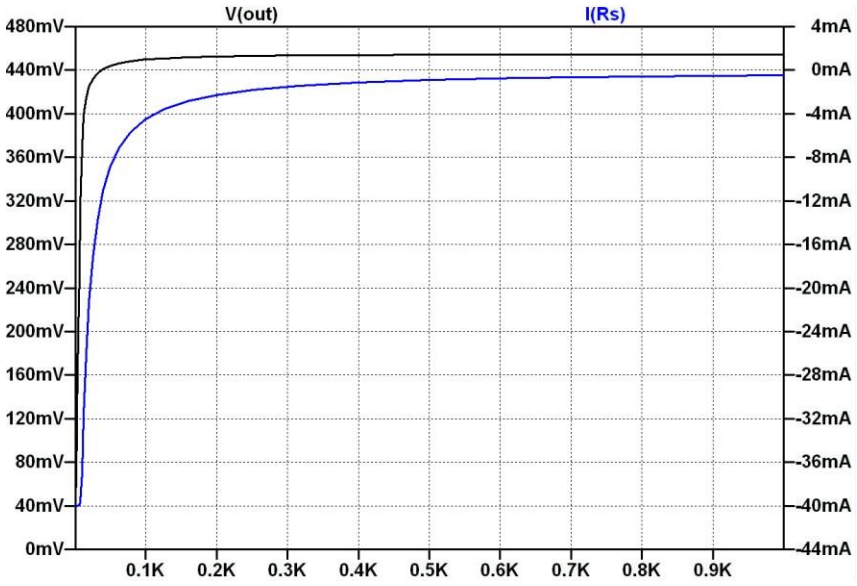


Figure 47: Simulation results of Vout and I(rs) vs Rload.

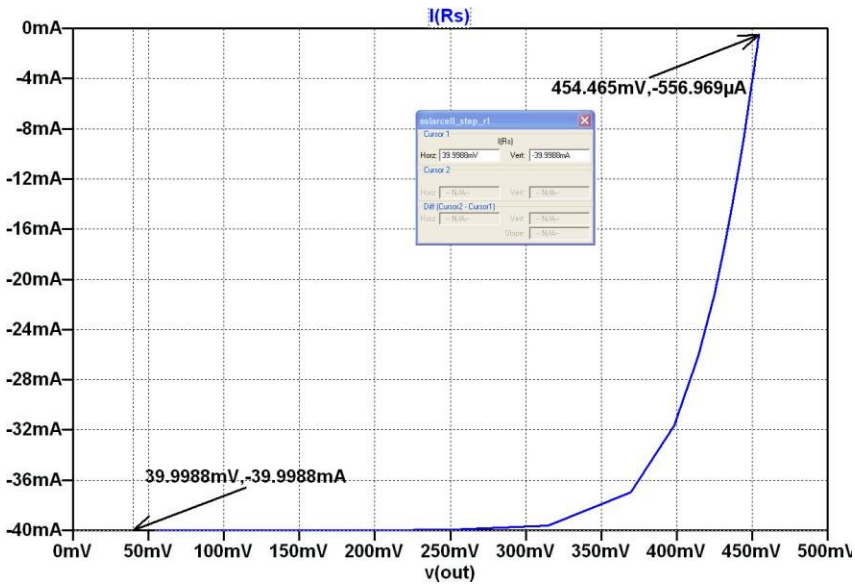


Figure 48: Finding V_{oc} and $I_{sc.}$

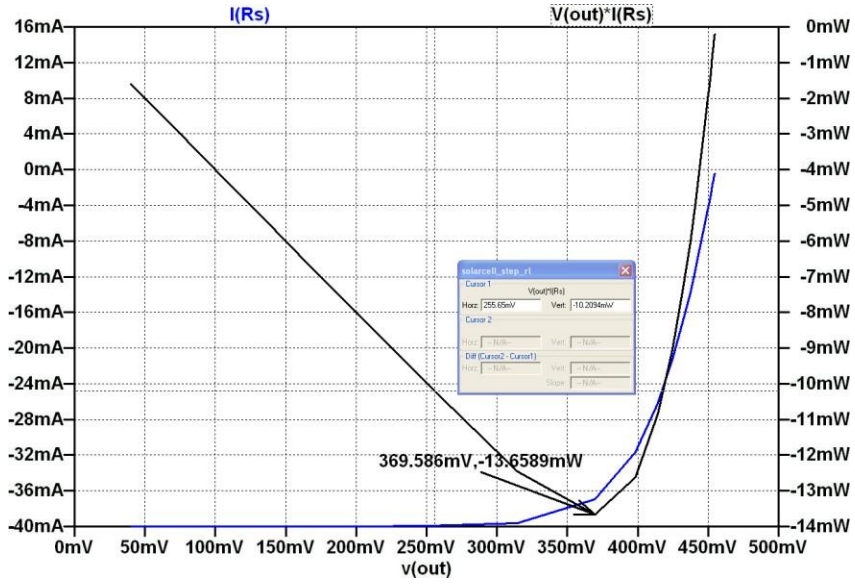


Figure 49: Finding maximum available power.

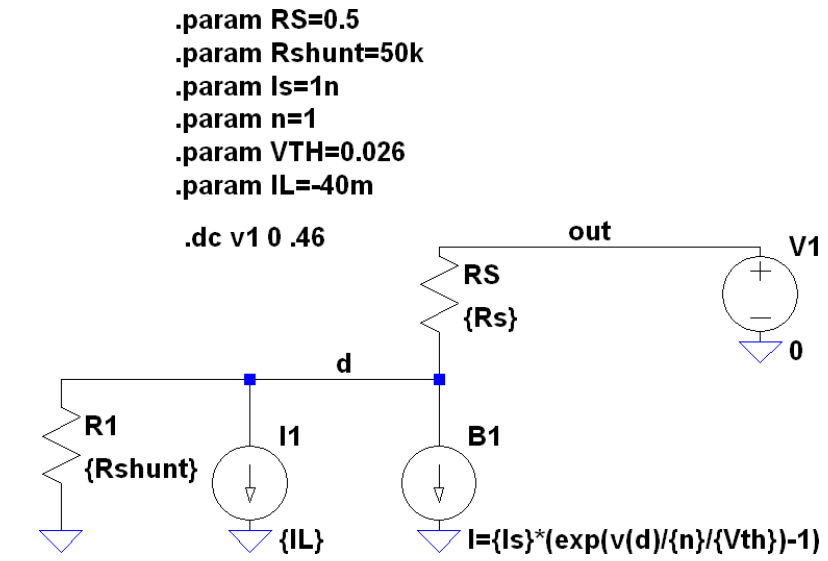


Figure 50: Measuring solar cell response with a voltage source.

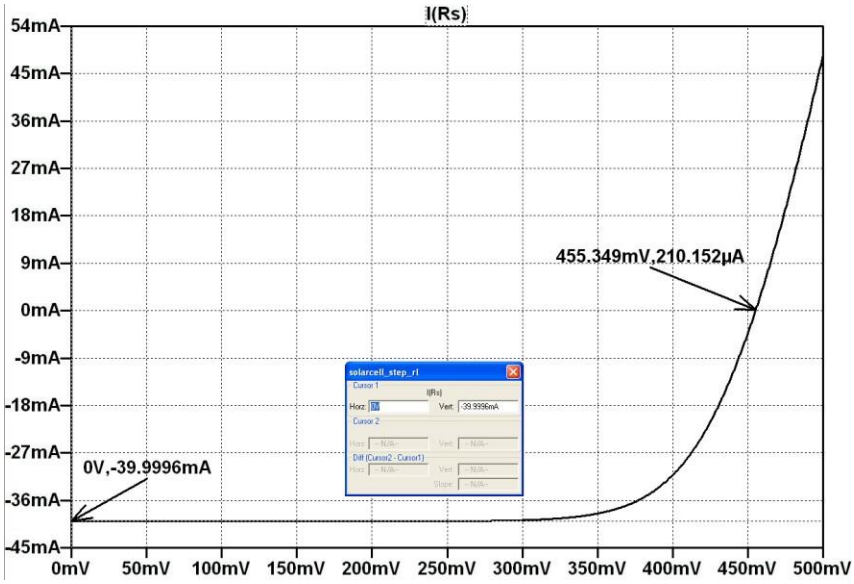


Figure 51: Measuring V_{oc} and I_{sc} from a swept voltage source.

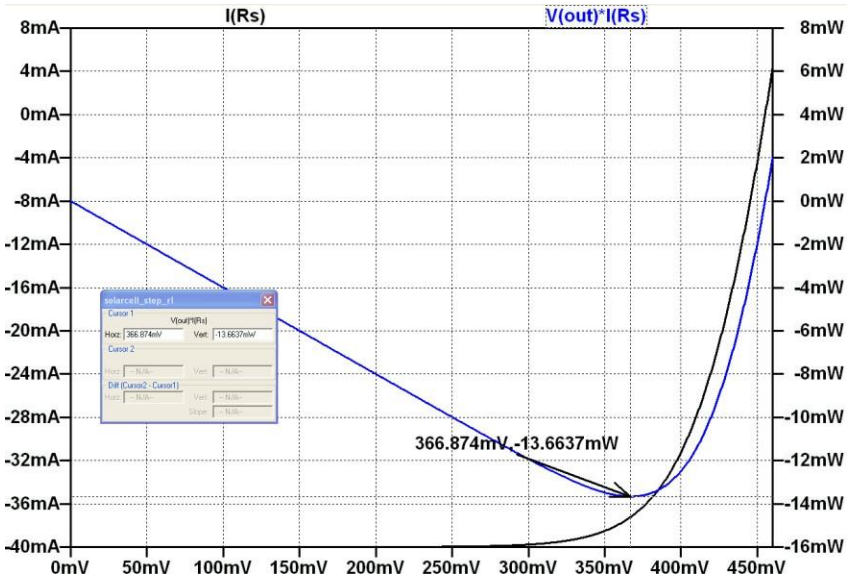


Figure 52: Finding power from a swept voltage source.

Energy Harvesting:

- Open up the LTC3105 test jig in LTspice (Figure 53). (You can create a new schematic, add a new part, and place the LTC3105 (located in power products). Then you can right click on the part and open up the test jig.)

- Run the simulation (Figure 54). (It takes a while.)

******TA Checkpoint D******

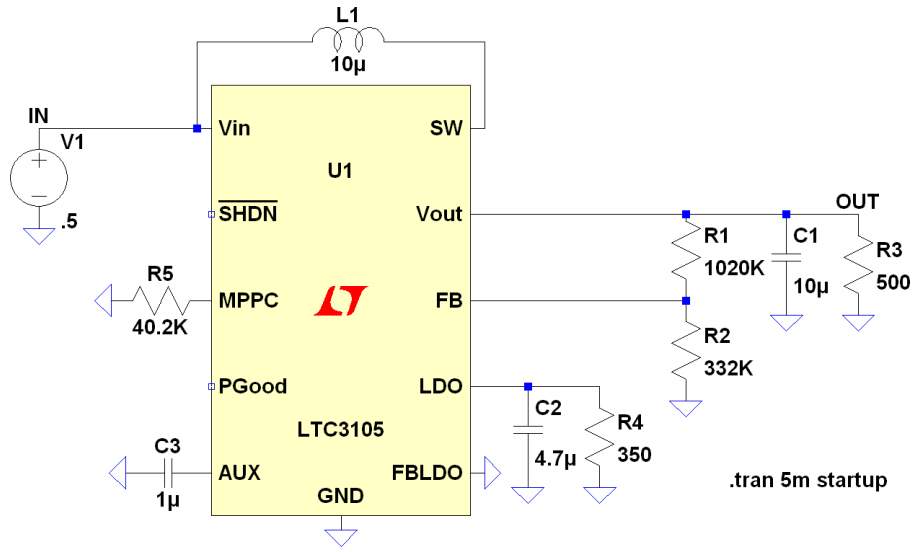


Figure 53: LTC3105 Test Jig.

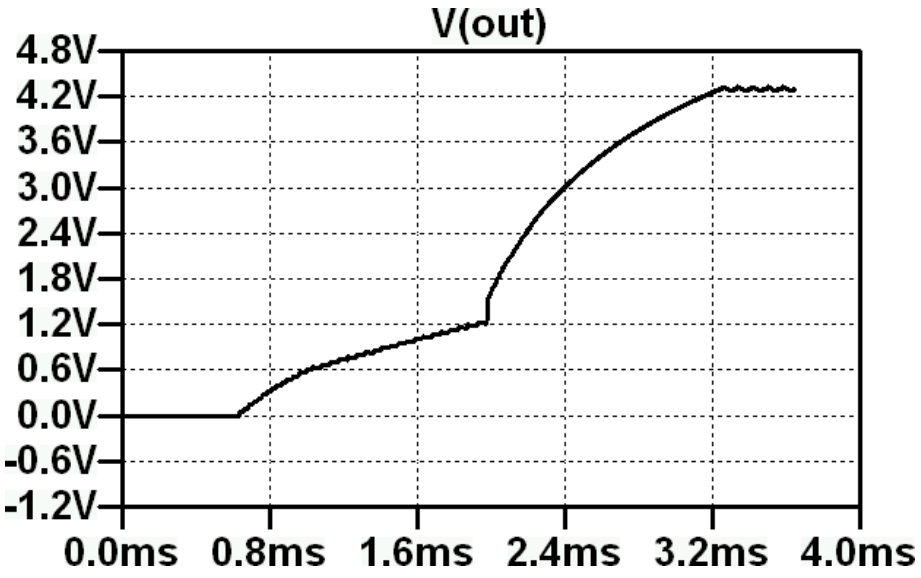


Figure 54: Transient response of LTC3105.

Design an energy harvesting system using the LTC3105 and two solar cells in parallel that have the following electrical characteristics: R_s=0.5 ohm, R_{shunt}=50k ohm, I_s=10nA, I_{load}=- 200mA, and n=1.2, at room temperature to charge a cell phone with a USB. Use the solar cell model you developed in the previous section. You have to research the specification for this. In addition, the design equations are in the LTC3105 Datasheet. (http://www.linear.com/product/LTC3105)

In order to get the simulation to run properly with the behavioral solar cell you have to add a capacitor to V(in) as shown in Figure 55. Also you have to add an initial condition, .ic V(d)=0, and .ic V(In)=0 to the schematic to get the simulation to start properly (Figure 56).

******TA Checkpoint E******

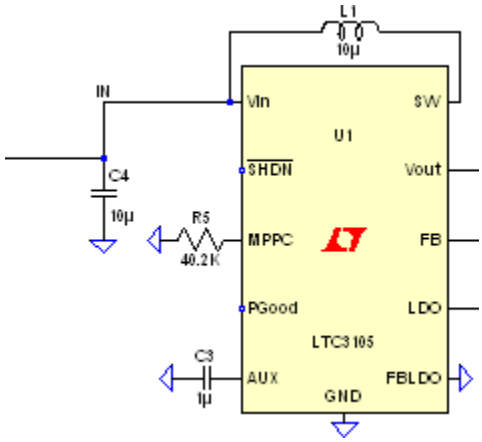


Figure 55: Add a 10uF capacitor to the In node (Vin port on the LTC3105) to make the simulation run properly.

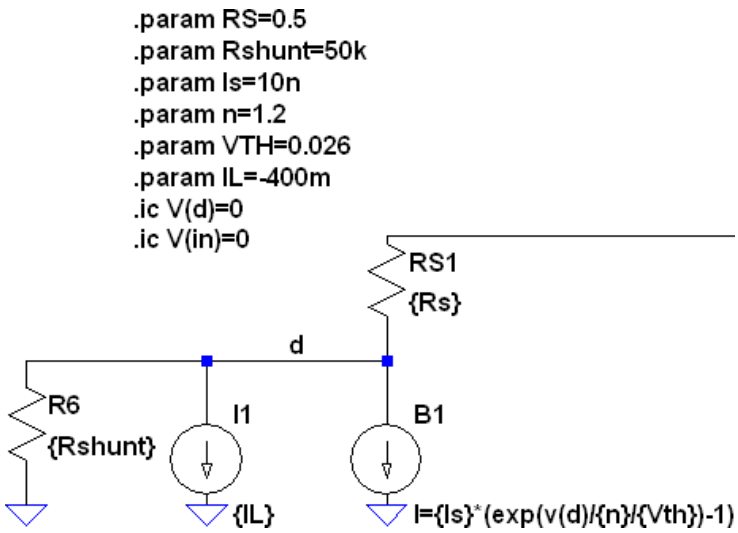


Figure 56: Add initial conditions to schematic.

Lab report:

NA: Show results for check pints A, B, C, D, and E to your TA as you do the lab.

Chapter 4:
Energy Harvesting PCB Design

Week 4

Pre-lab:

- Before starting your design, read the data sheet and highlights all the PCB layout tips.
- Watch these videos:
  - Video on making sure your board as the right layers:
  - Video on PCB hints
  - LTC3105 video
  - Video on past projects

Lab Activity:

You will design your PCB board in diptrace the TA will check your design before you turn it in. There is no lab report due, just the diptrace files.s

- Using Diptrace, design a single layer board that will create a 5V power supply:
  - Try to use the parts that are already created. For the LTC3105, USB, R's and C's use the pre-drawn packages. You have to make your own drawing for the solar cells, and the inductor.
    - Inductor Note: The inductor pad size should be 0.08 inches x 0.08 inches, the distance between the pads should be 0.2 inches from the middle of both pads and 0.12 inches edge to edge between the pads. The data sheet for the inductor can be found here.
  - Mount both solar cells in parallel Make one copper pad 2" by 2" (Figure 58, Figure 59).

(You might get one solar cell that is 2” by 2”.)

- Everything must be in the TOP layer. (Do not use Top Assy.)
    - If you accidentally put something in Top Assy, select the object, and change the layer type to signal.
- Place a + and – sign near your positive and ground signals in copper (Top)
- Place a mark in copper to show you the top of your IC (LT3105)
- Put your name in the copper layer away from the parts.
    - Use the TOP or signal Layer, not Silk!
    - Use the vector option for your text.
- Use surface mount parts from Figure 57. This is done so that we can buy the parts for every project in an efficient manner. Note you might not need all of them. You really need to choose the R values to set the voltage properly at the 5.0V side. The other outputs we do not need.
- Use the 12 pin MSOP package. Another link can be found here. https://dl.dropboxusercontent.com/u/35091424/EE122/05081668_A_MS12.pdf
    - In Diptrace, trace search for the pattern in layout as MSOP. A list of choices will appear,
- Your design must fit in a 3” by 2.5” area.
- You must add a board outline using the Objects, Place objects, board outline tool. You check and see if the board outline was done properly, turn the board outline layer on and off, and you should see it disappear and reappear.
- The output is USB and you need to use this SMT part: http://www.sparkfun.com/datasheets/Prototyping/Connectors/USBFemaleTy peA.pdf
- The holes shown in the USB, are not important because we do not use them. Pins 5 and 6 are just solder pads to hold the USB down.
- Pins 1-4 can be connected as shown at the bottom of:
    - http://en.wikipedia.org/wiki/USB

- Make sure your power and ground lines are wide enough. Current flowing through a thin wire can cause a large resistive loss.
- Make sure that you do not include the output resistor load that you used to see if your project works. The load will be the phone.

- The inductor part has changed. The data sheet for the correct inductor can be found here.

Table 1: BOM for 5V design.

Item	Qty	Reference	Description
1	1	L1	10uH inductor
2	2	C1, C2	10 uF capacitor (size 0805)
3	1	C3	1uH capacitor (size 0805)
4	1	R1	1MegΩ 1% (size 0402)
5	1	R2	250kΩ 1% (size 0402)
6	1	R5	40.2kΩ 1% (size 0402)

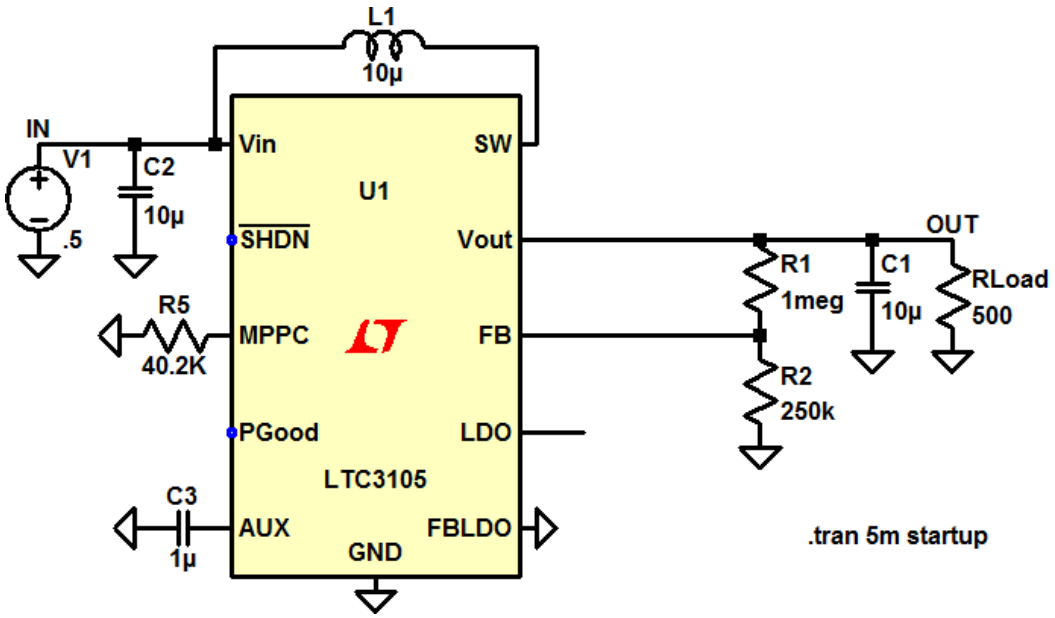


Figure 57: Reference schematic for 5-volt design. Note: R_{load} simulates a 10mA load (5V/500Ω) Note: LDO not connected on purpose.

Link to above schematic:

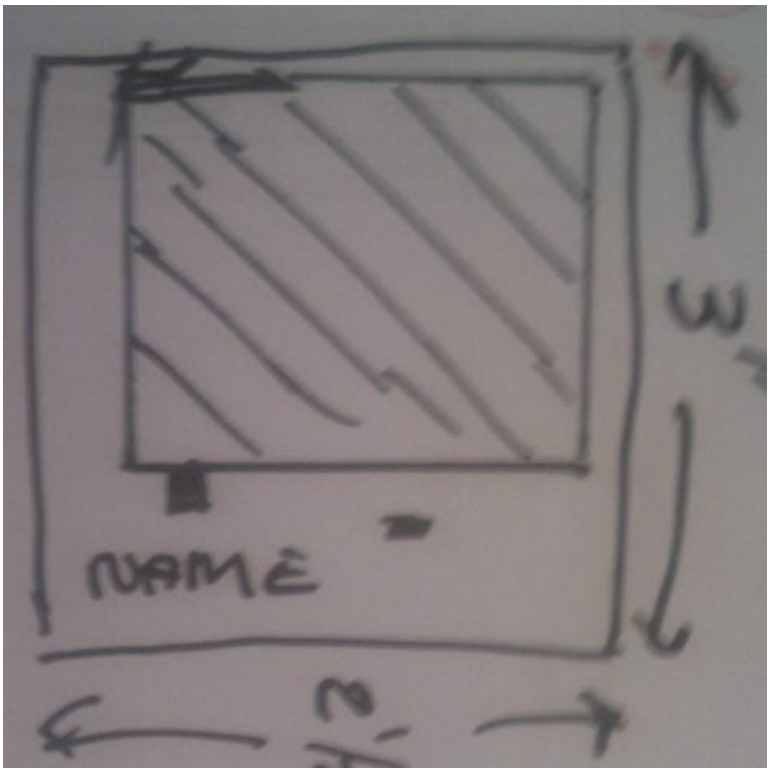


Figure 58: Very rough drawing of footprint of solar cell.

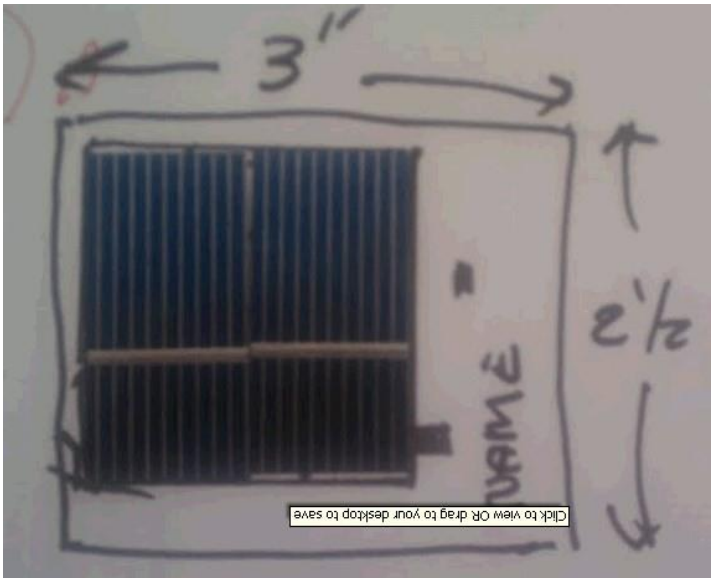


Figure 59: Very rough draft of board with solar cells. The top of the cell is negative, and the bottom is positive. Connect the negative side of the solar cells together with a wire, that then connects to the negative trace on your board.

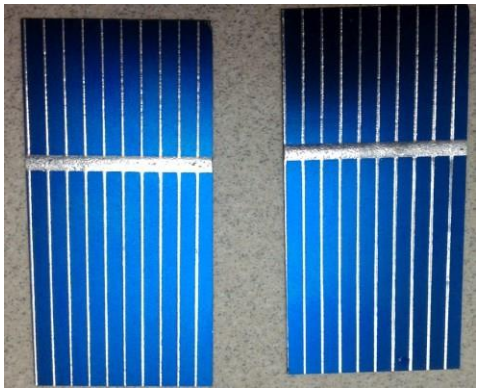


Figure 60: Cells you can use for your energy harvesting circuit. (Your solar cell might be one piece.

The top metal grid is the negative side of the solar cell (-). The bottom of the solar cell is positive (+). You will solder a piece of wire from the top of the solar cell to ground on the board.

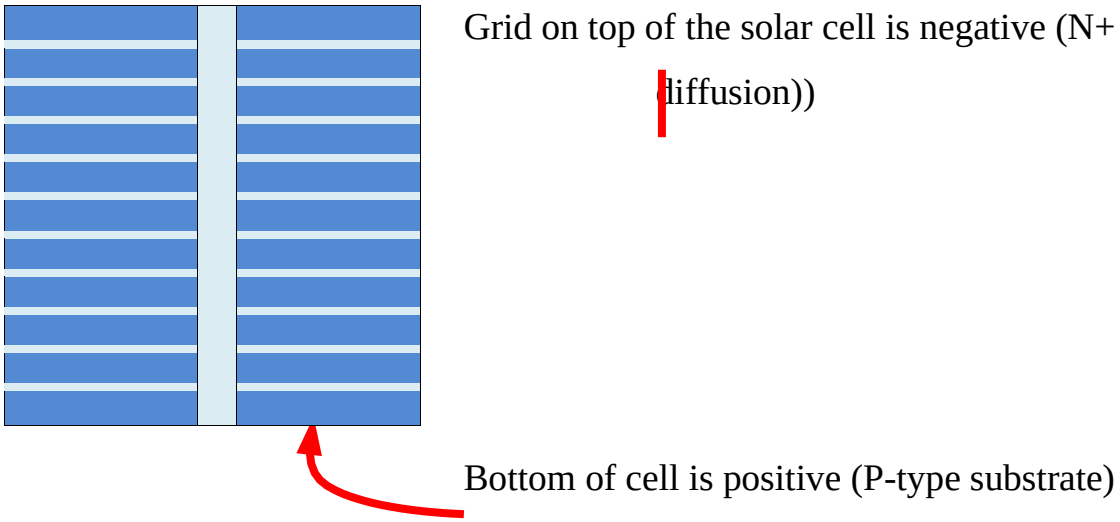


Figure 61: Positive and negative are labeled for solar cells.

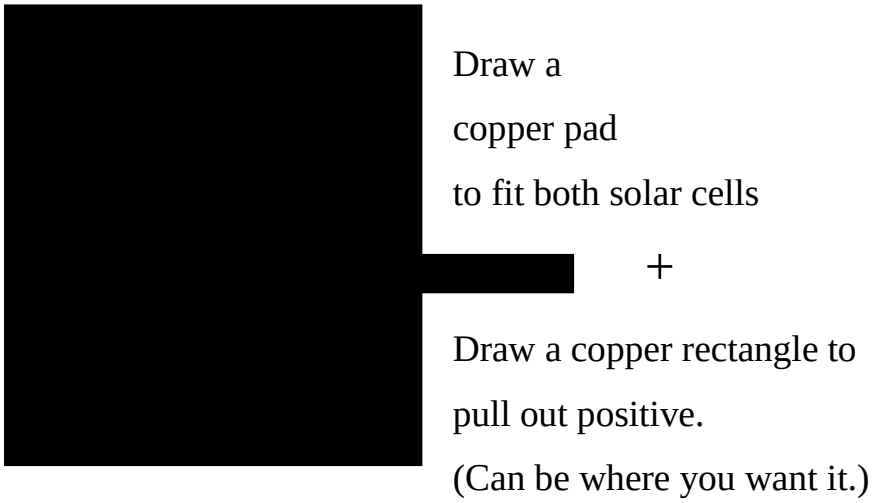


Figure 62: Draw pad for solar cells.

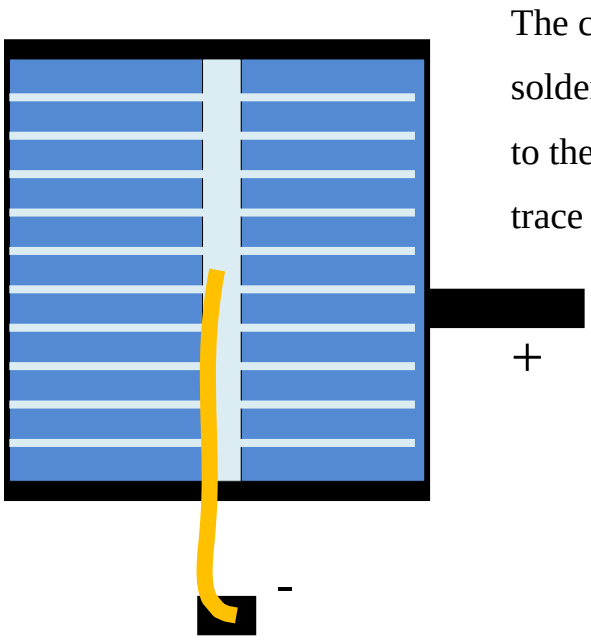


Figure 63: Hint on how to add solar cell to board. (Note: There is only one cell shown here.)

Lab Report / Dip Trace Files:

Watch this video, on how to double check your board for common mistakes: https://youtu.be/EMTmq4vKMJ0

- Turn the diptrace file in on Canvas. Make sure the file is named: Lastname1_solar_charger.dip
- Make sure that everything is in the TOP layer, and that the board outline was created with the objects, place board outline tool, and that the board outline is in the board outline layer.
- When the board comes back you will assemble it, test it, and document your design.

Chapter 5:
Diode Modeling and Applications

Week 5

Introduction

Diodes

Signal Conditioning. Watch this help video.

Objective

Students will learn how reality and simulation relate to one another and debugging skills, by extracting spice diode parameters.

Lab Activities

Extract Io, N and Rs from LTspice and Measurement.

1. Build the circuit shown in Figure 64 (LTspice link), and extract Io, N (The series resistance needs a different test system so it will not be done for this lab.) according to these notes. Your waveform should look like Figure 65. Hint: To plot the natural log response of the diode current, click on add trace, and type ln(I(D1)). Hint: Right click on the generic diode symbol, then click on Pick New Diode, and select the proper diode from the list.
2. Compare your extracted Io and N to the LTspice model parameters. This data is provided when you select which diode model to use as shown in Figure 67.

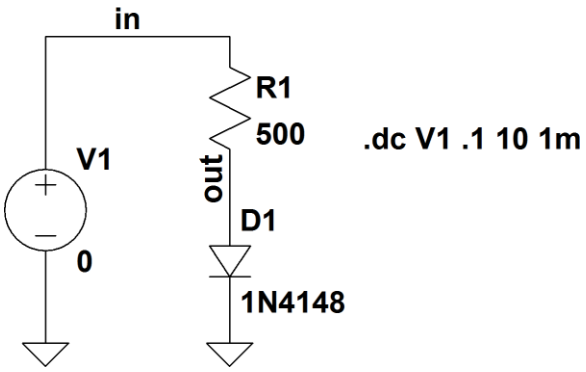


Figure 64: Diode DC test setup.

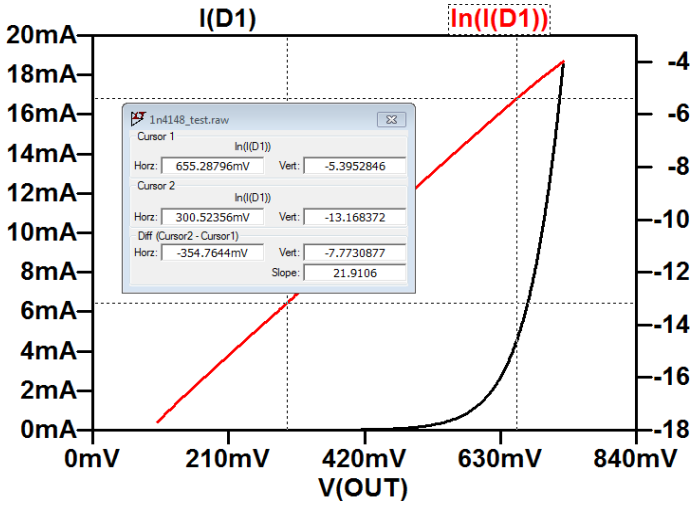


Figure 65: DC results for diode circuit. (Make sure to change the x-axis to V(out) or you will get a plot like Figure 66)

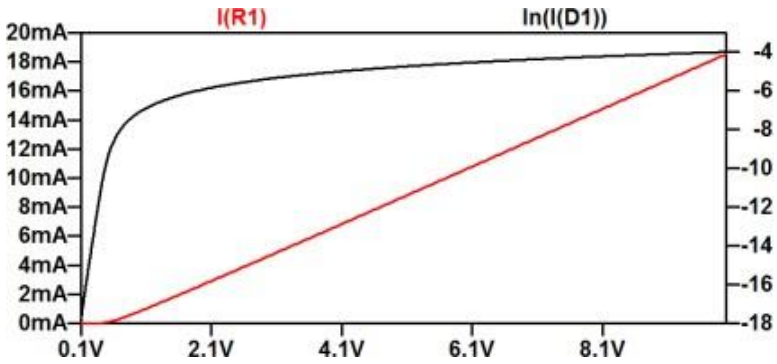


Figure 66: IV diode plot with wrong x-axis.

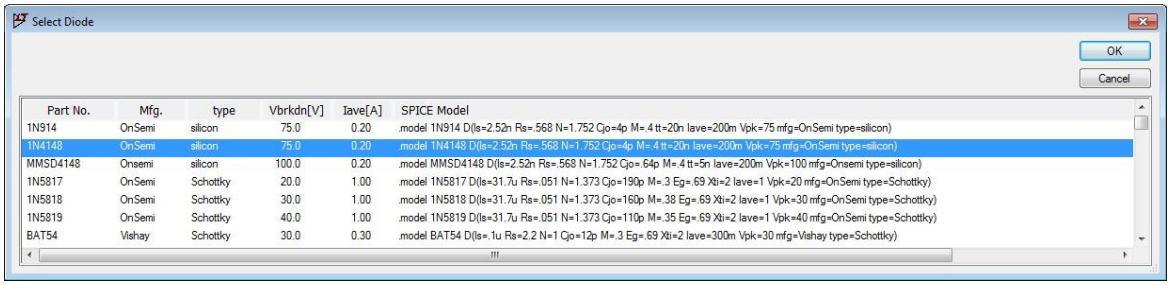


Figure 67: Diode parameters used by LTspice.

3. Build a behavioral model of the diode as shown in Figure 76. Use the values you extract for N and Io. Use the value for RS from the LTspice parameter data (.568Ω)
4. Compare the current through RS and D1. Are they the same? What are possible sources of error?
5. What is the voltage input range for which this diode can be used as an e^x or ln(x) function in an opamp based circuit?

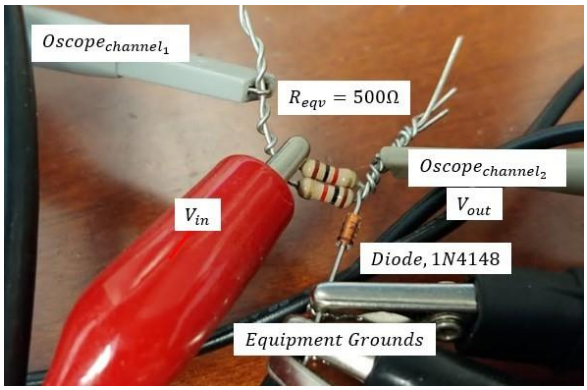


Figure 68: Diode test set up.

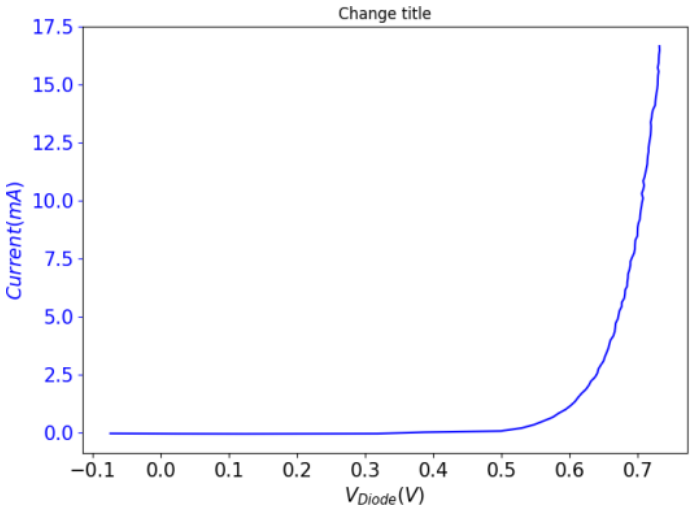


Figure 69: Diode IV curve for 1n4148.

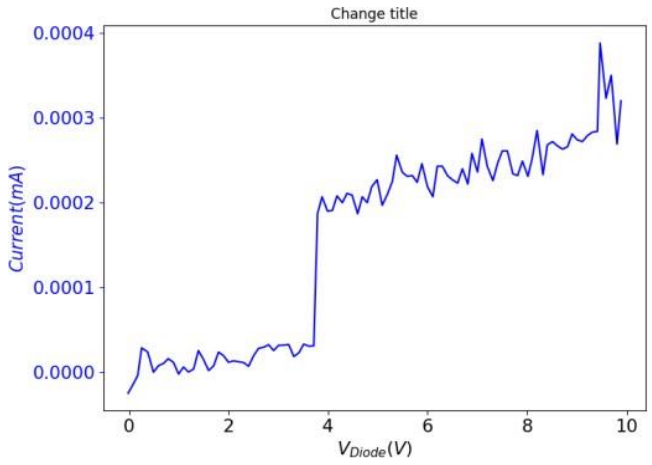


Figure 70: Accidental Reverse bias of diode IV.

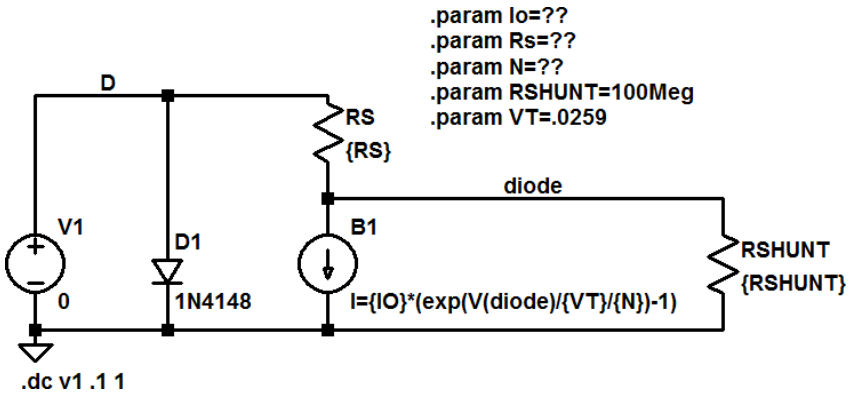


Figure 71: Behavioral Diode Model. Note: ?? should be replaced by the Io, n and Rs (from LTspice parameter data) that you have extracted from the previous step.

Design, and verify in LTspice a natural logarithmic amplifier.

- Design an opamp based circuit that implements the following function:

$$V_{OUT} = - (V_T/n) \ln(V_{in}/I_oR)$$

Where VT is the thermal voltage, n is the ideality factor and Io is the reverse diode current you extracted from the previous steps. Use any OPAMP of your choice. Please read these notes. R can be any resistor from 1kΩ to 10kΩ.

Lab report:

For this assignment, turn in individual reports in electronic form (PDF only please) to Canvas containing at minimum:

- Document all the lab activities.
- Make sure to include screen grabs of spice circuits, simulations, experimental setups, and measured data*.
- Describe what happened when you measured your data, show measured data. Explain differences between hand calculations, spice simulations and measured results.

Chapter 6:
Energy Harvesting PCB assembly and test - Presentation

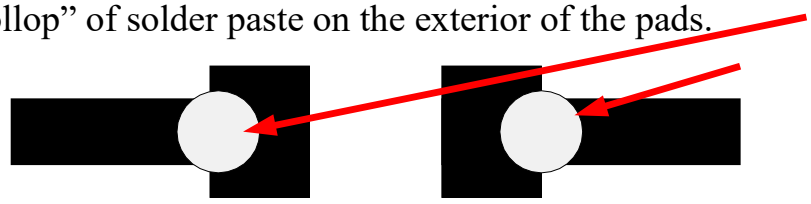
Weeks 6

Introduction:

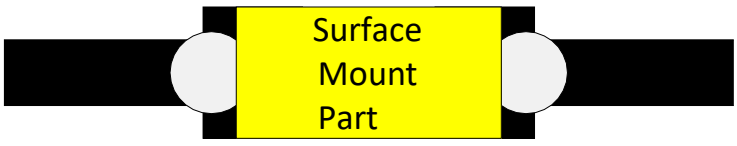
This lab is an extension of the DipTrace lab where you designed the PCB layout and now in this lab there will be a presentation on the PCB assembly and testing. The lab will consist of training how to use the surface mount soldering stations, followed by introducing you to the components and equipment we will be using, if doing fabrication/assembly. Basic information on the Energy Harvesting PCB assembly and testing:

Attaching surface mount parts:

Add “dollop” of solder paste on the exterior of the pads.



Place surface mount part so it slightly touches paste.



Lab Report:

There will be no lab report due for this week.

Chapter 7:
Using the gm/ID technique to design CS amplifiers

Week 7

There is nothing to turn in, you must have the TA verify your work at the designated checkpoints.

Pre-Lab:

- Read this:
- Watch these videos:
  - Video 1
  - Video 2
- In this lab you will:
  - Develop a gm/ID vs Id curve for the 2N7000 NMOSFET using LTspice
  - Use the gm/ID method to design common source amplifiers that meet real-word specifications.

Before lab please read up on electrolytic capacitors:
http://en.wikipedia.org/wiki/Electrolytic_capacitor

The polarity for these types of capacitors is critical to the circuit operating properly. The + terminal must all ways be at a higher potential then the – terminal. If not, the capacitor can become a resistive element, short, open, or even explode. If you have put the wrong polarity on an electrolytic capacitor, throw it away.

A sample circuit showing the proper polarity for a CS amplifier can be seen in Figure 72.

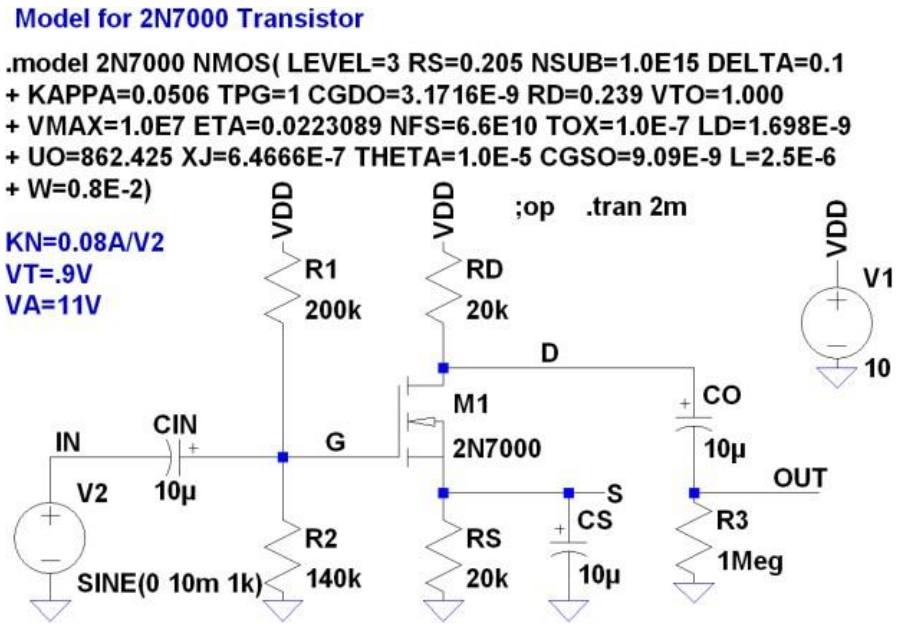


Figure 72: CS Amplifier.

Lab Activities:

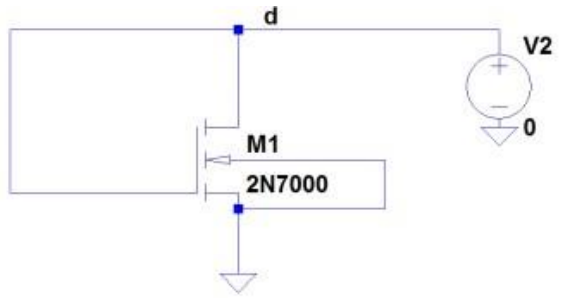
- In LTspice, using NMOS part 2n7000
    a) Extract VT, KN as shown here:
        - Use this file: (You will get different values because the MOSFET model are different KN=.11A/V2, and VT=1.53V for X1=1.70003V, and X2=1.80002.)
        - Note 1: Read Amp1/2 from the right side of the graph.

        ******TA Check point A******

    b) Extract VA as shown here:
        - Use file (Note VG should be set to 2.1V):
        - Note the file you will extract VA for lab is not the same file in the notes. (VT is more accurate to what you will measure in lab.) Depending on where you take your x-y pairs you should get VA=-70V.

        ******TA Check point B******

- Using LT spice create a gm/ID curve:
  a) Diode connect the MOSFET as in file (Figure 73):
  b) Run the simulation and plot Id(M1). You should see Figure 74.




```
.dc v2 0 5
.param W=1600u
.param L=4u

.MODEL 2N7000 NMOS( LEVEL=12  COX   = 3.45E-3  XJ    = 0.15E-6  VTO   = 1.6
+ GAMMA  = 0.71  PHI   = 0.97  KP    = 6.1E-4  E0    = 88.0E6  UCRIT  = 4.5E6
+ DL     = -0.05E-6  DW    = -0.02E-6  LAMBDA = .0025   LETA   = 0.28  WETA   = 0.05
+  LK    = 0.5E-6  IBN   = 1.0  IBA   = 200E6  IBB   = 350E6   TNOM   = 25.0
+ TCV    = 1.5E-3  BEX   = -1.5  UCEX  = 1.7  IBBT  = 0.0  KF    = 1E-27  AF    = 1
+ RSH    = 510  JS    = 8.0E-6  JSW   = 1.5E-10  XTI   = 0  N     = 1.5  CJ    = 8.0E-4
+ CJSW   = 3.0E-10  MJ    = 0.5  MJSW  = 0.3  PB    = 0.9  PBSW  = 0.5  FC    = 0.5
+ CGSO   = 1.5E-10  CGDO  = 1.5E-10  CGBO  = 4.0E-10 )
```

Figure 73: Diode connected MOSFET to extract gm/ID.

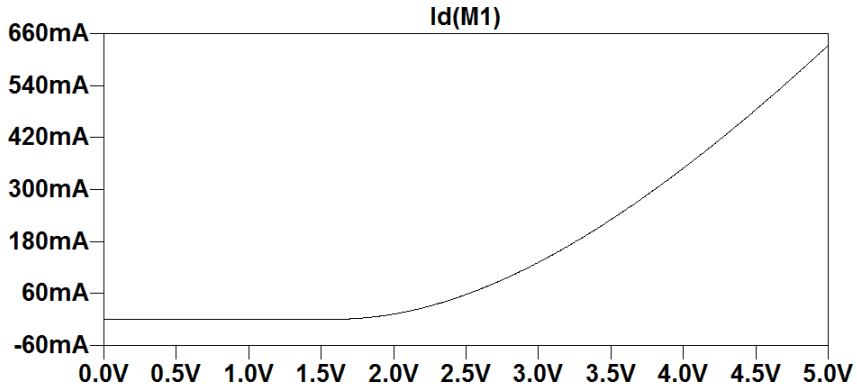


Figure 74: ID vs VDS for a 2N7000 Diode Connected MOSFET.

  c) Left click on the x-axis and in the quantity plotted pop-up enter in Id(M1) to plot the current. Click OK. You should see Figure 75.

d) Left click again on the x-axis and this time click plot logarithmically in the pop up. You should see Figure 76.

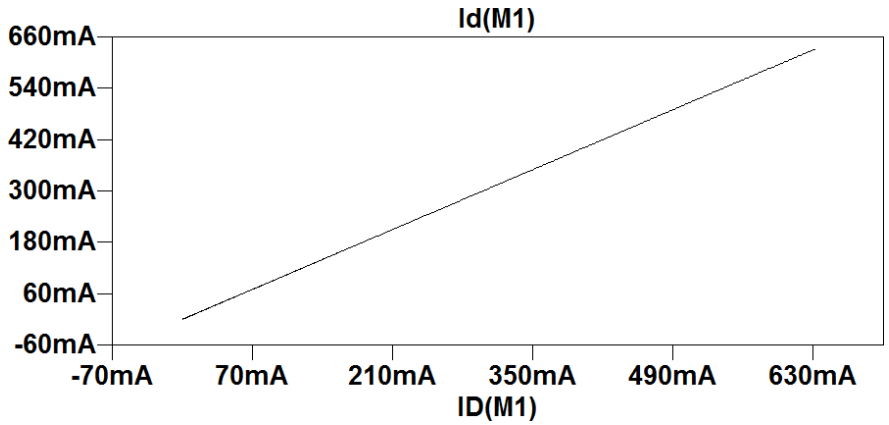


Figure 75: Plotting current on the x-axis.

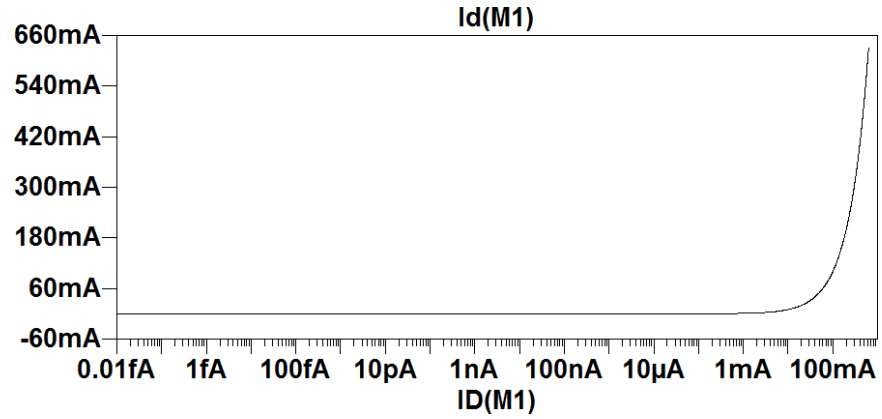


Figure 76: Changing the x-axis to plot logarithmically.

e) Go to plot settings and then add trace in the pop-up type: d(Id(m1))/Id(m1). d(Id(m1)) means take the derivative of the drain current of MOSFET M1. Delete the Id(M1) current plot. You should see Figure 77.

f) You have to scale the y-axis properly because gm/id goes to infinity when the drain current goes to zero.

g) Left click on the y axis and select logarithmic plotting and for the top type in 100 and the bottom type in 1. Leave the tick alone. You should see Figure 78.

- Left click on the x-axis again and enter in the left limit to be 10nA. You should see Figure 79.

  ******TA Check point C******

h) In order to bias a transistor, we need to know VGS. To get the VGS=VDS that caused a particular ID, go to plot setting and add plot plane. Plot VD, and scale it linearly as shown in Figure 80.

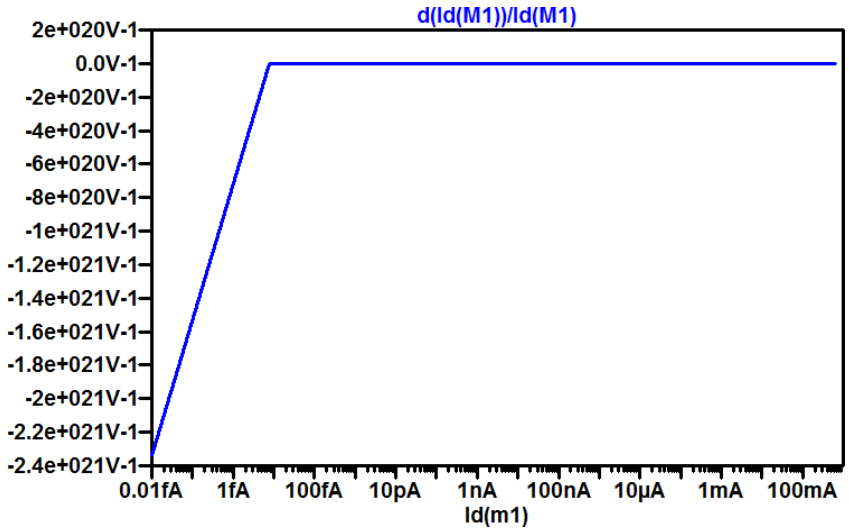


Figure 77: Non-scaled gm/ID plot.

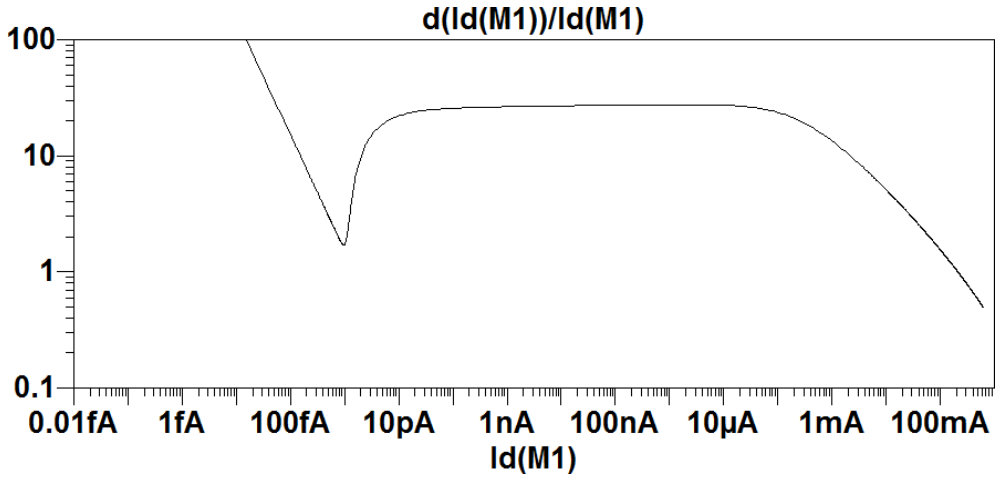


Figure 78: Almost properly scaled gm/ID plot.

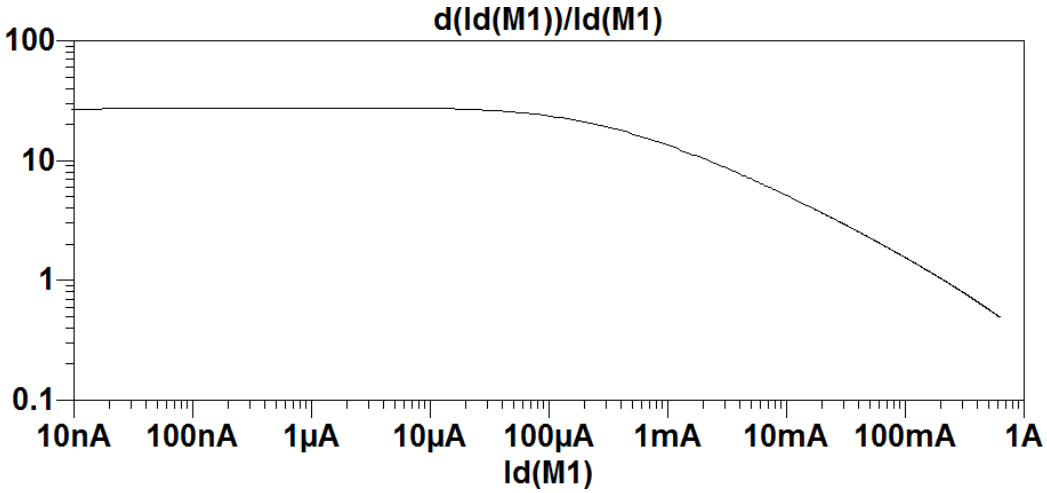


Figure 79: Properly scaled gm/ID plot.

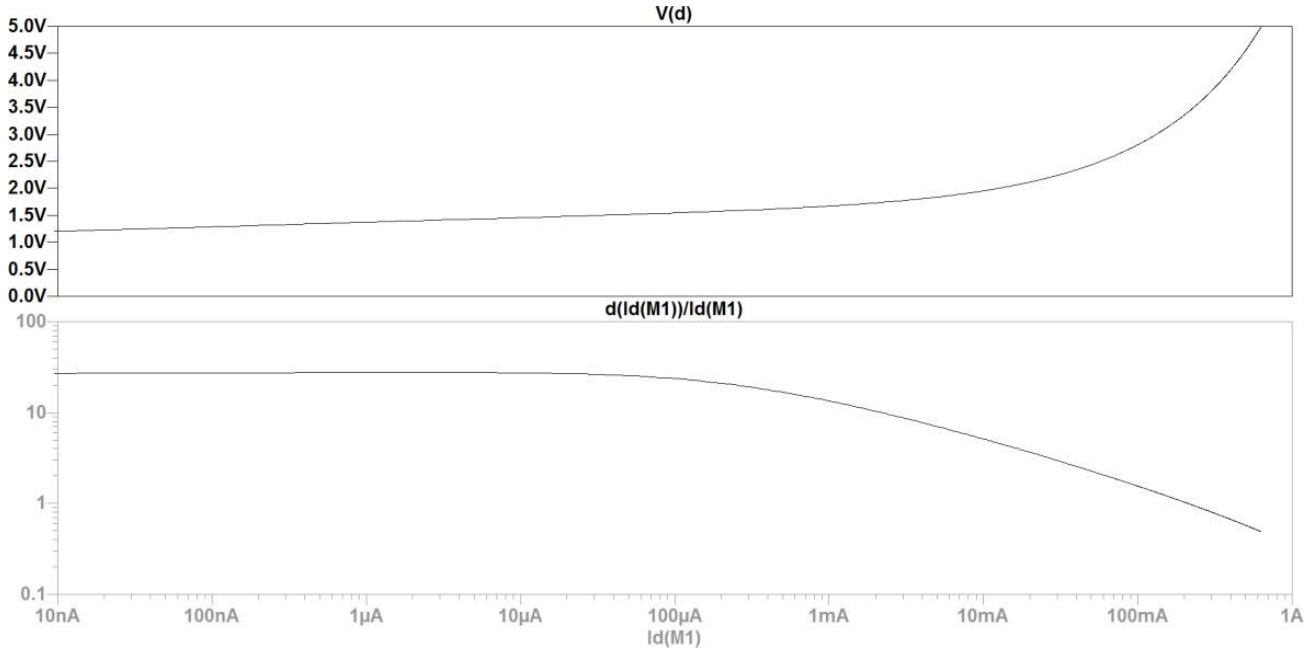


Figure 80: Gm/ID plot with VDS=VGS.

- Design example: Design a CS amplifier using the 2n7000 for maximum gain. Read though the following:

If we want maximum gain, that implies we use the CS amplifier structure that shorts RS at AC. The gain equation becomes:

$$A_V = -g_m(R_D||r_o||R_L)$$

If we assume that the load is a non-inverting amplifier, we can assume R_L is infinite, and that it drops out. We can assume that we want R_d to be 1/10 of r_o so that variance in r_o does not affect the circuit as much. We can re-write the gain equation to be:

$$Av = -g_m r_o/10$$

$$r_o = V_A/I_D$$

$$Av = -g_m V_A/(10*I_D)$$

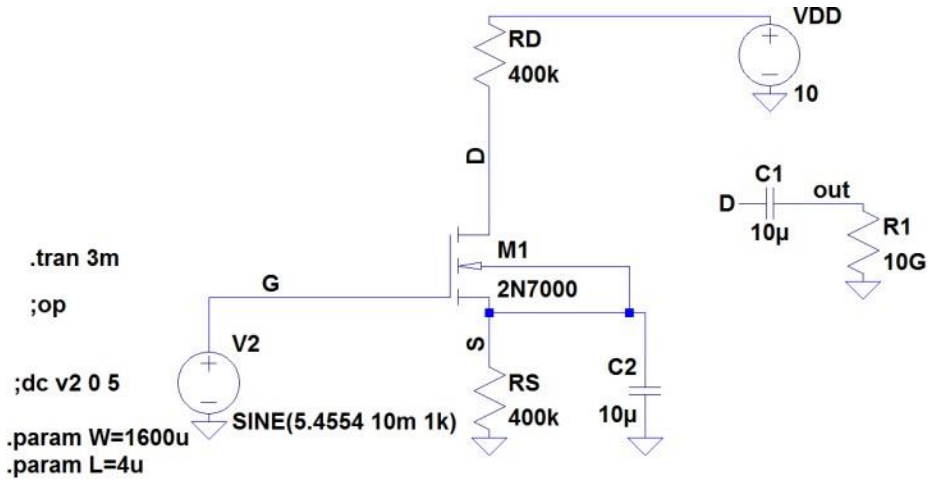
The gain becomes the value you read off the g_m/I_D chart times V_A divided by 10. Assuming V_A is 40V and the maximum g_m/I_D from the plot is 27.5. The maximum gain is -27.5×40/10=-110.

Pick I_D to be equal 10uA, then V_{GS} is 1.4554Volts. (Use the chart you generated.) $R_D=V_A/10/I_D$=40/10/10e-6=400kΩ.

For good DC stability, set R_S=400kΩ.
$V_G=V_{GS}+I_D\times R_S$=1.4554+10e-6×400× 103=5.4554.

We are in subthreshold so the VDS>VGS-VT assumption is not true. VDS min is about .2V. If the input is a 10mV signal VDS has to swing 2×10mV×110=2.2 Volt. The VDS needed to design the power supply is VDD=IDxRD+VDS+IDRS=4+2.2+.2+4=10.4V, which we can round to 11V.

a. Build the rapid prototype in spice by using a DC offset instead of R1, and R2 to set the DC bias level. (Figure 81).
b. Simulate the DC operating point, by running an .op simulation. You should get the results shown in Table 2.




```
.MODEL 2N7000 NMOS( LEVEL=12  COX    = 3.45E-3  XJ    = 0.15E-6  VTO   = 1.6
+ GAMMA  = 0.71  PHI    = 0.97  KP    = 6.1E-4  E0    = 88.0E6  UCRIT = 4.5E6
+ DL     = -0.05E-6  DW    = -0.02E-6  LAMBDA = .0025   LETA   = 0.28  WETA   = 0.05
+  LK    = 0.5E-6  IBN    = 1.0  IBA    = 200E6  IBB    = 350E6   TNOM   = 25.0
+ TCV    = 1.5E-3  BEX    = -1.5  UCEX   = 1.7  IBBT   = 0.0  KF    = 1E-27  AF    = 1
+ RSH    = 510  JS    = 8.0E-6  JSW    = 1.5E-10  XTI    = 0  N    = 1.5  CJ    = 8.0E-4
+ CJSW   = 3.0E-10  MJ    = 0.5  MJSW   = 0.3  PB    = 0.9  PBSW   = 0.5  FC    = 0.5
+ CGSO   = 1.5E-10  CGDO   = 1.5E-10  CGBO   = 4.0E-10 )
```

Figure 81: CS amplifier for maximum gain.

Table 2: Operating Point for CS amplifier.

V (d):	5.99956	voltage
V (g):	5.4554	voltage
V (s):	4.00044	voltage
V (n001):	10	voltage
V (out):	5.99956e-007	voltage
I (C2):	-4.00044e-017	device_current
I (C1):	-5.99956e-017	device_current
I (R1):	5.99956e-017	device_current
I (Rs):	1.00011e-005	device_current
I (Rd):	1.00011e-005	device_current
I (V2):	0	device_current

I (Vdd):	-1.00011e-005	device_current
Id (M1):	1.00011e-005	device_current
Ig (M1):	0	device_current
Ib (M1):	-8.88473e-011	device_current
Is (M1):	-1.0001e-005	device_current

c) The results in Table 2 should match the hand calculations well. Run a transient simulation for 3ms and plot V(OUT). You should see Figure 82.

******TA Check point D******

d) While you can use an offset voltage with a function generator you should, design the bias network, R1 and R2 according to this: Note that in the above schematics R1 is the load resistor. https://dl.dropbox.com/u/35091424/EE122/gmID for designing CS amplifiers.pdf

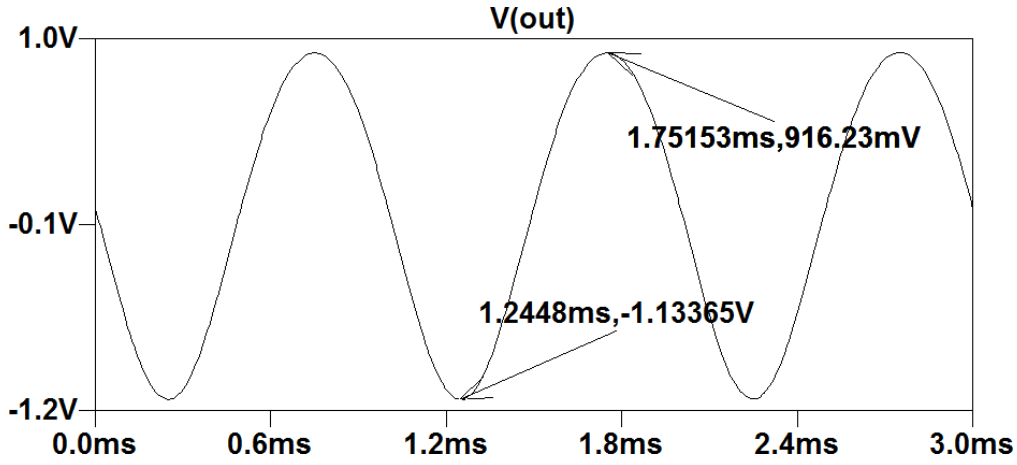


Figure 82: Transient simulation of CS amplifier.

- Using the Gm/ID method design and verify in LTspice a CS amplifier with a gain of -50. Select R1 and R2 according to this link.

******TA Check point E******

- Using the Gm/ID method design and verify in LT spice a CS amplifier with a gain of -10 that has a non-zero source resistance in the AC model. Select R1 and R2 according to link.

******TA Check point F******

Lab report:

NA: Show results for check pints A, B, C, D, E, and F to your TA as you do the lab.

Chapter 8:
Testing and documenting CS amplifiers.

Week 8

Pre-Lab:

Using hand calculations and LTspice, check how the gain varies for the two designs from the last lab if the resistors have a 5% tolerance, and if VTH changes by 20%.

Lab Activities:

To get a "feel" for statistics of the threshold voltage for discrete MOSFETs:

- Measure VTH of at least 10 2n7000 MOSFETS. The 2n7000 and 2n7002 are the same but the 2n7002 has a tighter control of VTH. (You need to find the data sheet on your own.)

- Use a voltmeter as RD

- Connect one side of the voltmeter to the power supply (greater than 5 volts)

- Connect the negative side of the voltmeter to the drain.

- Connect the source to ground and the negative side of the power supply to ground.

- V_{TH} will be approximately $V_{powersupply}$-$V_{voltmeter}$.

- Calculate the mean and standard deviation of the threshold voltage.

- Put this data into the lab report. Use the data to analysis why theory did not match simulation.

- Fabricate and test the two CS designs you did last week.

Lab Report

- Make sure to explain any variations between what you measured and what you observed.
- The lab report will use the theory and LTspice simulations/schematics you did last week.

Chapter 9:
Simulation and Testing of
OPAMP Multivibrator

Week 9

Introduction

While using just a few components, an Opamp multivibrator circuit can provide a good rectangular wave as an output signal. It uses three resistors and a timing capacitor. Opamp multivibrator is an astabe oscillator circuit which uses a RC timing network circuit connected to the inverting end and a voltage divider circuit at its non-inverting end.

Astable multivibrator is a circuit which switches continuously between the two unstable states without the need for any external triggering.

Pre-Lab

The configuration we will be using is based on Schmitt Trigger and it will then act as a comparator circuit. To generate hysteresis, the below given figure uses two resistors R1 and R2 at the positive feedback side. As this resistive network is connected between the amplifiers output and non-inverting (+) input, when Vout is saturated at the positive supply rail, a positive voltage is applied to the op-amps non-inverting input. Likewise, when Vout is saturated to the negative supply rail, a negative voltage is applied to the op-amps non-inverting input.

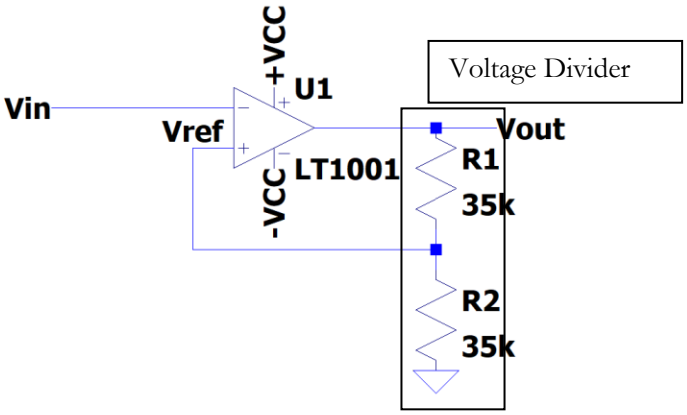


Figure 83: Opamp configuration as a Schmitt Trigger

So, generally we use the above configuration of Opamp as a Schmitt Trigger to convert any periodic waveform into a rectangular waveform.

Lab Exercises

1. Go to add a component and click on opamps, and then on the LT1001

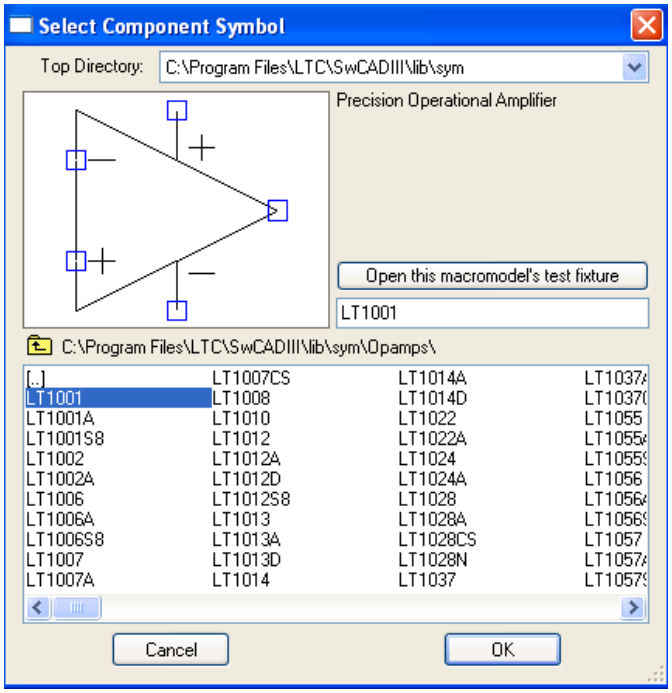


Figure 84: Selecting Opamp from the Component list

2. Design the below given circuit of opamp multivibrator in LTspice and perform simulation.

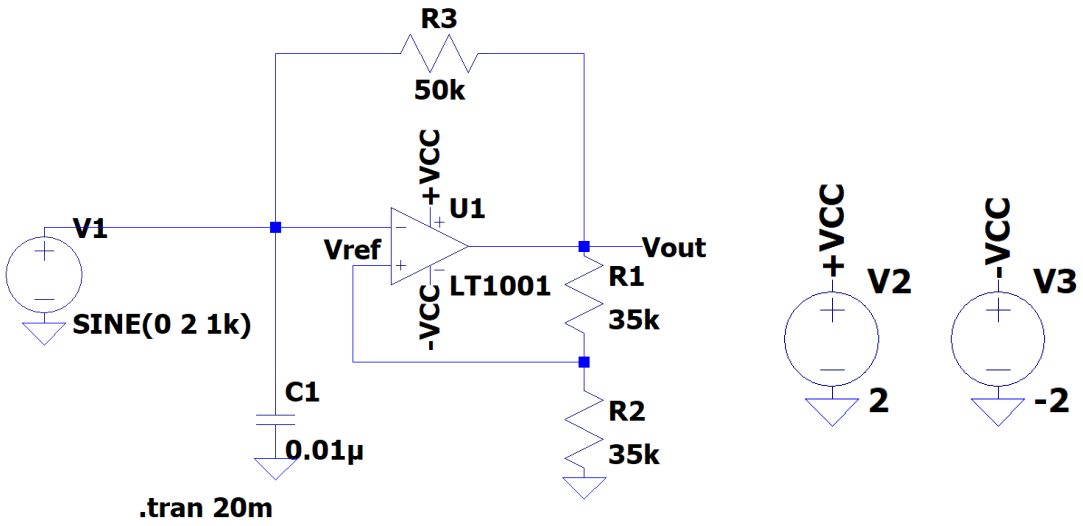


Figure 85: Opamp Multivibrator

3. Provide sine wave to the input and check the output. You should get a rectangular wave as shown in Figure 87.

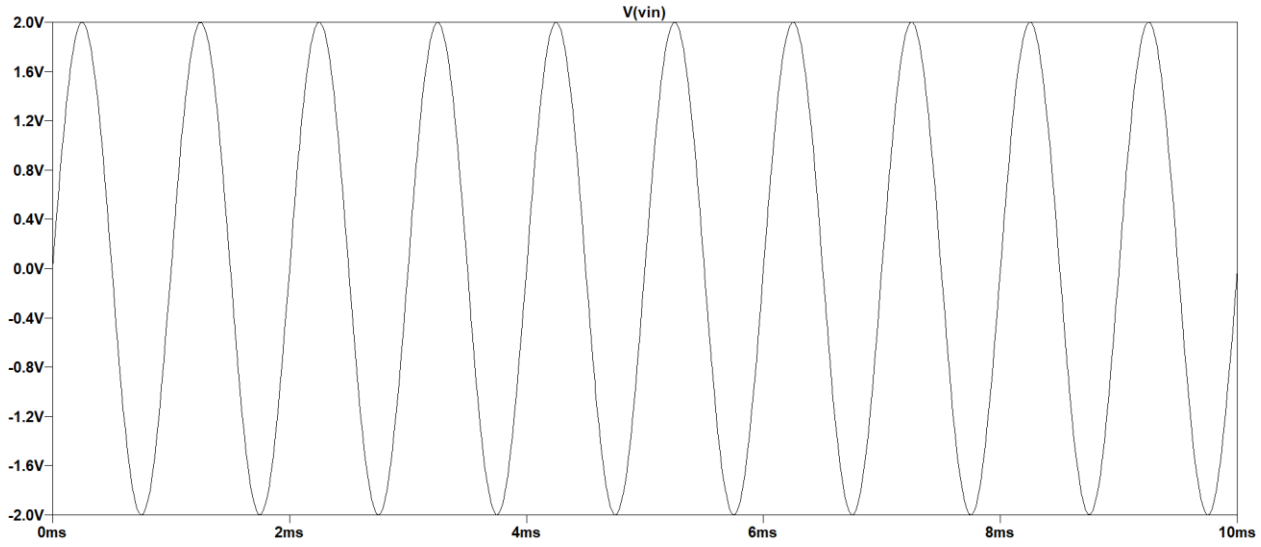


Figure 86: Input sine wave

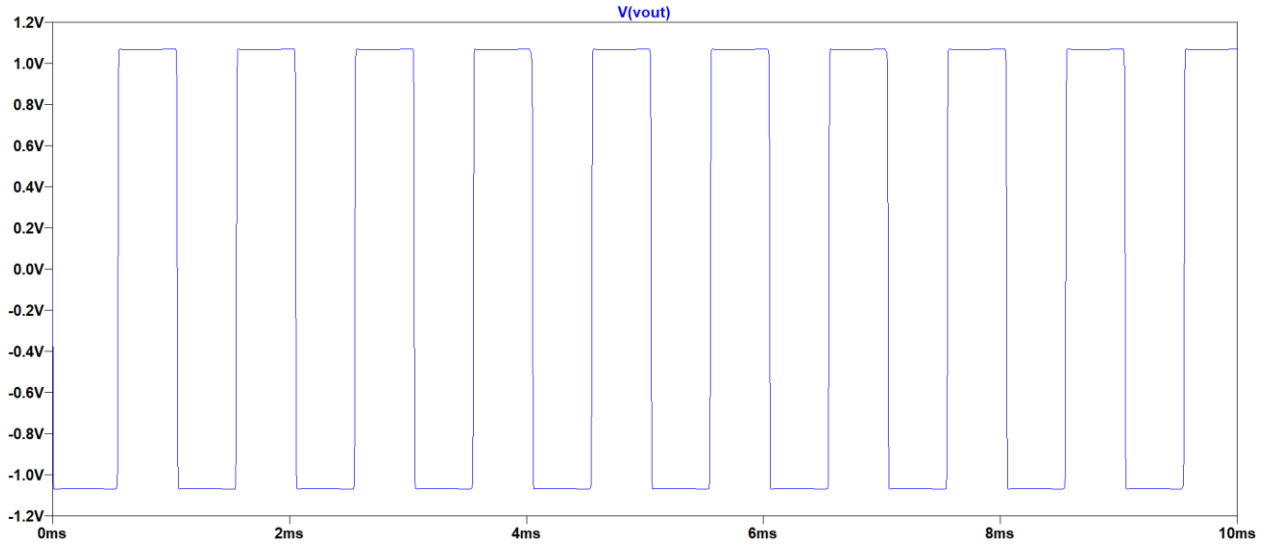


Figure 87: Output waveform at V(Vout)

4. Modify the above given circuit and add a potentiometer. Steps of creating a potentiometer can be found **here.** Check by changing the R and Val value of the potentiometer to 10ohm, 70V and 5kohm, 70V.

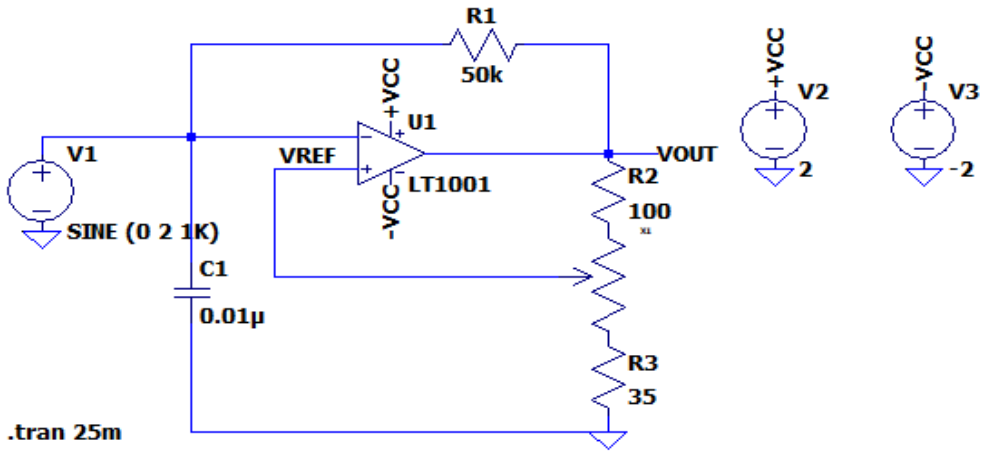


Figure 88: Opamp Multivibrator with Potentiometer

5. Test and fabricate Figure 85 onto the proto board/bread board. And check the output waveform in the oscilloscope.
6. Compare the waveform from LTspice with the one saved from oscilloscope. State the reason if they are not same.

Lab Report:

1. Submit the Report with all the required screenshots and the waveforms.
2. Include the photos of the testing circuit (made on proto board).
3. Also, include the screen grab of the waveform from the oscilloscope after testing the circuit.

Chapter 10:
Review Session

Week 10

Lab:

This session is an optional session to clear your doubts. Prepare the questions in advance and ask them to the TA. Questions must be related to EE122L in this session. Also, any suggestions and recommendations related to EE122L are welcome.

APPENDIX:

(Additional Information on Soldering)

Energy Harvesting PCB assembly and test

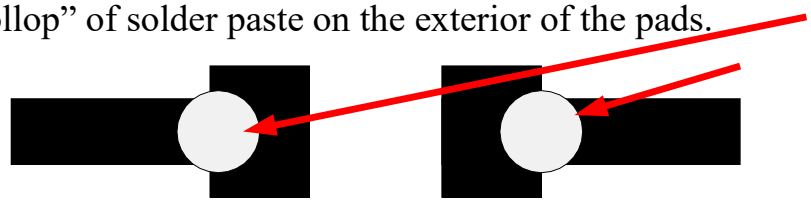
Introduction:

This lab is an extension of the DipTrace lab where you designed the PCB layout and now, the same will be used for further assembling and testing using soldering tools. All the required equipment and tools will be provided to you prior to the start of the session. This lab will be guided by the soldering experts and the TAs will help you to complete the lab. There will be a small presentation at the start of the lab session.

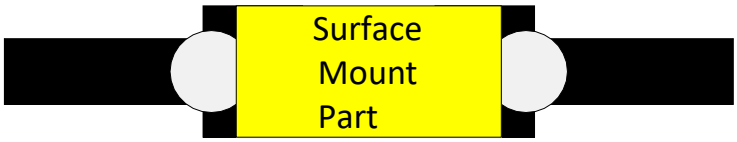
The lab will consist of training how to use the surface mount soldering stations, followed by you assembling your PCB, and ending with the testing of your design. An example of an application note is the actual design note for the LTC 3105 that we used for our design.

Attaching surface mount parts:

Add “dollop” of solder paste on the exterior of the pads.



Place surface mount part so it slightly touches paste.



BILLS OF MATERIALS:

1. Inductors:	
10 uH - For Soldering	**10 uH (Note the inductor looks like a resistor)**
2. Resistors:	
1 MegΩ 1% (size 0402) (1) – For Soldering	**250 kΩ 1% (size 0402) (1) – For Soldering**
40.2 kΩ 1% (size 0402) (1) – For Soldering	**500 Ω (1)**
400 KΩ (2)	**10 GΩ (1)**
35 KΩ (2)	**50 kΩ (1)**
3. Capacitors:	
10 uF (size 0805) (2) – For Soldering	**1 uF (size 0805) (1) – For Soldering**
10 uF (2)	**0.01uF (1)**
4. LTC3105 –MSOP-12 – For Soldering	**LTC3105 IC (1) – For Breadboard**
5. Solar Panel (1) with (Vin and Vout pin connections) – For Breadboard	
6. Solar Panel (1) – for Soldering	
7. USB (1) – For Soldering	
8. Proto board/ bread board (1)	
9. Connecting wires	
10. Diode: 1N4148 (1)	
11. MOSFET: 2N7000 (1)	
12. OPAMP: LT1001/LT1006 (1)	
13. Analog Device ADALM2000 PCIe measurement unit (+/-5 V adjustable DC supply with proper frequency range) (1)	
14. Soldering Equipment – Contact Audrey for the list of required equipment	