### **UPG** básica

In/Alu⊠≻ WrD⊠-

CIk⊠≻

@A 3

WR-OUT

# Formato Instrucciones SISA-I

| 15 | 14 | 13 | 12 | 11 | 10     | 9   | 8 | 7     | 6  | 5  | 4  | 3   | 2  | 1                   | 0              | Name                              | Mnemonic                                     |
|----|----|----|----|----|--------|-----|---|-------|----|----|----|-----|----|---------------------|----------------|-----------------------------------|--|
| 0  | 0  | 0  | 0  | а  | а      | а   | b | b     | b  | d  | d  | d   | f  | f                   | f              | Logic and Aritmetic<br>Operations | AND, OR, XOR, NOT,<br>ADD, SUB, SHA, SHL     |
| 0  | 0  | 0  | 1  | а  | а      | а   | b | b     | b  | d  | d  | d   | f  | f                   | f              | Compare Signed and Unsigned       | CMPLT, CMPLE, -, CMPEQ, CMPLTU, CMPLEU, -, - |
| 0  | 0  | 1  | 0  | а  | а      | а   | d | d     | d  | n  | n  | n   | n  | n                   | n              | Add Immediate                     | ADDI   |
| 0  | 0  | 1  | 1  | α  | а      | а   | d | d     | d  | n  | n  | n   | n  | n                   | n              | Load                              | LD   |
| 0  | 1  | 0  | 0  | а  | а      | а   | b | b     | р  | n  | n  | n   | n  | n                   | n              | Store                             | ST   |
| 0  | 1  | 0  | 1  | а  | а      | а   | d | d     | d  | n  | n  | n   | n  | n                   | n              | Load Byte                         | LDB  |
| 0  | 1  | 1  | 0  | а  | а      | а   | b | b     | b  | n  | n  | n   | n  | n                   | n              | Store Byte                        | STB  |
| 0  | 1  | 1  | 1  |    |        |     |   |       |    |    |    |     |    |                     |                |                                   | Branch future extension                      |
| 1  | Λ  | 0  | 0  | 1  | _      | 0   | 0 | n:    | 20 | 20 | 20 | n   | n  | n                   | n              | Branch on Zero                    | BZ   |
| Т  | U  |    |    | a  | a      | ı a | 1 |       | 11 | 11 | 11 |     |    |                     |                | Branch on Not Zero                | BNZ  |
| 1  | 0  |    |    | d  | d      | d   | 0 |       |    |    |    |     |    |                     | Move Immediate | MOVI                              |  |
|    |    | 0  | 1  |    | a<br>d | -   | 1 | nnnn  |    | n  | n  | n r | n  | Move Immediate High | MOVHI          |                                   |  |
| 1  | 0  | 1  | 0  | d  | d      | d   | 0 | n n   | 2  | 20 | 20 | Σ.  | ~  | 20                  | <b>5</b>       | Input                             | IN   |
|    |    | т  | U  | а  | а      | а   | 1 | 11 11 |    | 11 | 11 | 11  | 11 | 11                  | 11             | Output                            | OUT  |
| 1  | 0  | 1  | 1  |    |        |     |   |       |    |    |    |     |    |                     |                |                                   | Future extensions                            |

@A @B @B Rb/N Rb/N Rb/N

WrD

Wr-Out Rd-In

Byte

Wr-Mem

-/i/l/a **-i** @D

→ WrD

→ Wr-Out

→ Wr-Mem

→ Rd-In

#### **Funcionalidades ALU**

INSTRUCTION MEMORY

ADDR-I-MEM

| İ     | F     |          | OP |             |              |          |  |  |  |  |
|-------|-------|----------|----|-------------|--------------|----------|--|--|--|--|
| $b_2$ | $b_1$ | $b_0 \\$ | 11 | 10          | 01           | 00       |  |  |  |  |
| 0     | 0     | 0        |    | Х           | CMPLT (X,Y)  | AND(X,Y) |  |  |  |  |
| 0     | 0     | 1        |    | Υ           | CMPLE (X,Y)  | OR(X,Y)  |  |  |  |  |
| 0     | 1     | 0        |    | MOVHI (X,Y) |              | XOR(X,Y) |  |  |  |  |
| 0     | 1     | 1        |    |             | CMPEQ (X,Y)  | NOT(X)   |  |  |  |  |
| 1     | 0     | 0        |    |             | CMPLTU (X,Y) | ADD(X,Y) |  |  |  |  |
| 1     | 0     | 1        |    |             | CMPLEU (X,Y) | SUB(X,Y) |  |  |  |  |
| 1     | 1     | 0        |    |             |              | SHA(X,Y) |  |  |  |  |
| 1     | 1     | 1        |    |             |              | SHL(X,Y) |  |  |  |  |

## Lógica de control del SISC Harvard Uniciclo

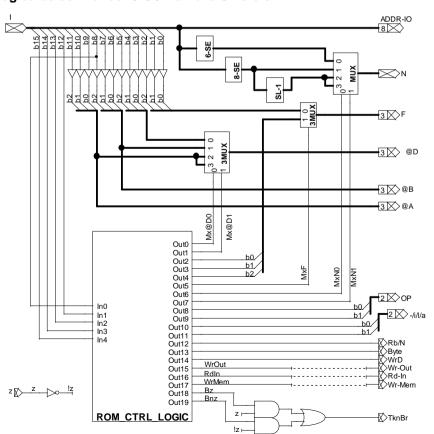
1 0 MUX

RD-IN

1 0 MUX

REGFILE

WrD D



**√**3 @D

**-**√3 @B

**∞** N

1 1 x x

# Computador SISC Harvard Uniciclo (UCG + UPG + IO + MEM)

REG

TknBr

