# LECTURE 03 - DEEP SUBMICRON (DSM) CMOS TECHNOLOGY

## LECTURE ORGANIZATION

**Outline**

- Characteristics of a deep submicron CMOS technology
- Typical deep submicron CMOS technology
- Summary

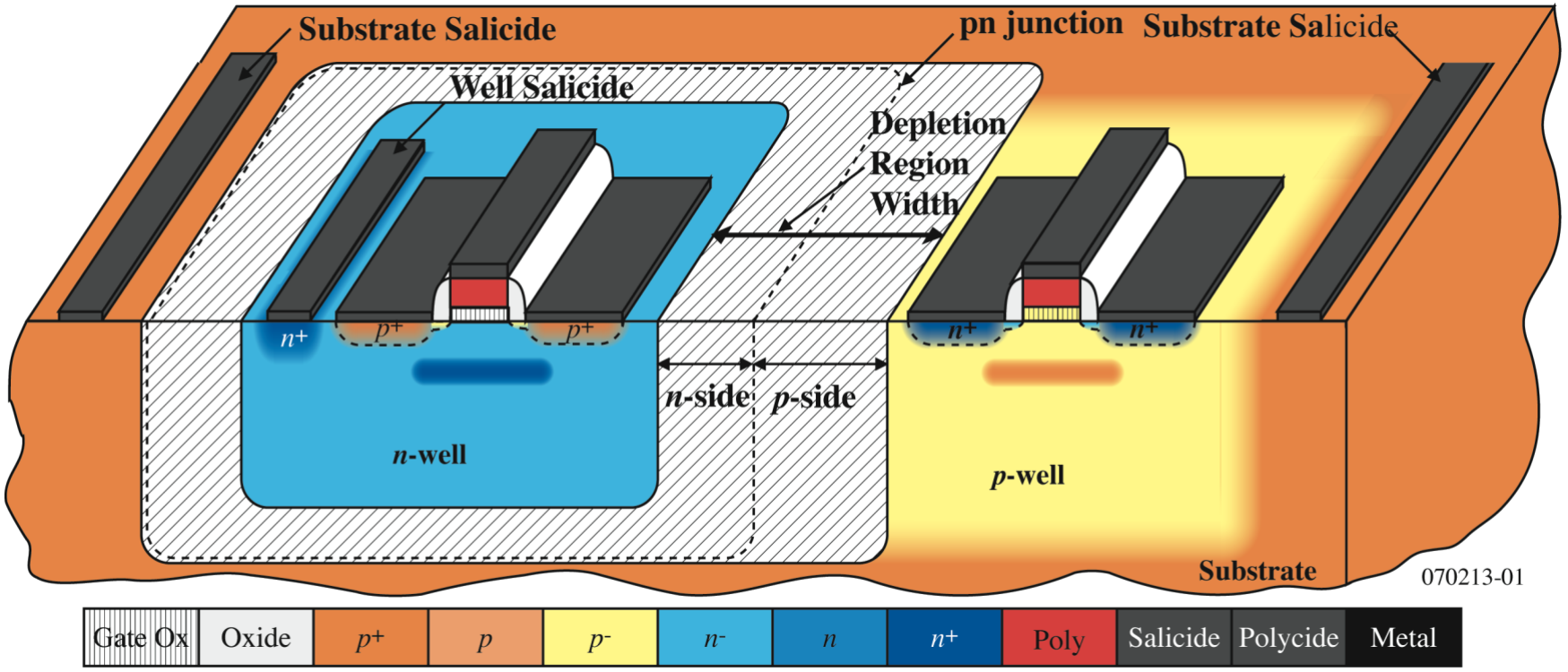
***CMOS Analog Circuit Design*, 3rd Edition Reference**

New material

# CHARACTERISTICS OF A DEEP SUBMICRON CMOS TECHNOLOGY

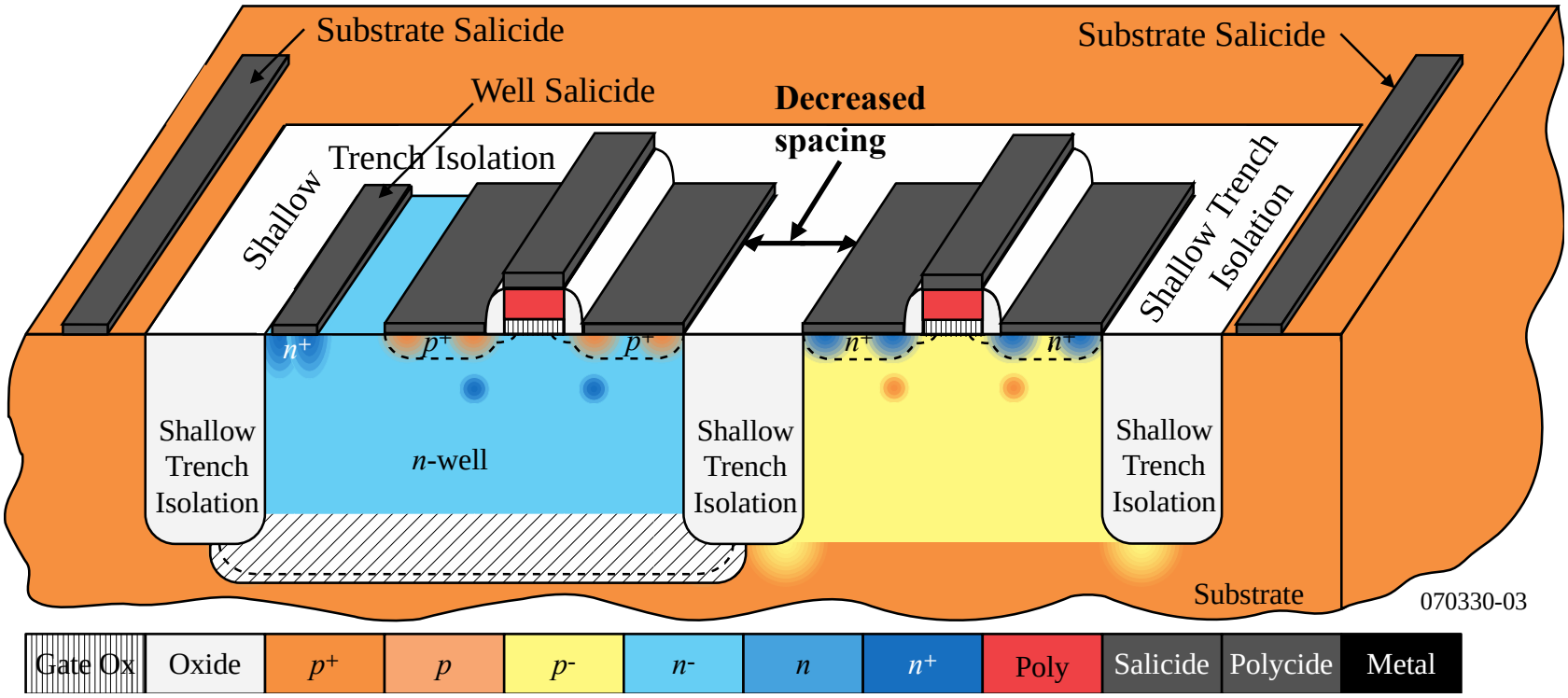
## Isolation of Transistors

The use of reverse bias pn junctions to isolate transistors becomes impractical as the transistor sizes decrease.



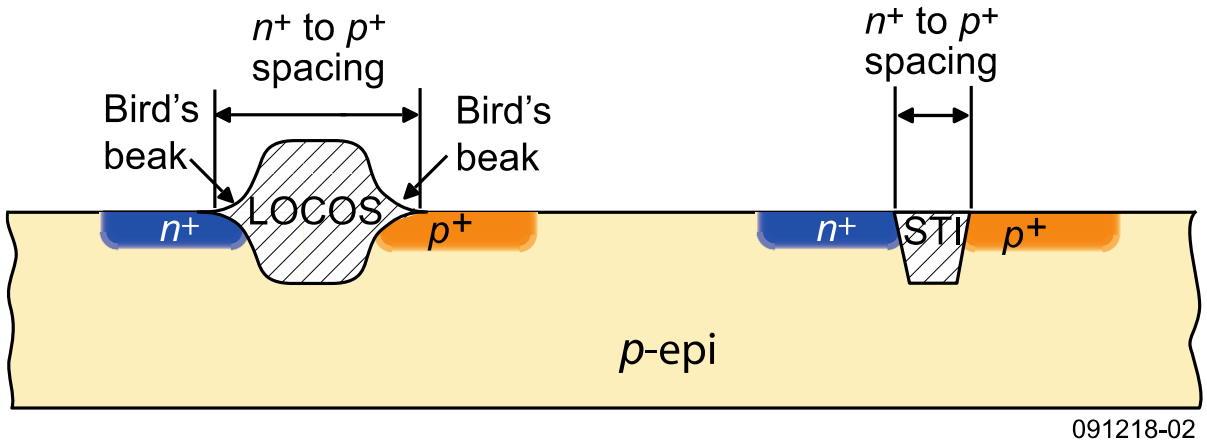
# Use of Shallow Trench Isolation Technology

Shallow trench isolation (STI) allows closer spacing of transistors by eliminating the depletion region at the surface.



## Comparison of STI and LOCOS

What are the differences between a LOCOS and STI technology?




Comments:

- If the $n^+$ to $p^+$ spacing is large, the Bird's beak can be compensated using techniques such as poly buffered LOCOS
- At some point as the $n^+$ to $p^+$ spacing gets smaller, the restricted bird's beak leads to undesirable stress effects in the transistor.
- An important advantage of STI is that it minimizes the heat cycle needed for $n^+$ or $p^+$ isolation compared to LOCOS. This is a significant advantage for any process where there are implants before STI.

## Shallow Trench Isolation (STI)

1.) Cover the wafer with pad oxide and silicon nitride.

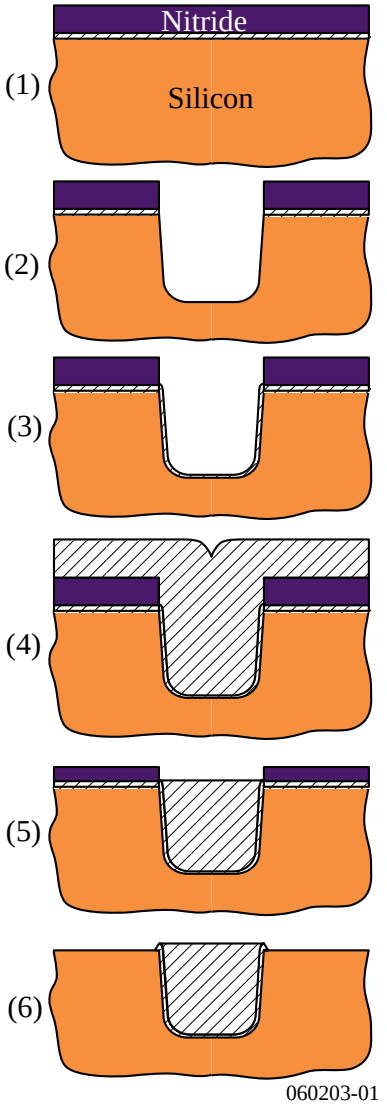
2.) First etch nitride and pad oxide. Next, an anisotropic etch is made in the silicon to a depth of 0.4 to 0.5 microns.

3.) Grow a thin thermal oxide layer on the trench walls.

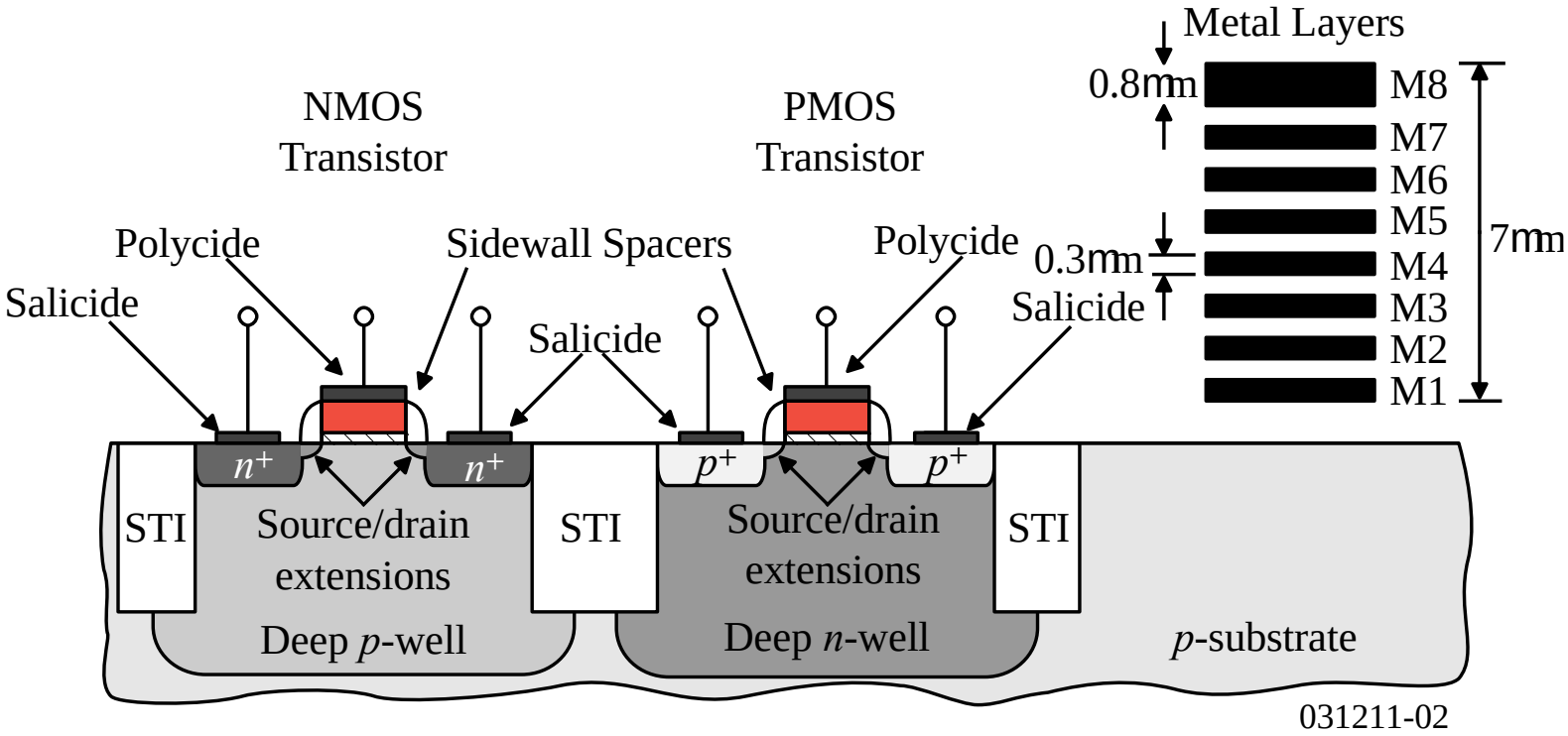
4.) A CVD dielectric film is used to fill the trench.

5.) A chemical mechanical polishing (CMP) step is used to polish back the dielectric layer until the nitride is reached. The nitride acts like a CMP stop layer.

6.) Densify the dielectric material at 900°C and strip the nitride and pad oxide.



# Illustration of a Deep Submicron (DSM) CMOS Technology




In addition to NMOS and PMOS transistors, the technology provides:

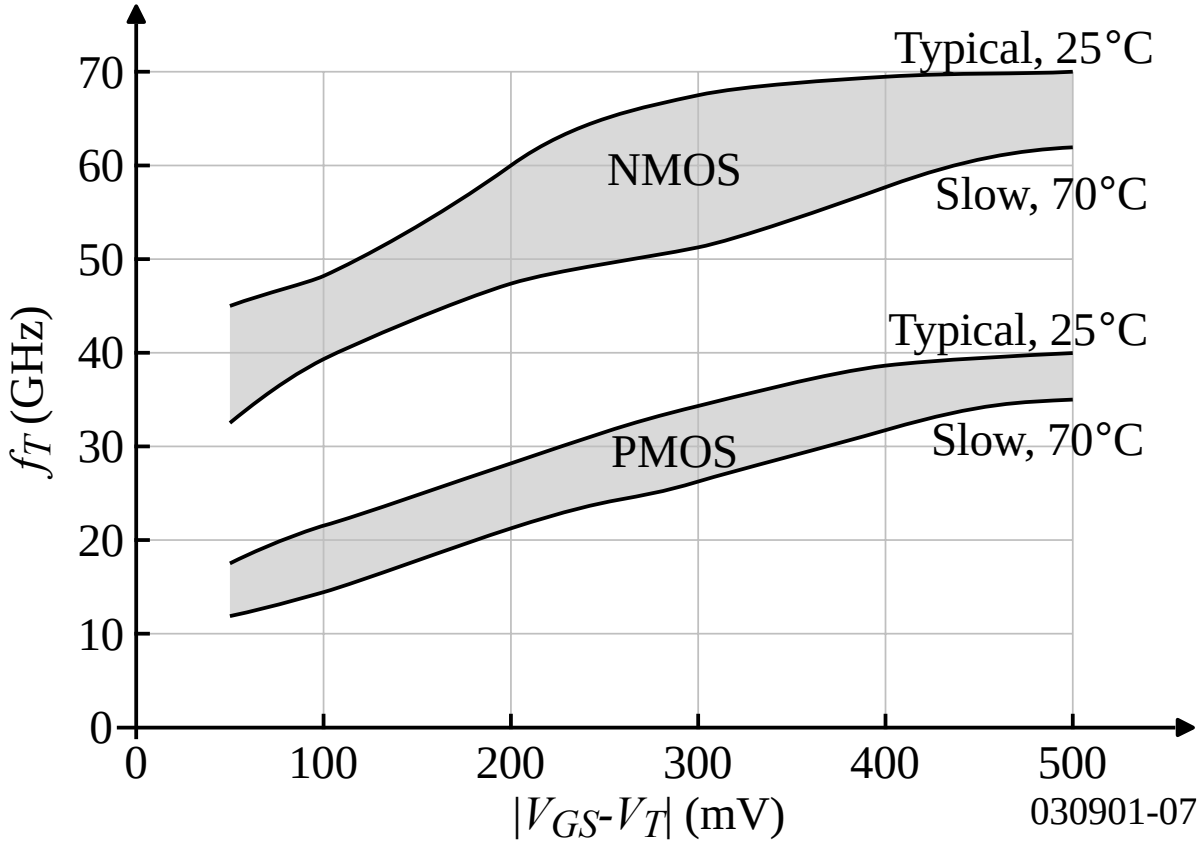
1.) A deep *n*-well that can be utilized to reduce substrate noise coupling.

2.) A MOS varactor that can serve in VCOs

3.) At least 6 levels of metal that can form many useful structures such as inductors, capacitors, and transmission lines.

## Transistors

$f_T$ as a function of gate-source overdrive, $V_{GS}$-$V_T$ (0.13µm):




The upper frequency limit of the transistors varies with overdrive and process corners. The NMOS transistor has an $f_T$ of 40GHz at low overdrives and increases to above 60GHz at the slow-high temperature corner with 0.5V overdrive.

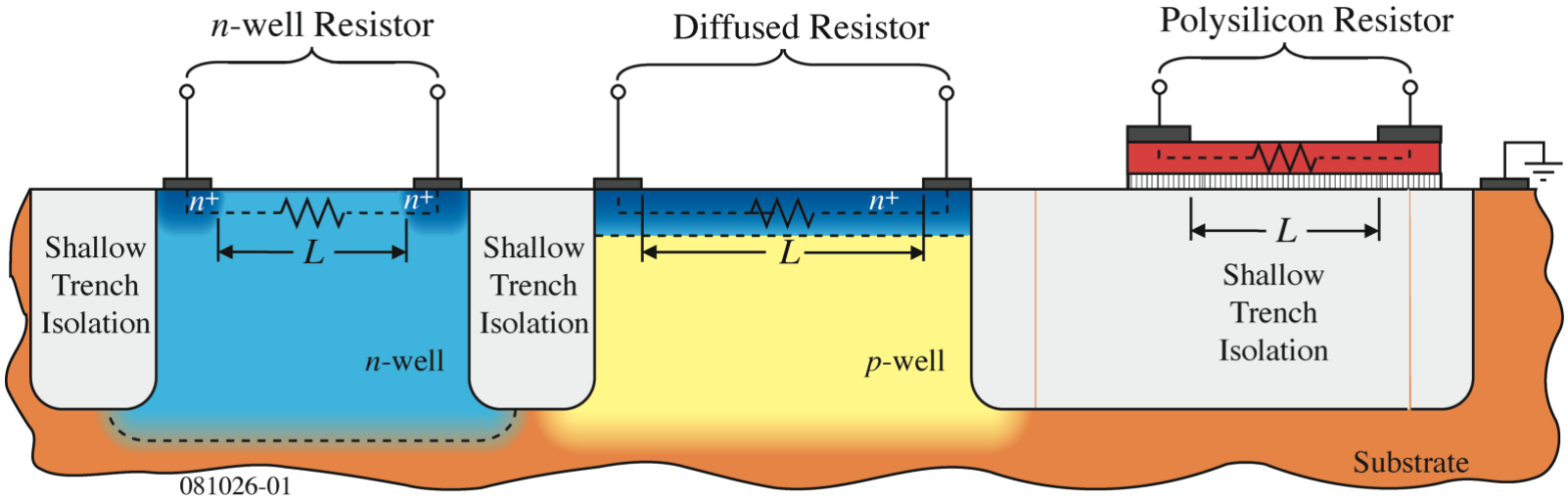
# Resistors

1.) Diffused and/or implanted resistors.

2.) Well resistors.

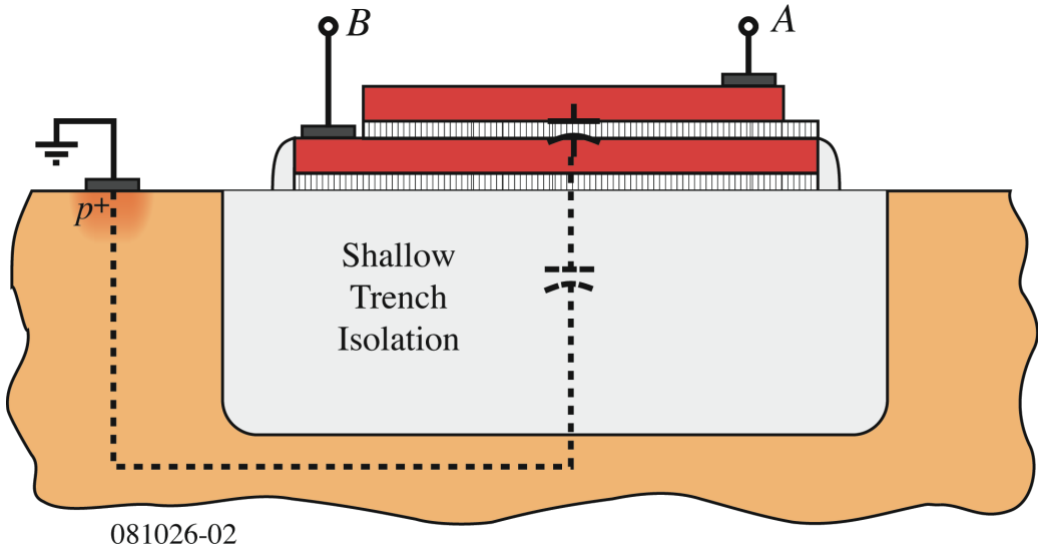
3.) Polysilicon resistors.

4.) Metal resistors.

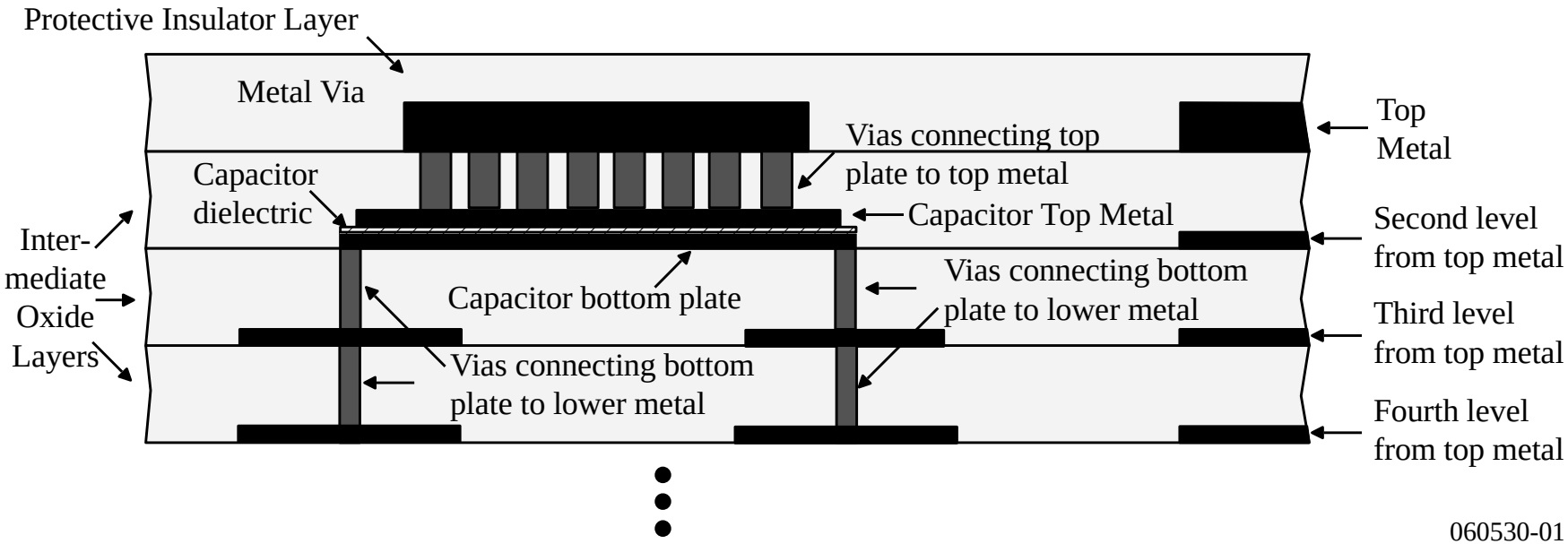


# Capacitors

Polysilicon-polysilicon capacitors:

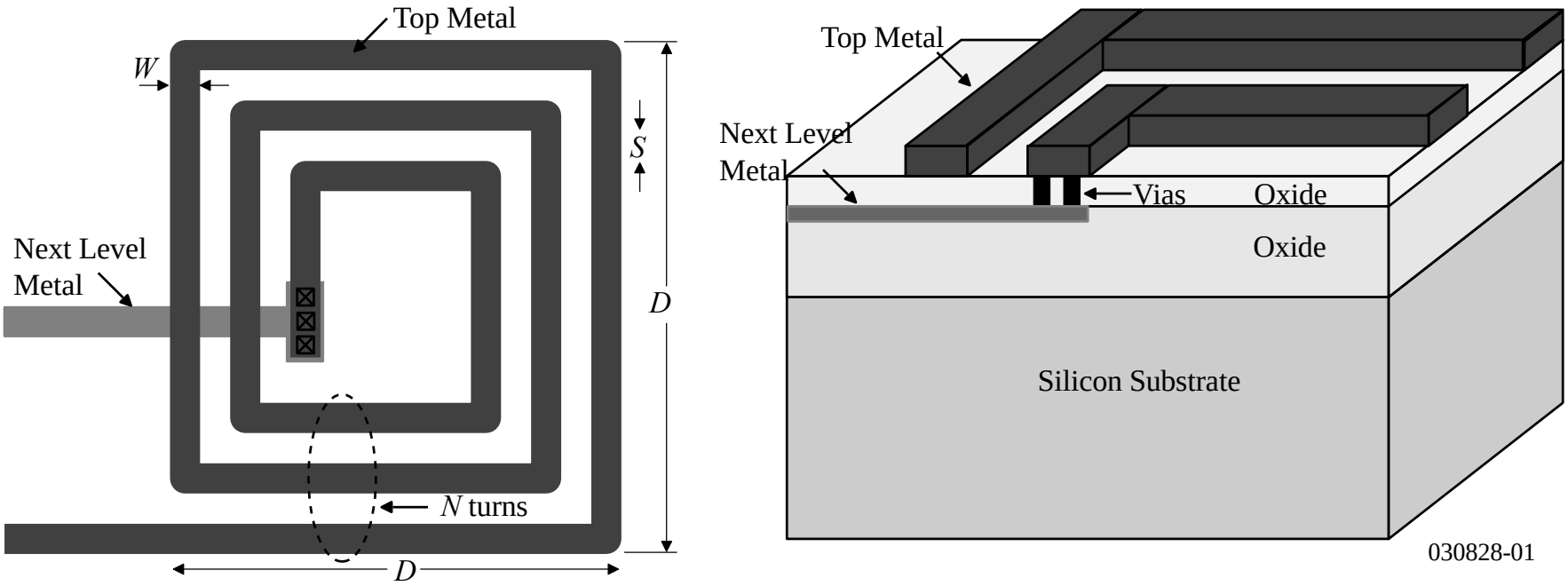



Metal-metal capacitors:

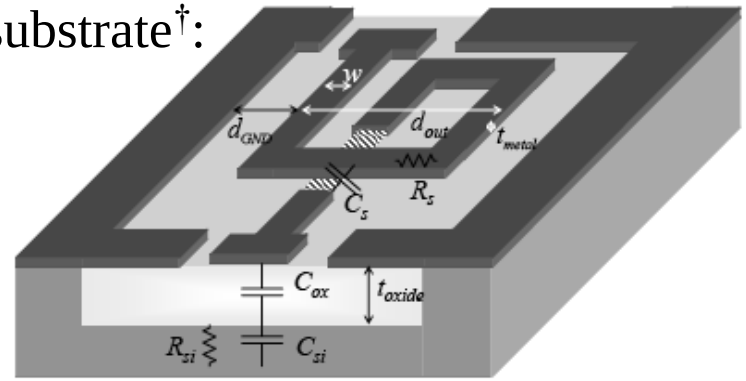


# Inductors

Top view and cross-section of a planar inductor:




Enhanced inductor removing the substrate†:




†M. Raieszadeh, Integrated Inductors on Trenched Silicon Islands, MS Thesis, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2005

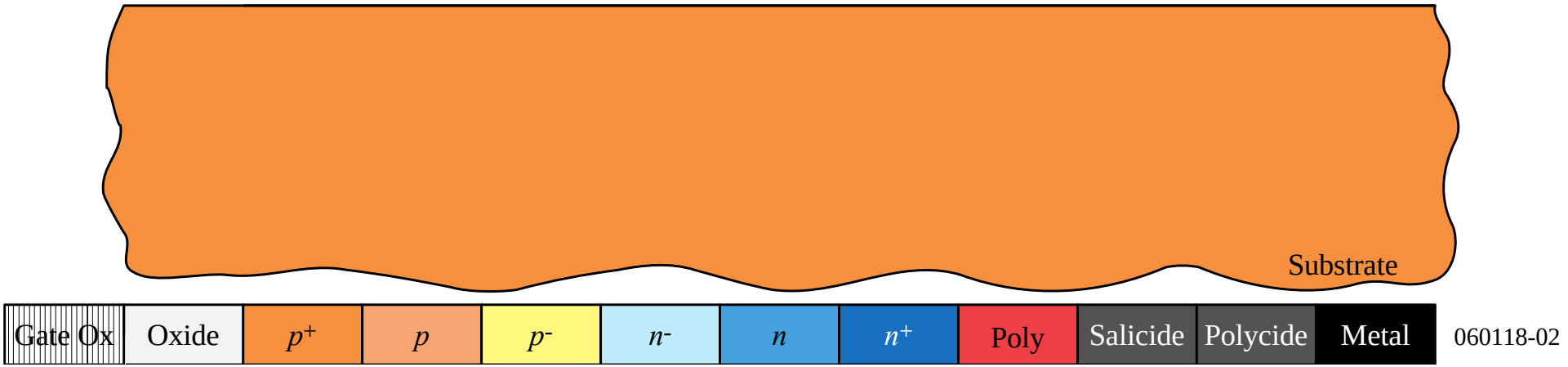
# TYPICAL DEEP SUBMICRON (DSM) CMOS FABRICATION PROCESS

## Major Fabrication Steps for a DSM CMOS Process

1.) *p* and *n* wells
2.) Shallow trench isolation
3.) Threshold shift and anti-punch through implants
4.) Thin oxide and gate polysilicon
5.) Lightly doped drains and sources
6.) Sidewall spacer
7.) Heavily doped drains and sources
8.) Siliciding (Salicide and Polycide)
9.) Bottom metal, tungsten plugs, and oxide
10.) Higher level metals, tungsten plugs/vias, and oxide
11.) Top level metal, vias and protective oxide

## Starting Material

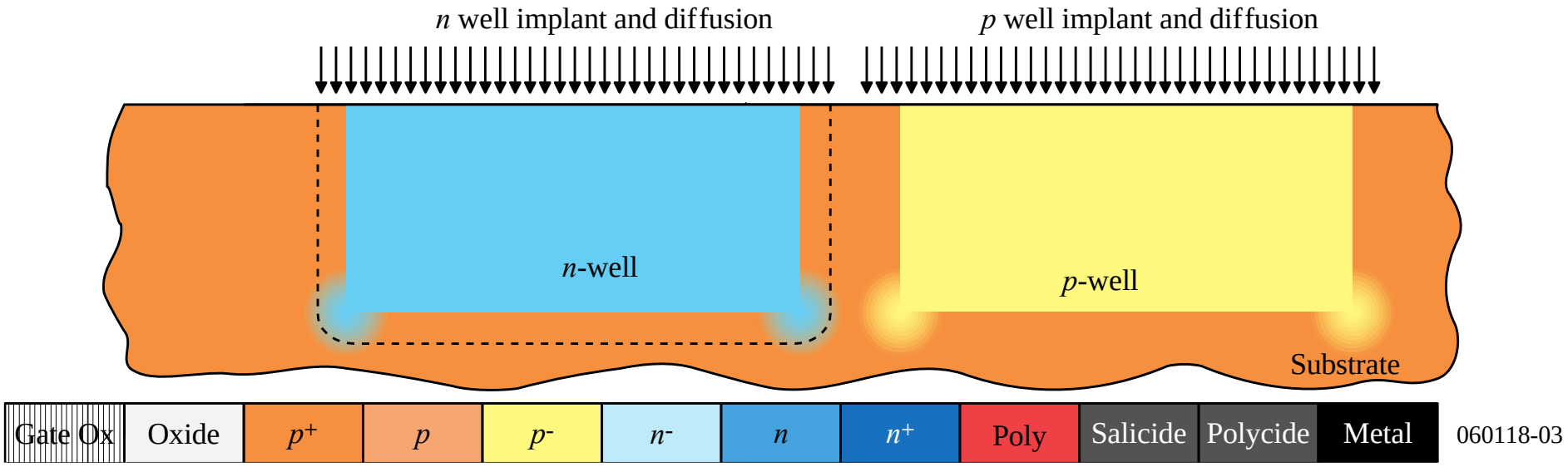
The substrate should be highly doped to act like a good conductor.



## Step 1 - *n* and *p* wells

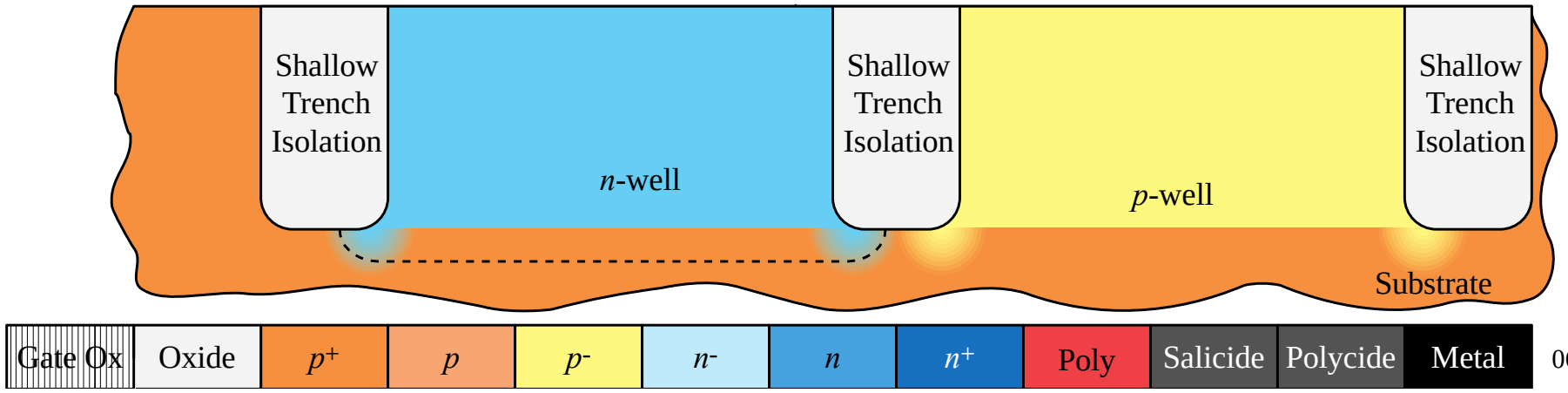
These are the areas where the transistors will be fabricated - NMOS in the *p*-well and PMOS in the *n*-well.

Done by implantation followed by a deep diffusion.



## Step 2 – Shallow Trench Isolation

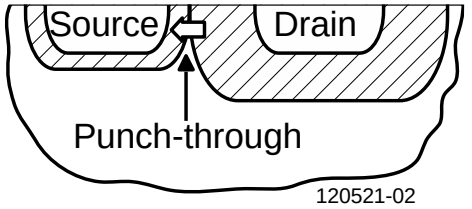
The shallow trench isolation (STI) electrically isolates one region/transistor from another.

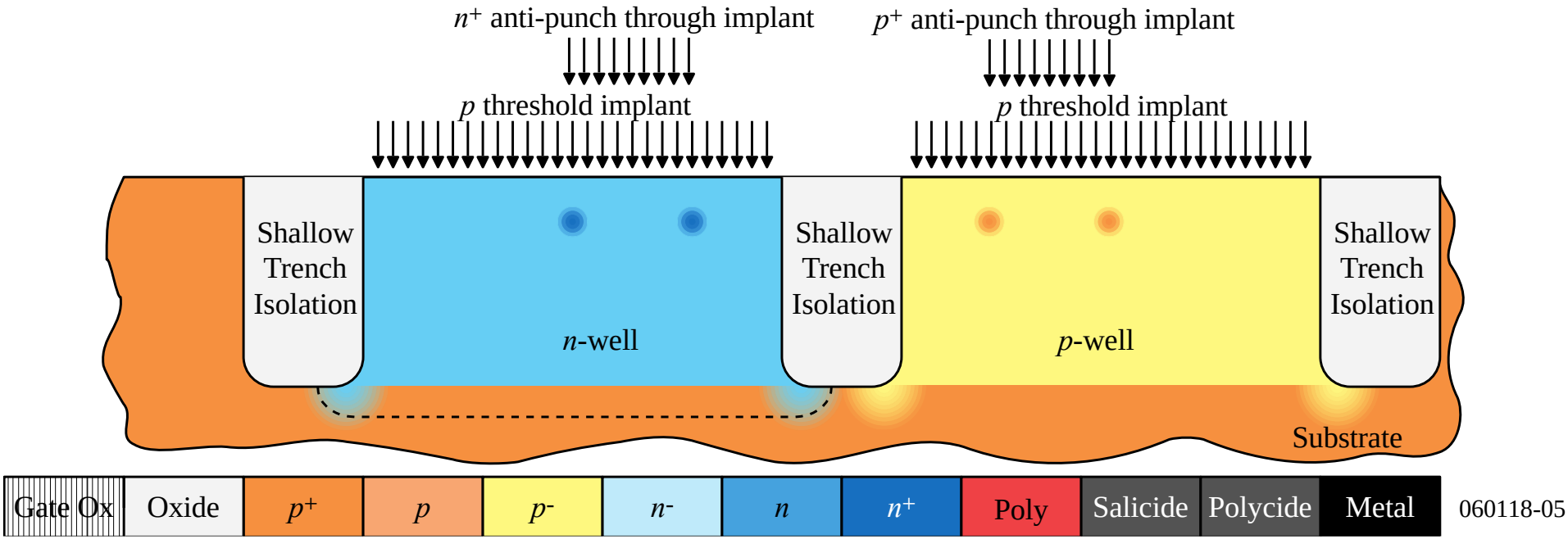


## Step 3 – Threshold Shift and Anti-Punch Through Implants

The natural thresholds of the NMOS is about 0V and of the PMOS is about –1.2V. An *p*-implant is used to make the NMOS harder to invert and the PMOS easier resulting in threshold voltages balanced around zero volts.

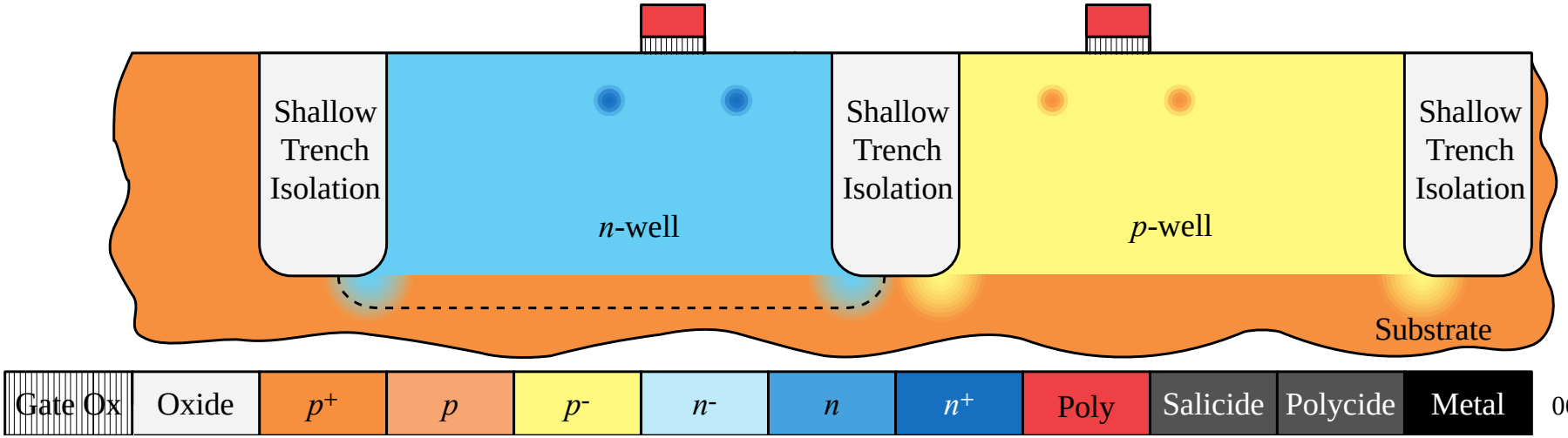
Also an implant can be applied to create a higher-doped region beneath the channels to prevent punch-through from the drain depletion region extending to source depletion region.



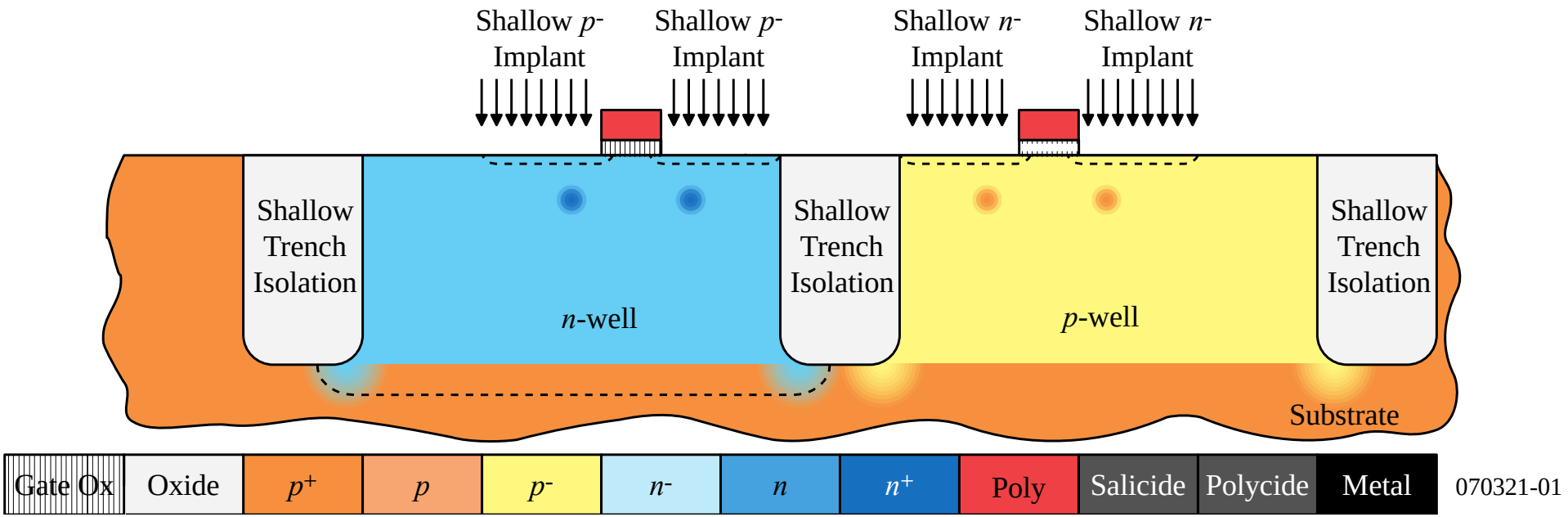
## Step 4 – Thin Oxide and Polysilicon Gates

A thin oxide is deposited followed by polysilicon. These layers are removed where they are not wanted.



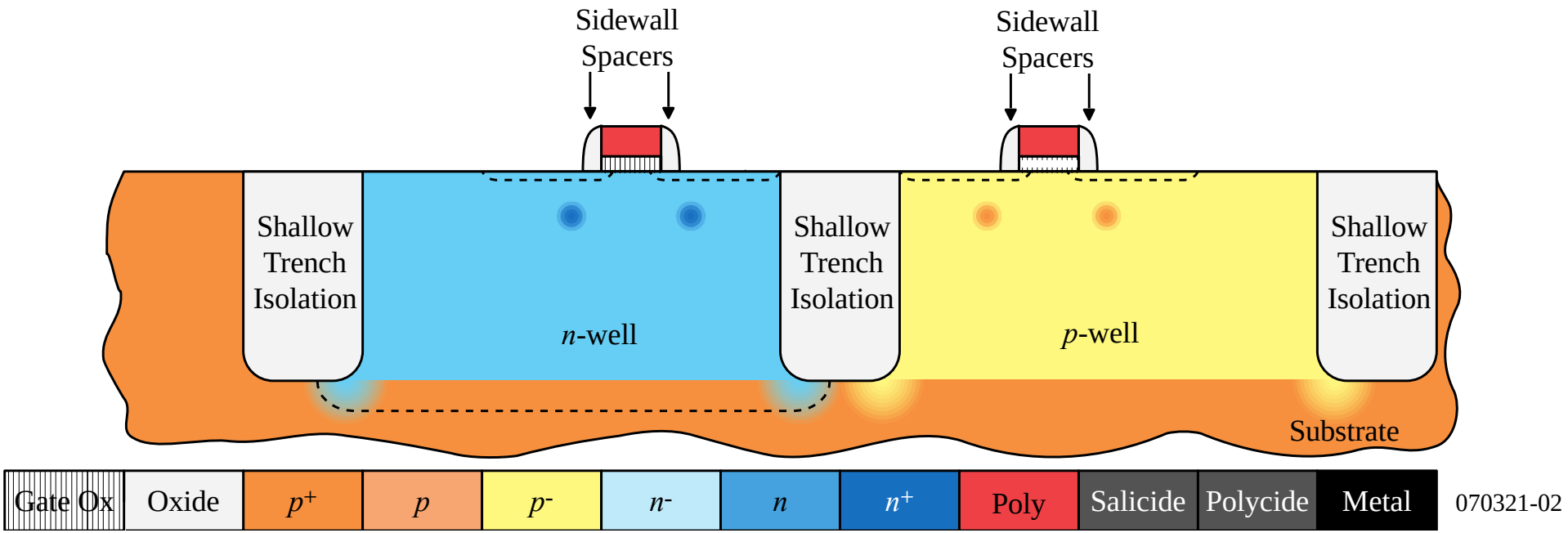
## Step 5 – Lightly Doped Drains and Sources

A lightly-doped implant is used to create a lightly-doped source and drain next to the channel of the MOSFETs.



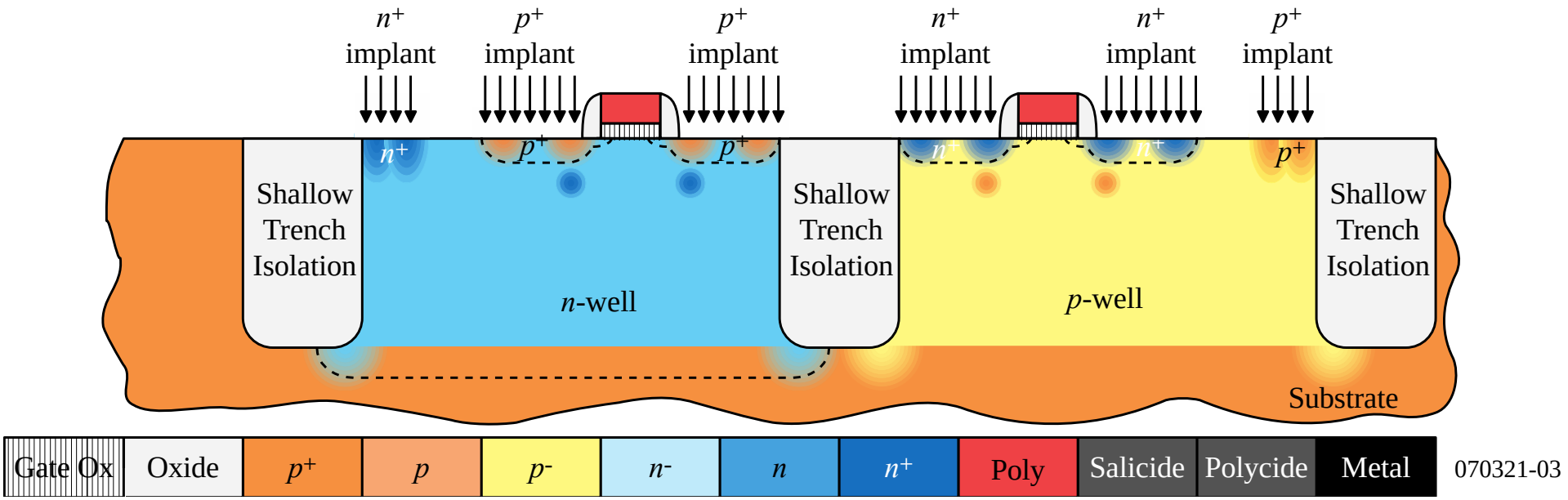
## Step 6 – Sidewall Spacers

A layer of dielectric is deposited on the surface and removed in such a way as to leave "sidewall spacers" next to the thin-oxide-polysilicon-polycide sandwich. These sidewall spacers will prevent the part of the source and drain next to the channel from becoming heavily doped.



## Step 7 – Implantation of the Heavily Doped Sources and Drains

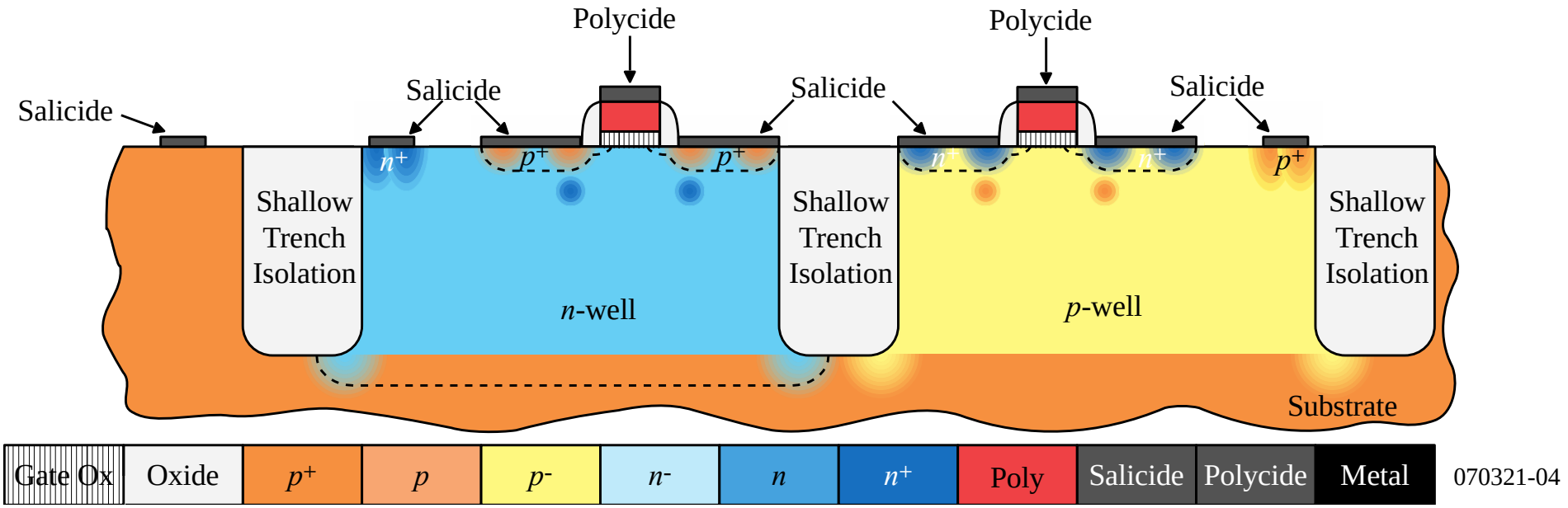
Note that not only does this step provide the completed sources and drains but allows for ohmic contact into the wells and substrate.



## Step 8 – Siliciding (Salicide and Polycide)

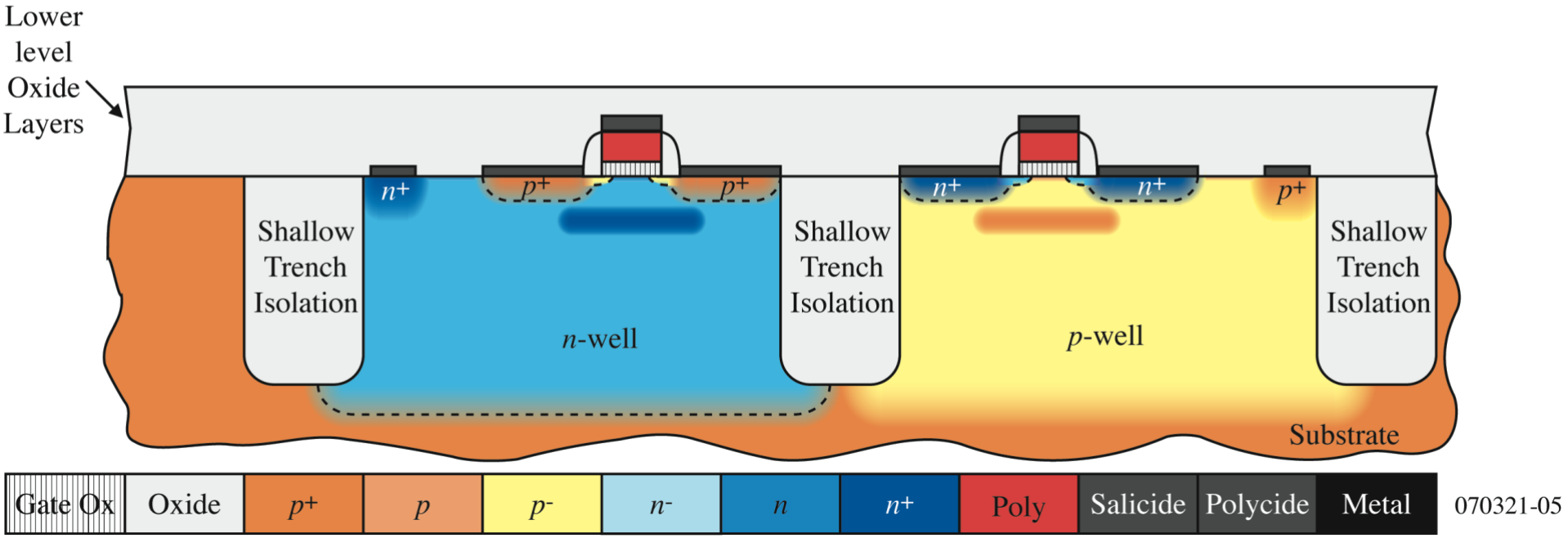
This step reduces the resistance of the bulk diffusions and polysilicon and forms an ohmic contact with material on which it is deposited.

Salicide = Self-aligned silicide



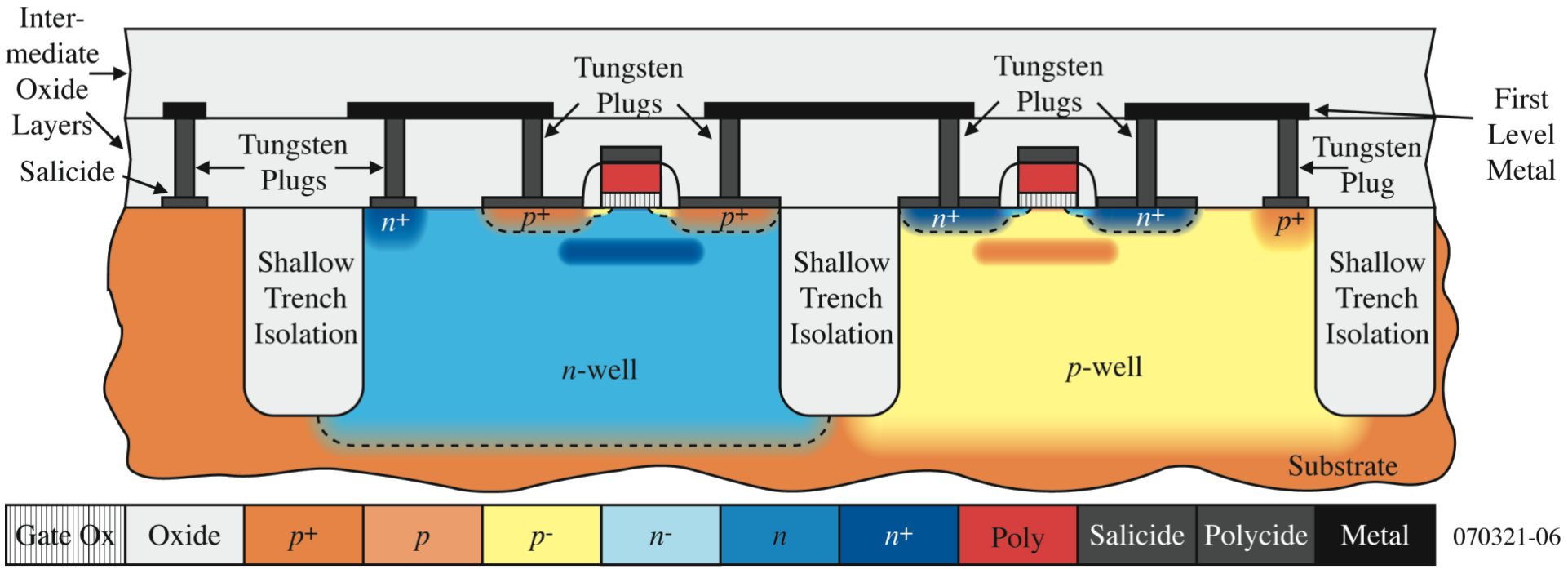
## Step 9 – Intermediate Oxide Layer

An oxide layer is used to cover the transistors and to planarize the surface.



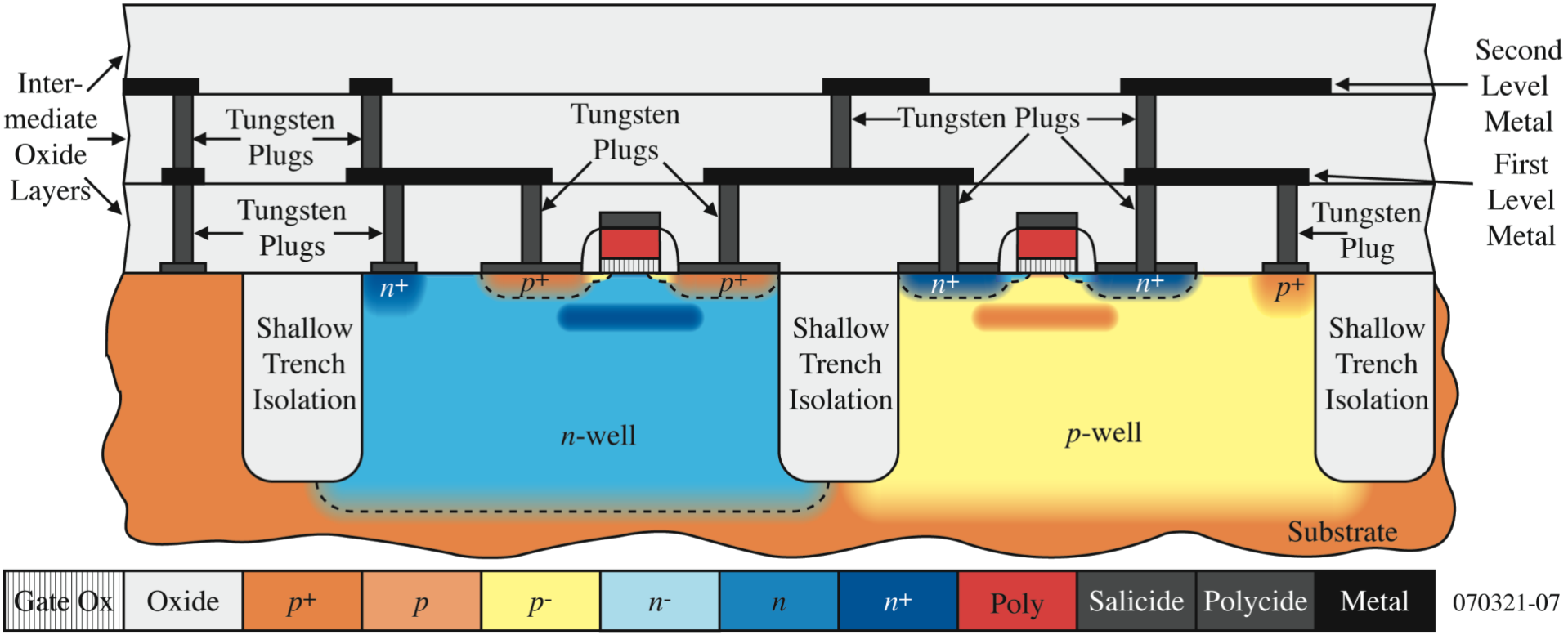
## Step 10- First-Level Metal

Tungsten plugs are built through the lower intermediate oxide layer to provide contact between the devices, wells and substrate to the first-level metal.



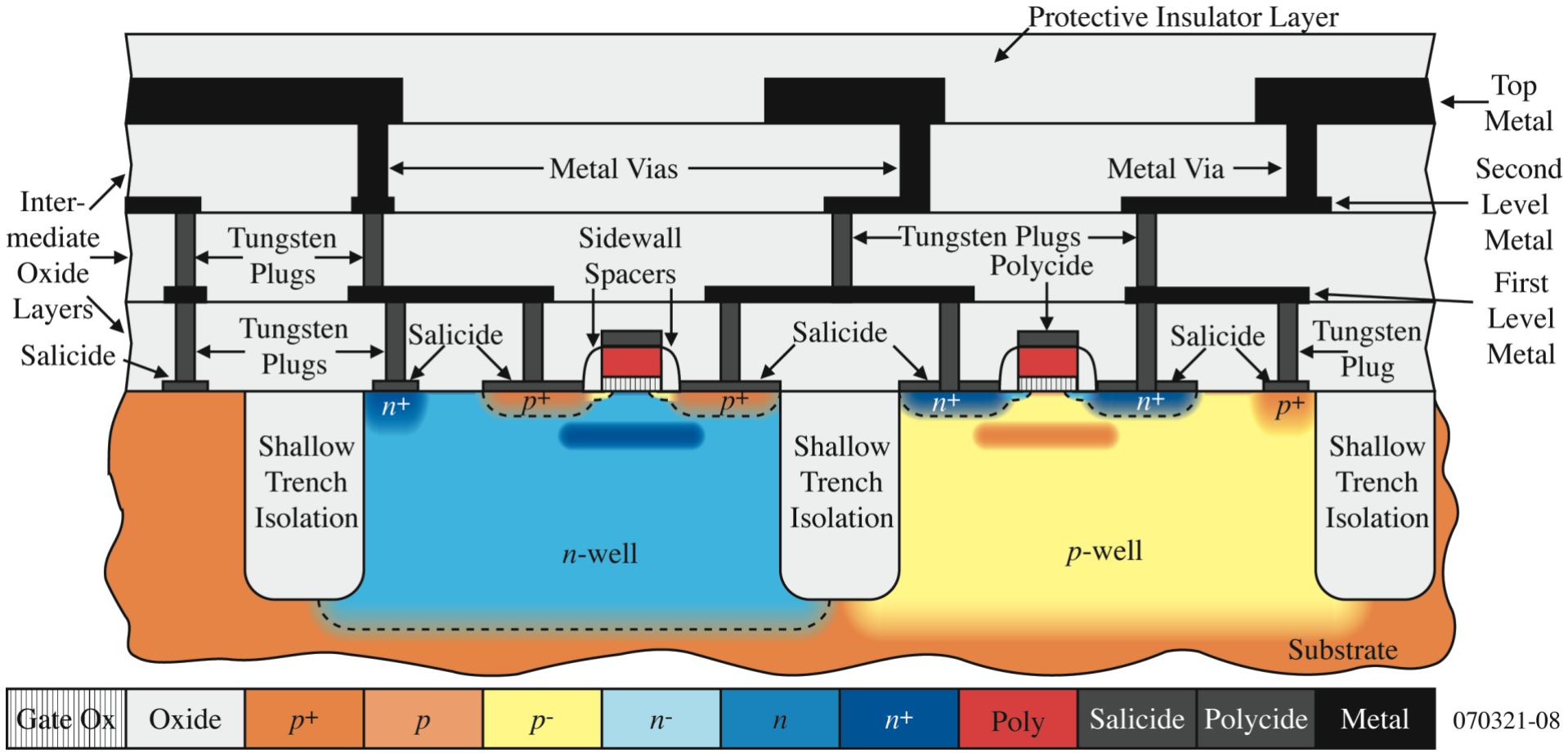
## Step 11 – Second-Level Metal

The previous step is repeated for the second-level metal.



## Completed Fabrication

After multiple levels of metal are applied, the fabrication is completed with a thicker top-level metal and a protective layer to hermetically seal the circuit from the environment. Note that metal is used for the upper level metal vias. The chip is electrically connected by removing the protective layer over large bonding pads.



# Scanning Electron Microscope of a MOSFET Cross-section

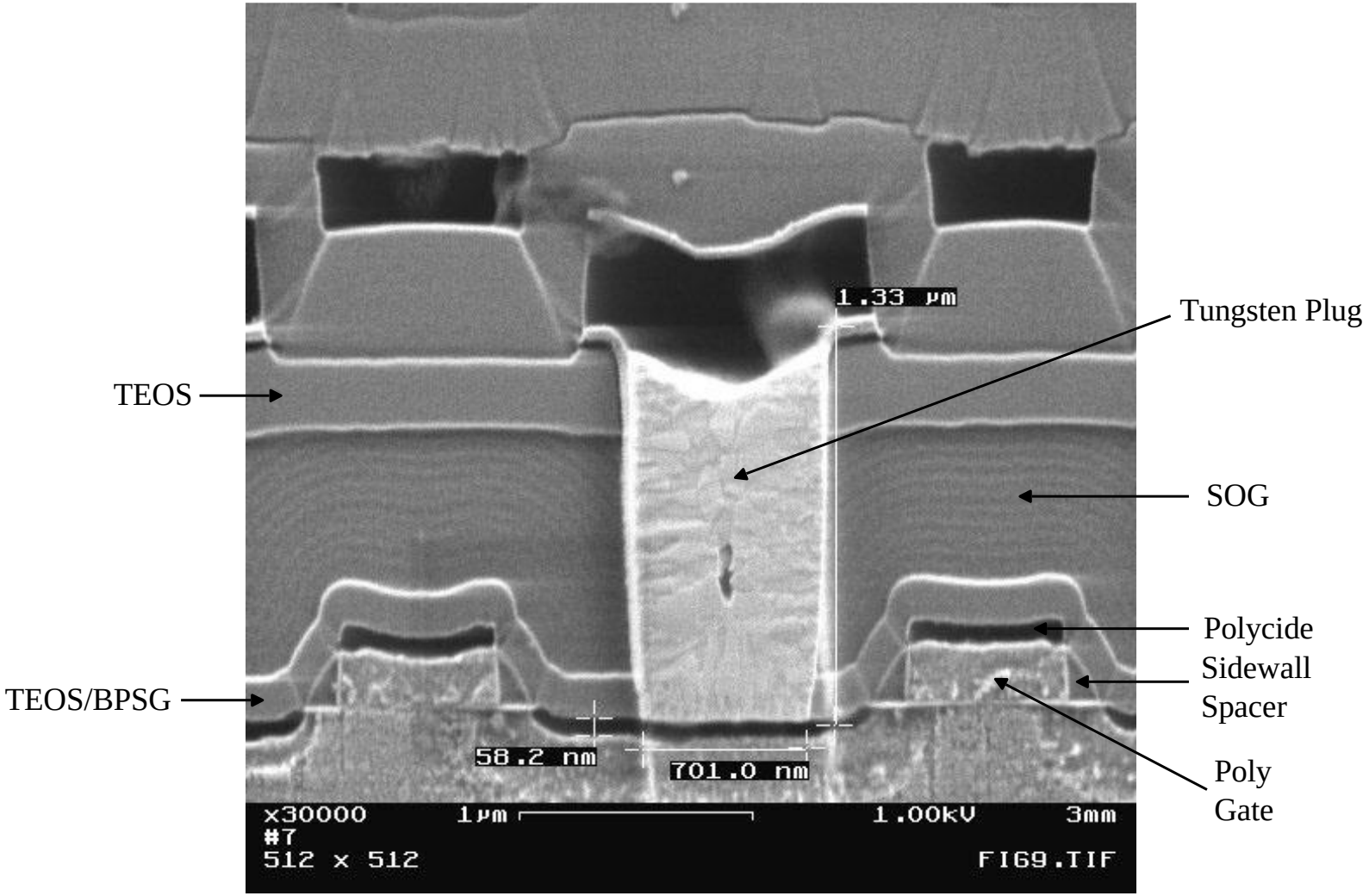



Fig. 2.8-20

# Scanning Electron Microscope Showing Metal Levels and Interconnect

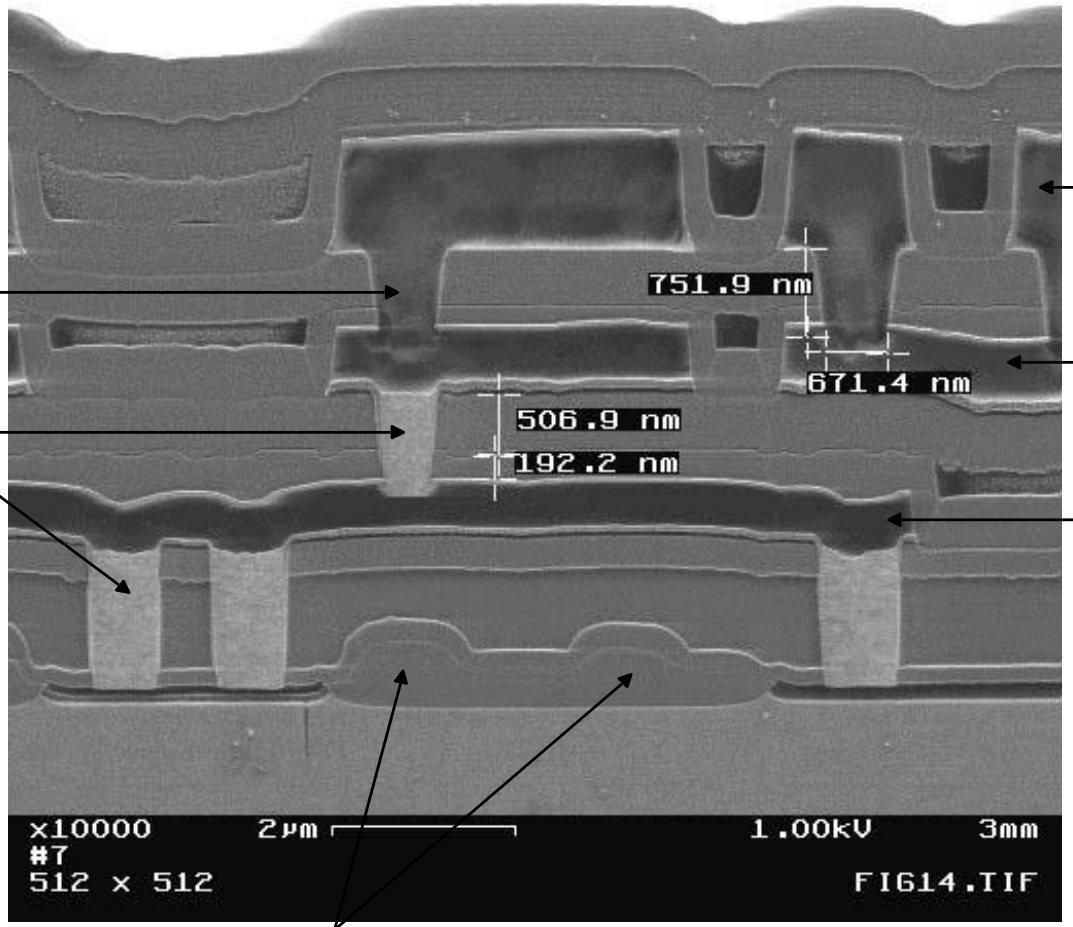



Fig.180-11

## SUMMARY

- DSM technology typically has a minimum channel length between 0.35μm and 0.1μm
- DSM technology addresses the problem of excessive depletion region widths in junction isolation techniques by using shallow trench isolation
- DSM technology may have from 4 to 8 levels of metal
- Lightly doped drains and sources are a key aspect of DSM technology