LECTURE 40 – OVERSAMPLING ADCS – PART II

LECTURE ORGANIZATION

Outline

- Implementation of ΔΣ modulators
- Decimation and filtering
- Bandpass ΔΣ modulators
- Digital-analog oversampling converters
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 596-607

IMPLEMENTATION OF ΔΣ MODULATORS

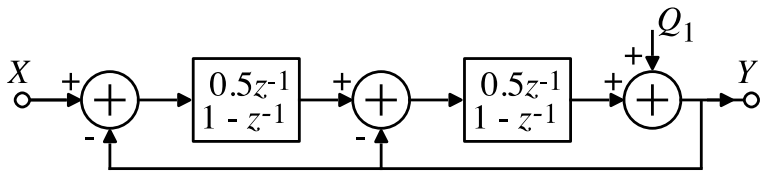
ΔΣ Modulators – The Analog Part of the Oversampling ADC

Most of today's delta-sigma modulators use fully differential switched capacitor circuits.

Advantages are:

- Doubles the signal swing and increases the dynamic range by 6dB
- Common-mode signals that may couple to the signal through the supply lines and substrate are canceled
- Charge injected by the switches are canceled to a first-order

Example:



First integrator dissipates the most power and requires the most accuracy.

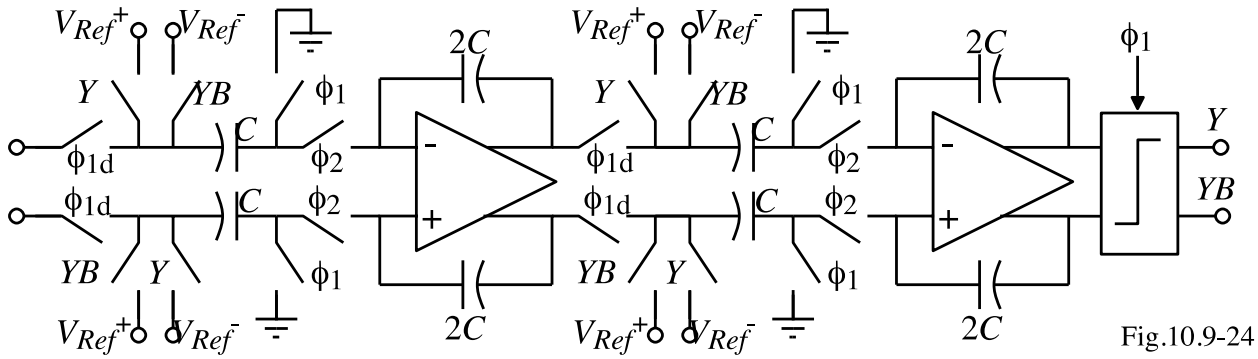


Fig.10.9-24

1.5V, 1mW, 98db ΔΣ Analog-Digital Converter†

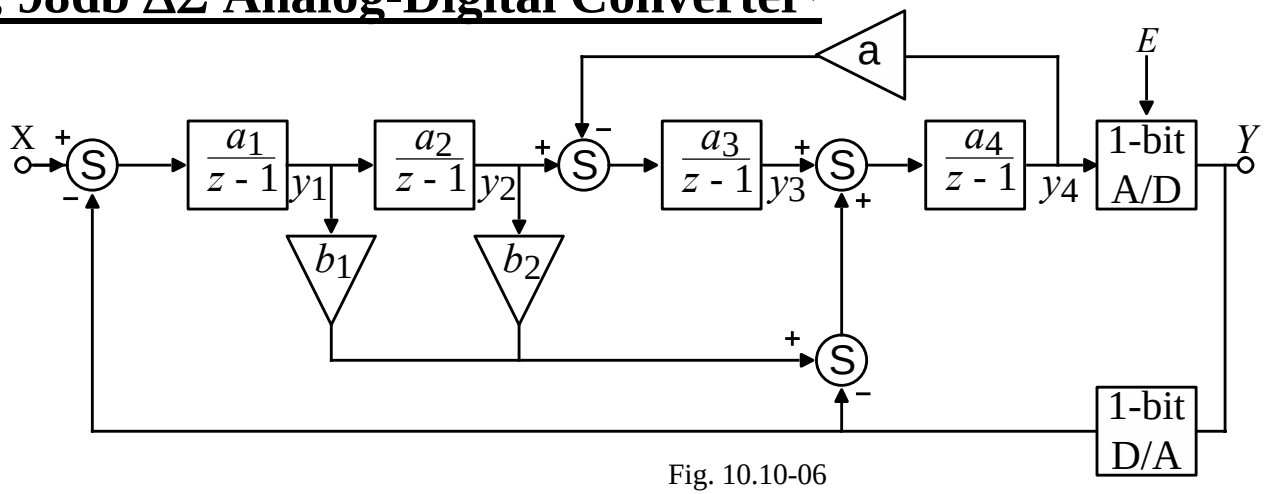


Fig. 10.10-06

where $a_1 = 1/3$, $a_2 = 3/25$, $a_3 = 1/10$, $a_4 = 1/10$, $b_1 = 6/5$, $b_2 = 1$ and $\alpha = 1/6$

Advantages:

- The modulator combines the advantages of both DFB and DFF type modulators:

  Only four op amps are required. The 1st integrator's output swing is between $\pm V_{REF}$ for large input signal amplitudes ($0.6V_{REF}$), even if the integrator gain is large (0.5).
- A local resonator is formed by the feedback around the last two integrators to further suppress the quantization noise.
- The modulator is fully pipelined for fast settling.

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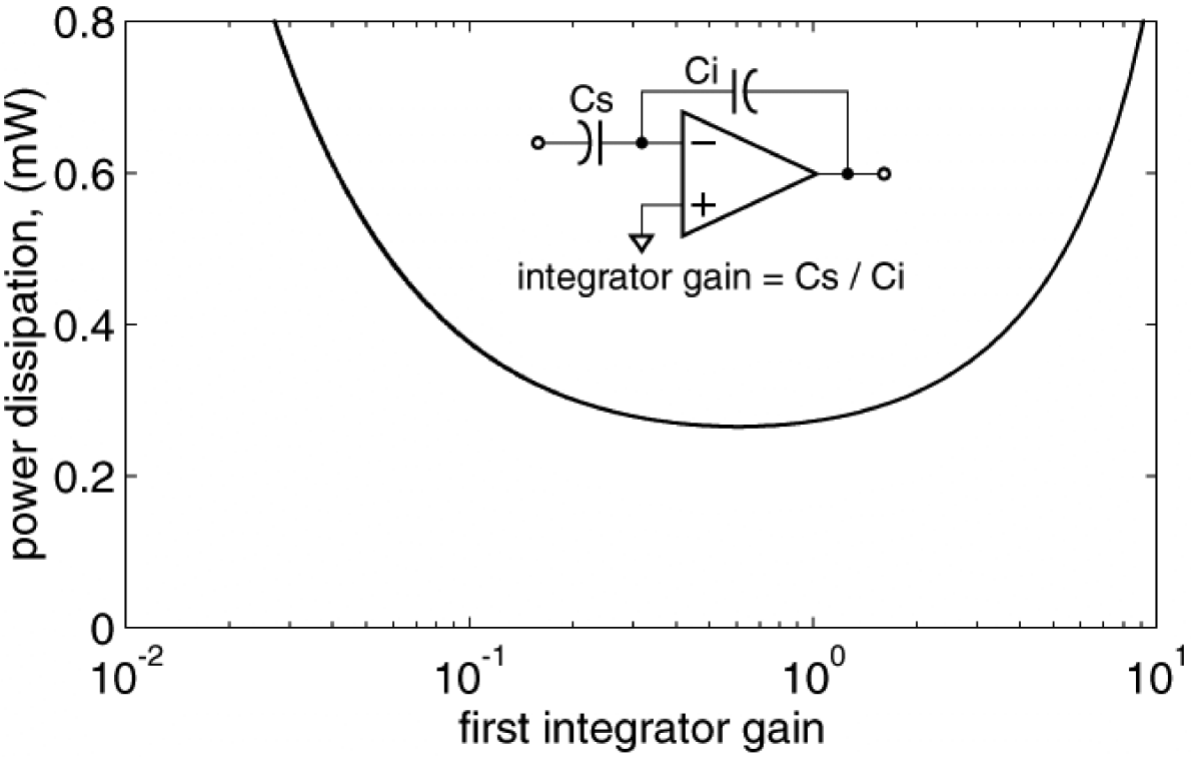
† A.L. Coban and P.E. Allen, "A 1.5V, 1mW Audio ΔΣ Modulator with 98dB Dynamic Range, "*Proc. of 1999 Int. Solid-State Circuits Conf.*, Feb. 1999, pp. 50-51.

1.5V, 1mW, 98dB ΔΣ Analog-Digital Converter - Continued

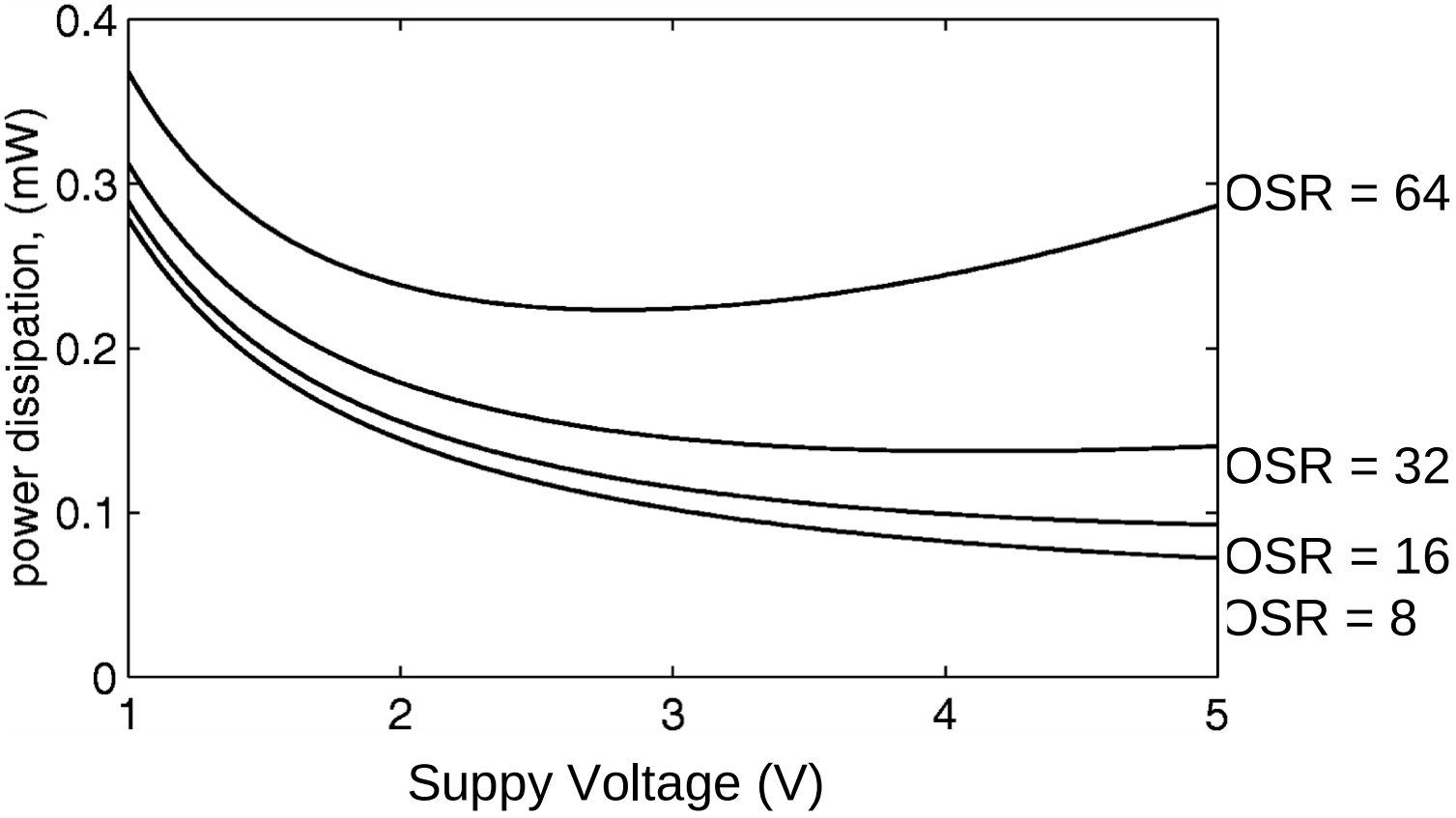
Integrator power dissipation vs. integrator gain



DR = 98 dB
BW = 20 kHz
C_S = 5 pF
0.5 µm CMOS

1.5V, 1mW, 98db ΔΣ Analog-Digital Converter - Continued

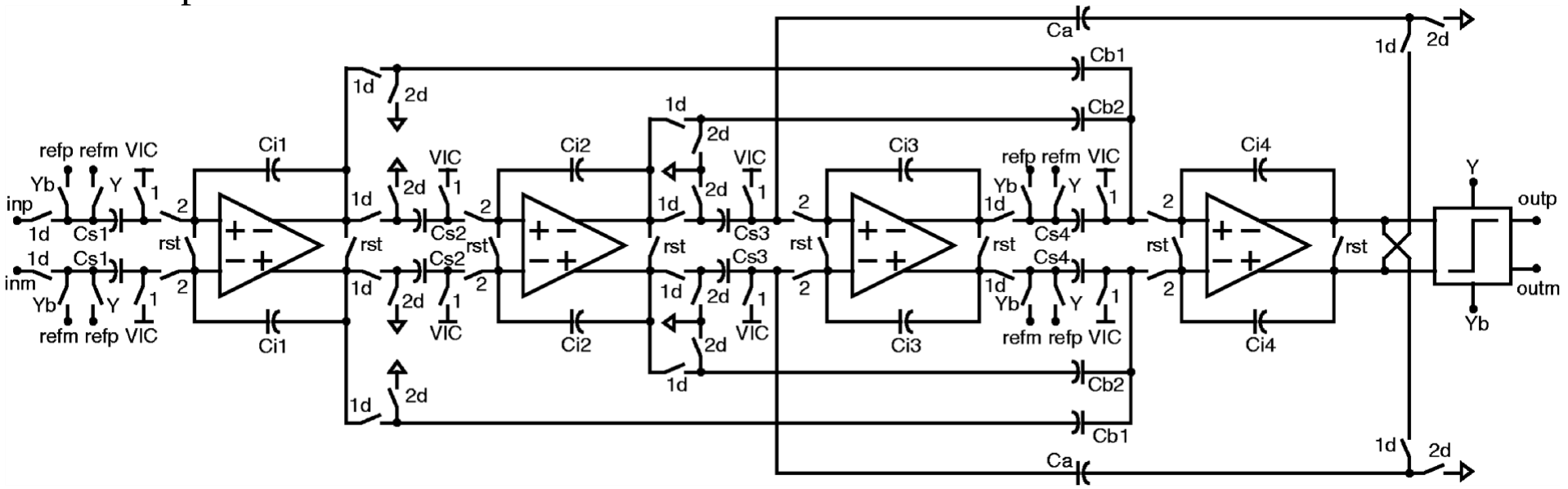
Modulator power dissipation vs. oversampling ratio



DR = 98 dB
BW = 20 kHz
Integrator gain = 1/3
0.5μm CMOS

1.5V, 1mW, 98dB ΔΣ Analog-Digital Converter - Continued

Circuit Implementation:



Capacitor Values				
Capacitor	Integrator 1	Integrator 2	Integrator 3	Integrator 4
C_s	5.00pF	0.15pF	0.30pF	0.10pF
C_i	15.00pF	1.25pF	3.00pF	1.00pF
C_a	-	-	0.05pF	-
C_{b1}	-	-	-	0.12pF
C_{b2}	-	-	-	0.10pF

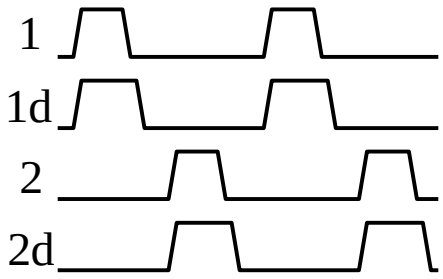
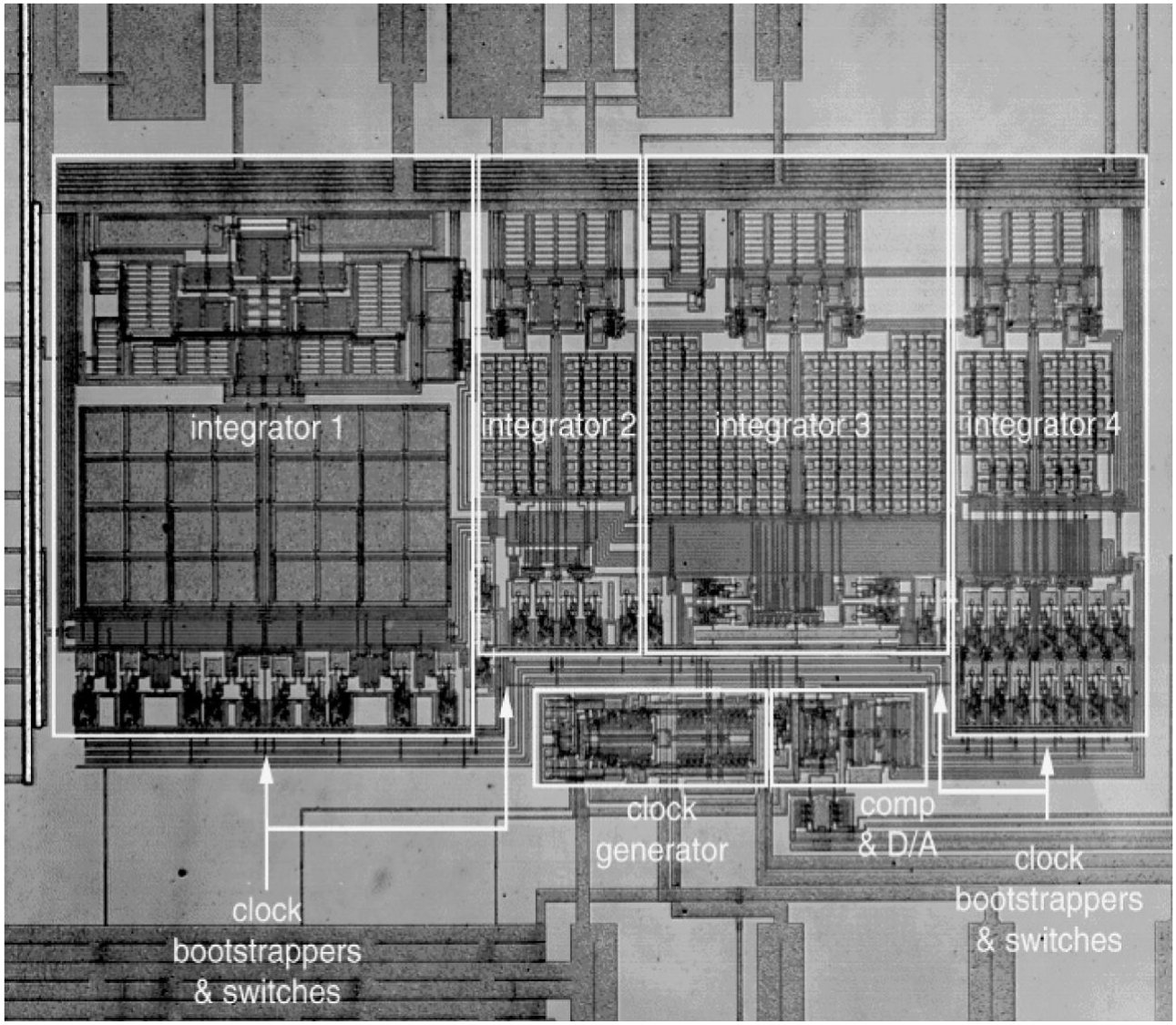


Fig.10.9-25

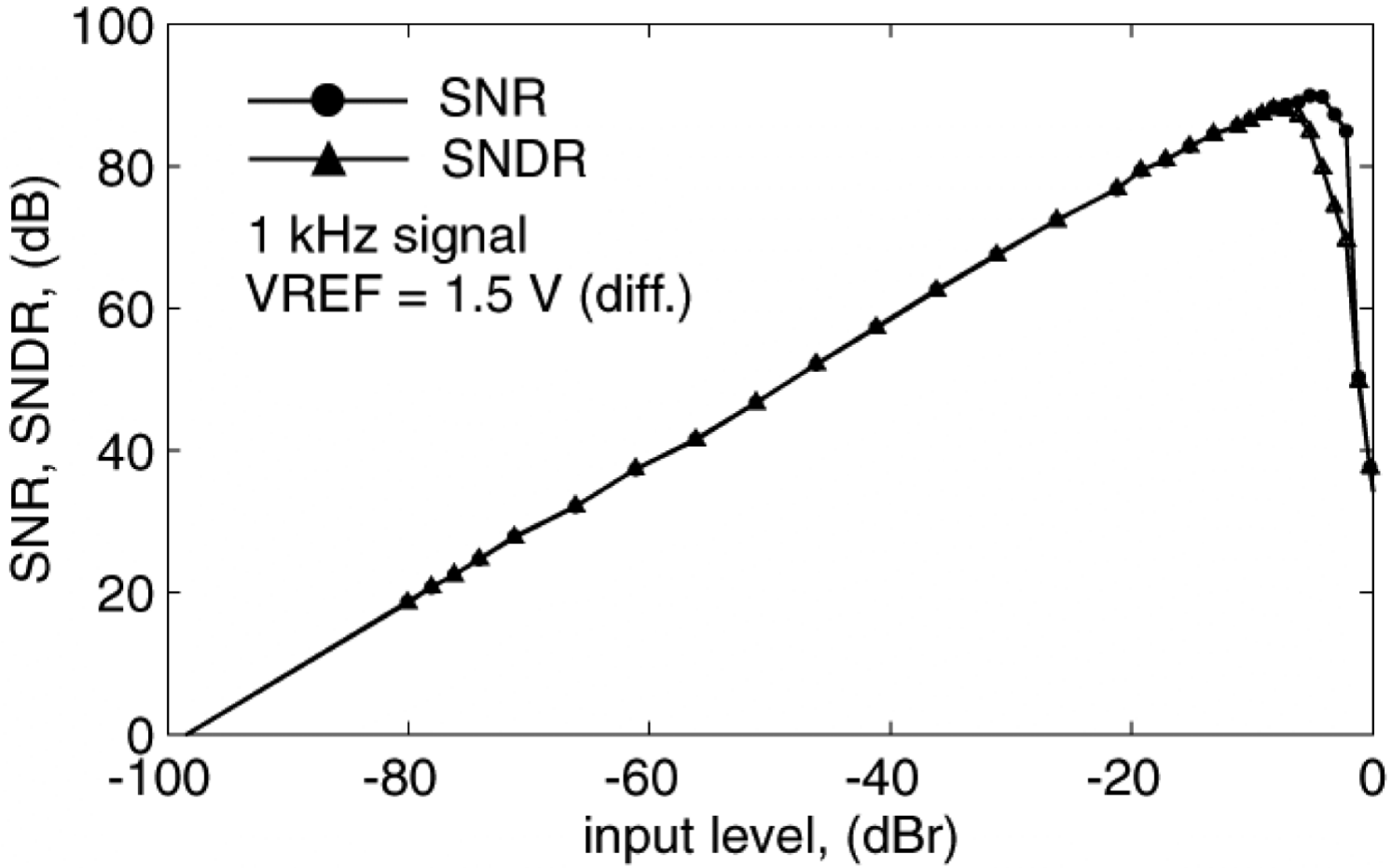
1.5V, 1mW, 98dB ΔΣ Analog-Digital Converter - Continued

Microphotograph of the ΔΣ modulator.



1.5V, 1mW, 98dB ΔΣ Analog-Digital Converter - Continued

Measured SNR and SNDR versus input level of the modulator.



1.5V, 1mW, 98dB ΔΣ Analog-Digital Converter - Continued

Measured 4th-Order ΔΣ Modulator Characteristics:

Table 5.4

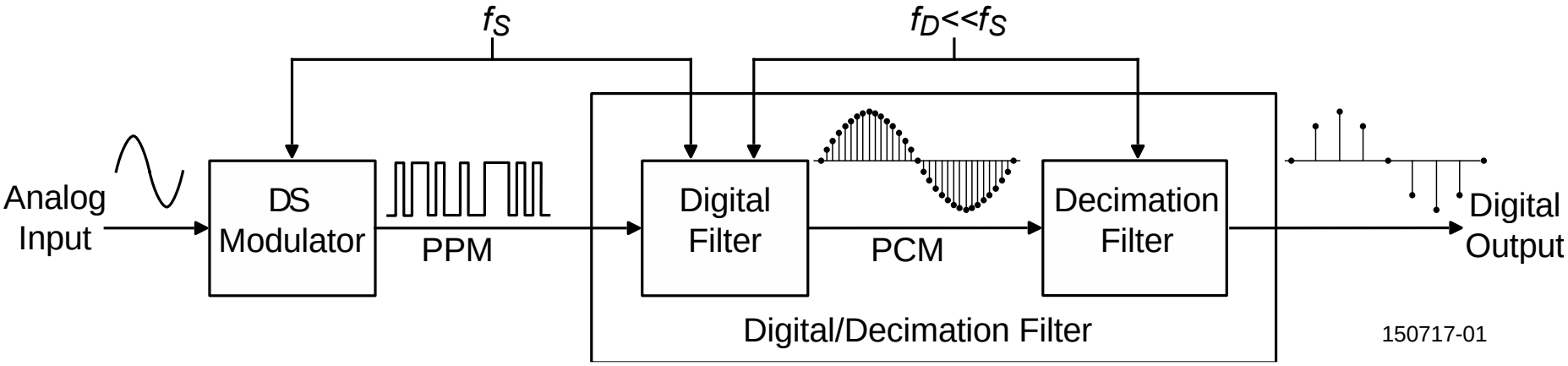
Measured fourth-order delta-sigma modulator characteristics

Technology : 0.5 μm triple-metal single-poly n-well CMOS process	
Supply voltage	1.5 V
Die area	1.02 mm x 0.52 mm
Supply current	660 μA
analog part	630 μA
digital part	30 μA
Reference voltage	0.75V
Clock frequency	2.8224MHz
Oversampling ratio	64
Signal bandwidth	20kHz
Peak SNR	89 dB
Peak SNDR	87 dB
Peak S/D	101dB
HD_3 @ -5dBv 2kHz input	-105dBv
DR	98 dB

DECIMATION AND FILTERING

Delta-Sigma ADC Block Diagram

The decimator and filter are implemented digitally and consume most of the area and the power.



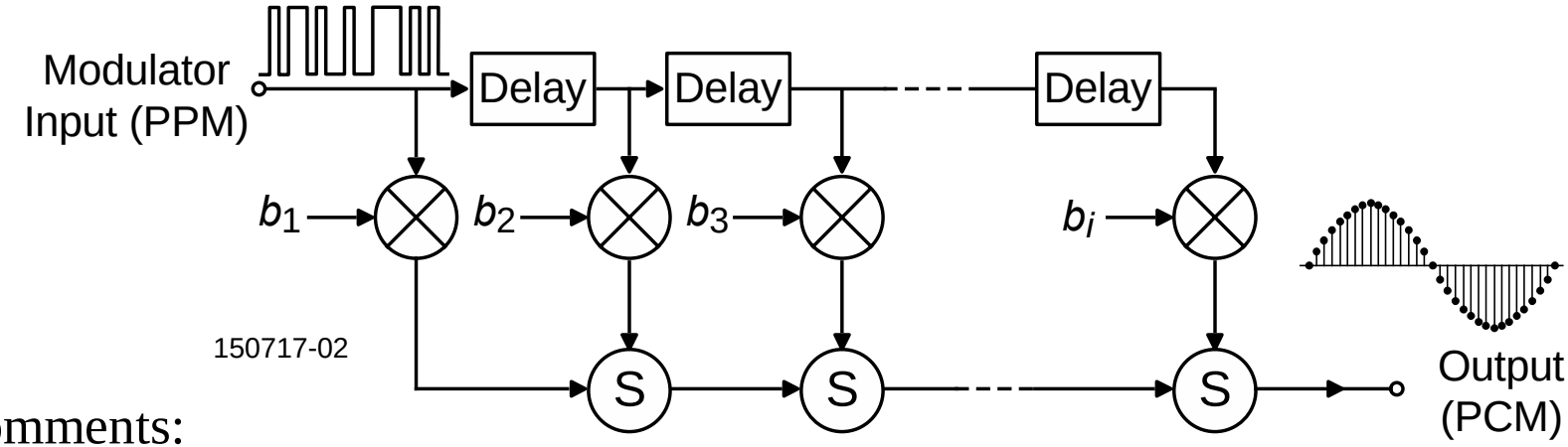
Function of the digital filter and digital decimator are;

1.) To attenuate the quantization noise above the baseband
2.) Bandlimit the input signal
3.) Suppress out-of-band spurious signals and circuit noise

Digital Filter

Implements a low pass filter by sampling the modulator stream of the 1-bit or multi-bit code (PPM)

First-order averaging filter:

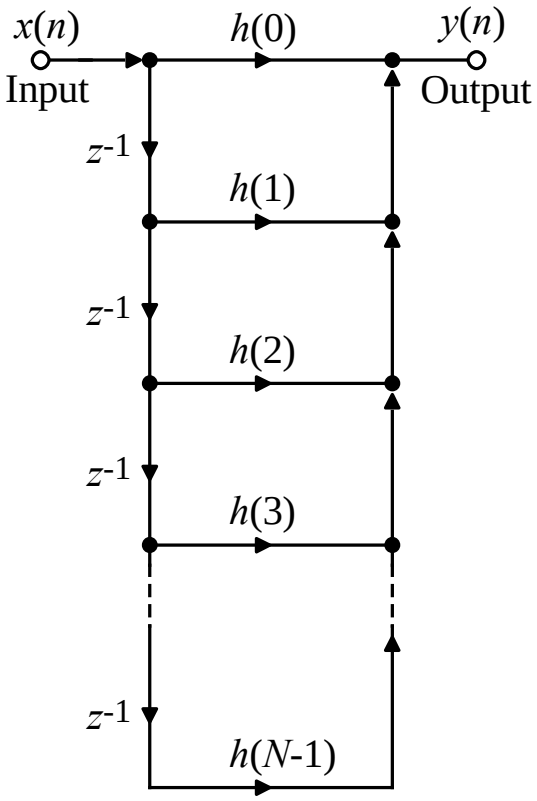


Comments:

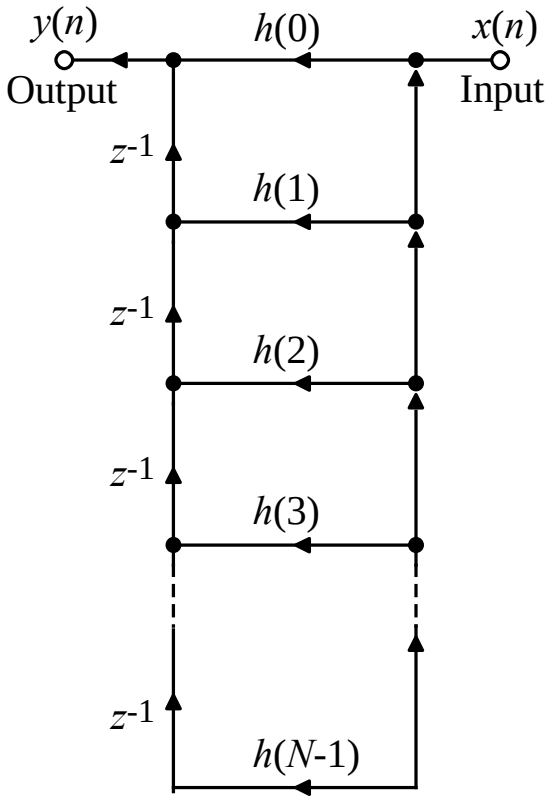
- The low pass filter removes the quantization noise
- With the quantization noise reduced, the output is now a high resolution digital version of the input signal
- However, the output rate is too fast to be practical
  - To use the output samples would require a very fast controller or processor
  - Since a low pass filter has been applied, most of the fast samples don't provide any useful information

Implementation of Digital Filters†

Digital filter structures:



Direct-form structure for an FIR digital filter.



Transposed direct-form FIR filter structure.

Fig.10.9-29

† S.R. Norsworthy, R. Schreier, and G.C. Temes, *Delta-Sigma Data Converters-Theory, Design, and Simulation*, IEEE Press, NY, Chapter 13, 1997.

Digital Decimator

The purpose of the decimator is to:

1.) Reduce the sample rate from f_S down to the Nyquist frequency, $2f_B$.

2.) Help to remove the quantization noise.

3.) Perform the anti-aliasing filtering.

Challenges for the decimator:

1.) The input sampling rate is very high which makes it difficult to implement an efficient digital decimation filter.

2.) Higher-order modulators produce highly shaped noise and require the filter to remove this noise with not much frequency transition region.

3.) Should not distort the magnitude and phase characteristics of the input signal in the baseband.

Goal:

Implement the digital decimator in a minimum amount of logic and make it feasible for integrated circuit implementation.

A Multi-Stage Decimation Filter

To reduce the number of stages, the decimation filters are typically implemented in several stages.
Typical multi-stage decimation filter:

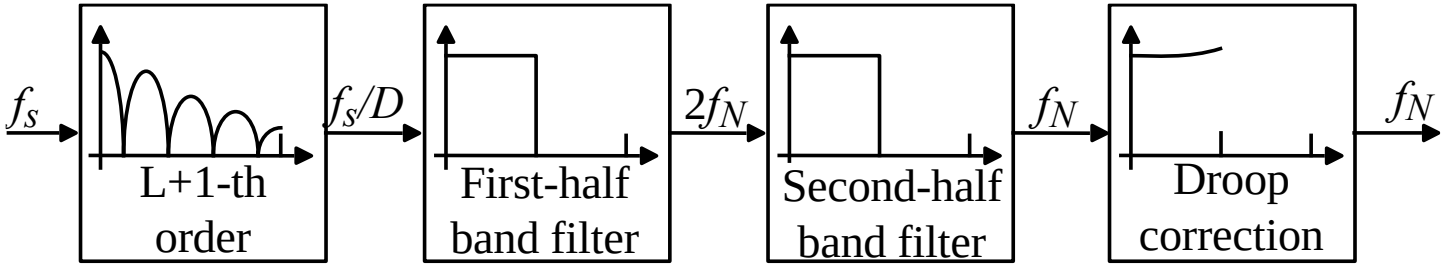


Fig.10.9-26

1.) For ΔΣ modulators with $(1\text{-}z^{-1})^L$ noise shaping comb filters are very efficient.
   - Comb filters are suitable for reducing the sampling rate to four times the Nyquist rate.
   - Designed to suppress the quantization noise that would otherwise alias into the signal band upon sampling at an intermediate rate of f_{s1}.

2.) The remaining filtering is performed in stages by FIR or IIR filters.
   - Suppresses out-of-band components of the signal

3.) Droop correction - may be required depending upon the ADC specifications

Comb Filters

A comb filter that computes a running average of the last D input samples is given as

$$y[n] = \frac{1}{D}\sum_{i=0}^{D-1} x[n-i]$$

where D is the decimation factor given as

$$D = \frac{f_s}{f_{s1}}$$

The corresponding z-domain expression is,

$$H_D(z) = \sum_{i=1}^{D} z^{-i} = \frac{1}{D}\frac{1 - z^{-D}}{1 - z^{-1}}$$

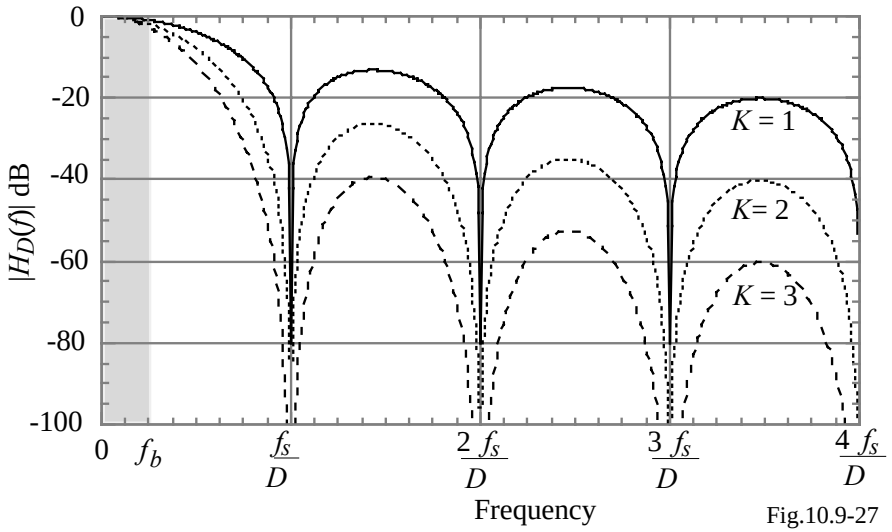


Fig.10.9-27

The frequency response is obtained by evaluating $H_D(z)$ for $z = e^{j2\pi fT_s}$,

$$H_D(f) = \frac{1}{D}\frac{\sin\pi fDT_s}{\sin\pi fT_s}\, e^{-j2\pi fT_s/D}$$

where T_S is the input sampling period (=$1/f_S$). Note that the phase response is linear.

For an L-th order modulator with a noise shaping function of $(1-z^{-1})^L$, the required number of comb filter stages is L+1. The magnitude of such a filter is,

$$|H_D(f)| = \left(\frac{1}{D}\frac{\sin\pi fDT_S}{\sin\pi fT_S}\right)K$$

Implementation of a Cascaded Comb Filter

Implementation:

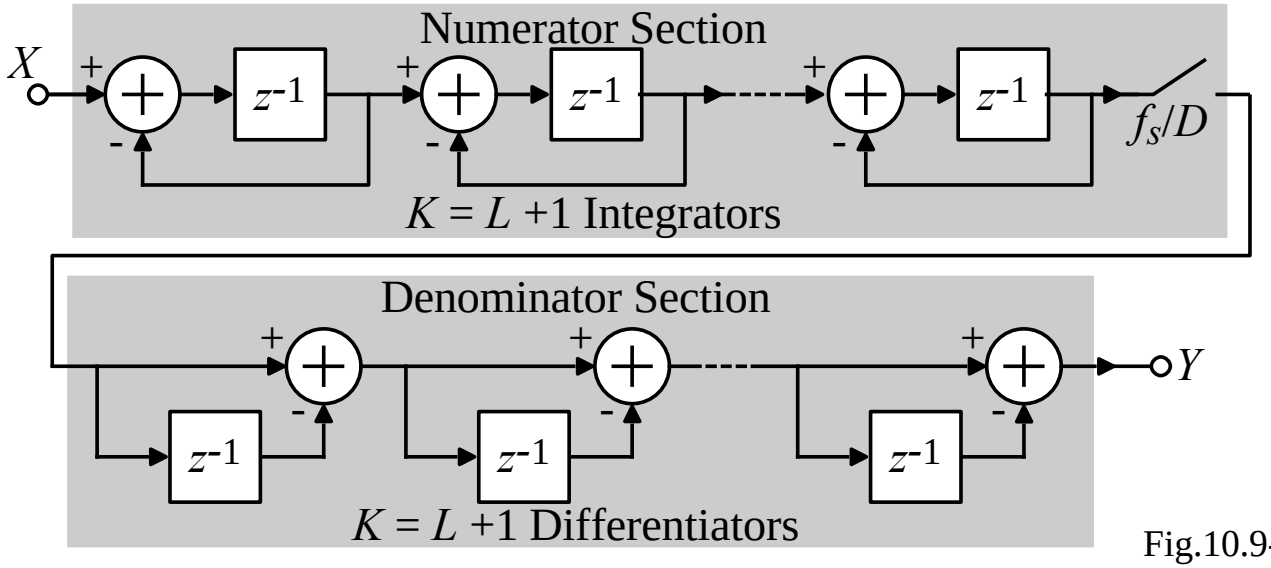


Fig.10.9-28

Comments:

1.) The L+1 integrators operating at the sampling frequency, f_S, realize the denominator of $H_D(z)$.

2.) The L+1 differentiators operating at the output rate of f_{S1} (= f_S/D) realize the numerator of $H_D(z)$.

3.) Placing the integrator delays in the feedforward path reduces the critical path from L+1 adder delays to a single adder delay.

Digital Lowpass Filter

Example of a typical digital filter used in removal of the quantization noise at higher frequencies

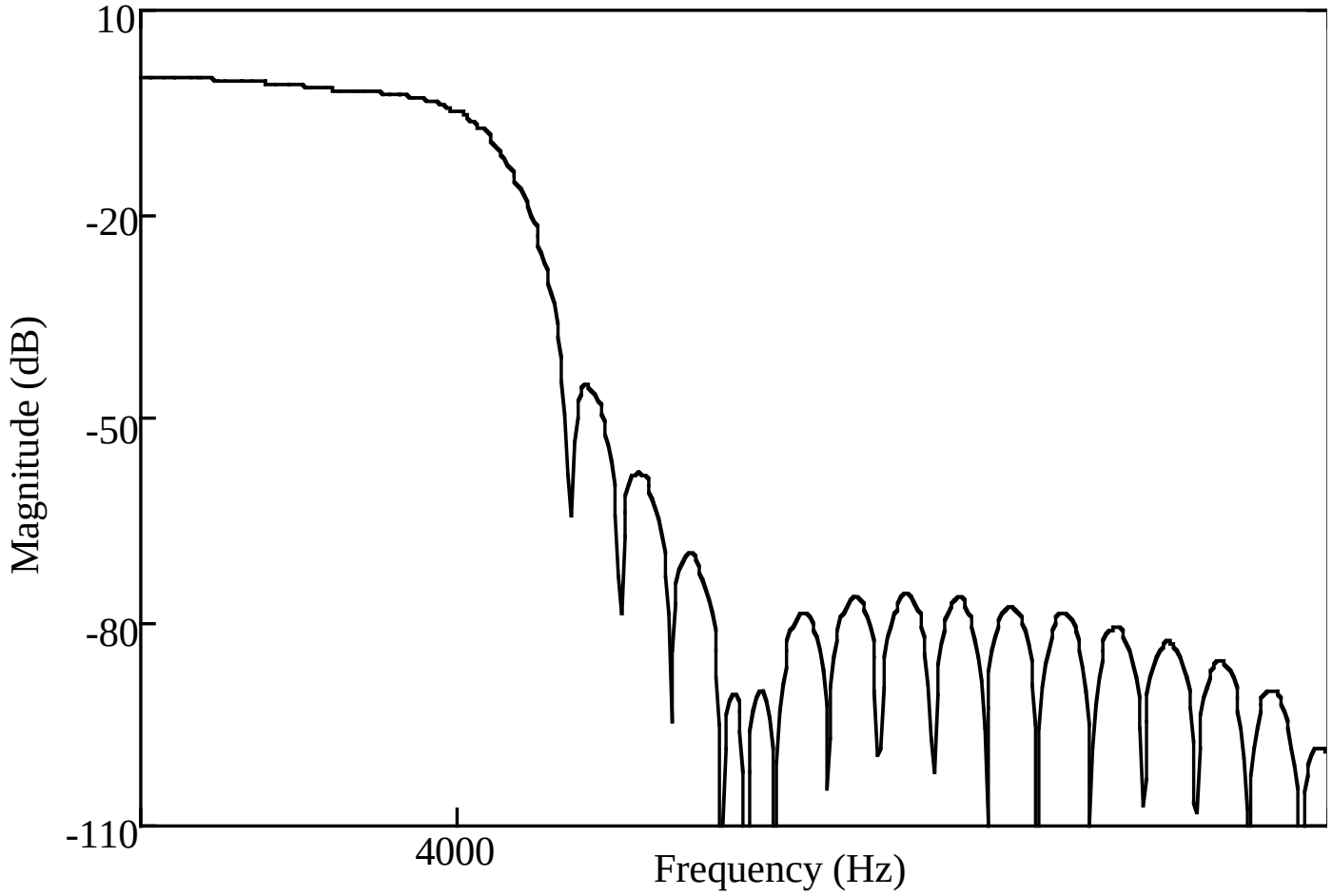
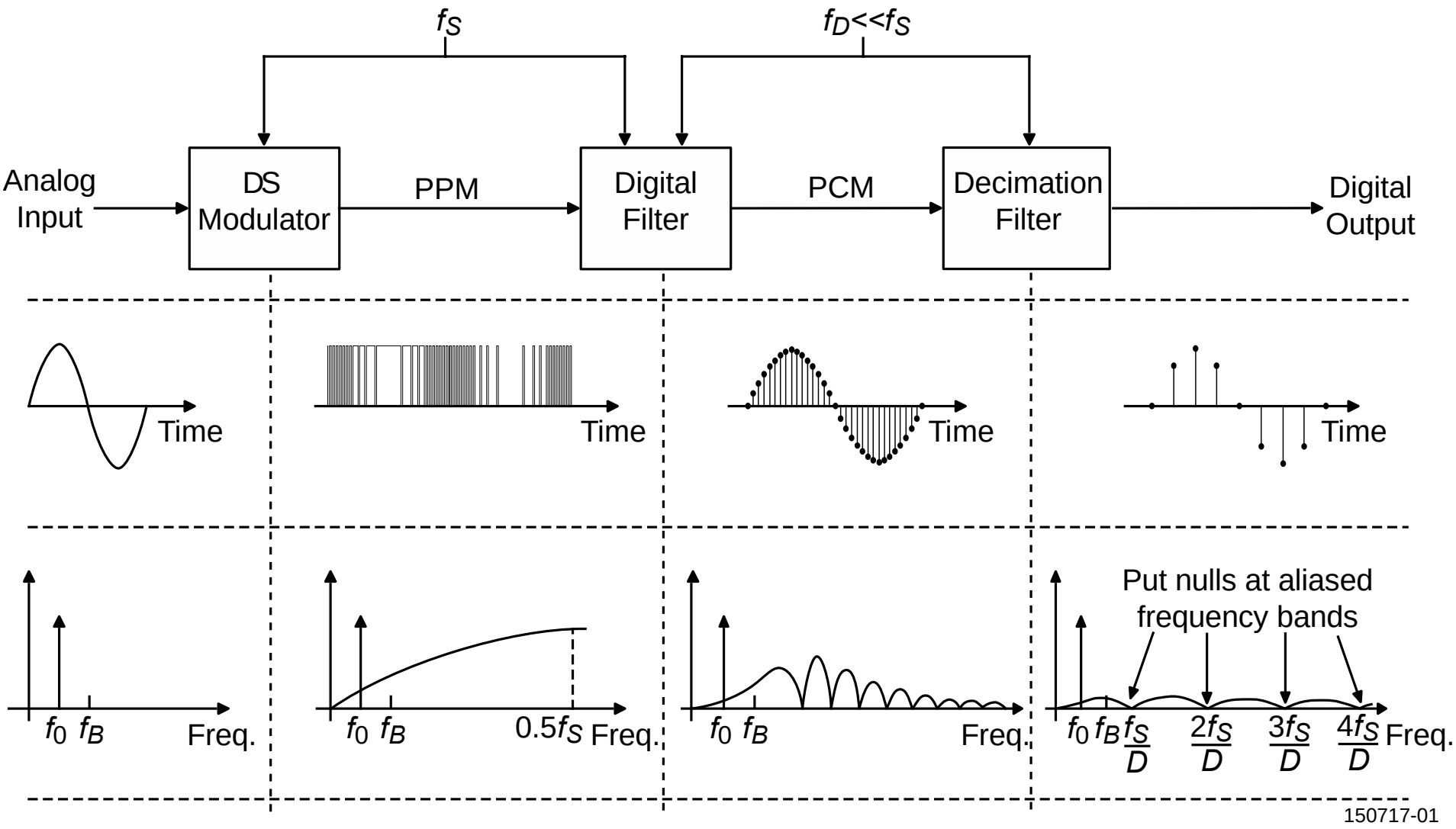


Illustration of the Delta-Sigma ADC in Time and Frequency Domain



BANDPASS DELTA-SIGMA MODULATORS

Bandpass ΔΣ Modulators

Block diagram of a bandpass modulator:

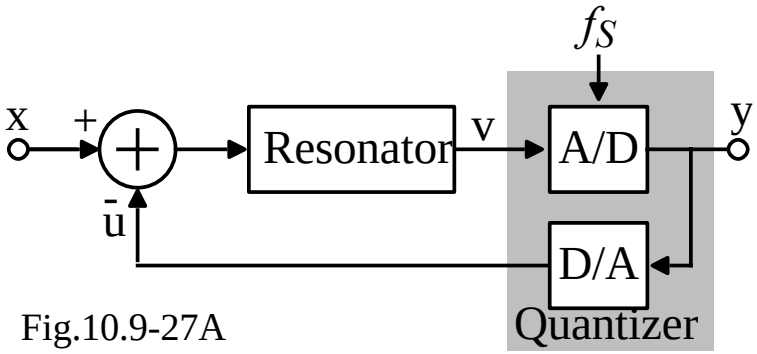


Fig.10.9-27A

Components:

- Resonator - a bandpass filter of order $2N$, N= 1, 2,....
- Coarse quantizer (1 bit or multi-bit)

The noise-shaping of the bandpass oversampled ADC has the following interesting characteristics:

Center frequency = $f_S \cdot(2N\text{-}1)/4$

Bandwidth = BW = f_S / M

Illustration of the Frequency Spectrum (N=1):

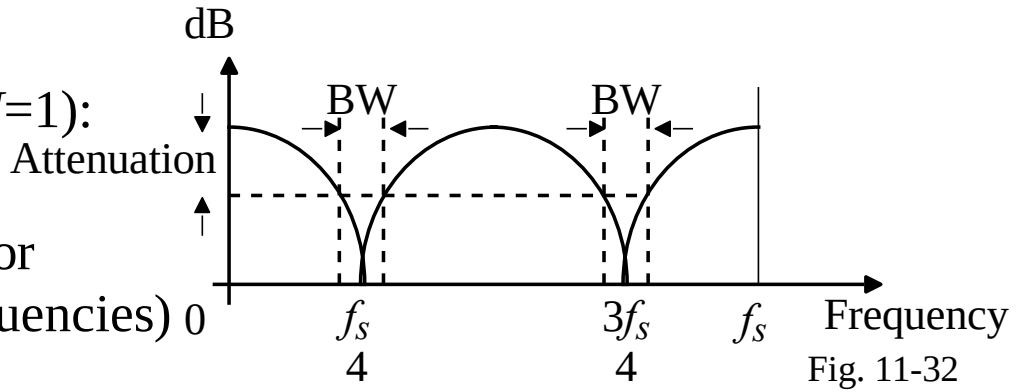


Fig. 11-32

Application of the bandpass ΔΣ ADC is for systems with narrowband signals (IF frequencies)

A Second-Order ΔΣ Bandpass Modulator

Bandpass Resonator:

$$V(z) = z\text{-}1\,[X(z) - z\text{-}1V(z)] = z\text{-}1X(z) - z\text{-}2V(z)$$

$$V(z)\,(1+z\text{-}2) = z\text{-}1X(z) \rightarrow \frac{V(z)}{X(z)} = \frac{z^{-1}}{1+z^{-2}}$$

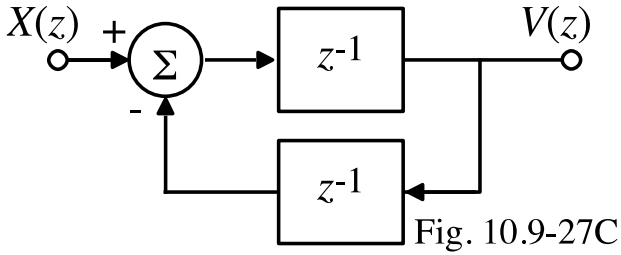


Fig. 10.9-27C

Modulator:

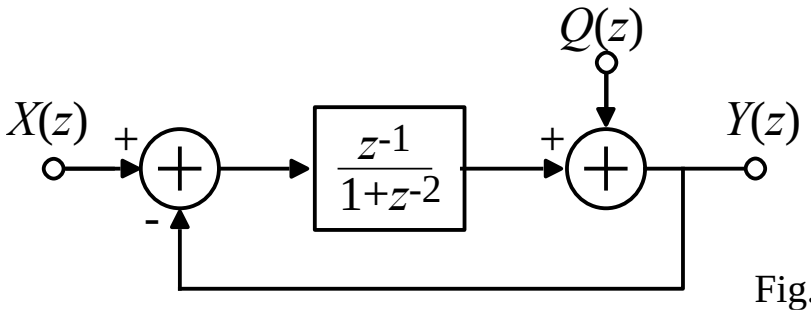


Fig.10.9-27B

$$Y(z) = Q(z) + [X(z) - Y(z)]\left(\frac{z^{-1}}{1+z^{-2}}\right) \rightarrow Y(z) = \left(\frac{1+z^{-2}}{1+ z^{-1}-z^{-2}}\right)Q(z) + \left(\frac{z^{-1}}{1+ z^{-1}-z^{-2}}\right)X(z)$$

$$NTF_Q\,(z) = \left(\frac{1+z^{-2}}{1+ z^{-1}-z^{-2}}\right)$$

The $NTF_Q\,(z)$ has two zeros on the $j\omega$ axis.

Fourth-Order Bandpass ΔΣ Modulator

Block diagram:

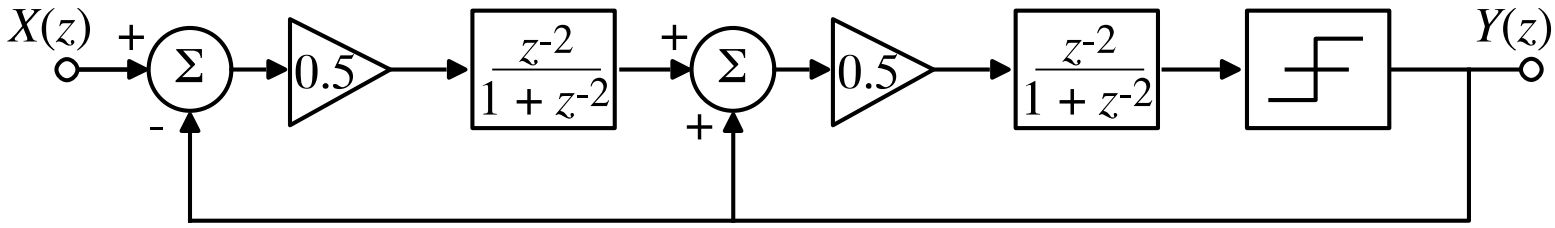


Fig. 10.9-27E

Comments:

- Designed by applying a lowpass to bandpass transform to a second-order lowpass ΔΣ modulator
- The stabilty and SNR characteristics are the same as those of a second-order lowpass modulator
- The z-domain output is given as,

$$Y(z) = z^{-4}X(z) + (1+z^{-2})^2Q(z)$$

- The zeros are located at $z = \pm j$ which corresponds to notches at $f_S/4$.

Resonator Circuit Implementation

Block diagram of $z^{-2}/(1+z^{-2})$:

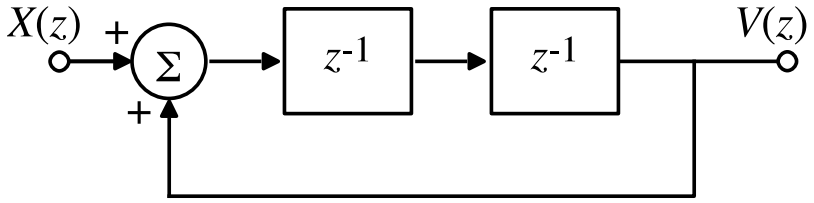


Fig. 10.9-27F

Fully differential switch-capacitor implementation:

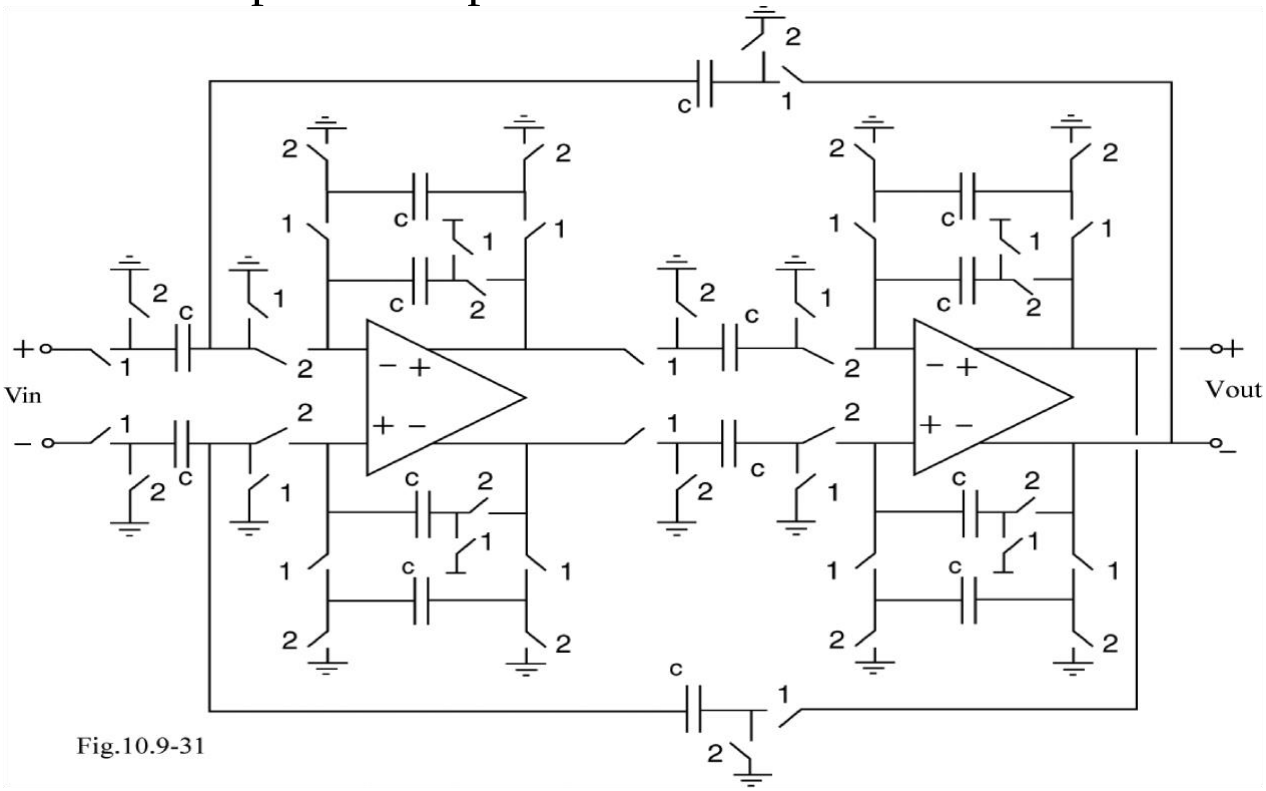
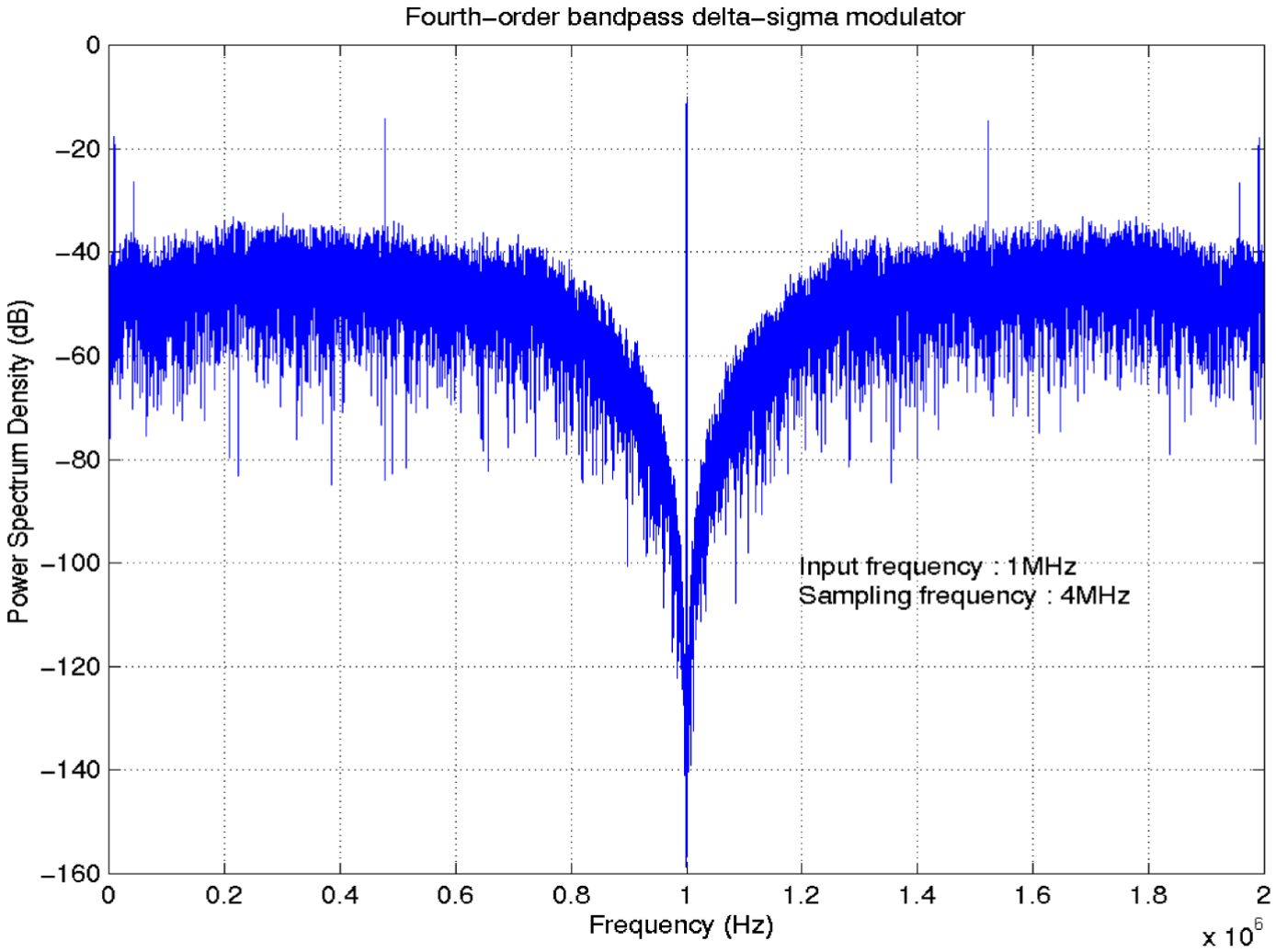


Fig.10.9-31

Power Spectral Density of the Previous Fourth-Order Bandpass ΔΣ Modulator

Simulated result:



DELTA-SIGMA DIGITAL-TO-ANALOG CONVERTERS

Principles

The principles of oversampling and noise shaping are also widely used in the implementation of ΔΣ DACs.

Simplified block diagram of a delta-sigma DAC:

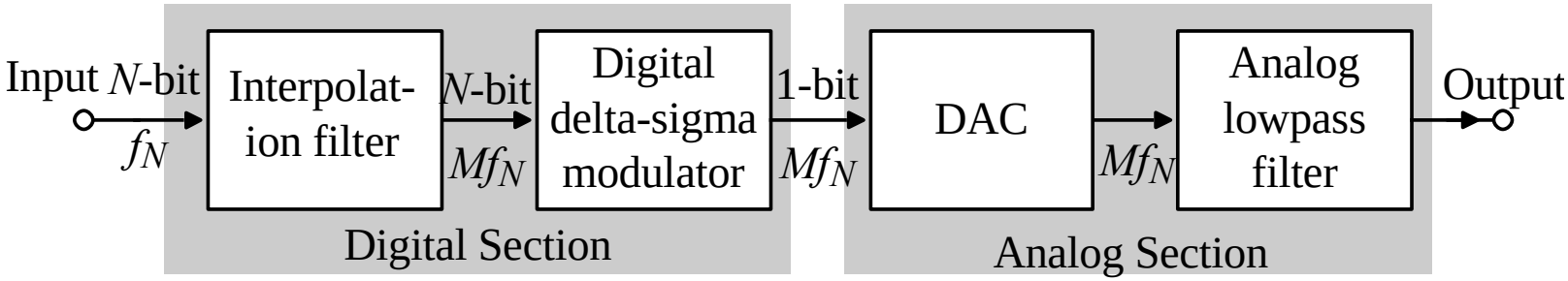


Fig10.9-29

Operation:

1.) A digital signal with N-bits with a data rate of f_N is sampled at a higher rate of Mf_N by means of an interpolator.

2.) Interpolation is achieved by inserting "0"s between each input word with a rate of Mf_N and then filtering with a lowpass filter.

3.) The MSB of the digital filter is applied to a DAC which is applied to an analog lowpass filter to achieve the analog output.

Block Diagram of a ΔΣ DAC

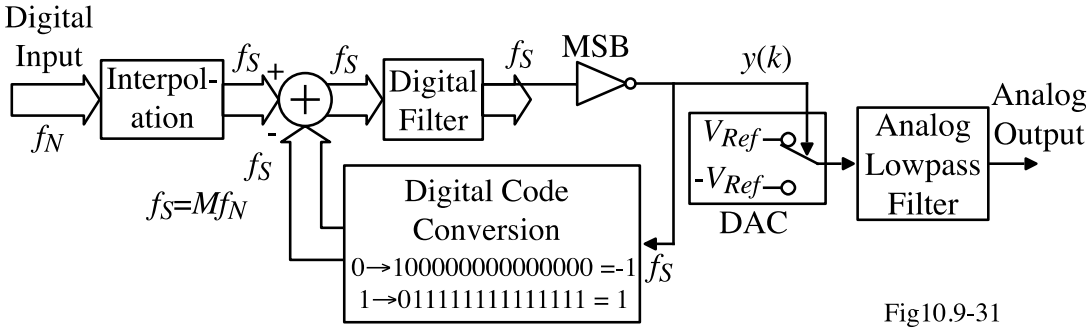


Fig10.9-31

Operation:

1.) Interpolate a digital word at the conversion rate of the converter (f_N) up to the sample frequency, f_s.

2.) The word length is then reduced to one bit with a digital sigma-delta modulator.

3.) The one bit PDM signal is converted to an analog signal by switching between two reference voltages.

4.) The high-frequency quantization noise is removed with an analog lowpass filter yielding the required analog output signal.

Sources of error:

- Device mismatch (causes harmonic distortion rather than DNL or INL)
- Component noise
- Device nonlinearities
- Clock jitter sensitivity
- Inband quantization error from the Δ-Σ modulator

Frequency Viewpoint of the ΔΣ DAC

Frequency spectra at different points of the delta-sigma ADC:

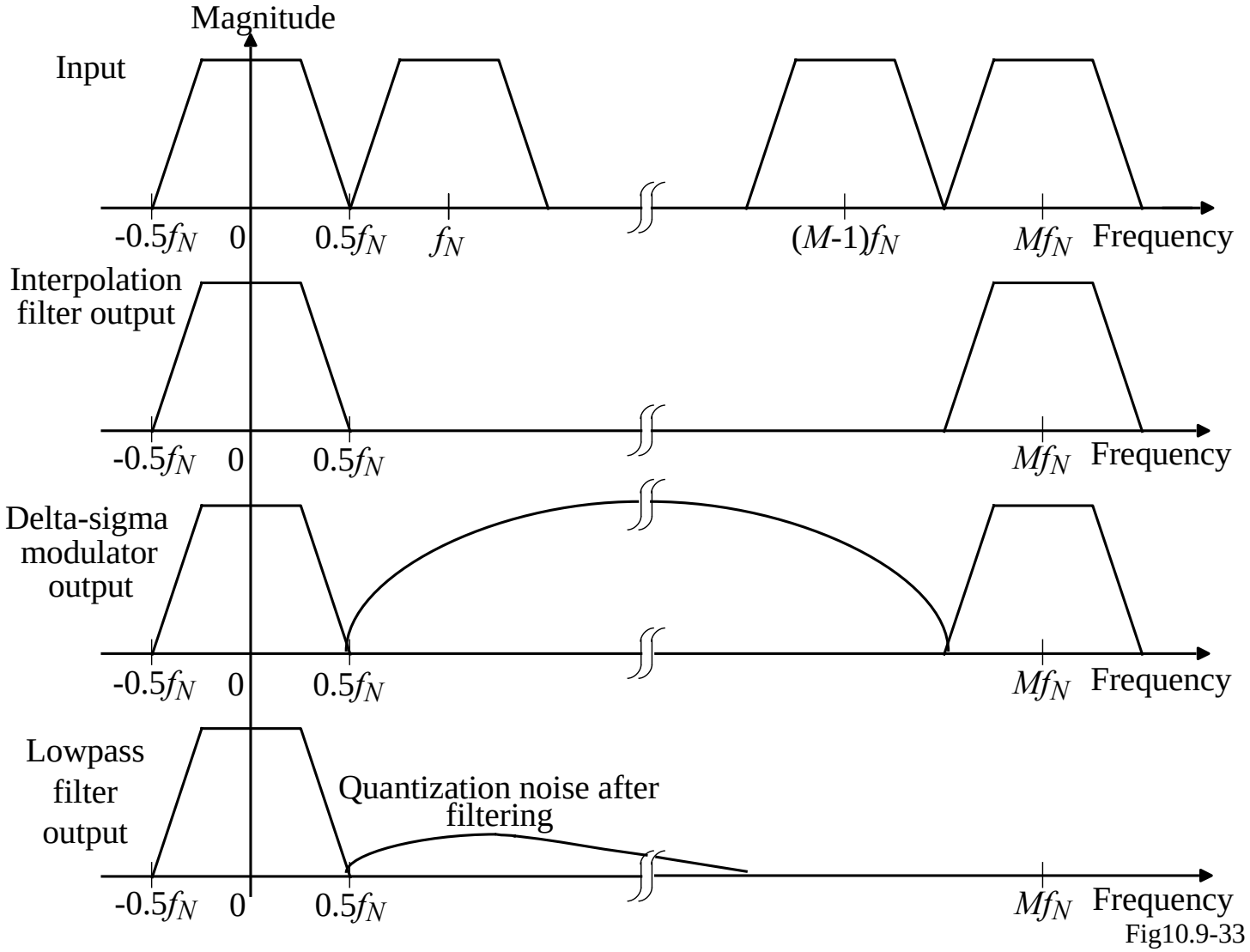
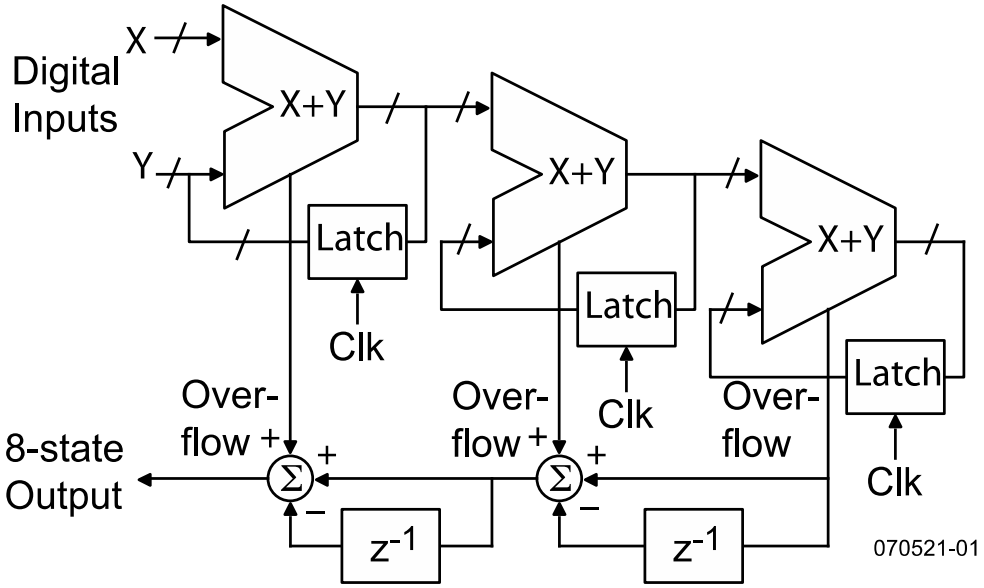


Fig10.9-33

A Third-Order, ΔΣ Modulator for a DAC

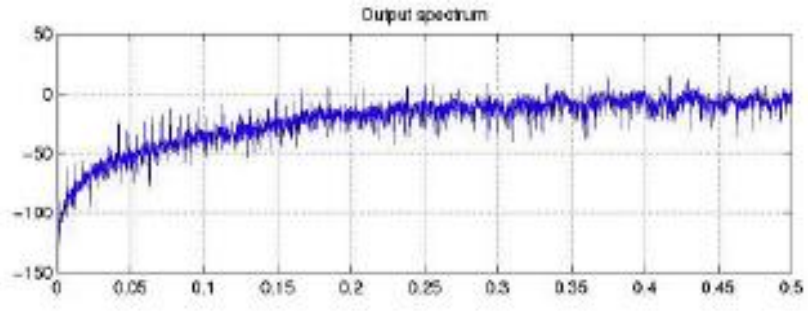
A digital equivalent of the third-order MASH ΔΣ modulator is shown below.

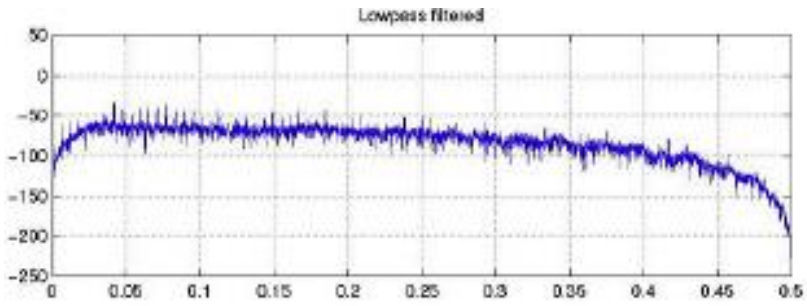


The *m*-bit accumulators consist of an *m*-bit adder and *m*-bit latches.

The 8-state digital output is converted to an analog through means of an analog filter.

Spectral outputs:

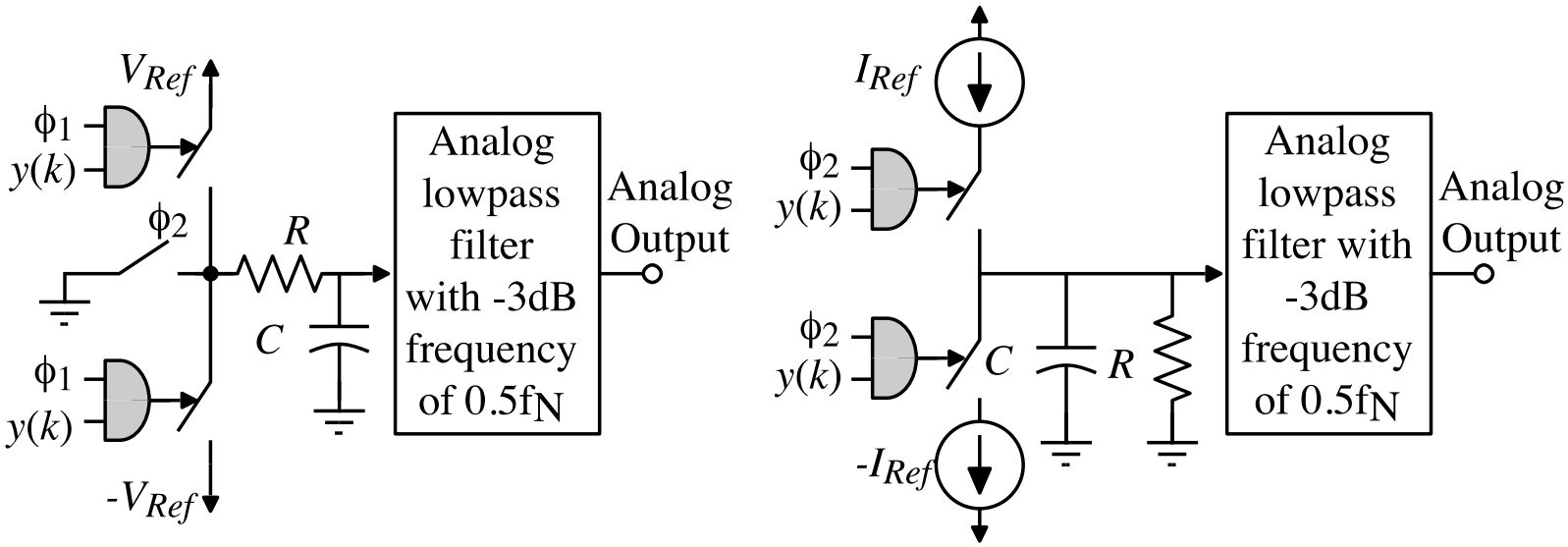




1-BitDAC for the ΔΣ Digital-to-Analog Converter - The Analog Part

The MSB output from the digital filter is used to drive a 1-bit DAC.

Possible architectures:



Voltage-driven DAC with a passive lowpass filter stage.

Current-driven DAC with a passive lowpass filter stage.

Fig10.9-32

A multi-bit output would consist of more parallel, controlled current sources and sinks.

Switched-Capacitor DAC and Filter

Typically, the DAC and the first stage of the lowpass filter are implemented using switched-capacitor techniques.

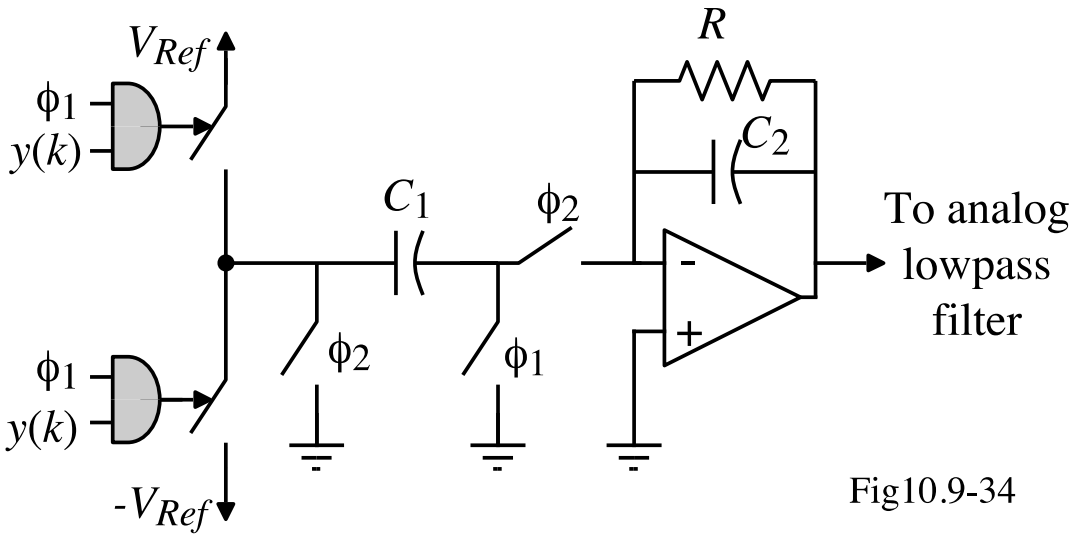


Fig10.9-34

It is necessary to follow the switched-capacitor filter by a continuous time lowpass filter to provide the necessary attenuation of the quantization noise.

SUMMARY

Comparison of the Various Types of ADCs

A/D Converter Type	Maximum Practical Number of Bits (±1)	Speed (Expressed in terms of T a clock period)	Area Dependence on the number of bits, N, or other ADC parameters
Dual Slope	12-14 bits	$2(2^{NT})$	Independent
Successive Approximation with self-correction	12-15 bits	NT	$\propto N$
1-Bit Pipeline	10 bits	T (After NT delay)	$\propto N$
Algorithmic	12 bits	NT	Independent
Flash	6 bits	T	$\propto 2^N$
Two-step, flash	10-12 bits	$2T$	$\propto 2^{N/2}$
Multiple-bit, M-pipe	12-14 bits	MT	$\propto 2^{N/M}$
Δ-Σ Oversampled (1-bit, L loops and M= oversampling ratio = $f_{clock}/2f_b$)	15-17 bits	MT	$\propto L$

ADC Performance Survey 1997-2015

Professor Boris Murmann, Stanford University has compiled a survey of the performance of converters presented at ISSCC and VLSI from 1997 to 2015. This survey is found at

http://www.stanford.edu/~murmann/adcsurvey.html

Notes on the primary raw data:

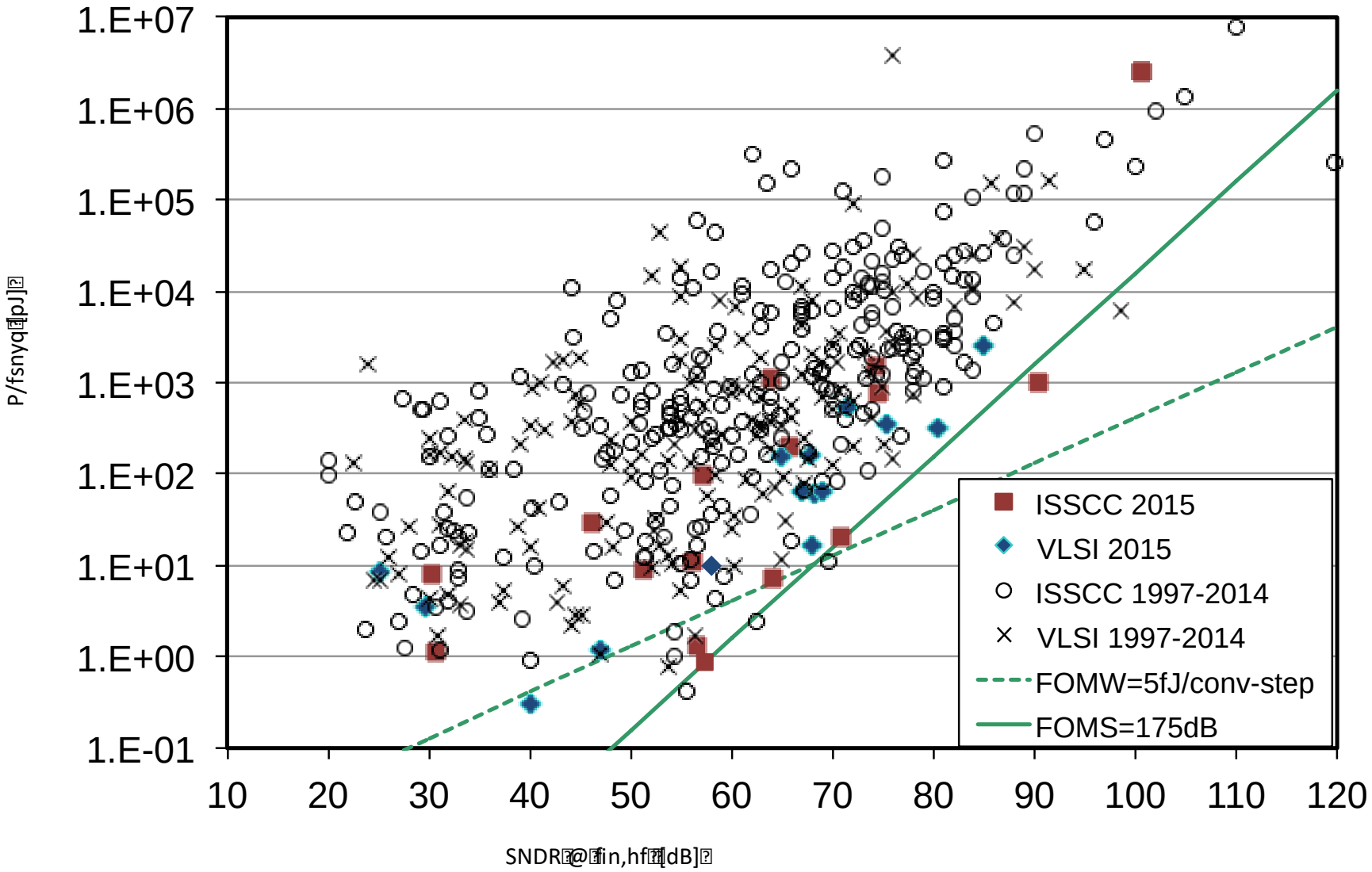
Power (P) - Taken as specified by the authors. Sometimes this number includes power for clocks, references, etc; sometimes it doesn't. For delta-sigma modulators, the power for the decimation filter is not included. This is fair since the Nyquist converter data also does not include any power typically needed for anti-alias filtering.

THD, (peak) SNDR, (peak) SNR, SFDR are tabulated as the values measured near $f_s/2$ for a Nyquist converter. When this data was not available, data for lower input frequencies is used instead. Fortunately, in recent years most Nyquist converters are properly evaluated up to $f_s/2$. Only older data points (before ~2003) tend to suffer from "low frequency only" issues. Multi-GHz converters tend to roll off for frequencies much lower than $f_s/2$. For these designs, the SNDR at the highest reasonable/usable fin is used (example: ISSCC 2003, paper 18.2, f_s = 20GHz, SNDR measured at f_{in}=6GHz).

DR is the measured "instantaneous dynamic range" of the converter, i.e. this metric does not contain any extra dBs obtained through variable gain.

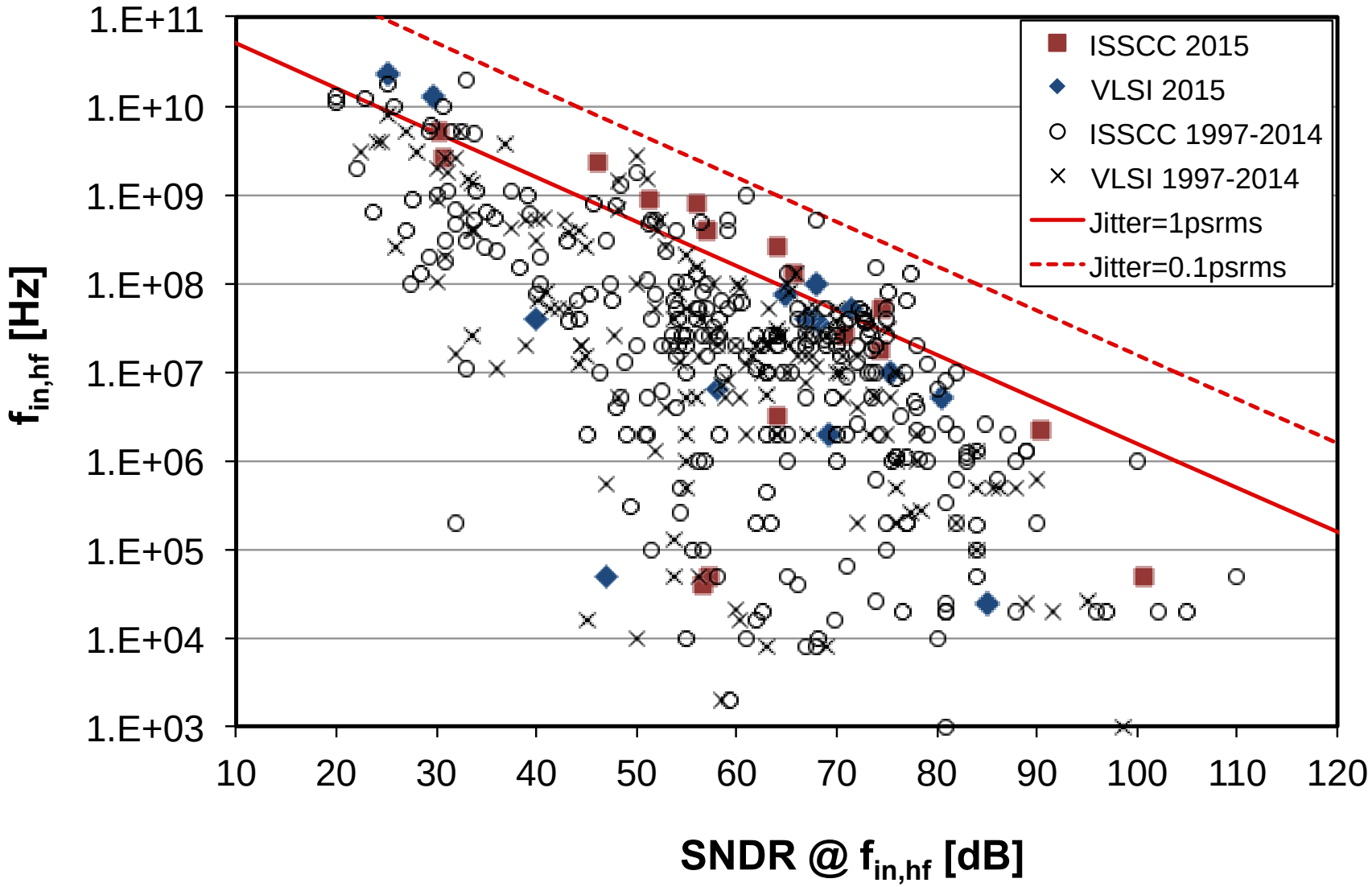
ADC Performance Survey - Continued

Energy versus resolution:



ADC Performance Survey - Continued

Bandwidth versus resolution:



CONCLUDING THOUGHTS

- What is analog circuit design?

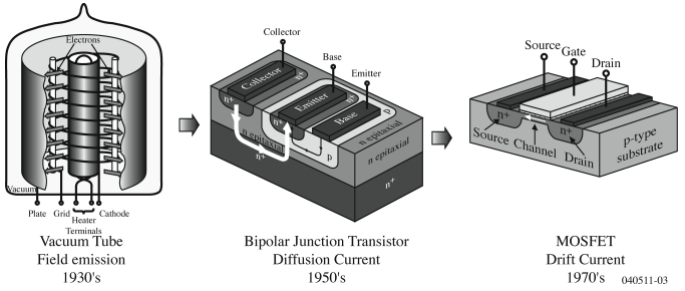
  The complex process of creating circuit solutions using analog circuit techniques.

- What is the analog integrated circuit design process?

  The even more complex process of combining analog design with IC technology which includes electrical, physical and test design.

- What are the key principles, concepts and techniques for analog IC design?

  Key principles – Fundamental laws
  Key concepts – Important relationships and ideas
  Key techniques – Tools that allow simplification or insight



Technology changes but principles, concepts and techniques remain the same.

- How can the analog IC designer enhance creativity and solve new problems in today's industrial environment?

  Learn the key principles, concepts and techniques of analog circuit design
  Learn from mistakes
  Learn the technology
  Always try to understand the concept and operation of the circuit, never rely on a computer or someone else for this understanding