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# The Design of a Bootstrapped Sampling Circuit

Bootstrapped samplers serve as an integral component of analog-to-digital converters (ADCs). The bootstrapping action reduces the distortion and improves the speed with a minimal power penalty. In this article, we present the step-by-step design of this circuit to see how the analog mind goes about such a task. The reader is encouraged to review the sampler's detailed operation [1]–[4] before continuing with this article.

## Basic Operation

As explained in [4], metal–oxide semiconductor (MOS) sampling switches exhibit two sources of distortion: their on-resistance and channel charge vary with their gate source voltage,  $V_{GS}$ , and hence with the analog input level. These effects can be minimized if  $V_{GS}$  is maintained constant in the sampling phase, e.g., by tying a battery between the gate and the source terminals [Figure 1(a)]. We say the gate is “bootstrapped” to the source, as the former's voltage varies in unison with the latter's.

The circuit in Figure 1(a) requires two modifications so it can act as a sampler. First, a means of disengaging  $V_B$  from  $M_1$  is necessary so that  $M_1$  can be turned off. Second, the battery can be approximated by a capacitor,  $C_B$ , but the charge on  $C_B$  must be periodically refreshed. We thus arrive at the basic topology shown in Figure 1(b). In the sampling mode (also called the *track mode*),  $M_2$  and  $M_3$  are on, reducing the cir-

cuit to that in Figure 1(a). In the hold mode,  $M_4$ – $M_6$  are on, grounding the gate of  $M_1$  and charging  $C_B$  to  $V_{DD}$ . The choice of PMOS and NMOS devices for these switches is described in [3] and [4].

## Design Specifications

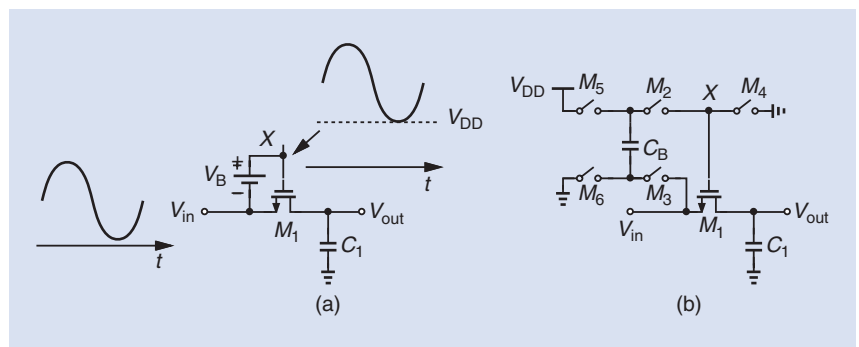
We wish to design a differential sampler for the front end of a Nyquist-rate ADC with a resolution of 10 b and a sampling rate of 5 GHz. Of the clock period of  $T_{CK} = 200$  ps, we allocate one half to the sampling mode and the other half to the hold mode. The design proceeds in a 28-nm CMOS process in the slow-slow corner, at a temperature of  $75^\circ\text{C}$  and with a worst-case supply of  $1\text{ V} - 5\% = 0.95\text{ V}$ . We assume a single-ended input range from 0.25 to 0.75 V, which translates to a least-significant-bit (LSB) size of  $1\text{ V}/1,024 \approx 1\text{ mV}$  for the differential ADC. The bootstrapped sampler accommodates greater swings, but the stage preceding it—typically, a buffer—may not. For an  $N$ -bit ADC sensing a signal of the form  $A\cos\omega_{in}t$ , the ideal signal-to-noise ratio (SNR) is given by  $(A^2/2)/(\Delta^2/12)$ , where

$\Delta$  is the LSB and equal to  $2A/2^N$ . It follows that  $\text{SNR} = 6.02N + 1.76\text{ dB}$ , which amounts to 62 dB for  $N = 10$ . In our differential system,  $A = 0.5\text{ V}$ .

The ADC specifications readily dictate certain values for the sampler. First, the harmonic distortion (HD) must remain well below  $-62\text{ dB}$ . Our ambition is to achieve an HD of roughly  $-65\text{ dB}$  in the worst case, namely, when  $A = 0.5\text{ V}$  and  $f_{in} = \omega_{in}/(2\pi)$  is near 2.5 GHz (i.e., at the Nyquist rate). Second, the noise introduced by the sampler must negligibly degrade the overall SNR. Thus, the  $kT/C$  noise associated with  $M_1$  and  $C_1$  in Figure 1(b) must be sufficiently small. We express the SNR of the sampler–ADC cascade as

$$\text{SNR} = \frac{\frac{A^2}{2}}{\frac{\Delta^2}{12} + \frac{2kT}{C_1}}, \quad (1)$$

where the factor of 2 in the denominator accounts for the noise in a differential sampling configuration. Let us target a 1-dB penalty due to  $kT/C$  noise, divide the SNR in (1) by the ideal SNR equation, take



**FIGURE 1:** (a) A simple bootstrapped switch. (b) A more complete implementation.

10log of the result, and equate it to  $-1$  dB. With  $\Delta = 1$  mV and  $T = 75^\circ\text{C} = 348\text{K}$ , we obtain  $C_1 = 445$  fF, which we round up to  $0.5$  pF.

Third, the low-pass filter formed by  $M_1$  and  $C_1$  in Figure 1(b) must negligibly attenuate the input signal in the track mode. The output amplitude is equal to  $A/\sqrt{1 + R_{\text{on}1}^2 C_1^2 \omega_{\text{in}}^2}$ , where  $R_{\text{on}1}$  denotes the on-resistance of  $M_1$ . We aim for an attenuation less than  $0.5$  dB at the Nyquist rate, arriving at  $R_{\text{on}} = 44.5\Omega$ . We should select  $M_1$  so that it is wide enough to ensure such a low resistance with  $V_{\text{GS}1} \approx V_{\text{DD}} = 0.95\text{V}$ . This constraint yields  $W_1 \approx 10\text{ }\mu\text{m}$  if  $L_1 = 28\text{ nm}$ .

## Design Procedure

To understand the effect of device nonidealities, we follow an incremental design procedure. Specifically, we proceed in five steps: 1) we keep the battery in Figure 1(a) and examine the distortion in only the track mode; 2) we allow the circuit to act as a sample-and-hold stage but, except for  $M_1$  in Figure 1(b), use ideal switches; 3) we change  $M_2$  and  $M_4$  to MOS devices; 4) we change the remaining switches to MOSFETs; and 5) we replace the battery with a capacitor. In each case, we apply the full-scale input amplitude and measure the harmonic content of the differential output at a moderate input frequency and at the Nyquist rate. The incremental approach also permits us to optimize the design in every step. We prefer to select minimum widths and lengths for the transistors unless there is a compelling rea-

son not to do so. In this article, all channel lengths are equal to  $28\text{ nm}$ .

## Simulation Issues

In the design of sampling circuits, the clock and the input frequencies must be carefully chosen. If  $f_{\text{CK}}$  is an integer multiple of  $f_{\text{in}}$ , then the circuit samples only certain points on the input waveform [Figure 2(a)], failing to reveal its true performance. Even if we select  $f_{\text{CK}}/f_{\text{in}} = P/Q$ , where  $P$  and  $Q$  are integers, we still have  $QT_{\text{in}} = PT_{\text{CK}}$ , where  $T_{\text{in}} = 1/f_{\text{in}}$ . This means that every  $Q$  cycles of the input exactly coincide with  $P$  cycles of the clock; thus, only  $Q$  values of the input are periodically sampled. For this reason, we should select  $f_{\text{CK}}$  and  $f_{\text{in}}$  such that the samples gradually slide along the input sinusoid and eventually assume all (or most) of the input values [Figure 2(b)]. This is accomplished if  $f_{\text{CK}}/f_{\text{in}}$  is an irrational number. For simulations, we simply guarantee that  $P/Q$  yields a long periodicity. For example, with  $f_{\text{CK}}/f_{\text{in}} = 5\text{ GHz}/570\text{ MHz} = 500/57$ , the sampled points repeat themselves after every 500 clock cycles; i.e., 500 distinct points of the input voltage are collected.

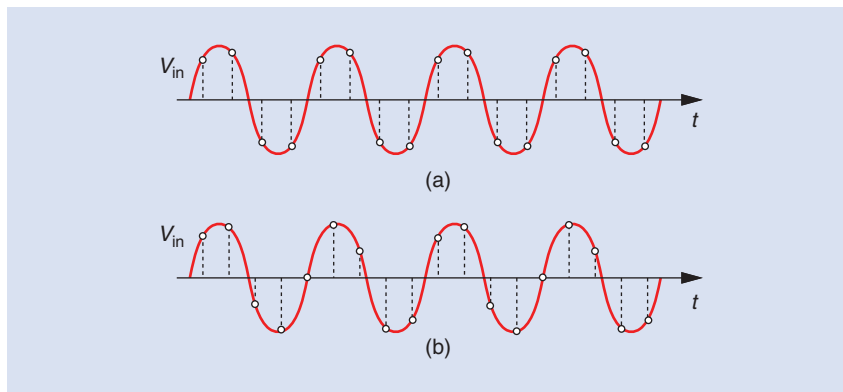
Another issue relates to how we process the output time-domain waveform in Figure 1(b) to go to the frequency domain. Since the ADC following the sampler senses only the held values on  $C_1$ , the time points taken by the fast Fourier transform (FFT) must be confined to the hold mode [Figure 3(a)]. That the ADC digitizes only the held values also sug-

gests that the sampler-ADC cascade equivalently multiplies the analog input by a train of impulses in the time domain [Figure 3(b)] and hence convolves the input spectrum with a train of impulses in the frequency domain [Figure 3(c)]. We call the range between  $-f_{\text{CK}}/2$  and  $+f_{\text{CK}}/2$  the *first Nyquist zone* and generally confine our inspection of unwanted components to this region.

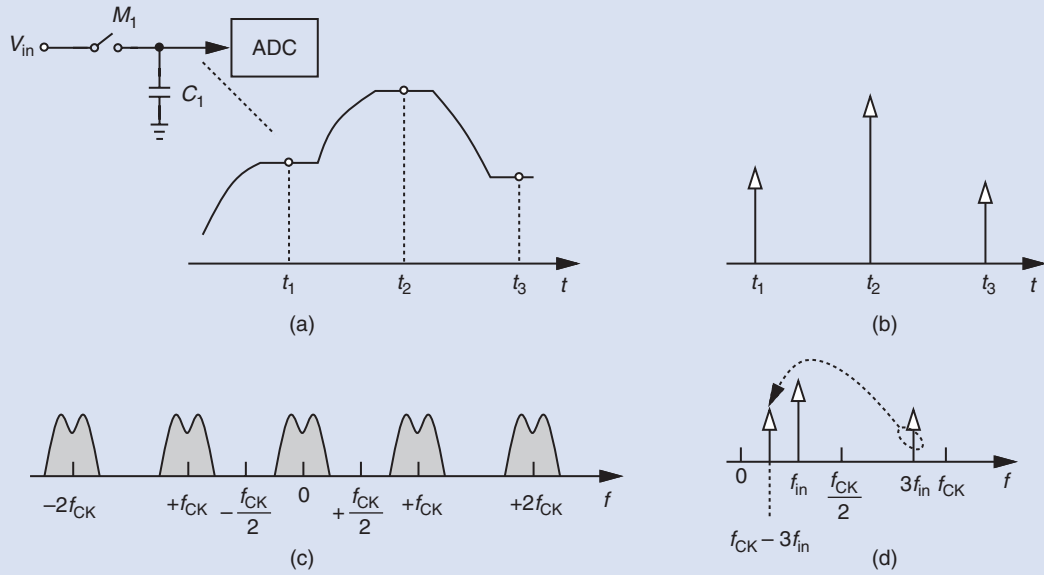
If the FFT senses only the values at  $t_1, t_2$ , and so on, the resulting spectrum is given by the convolution of the input spectrum and a train of impulses. This point proves useful in understanding the FFT results. For example, if the sampler introduces third-order distortion at  $3f_{\text{in}}$  and this component lies above  $f_{\text{CK}}/2$ , then it is aliased to the first Nyquist zone. Depicted in Figure 3(d), this phenomenon causes the third harmonic to land at  $f_{\text{CK}} - 3f_{\text{in}}$ .

## Track-Mode Distortion

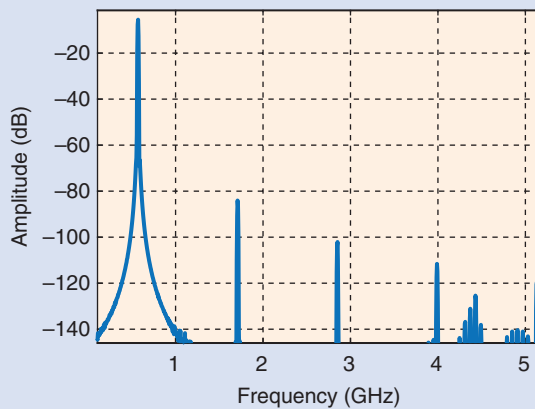
We begin by simulating two instances of Figure 1(a) with differential inputs and  $f_{\text{in}} = 570\text{ MHz}$ . As mentioned,  $W_1 = 10\text{ }\mu\text{m}$  for now. We surmise that this test yields a lower bound for the distortion because higher input frequencies and the sample-and-hold action tend to introduce greater nonlinearity. Figure 4 plots the FFT of the differential output. As expected, even harmonics are absent. The third and fifth harmonics are  $79$  and  $97$  dB below the fundamental, respectively. We denote the relative level of the former by  $HD_3$  and that of the latter by  $HD_5$ . Next, we increase  $f_{\text{in}}$  to  $2.47\text{ GHz}$  and repeat the simulation. Figure 5(a) shows the time-domain outputs, revealing a peak-to-peak single-ended swing of  $483\text{ mV}$ , which satisfies our attenuation constraint of  $0.5$  dB. The output spectrum is plotted in Figure 5(b), exhibiting a third harmonic at  $-56$  dB. This high level of distortion occurs because  $R_{\text{on}1}$  varies significantly due to the body effect. As explained in [4], the output phase then varies considerably with the input voltage. We must therefore reduce  $R_{\text{on}1}$ . Changing  $W_1$  from  $10$  to



**FIGURE 2:** Sampling the input with (a) an integer  $f_{\text{CK}}/f_{\text{in}}$  ratio and (b) an irrational  $f_{\text{CK}}/f_{\text{in}}$  ratio.



**FIGURE 3:** (a) Sensing the held values via an ADC. (b) The equivalent ADC output in the time domain. (c) The corresponding spectrum. (d) The aliasing of the third input harmonic.

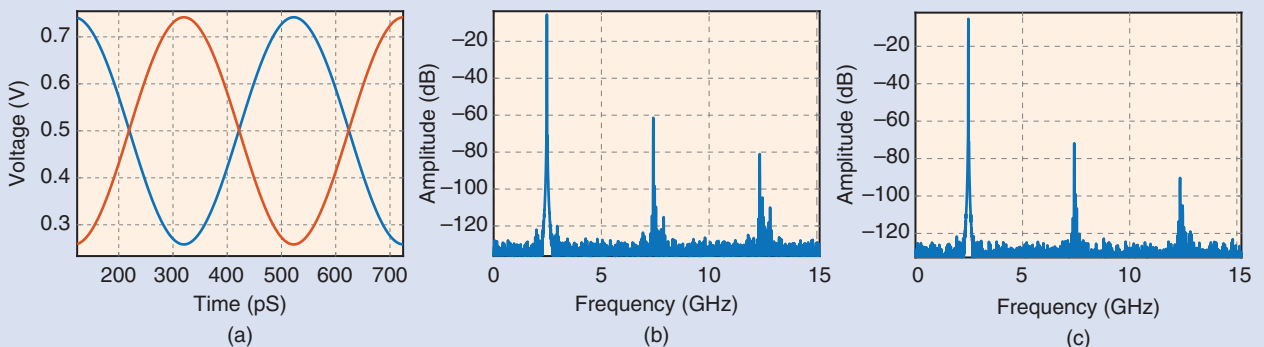


**FIGURE 4:** The track-mode output spectrum for  $f_{in} = 570$  MHz.

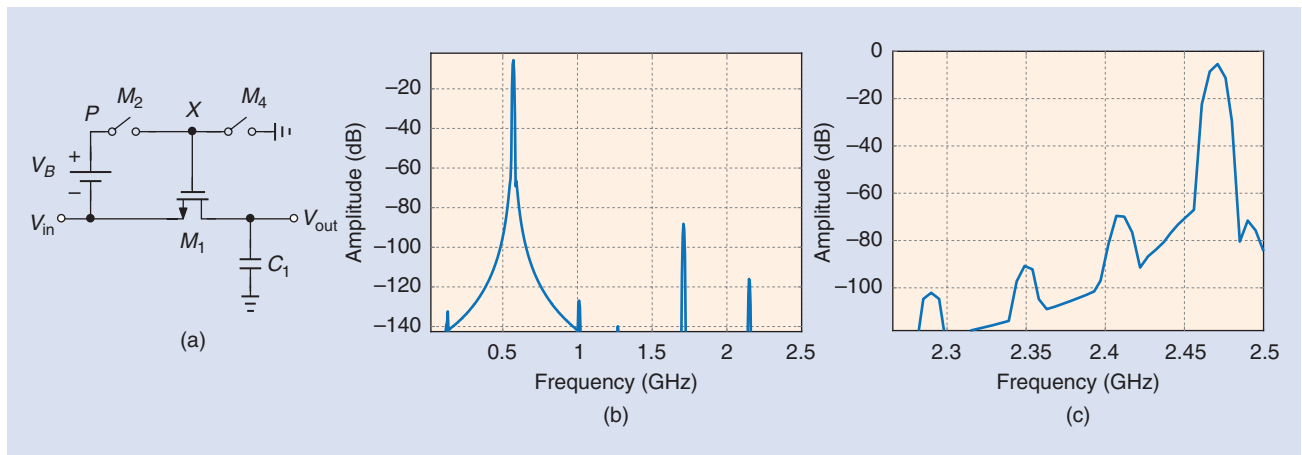
20  $\mu\text{m}$  yields the spectrum shown in Figure 5(c), achieving an  $\text{HD}_3$  of  $-66$  dB and an  $\text{HD}_5$  far below this level. We hereafter assume  $W_1 = 20$   $\mu\text{m}$ .

### Basic Sampler

In the next step of our design effort, we add two ideal switches to Figure 1(a) so that  $M_1$  is turned on and off by the clock [Figure 6(a)]. To create some similarity to the actual circuit, we define an on-resistance of 50  $\Omega$  for  $M_2$  and  $M_4$ . Figure 6(b) plots the output spectrum for  $f_{in} = 570$  MHz. The third harmonic is at 1.71 GHz and has a relative level of  $-83$  dB. The fifth harmonic, on the other hand,



**FIGURE 5:** (a) The track-mode output waveforms for  $f_{in} = 2.47$  GHz. (b) The corresponding spectrum. (c) The reduced distortion as a result of doubling  $W_1$ .



**FIGURE 6:** (a) A sampler using ideal switches  $M_2$  and  $M_4$ . (b) The output spectrum for  $f_{in} = 570$  MHz. (c) The output spectrum for  $f_{in} = 2.47$  GHz.

is aliased to  $f_{CK} - 5f_{in} = 2.15$  GHz, exhibiting a normalized level of  $-110$  dB. Next, we raise  $f_{in}$  to 2.47 GHz and note that its third harmonic appears at  $f_{CK} - 3f_{in} = 2.41$  GHz. Depicted in Figure 6(c), the output spectrum yields  $HD_3 = -64.4$  dB, 1.3 dB higher than the track-mode distortion found in the preceding. This can

be attributed to the channel charge injected by  $M_1$  onto  $C_1$  in Figure 6(a); even though  $V_{GS1}$  is constant, the transistor's threshold is not, modulating the charge as  $V_{in}$  varies.

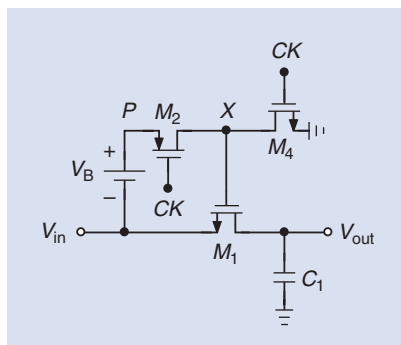
### Sampler With MOS Switches

At this point, we wish to implement  $M_2$  and  $M_4$  in Figure 6(a) by using MOS devices. We recognize that  $M_4$  must be an NMOS device because it pulls  $X$  to the ground, whereas  $M_2$  must be a PMOS device as it ties  $X$  to a high potential (Figure 7). But we must also decide to which node the n-well of  $M_2$  should be connected. If attached to  $X$ , the n-well is drawn toward the ground by  $M_4$  when  $M_2$  is off, thereby forward-biasing the junctions between the n-well and the source and the drain of  $M_2$ . To avoid this issue, we tie the n-well to node  $P$ .

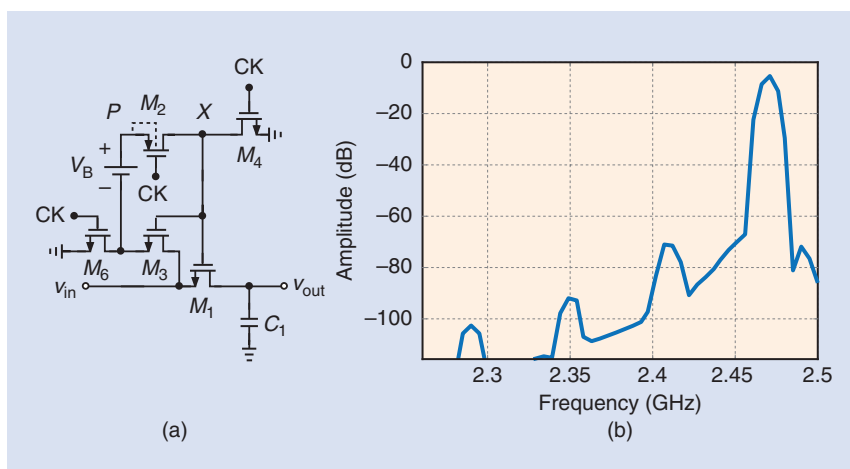
The minimum widths of  $M_2$  and  $M_4$  are dictated by the following constraints. We note that  $R_{on2}$  and the total capacitance at  $X$ —primarily, the gate source capacitance of  $M_2$ —form a low-pass filter, attenuating the input swing as it reaches  $X$ . Thus,  $R_{on2}$  must be chosen so that it provides a bandwidth far beyond 2.5 GHz. This is readily possible with a  $W_2$  of a few microns. We select  $W_2 = 2.5$   $\mu$ m. Moreover,  $M_4$  must pull  $X$  down at a high slew rate so as to rapidly turn off  $M_1$ . If it does not, the on-resistance of  $M_1$  increases slowly, causing distortion. We select  $W_4 = 2.5$   $\mu$ m for now. For the clock driving these two switches, we choose 10-ps rise and fall times, as a representative in 28-nm technology.

Upon simulating the topology of Figure 7 with  $f_{in} = 570$  MHz and 2.47 GHz, we obtain an  $HD_3$  of  $-68$  and  $-58$  dB, respectively. Why is the linearity degraded by such a large amount? The reason is that  $M_2$  fails to turn off for part of the input swing: if  $V_{in} > 0.5$  V, then  $V_P > 1.5$  V, keeping  $M_2$  on, even if its gate is raised to 1 V. Consequently,  $M_4$  cannot pull  $X$  to zero, and  $M_1$  does not completely turn off.

To resolve this issue, we must remove the bootstrapping action in the hold mode. That is, the battery must be disconnected from the analog input. We thus add switches  $M_3$  and  $M_6$  [Figure 8(a)]. Now, when  $CK$  is high,  $V_B$  generates  $V_P = V_{DD}$ , allowing  $M_2$  to turn off. The gate of  $M_3$  could not be driven by the rail-to-rail clock because



**FIGURE 7:** The realization of  $M_2$  and  $M_4$ .



**FIGURE 8:** (a) The addition of switches to disengage  $V_B$  in the hold mode. (b) The output spectrum for  $f_{in} = 2.47$  GHz.

the on-resistance of  $M_3$  would vary considerably in the track mode. For this reason, we bootstrap its gate to  $V_{in}$  in a manner similar to  $M_1$ . The on-resistance of  $M_3$  should be comparable to that of  $M_2$  and not limit the bandwidth at node  $X$ . We tentatively choose  $W_3 = 2.5\mu\text{m}$  and  $W_6 = 1\mu\text{m}$ . Simulations indicate an  $HD_3$  of  $-84$  and  $-60$  dB for  $f_{in} = 570$  MHz and  $f_{in} = 2.47$  GHz, respectively. The latter case is shown in Figure 8(b). The circuit performs satisfactorily at this stage of the design.

In the last step, we replace the bootstrapping battery with a capacitor, as indicated in Figure 1(b). This requires that  $M_5$  be added so that  $C_B$  can be charged to  $V_{DD}$  in the hold mode. Several questions arise. First, to which node should the gate of  $M_5$  be connected? If driven as in Figure 9(a),  $M_5$  fails to turn off when  $\overline{CK}$  is high because  $V_P = V_{in} + V_{DD}$  can reach 1.75 V. We therefore surmise that the gate of  $M_5$  must be bootstrapped to  $V_{in}$  as well [Figure 9(b)]. Second, to which node should the n-well of  $M_5$  be connected? For the same reason mentioned for  $M_2$ , this n-well must be tied to node  $P$ .

The third question relates to the minimum acceptable value of  $C_B$ . Two effects play a role here. When  $C_B$  is switched to  $X$ , it experiences charge sharing with the total parasitic capacitance at this node, thereby providing a bootstrapping voltage that is less than

$V_{DD}$ . The parasitics at  $X$  include the gate capacitances of  $M_1, M_3$ , and  $M_5$  (the first two conducting and the third remaining off) and the drain capacitances of  $M_2, M_4$ , and  $M_5$ . Thus,  $C_B$  must be large enough to minimize the voltage loss. For  $C_B$  to fully charge to  $V_{DD}$  during the hold mode, the series combination of  $M_5, C_B$ , and  $M_6$  must exhibit a time constant that is less than half of the clock period. As an example, with  $T_{CK}/2 = 100$  ps and  $C_B = 0.25$  pF, the total on-resistance of  $M_5$  and  $M_6$  must remain lower than  $400\Omega$ .

We select  $C_B = 0.25$  pF and  $W_5 = 2.5\mu\text{m}$  in Figure 9(b) and increase  $W_6$  from 1 to  $2.5\mu\text{m}$ . The simulation yields an  $HD_3$  of  $-63$  dB at  $f_{in} = 2.47$  GHz. To assess the bootstrapping ability of  $C_B$ , we plot its voltage as a function of time [Figure 9(c)]. We observe that  $C_B$  charges to only 0.895 V (rather than to  $V_{DD} = 0.95$  V) due to the long time constant. Moreover, the bootstrapping voltage is less than 0.83 V due to charge sharing. From the difference between 0.895 and 0.83 V, we estimate a parasitic capacitance of 20 fF at node  $X$ .

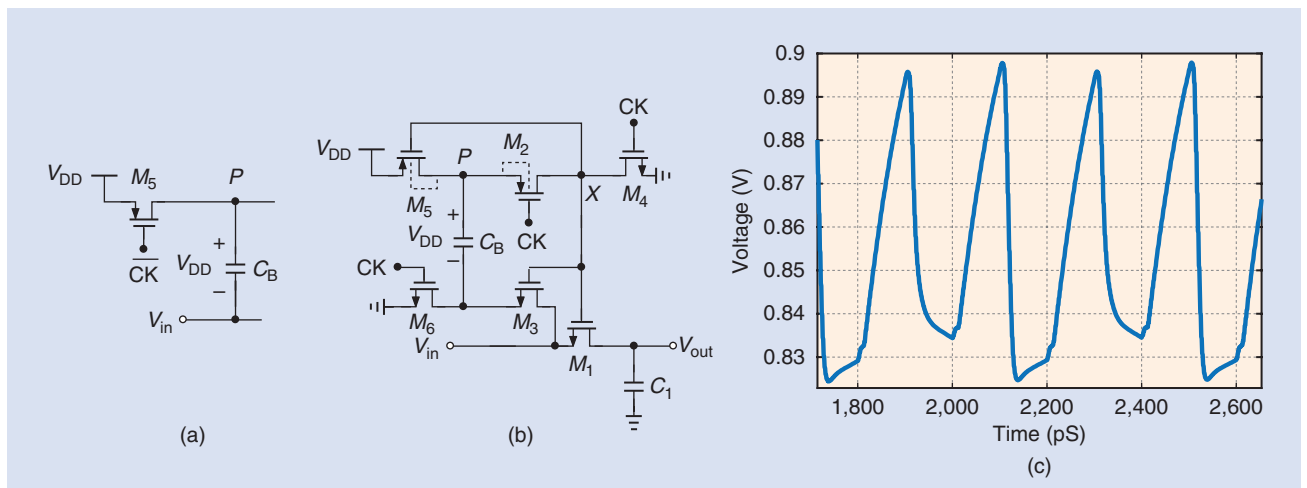
To improve the charge replenishment of  $C_B$ , we must further widen  $M_5$  and  $M_6$ , and to remedy the charge sharing, we must increase the value of  $C_B$ . Of course, an excessively wide  $M_5$  raises the parasitic at  $X$  and exacerbates the problem of charge sharing. Let us then choose  $C_B = 500$  fF,  $W_5 = 5\mu\text{m}$ , and  $W_6 = 5\mu\text{m}$ . Simula-

tions still suggest an  $HD_3$  of  $-63$  dB at  $f_{in} = 2.47$  GHz. We face diminishing returns, partially because the large parasitic at  $X$  now creates a long time constant with  $M_4$ , slowing down the turn-off transition of  $M_1$ . This is alleviated by increasing  $W_4$  to  $5\mu\text{m}$ . The circuit now exhibits an  $HD_3$  of  $-65$  dB at 2.47 GHz.

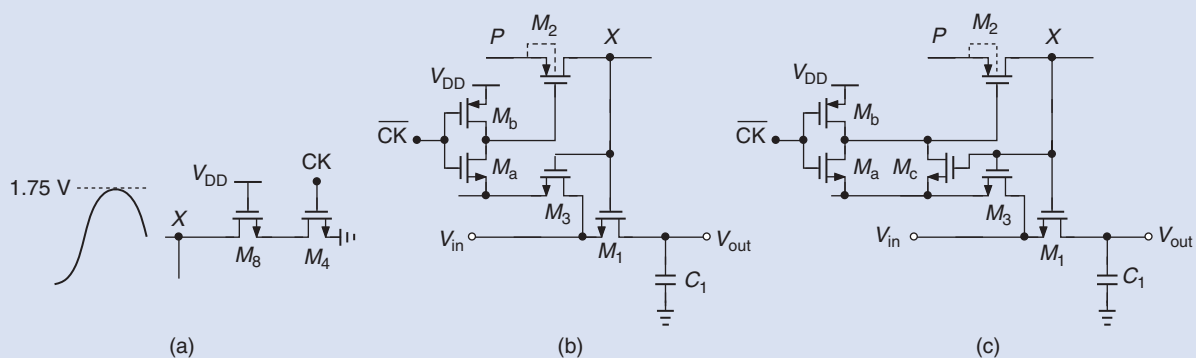
## Device Stress Issues

The topology of Figure 9(b) applies a drain source or gate source voltage well above 1 V to two of the MOSFETs in the track mode. Called *device stress*, this effect degrades the transistors' performance over time. We recognize that, when it is off,  $M_4$  experiences a peak drain source voltage of  $V_{in} + V_{DD} \approx 1.75$  V. Similarly,  $M_2$  sees the same voltage difference between its gate and its source. To protect the former, we place a cascode device in series with it. As depicted in Figure 10(a),  $M_8$  shields  $M_4$ , ensuring that  $V_{DS4} < V_{DD}$ ;  $M_8$  itself sustains a maximum  $V_{DS}$  of  $1.75\text{ V} - (V_{DD} - V_{TH4}) \approx 1.05$  V. The series action of these two devices demands that they both be  $10\mu\text{m}$  wide.

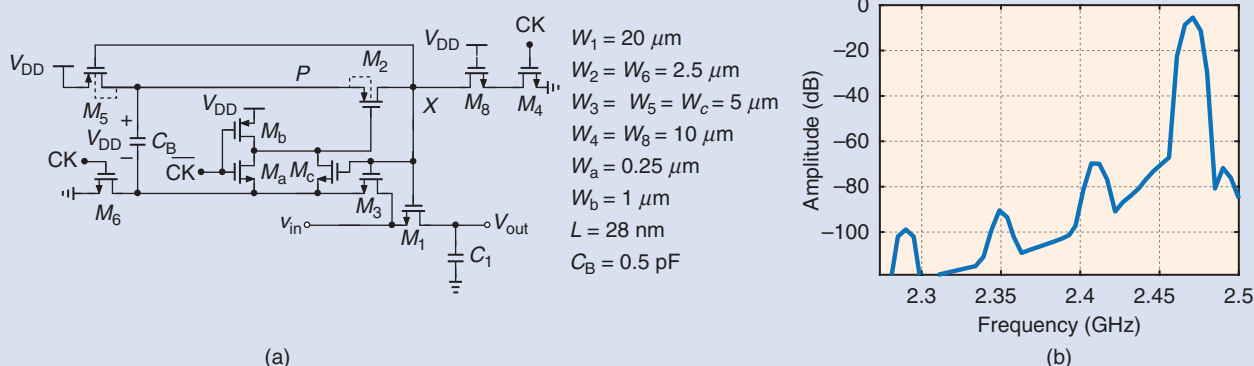
The solution for reducing the stress on  $M_2$  in Figure 9(b) is more complex. We note that the only possibility is to allow the gate voltage of  $M_2$  to change in unison with  $V_X$  and hence with  $V_{in}$ . That is, this gate must be connected to  $V_{in}$  in the track mode and to  $V_{DD}$  in the hold mode. Figure 10(b) presents an



**FIGURE 9:** (a) A PMOS pull-up device driven by  $\overline{CK}$ . (b) Bootstrapping the gate of  $M_5$  to  $V_{in}$  through  $V_X$ . (c) The voltage across  $C_B$ .



**FIGURE 10:** (a) The use of  $M_8$  to shield  $M_4$ . (b) The addition of  $M_a$  and  $M_b$  to bootstrap the gate of  $M_2$ . (c) The addition of  $M_c$  to provide a low resistance in series with the gate of  $M_2$ .



**FIGURE 11:** (a) The final design. (b) The final design's output spectrum for  $f_{in} = 2.47$  GHz.

implementation example, where  $M_a$  and  $M_b$ , respectively, perform these tasks. However, if  $\overline{CK}$  reaches only  $V_{DD}$ , then  $M_a$  turns off as  $V_{in}$  approaches its peak value of 0.75 V. This issue is resolved as depicted in Figure 10(c), where  $M_c$ , with its gate voltage bootstrapped to  $V_{in}$ , provides a low resistance in series with the gate of  $M_2$ . While appearing redundant,  $M_a$  is still necessary for the proper start-up of the circuit. We select  $W_a = 0.25 \mu\text{m}$ ,  $W_b = 1 \mu\text{m}$ , and  $W_c = 2.5 \mu\text{m}$ , the last one wide enough to avoid limiting the bandwidth at the gate of  $M_2$ .

Simulation of the modified circuit yields an  $HD_3$  of  $-63.4$  dB. We surmise that the bandwidth at the gate of  $M_2$  is still limited by the on-resistance of  $M_c$ . We then double  $W_c$ . The final design appears in Figure 11(a), and its output spectrum is in Figure 11(b). The  $HD_3$  is

$-64.3$  dB, the  $HD_5$  is approximately 20 dB lower, and the total power consumption is roughly 1 mW. The principal factor limiting the linearity is that the clock pulses arriving at node X are only some 80 ps wide, providing insufficient track time.

### Input Current Issues

Recall that we initially selected an on-resistance of roughly  $45 \Omega$  for the sampling switch in Figure 1(a) to ensure an attenuation less than 0.5 dB at  $f_{in} = 2.5$  GHz. We later doubled the width of  $M_1$  to meet the linearity requirement. With  $R_{on1} \approx 23 \Omega$ , the circuit draws a large input current when operating near the Nyquist rate. This occurs because the previous sample on  $C_1$  and the present input value at the beginning of the track mode can differ by as much as the entire single-ended swing, about 0.5 V. Thus,  $M_1$  carries an initial cur-

rent of  $0.5 \text{ V} / R_{on1} \approx 22 \text{ mA}$ . This current must be provided by the stage preceding the sampler, typically, a buffer. From another perspective, if the buffer must not limit the sampling speed, its output impedance must be well below  $23 \Omega$ , a great challenge in circuit design.

### References

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