LECTURE 10 – MOS CAPACITOR MODEL AND LARGE SIGNAL MODEL DEPENDENCE

LECTURE ORGANIZATION

Outline

- MOSFET capacitor model
- Dependence of the large signal model on process
- Dependence of the large signal model on voltage
- Dependence of the large signal model on temperature
- MOSFET reliability
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 77-86 and new material

MOSFET CAPACITOR MODEL

Submicron Technology

Physical perspective:

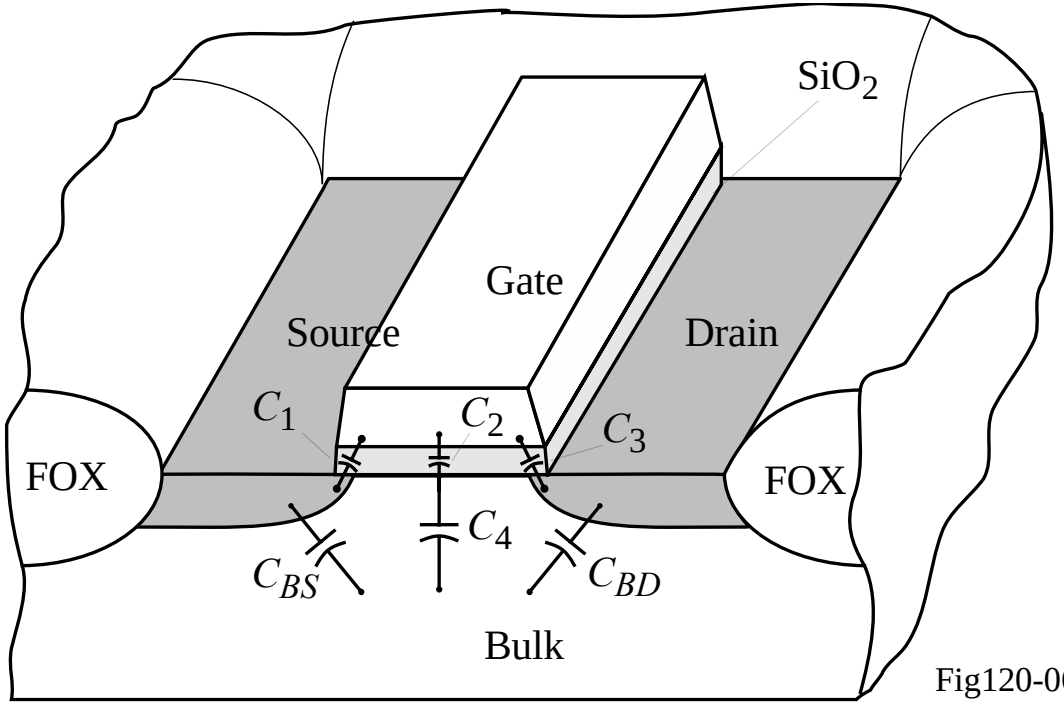


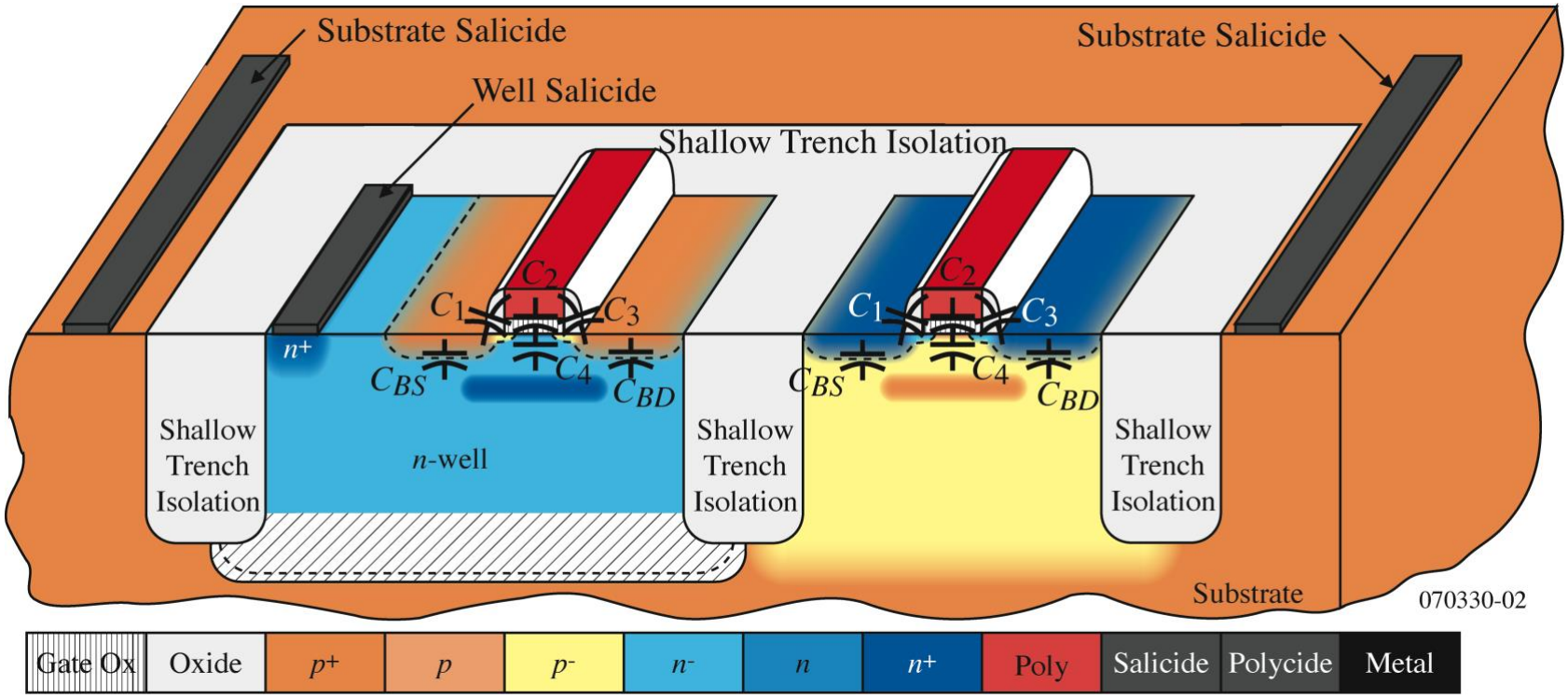
Fig120-06

MOSFET capacitors consist of:

- Depletion capacitances
- Charge storage or parallel plate capacitances

Deep Submicron Technology

Physical perspective:



MOSFET capacitors consist of:

- Depletion capacitances
- Charge storage or parallel plate capacitances

MOSFET Depletion Capacitors

Model:

1.) $v_{BS} \le FC \cdot PB$

$$C_{BS} = \frac{CJ \cdot AS}{\left(1 - \frac{v_{BS}}{PB}\right)^{MJ}} + \frac{CJSW \cdot PS}{\left(1 - \frac{v_{BS}}{PB}\right)^{MJSW}},$$

and

2.) $v_{BS} > FC \cdot PB$

$$C_{BS} = \frac{CJ \cdot AS}{(1 - FC)^{1+MJ}}\left(1 - (1+MJ)FC + MJ\frac{V_{BS}}{PB}\right)$$

$$+ \frac{CJSW \cdot PS}{(1 - FC)^{1+MJSW}}\left(1 - (1+MJSW)FC + MJSW\frac{V_{BS}}{PB}\right)$$

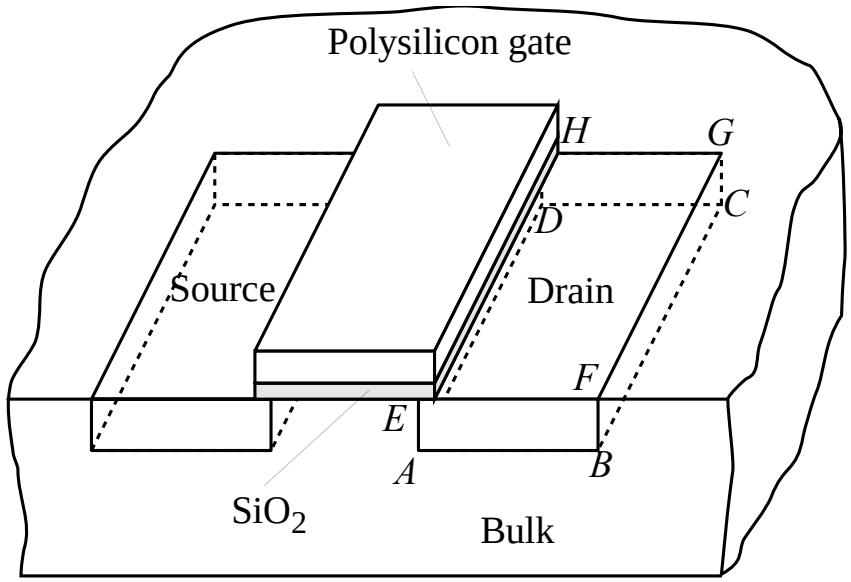


Fig. 120-07

Drain bottom = *ABCD*

Drain sidewall = *ABFE* + *BCGF* + *DCGH* + *ADHE*

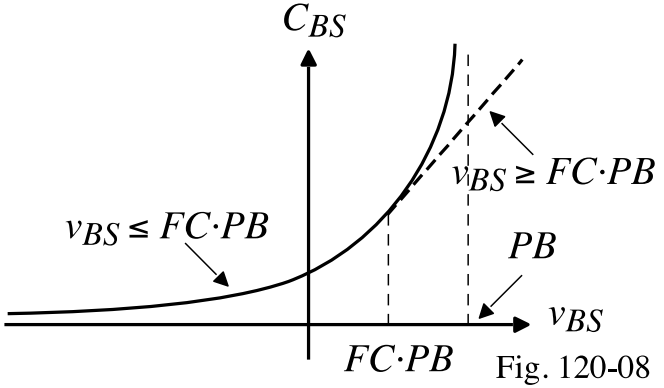


Fig. 120-08

where

AS = area of the source

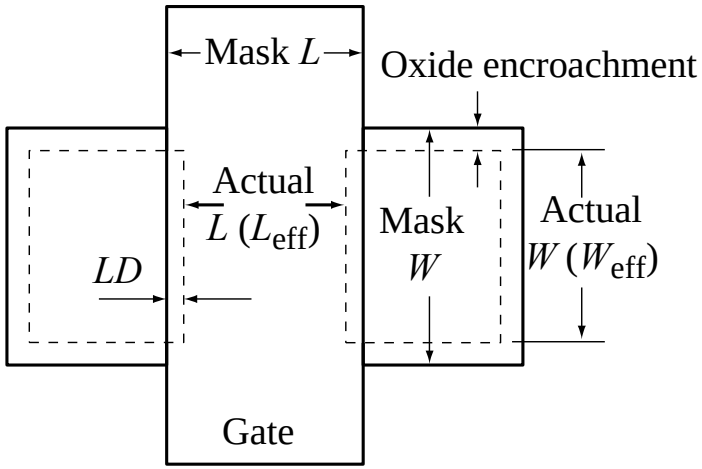
PS = perimeter of the source

CJSW = zero bias, bulk source sidewall capacitance

MJSW = bulk-source sidewall grading coefficient

For the bulk-drain depletion capacitance replace "*S*" by "*D*" in the above.

SM Charge Storage (Parallel Plate) MOSFET Capacitances - C_1, C_2, C_3 and C_4



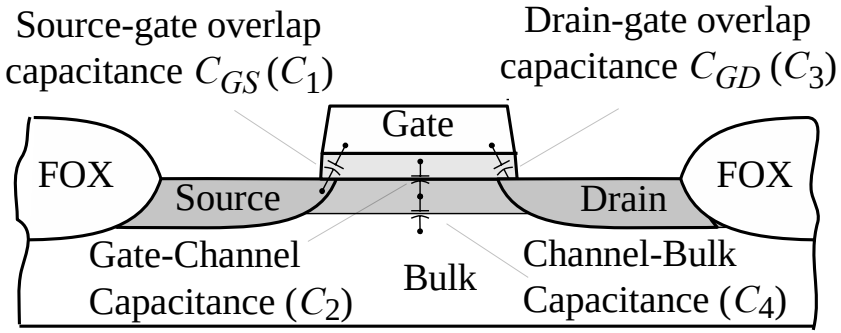


Fig. 120-09

Overlap capacitances:

$C_1 = C_3 = \text{LD} \cdot W_{\text{eff}} \cdot C_{ox}$ = CGSO or CGDO (LD ≈ 0.015 μm for LDD structures)

Channel capacitances:

C_2 = gate-to-channel = $C_{ox} W_{\text{eff}} \cdot (L\text{-}2\text{LD})$

$= C_{ox} W_{\text{eff}} \cdot L_{\text{eff}}$

C_4 = voltage dependent channel-bulk/substrate capacitance

SM Charge Storage (Parallel Plate) MOSFET Capacitances - C_5

View looking down the channel from source to drain

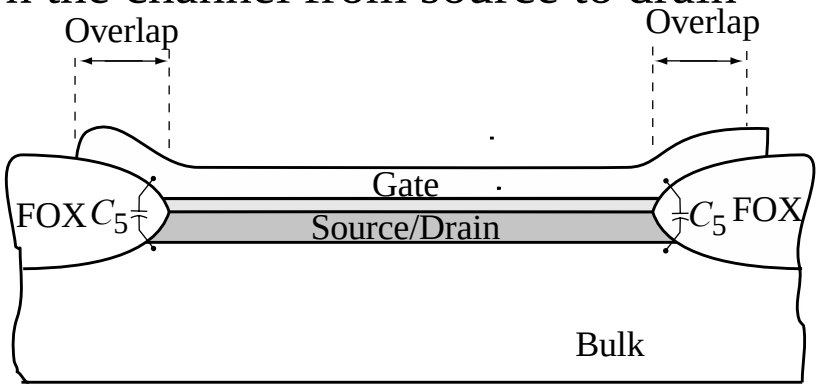


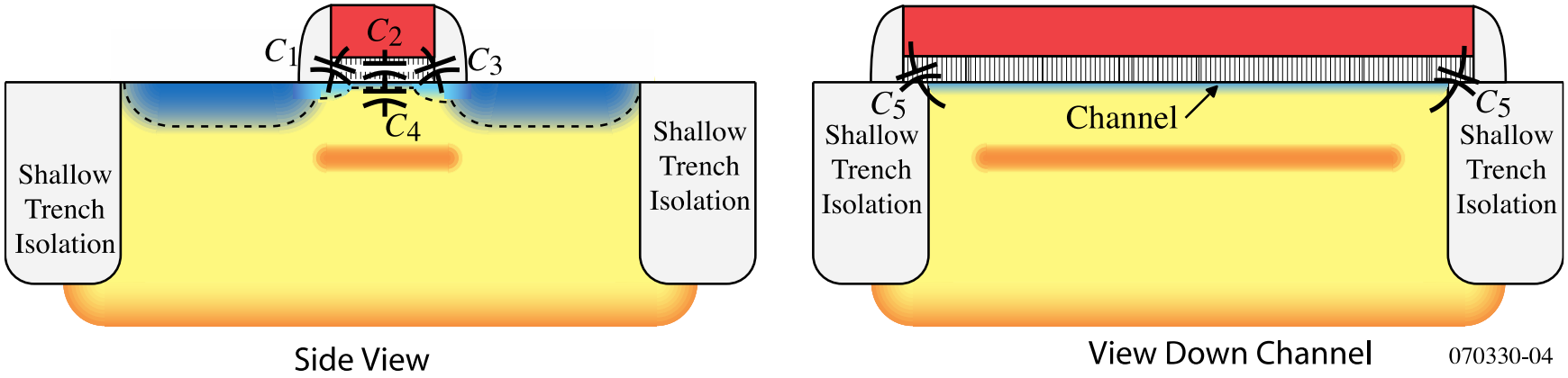
Fig120-10

C_5 = CGBO

Capacitance values based on an oxide thickness of 140 Å or $C_{ox}=24.7 \times 10^{-4}$ F/m^2:

Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

DSM Charge Storage MOSFET Capacitances - C_1, C_2, C_3, C_4 and C_5



C_1 and C_3 are overlap capacitors due to lateral diffusion of the source and drain

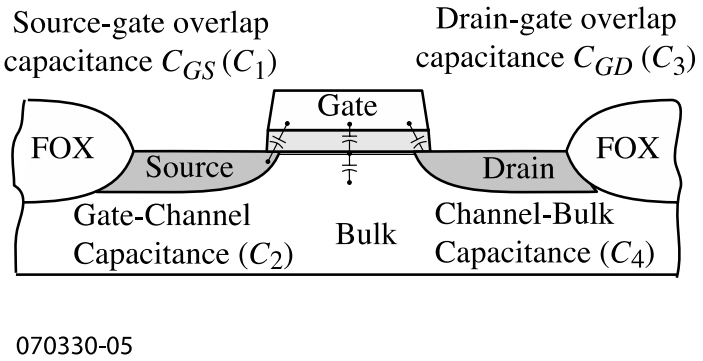
C_2 is the gate to channel capacitance

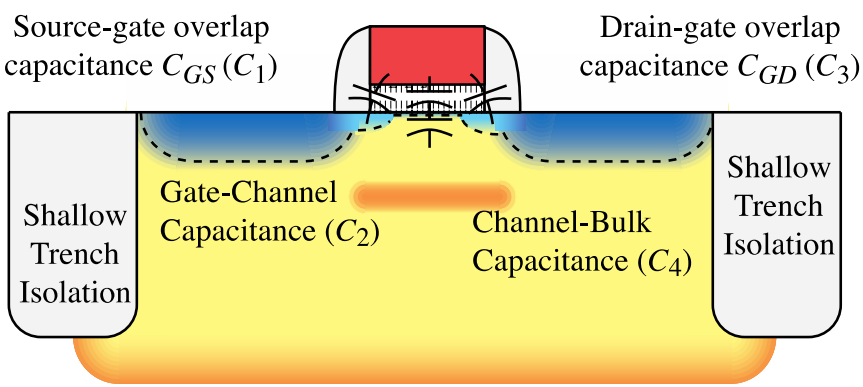
C_4 is the depletion capacitance between the channel and the bulk

C_5 is the fringing capacitance between the gate and the bulk around the edges of the channel

MOSFET Capacitors for the Cutoff Region

Side view:





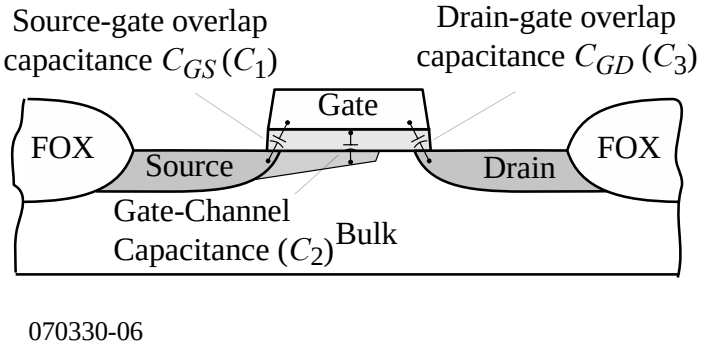
As the gate-source voltage varies from 0 to V_T, the channel-bulk capacitor varies from a very large capacitor (because of a very small depletion region) to a capacitor much smaller than C_2.

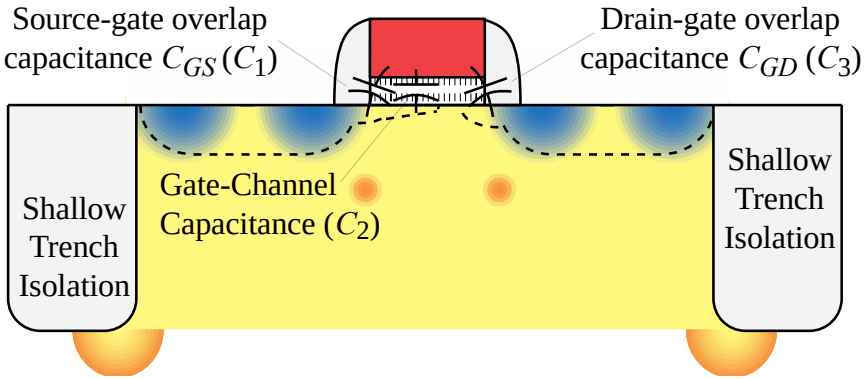
Capacitors in Cutoff:

C_{GS}	$C_1 = C_{ox} \cdot LD \cdot W = CGSO \cdot W$
C_{GD}	$C_3 = C_{ox} \cdot LD \cdot W = CGDO \cdot W$
C_{GB}	C_2 varies from $C_{ox} \cdot L \cdot W$ to $2C_5$
C_{BD}	$C_{BD} = (CJ \cdot AD)/[1 - (v_{BD}/PB)]^{MJ} + (CJSW \cdot PD)/[1 - (v_{BD}/PB)]^{MJSW}$
C_{BS}	$C_{BS} = (CJ \cdot AS)/[1 - (v_{BS}/PB)]^{MJ} + (CJSW \cdot PS)/[1 - (v_{BS}/PB)]^{MJSW}$

MOSFET Capacitors for the Saturation Region

Side view:





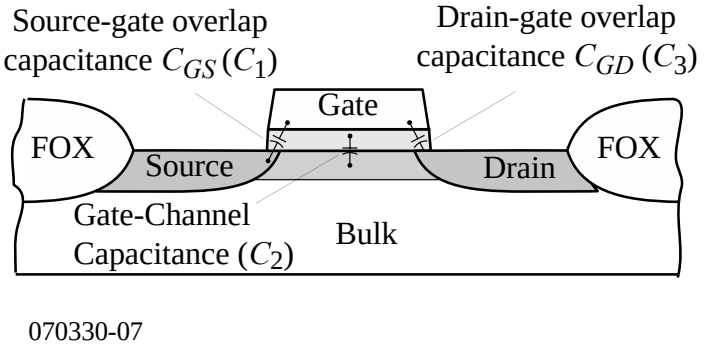
In the saturation region, C_4, becomes small and is not shown above.

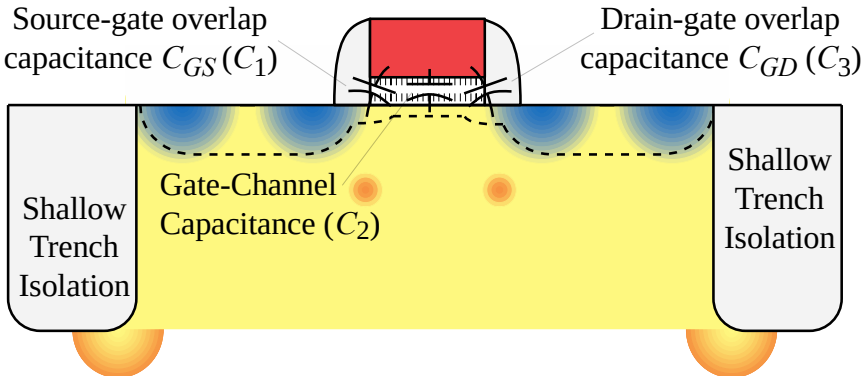
Capacitors in Saturation:

C_{GS}	$C_1 = C_{ox}\cdot LD\cdot W + (2/3)C_{ox}\cdot L\cdot W = [CGSO + (2/3)C_{ox}\cdot L]W$
C_{GD}	$C_3 = C_{ox}\cdot LD\cdot W = CGDO\cdot W$
C_{GB}	$2C_5 = 2\cdot CGBO\cdot W$
C_{BD}	$C_{BD} = (CJ\cdot AD)/[1 - (v_{BD}/PB)]^{MJ} + (CJSW\cdot PD)/[1 - (v_{BD}/PB)]^{MJSW}$
C_{BS}	$C_{BS} = (CJ\cdot AS)/[1 - (v_{BS}/PB)]^{MJ} + (CJSW\cdot PS)/[1 - (v_{BS}/PB)]^{MJSW}$

MOSFET Capacitors for the Active Region

Side view:





In the saturation region, C_4, becomes small and is not shown above.

Capacitors in Active:

C_{GS}	$C_1 = C_{ox}\cdot LD\cdot W + (1/2)C_{ox}\cdot L\cdot W = [CGSO + (1/2)C_{ox}\cdot L]W$
C_{GD}	$C_3 = C_{ox}\cdot LD\cdot W + (1/2)C_{ox}\cdot L\cdot W = [CGDO + (1/2)C_{ox}\cdot L]W$
C_{GB}	$2C_5 = 2\cdot CGBO\cdot W$
C_{BD}	$C_{BD} = (CJ\cdot AD)/[1 - (v_{BD}/PB)]^{MJ} + (CJSW\cdot PD)/[1 - (v_{BD}/PB)]^{MJSW}$
C_{BS}	$C_{BS} = (CJ\cdot AS)/[1 - (v_{BS}/PB)]^{MJ} + (CJSW\cdot PS)/[1 - (v_{BS}/PB)]^{MJSW}$

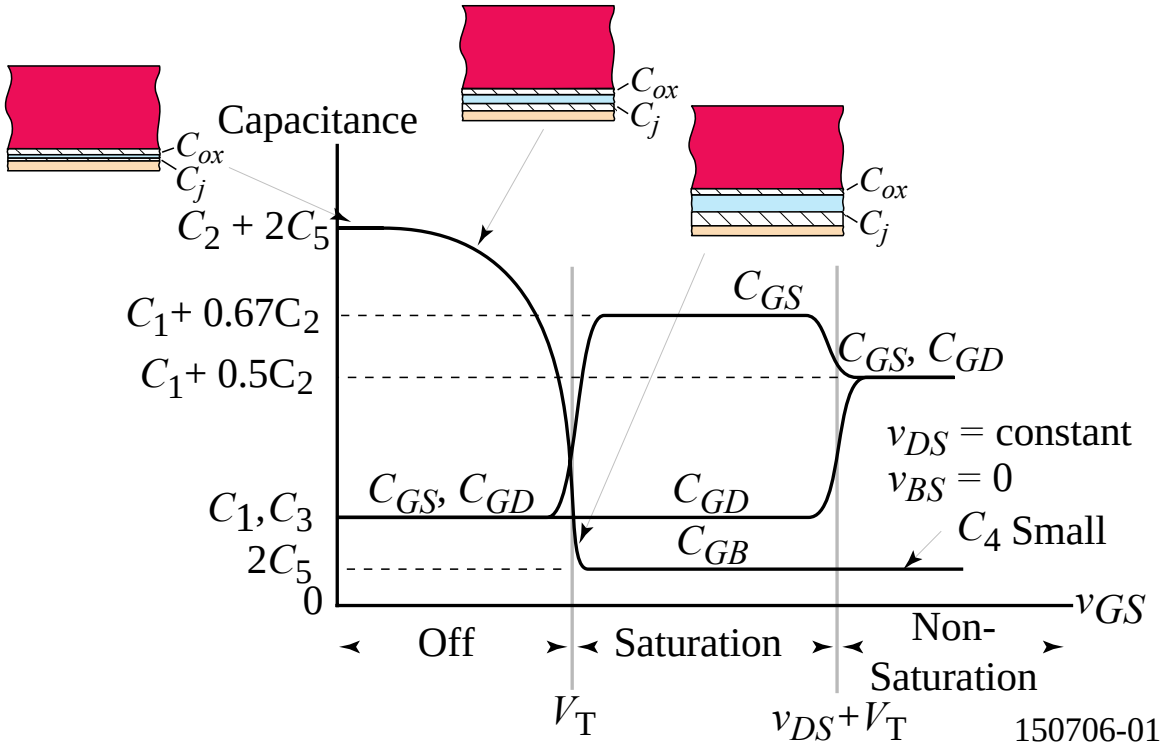
Illustration of C_{GD}, C_{GS} and C_{GB}

Comments on the variation of C_{BG} in the cutoff region:

$$C_{BG} = \frac{1}{\frac{1}{C_2} + \frac{1}{C_4}} + 2C_5$$

1.) For $v_{GS} \approx 0$, $C_{GB} \approx C_2 + 2C_5$ (C_4 is large because of the thin inversion layer in weak inversion where V_{GS} is slightly less than V_T))

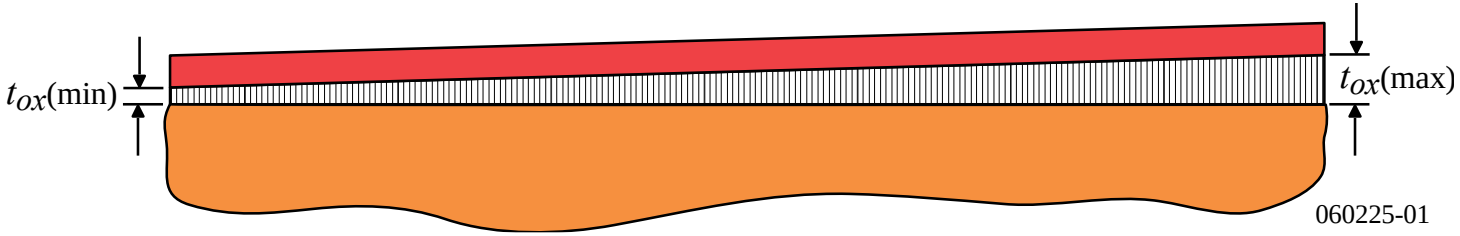
2.) For $0 < v_{GS} \leq V_T$, $C_{GB} \approx 2C_5$ (C_4 is small because of the thicker inversion layer in strong inversion)



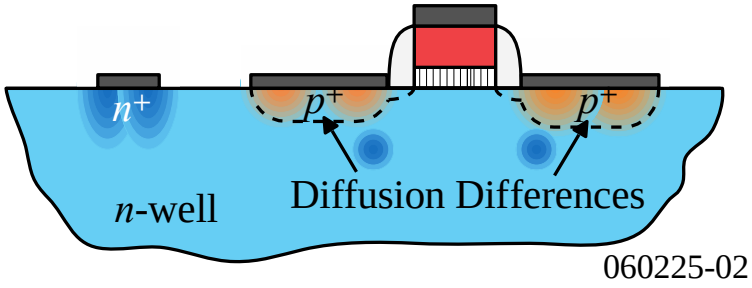
DEPENDENCE OF THE LARGE SIGNAL MODEL ON PROCESS

How Does Technology Vary?

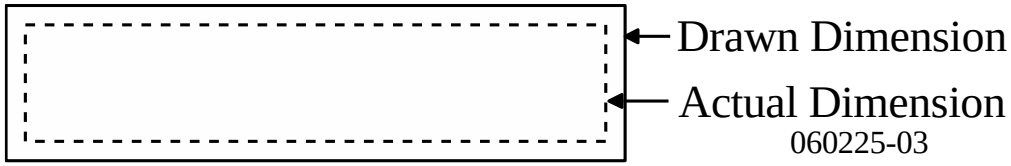
1.) Thickness variations in layers (dielectrics and metal)



2.) Doping variations



3.) Process biases – differences between the drawn and actual dimensions due to process (etching, lateral diffusion, etc.)



Large Signal Model Dependence on Process Variations

1.) Threshold voltage

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

where

$$V_{T0} = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} \qquad \text{and} \qquad \gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

If $V_{BS} = 0$, then V_T is dependent on doping and oxide thickness because

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right) \qquad \text{and} \qquad C_{ox} \propto \frac{1}{t_{ox}}$$

(Recall that the threshold is also determined by the threshold implant during processing)

2.) Transconductance parameter

$$K' = \mu_o C_{ox} \propto \frac{1}{t_{ox}}$$

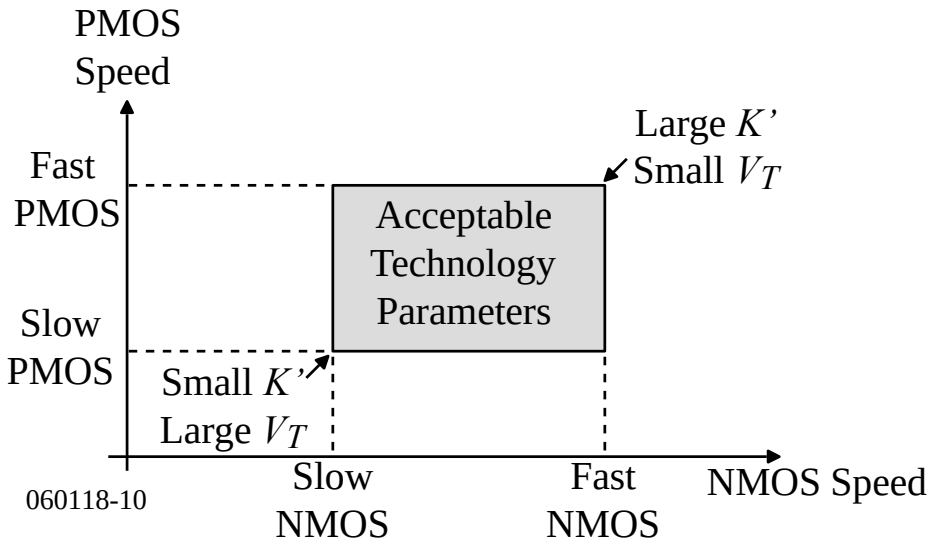
For short channel devices, the mobility is degraded as given by

$$\mu_{eff} = \frac{\mu_o}{1 + \theta(V_{GS} - V_T)} \qquad \text{and} \qquad \theta \approx \frac{2\text{x}10^{-9}\text{m/V}}{t_{ox}}$$

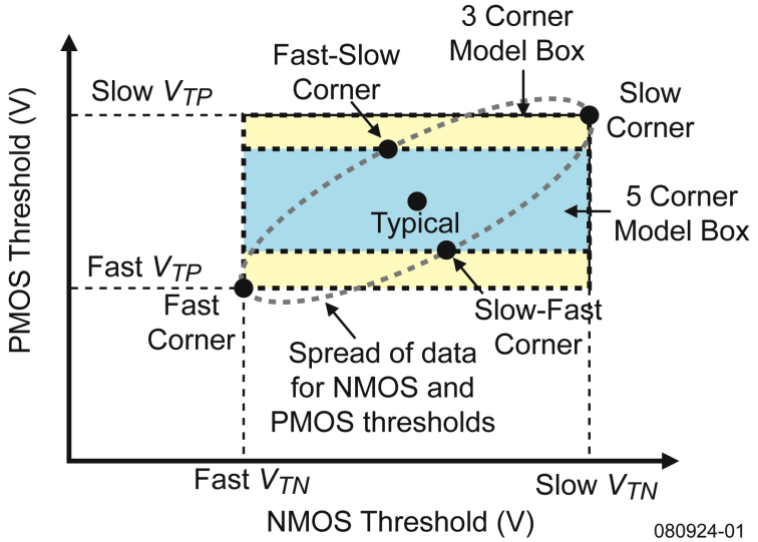
Process Variation "Corners"

For strong inversion operation, the primary influence is the oxide thickness, t_{ox}. We see that K' will tend to increase with decreasing oxide thickness whereas V_T tends to decrease.

If the "speed" of a transistor is increased by increasing K' and decreasing V_T, then the variation of technology can be expressed on a two-dimensional graph resulting in a rectangular area of "acceptable" process limitation.



Three corner versus five corner models



DEPENDENCE OF THE LARGE SIGNAL MODEL ON VOLTAGE

What is Voltage Variation?

Voltage variation is the influence of power supply voltage on the component.

(There is also power supply influence on the circuit called power supply rejection ratio, PSRR. We will deal with this in a later lecture.)

Power supply variation comes from:

1.) Influence of depletion region widths on components.

2.) Nonlinearity (e.g., velocity saturation)

3.) Breakdown voltage

Note: Because the large-signal model for the MOSFET includes all the influences of voltage on the transistor, we will focus on passive components except for breakdown.

Models for Voltage Dependence of a Component

1.) *i*th-order Voltage Coefficients

In general a variable $y = f(v)$ which is a function of voltage, v, can be expressed as a Taylor series,

$$y(v = V_0) \approx y(V_0) + a_1(v - V_0) + a_2(v - V_0)^2 + a_3(v - V_0)^3 + \cdots$$

where the coefficients, a_i, are defined as,

$$a_1 = \frac{df(v)}{dv}\bigg|_{v=V_0}, \; a_2 = \frac{1}{2}\frac{d^2f(v)}{dv^2}\bigg|_{v=V_0}, \; \ldots.$$

The coefficients, a_i, are called the first-order, second-order, …. voltage coefficients.

2.) Fractional Voltage Coefficient or Voltage Coefficient

Generally, only the first-order coefficients are of interest.

In the characterization of temperature dependence, it is common practice to use a term called *fractional voltage coefficient*, VC_F, which is defined as,

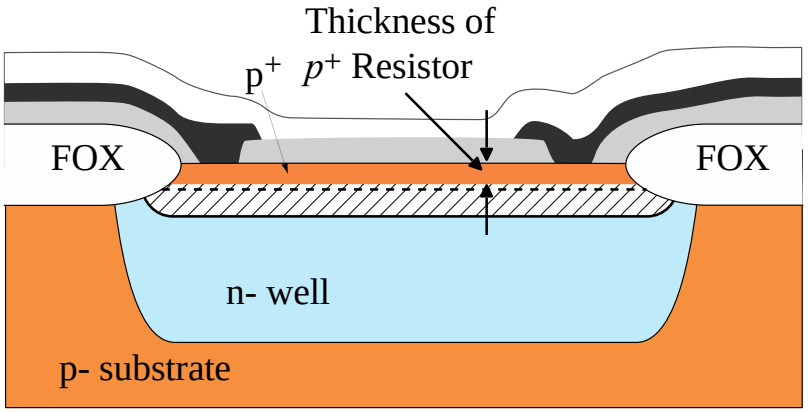
$$VC_F(v=V_0) = \frac{1}{f(v=V_0)}\frac{df(v)}{dv}\bigg|_{v=V_0} \text{ parts per million/V (ppm/V)}$$

or more simply,

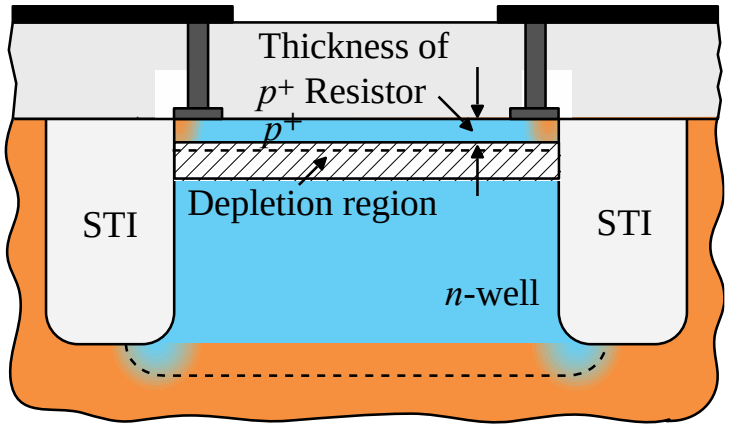
$$VC_F = \frac{1}{f(v)}\frac{df(v)}{dv} \text{ parts per million/V (ppm/V)}$$

Influence of Voltage on a Diffused Resistor – Depletion Region

Influence of the depletion region on the p^+ resistor:



060305-01 Older LOCOS Technology



As the voltage at the terminals of the resistor become smaller than the *n*-well potential, the depletion region will widen causing the thickness of the resistor to decrease.

$$R = \frac{\rho L}{tW} \propto \sqrt{V_R}$$

where V_R is the reverse bias voltage from the resistor to the well.

This effect is worse for well resistors because the doping concentration of the resistor is smaller.

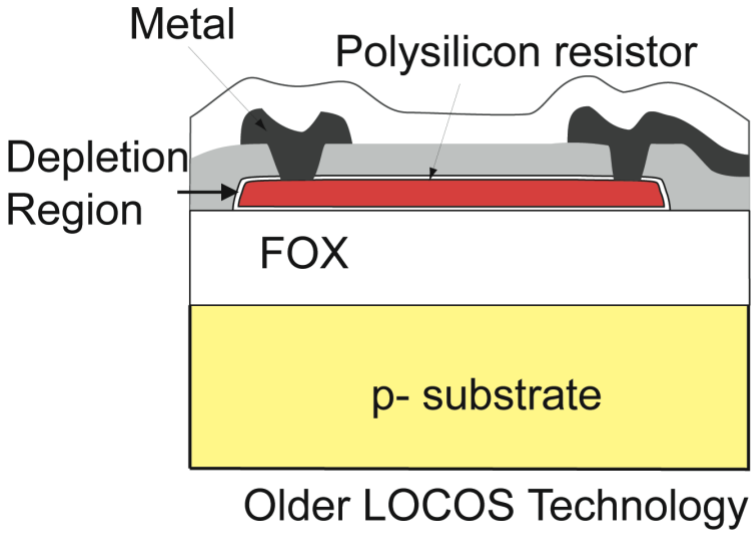
Voltage coefficient for diffused resistors ≈ 200-800 ppm/V

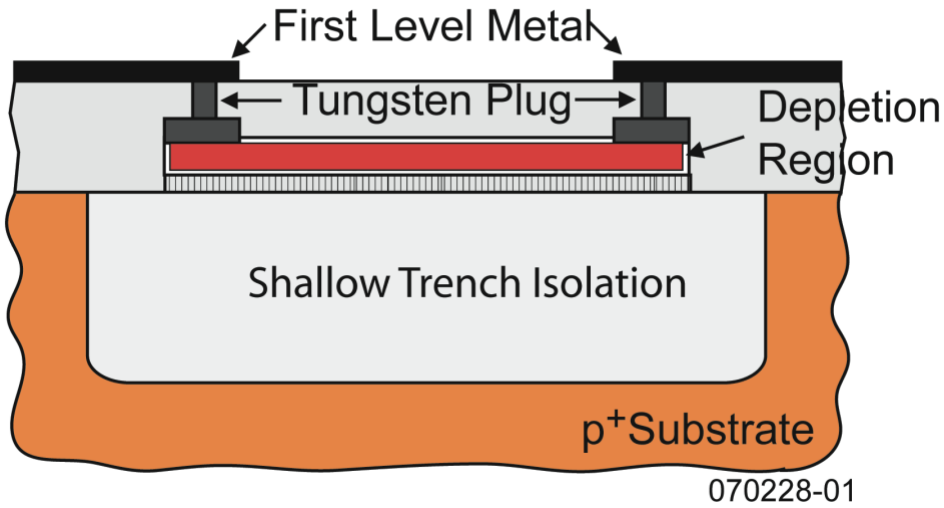
Voltage coefficient for well resistors ≈ 8000 ppm/V

Voltage Coefficient of Polysilicon Resistors

Why should polysilicon resistors be sensitive to voltage?

There is a small depletion region between the polysilicon and its surrounding material that has a very small dependence on the voltage between the polysilicon and the surrounding material.



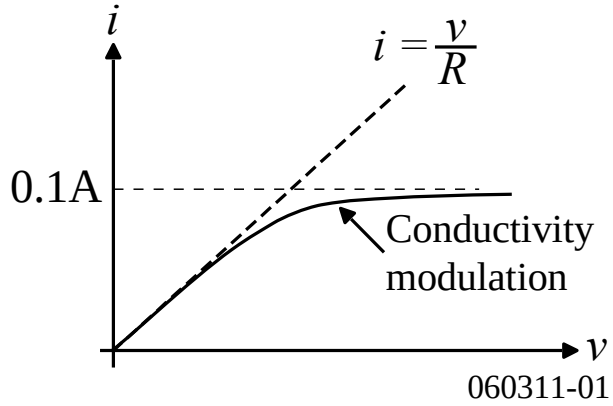


Voltage Nonlinearity and Breakdown Voltage

Conductivity modulation:

As the current in a resistor increases, the conductivity becomes modulated and the resistance increases.

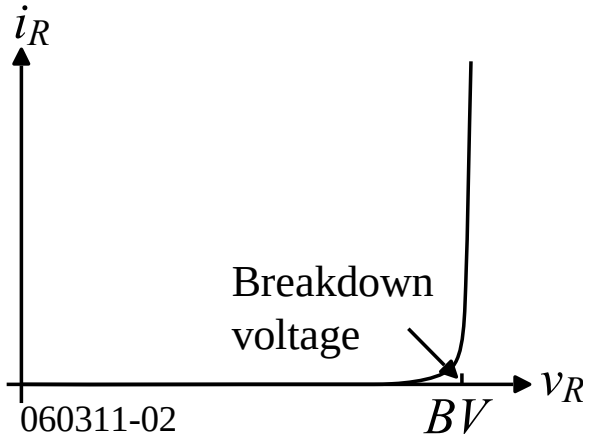
Example of a *n*-well resistor:



As the reverse bias voltage across a *pn* junction becomes large, at some point, called the breakdown voltage, the current will rapidly increase. Both transistors, diodes and depletion capacitors experience this breakdown.

Model for current multiplication factor:

$$i_R = M \cdot I_R \text{ where } \quad M = \frac{1}{1 - \left(\frac{v_R}{BV}\right)^n}$$



DEPENDENCE OF THE LARGE SIGNAL MODEL ON TEMPERATURE

Temperature Dependence of the MOSFET

Transconductance parameter:

$$K'(T) = K'(T_0)\,(T/T_0)^{-1.5}$$ (Exponent becomes +1.5 below 77°K)

Threshold Voltage:

$$V_T(T) = V_T(T_0) + \alpha(T-T_0) + \cdots$$

Typically α_{NMOS} = -2mV/°C to –3mV/°C from 200°K to 400°K (PMOS has a + sign)

Example

Find the value of I_D for a NMOS transistor at 27°C and 100°C if V_{GS} = 2V and W/L = 5µm/1µm if $K'(T_0)$ = 110µA/V^2 and $V_T(T_0)$ = 0.7V and T_0 = 27°C and α_{NMOS} = -2mV/°C.

Solution

At room temperature, the value of drain current is,

$$I_D(27°C) = \frac{110\mu A/V^2 \cdot 5\mu m}{2 \cdot 1\mu m}(2-0.7)^2 = 465\mu A$$

At T = 100°C (373°K), $K'(100°C)=K'(27°C)\,(373/300)^{-1.5}=110\mu A/V^2 \cdot 0.72=79.3\mu A/V^2$

and $V_T(100°C) = 0.7 – (.002)(73°C) = 0.554V$

$$\therefore \quad I_D(100°C) = \frac{79.3\mu A/V^2 \cdot 5\mu m}{2 \cdot 1\mu m}(2-0.554)^2 = 415\mu A$$ (Repeat with V_{GS} = 2.0855V)

Zero Temperature Coefficient (ZTC) Point for MOSFETs

For a given value of gate-source voltage, the drain current of the MOSFET will be independent of temperature. Consider the following circuit:

Assume that the transistor is saturated and that:

$$\mu = \mu_o\left(\frac{T}{T_o}\right)^{-1.5} \quad \text{and} \quad V_T(T) = V_T(T_o) + \alpha(T-T_o)$$

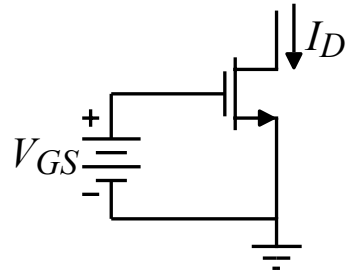


Fig. 4.5-12

$$\therefore \quad I_D(T) = \frac{\mu_o C_{ox} W}{2L}\left(\frac{T}{T_o}\right)^{-1.5}[V_{GS} - V_{T0} - \alpha(T-T_o)]^2$$

$$\frac{dI_D}{dT} = \frac{-3\mu_o C_{ox} W}{4LT_o}\left(\frac{T}{T_o}\right)^{-2.5}[V_{GS}-V_{T0}-\alpha(T-T_o)]^2 - \alpha\frac{\mu_o C_{ox} W}{L}\left(\frac{T}{T_o}\right)^{-1.5}[V_{GS}-V_{T0}-\alpha(T-T_o)] = 0$$

$$\therefore \quad V_{GS} - V_{T0} - \alpha(T-T_o) = \frac{-4T\alpha}{3} \qquad \Rightarrow \qquad \boxed{V_{GS}(\text{ZTC}) = V_{T0} - \alpha T_o - \frac{\alpha T}{3}}$$

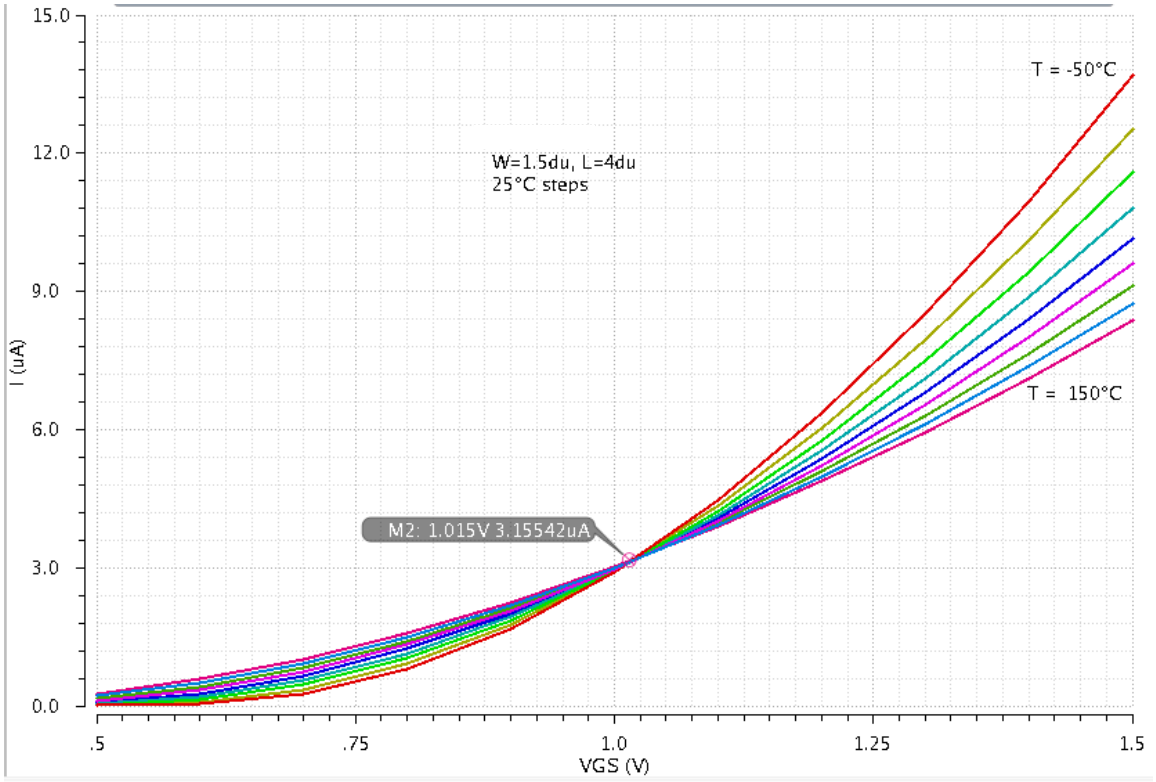
Let K' = 20μA/V^2, W/L = 0.375, α = -0.0016V/°C and V_{T0} = 0.46V.

At T=27°C(300°K), V_{GS}(ZTC)=0.46-(-0.0016)(300°K)-(0.333)(-0.0016)(300°K)=1.10V

At T = 27°C (300°K), I_D = (20μA/V^2)(1.5/4)(1.10-0.46)^2 = 3.07μA

Experimental Verification of the ZTC Point

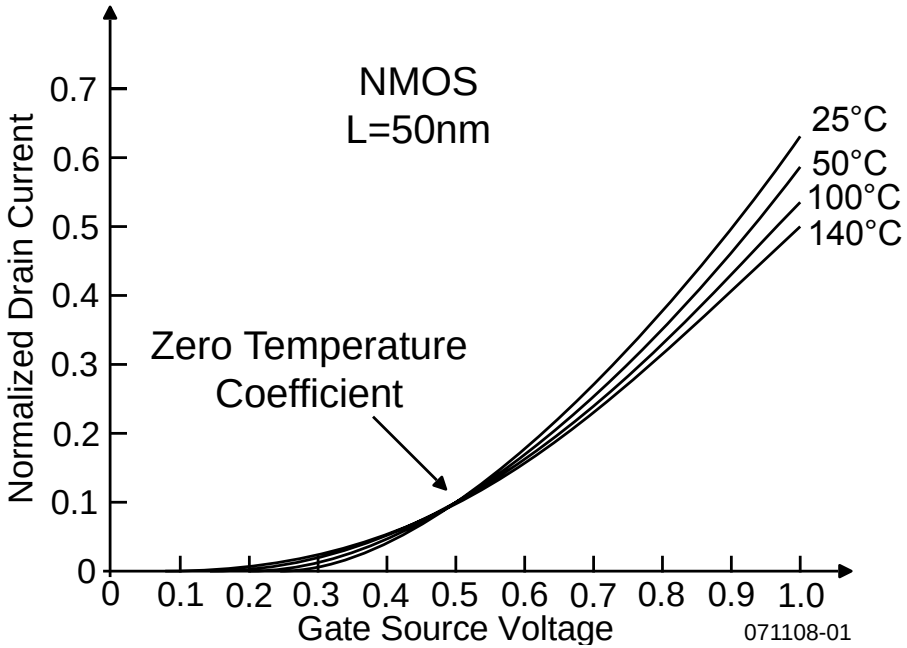
The plot below is the simulation results for an n-channel MOSFET with W = 1.5µm and L = 4µm.

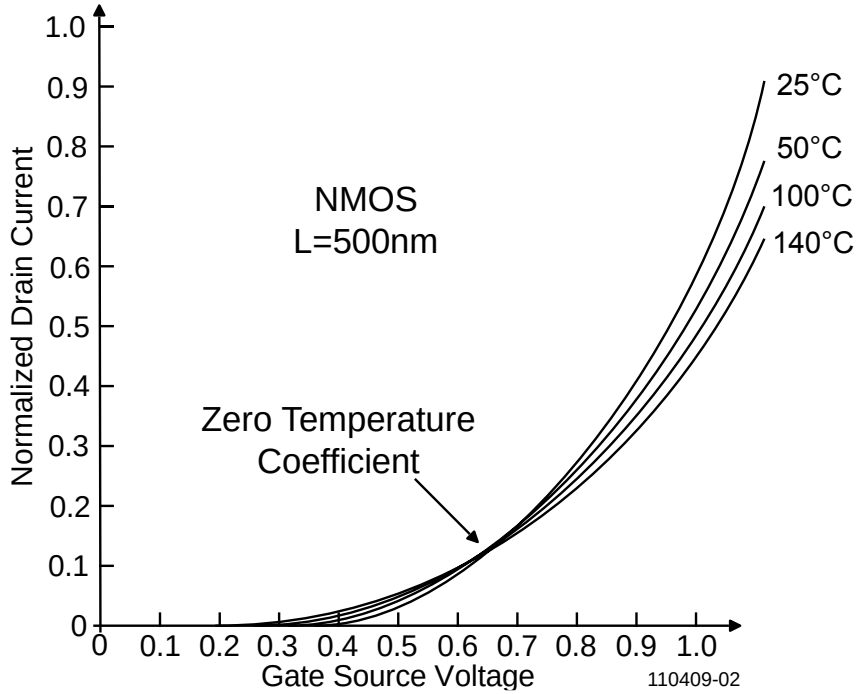


A similar result holds for the p-channel MOSFET.

ZTC Point for UDSM Technology

50 nm CMOS:





Note that the ZTC point can be close to V_{DD}.

PMOS will have similar characteristics.

Bulk-Drain (Bulk-Source) Leakage Currents

Cross-section of a NMOS in a p-well:

$V_{GS}>V_T$:

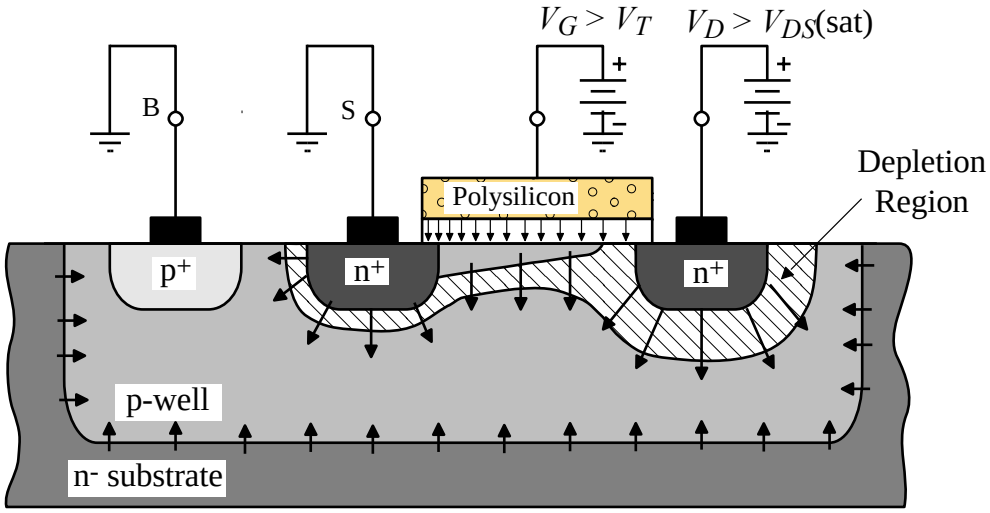


Fig.3.6-5

$V_{GS}<V_T$:

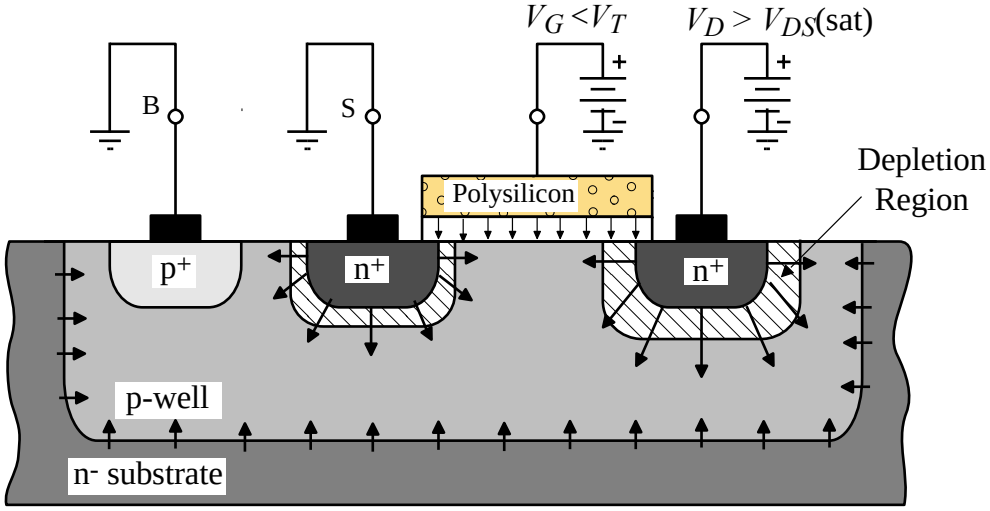


Fig.3.6-6

Temperature Modeling of the PN Junction

PN Junctions (Reverse-biased only):

$$-i_D \cong I_s = qA\left[\frac{Dppno}{L_p} + \frac{Dnnpo}{L_n}\right] \cong \frac{qAD}{L}\frac{n_i^2}{N} = KT^3 \exp\left(\frac{-V_{Go}}{V_t}\right)$$

Differentiating with respect to temperature gives,

$$\frac{dI_s}{dT} = \frac{3KT^3}{T}\exp\left(\frac{-V_{Go}}{V_t}\right) + \frac{qKT^3V_{Go}}{KT^2}\exp\left(\frac{-V_{Go}}{V_t}\right) = \frac{3I_s}{T} + \frac{I_s}{T}\frac{V_{Go}}{V_t}$$

$$TC_F = \frac{dI_S}{I_S dT} = \frac{3}{T} + \frac{1}{T}\frac{V_{Go}}{V_t}$$

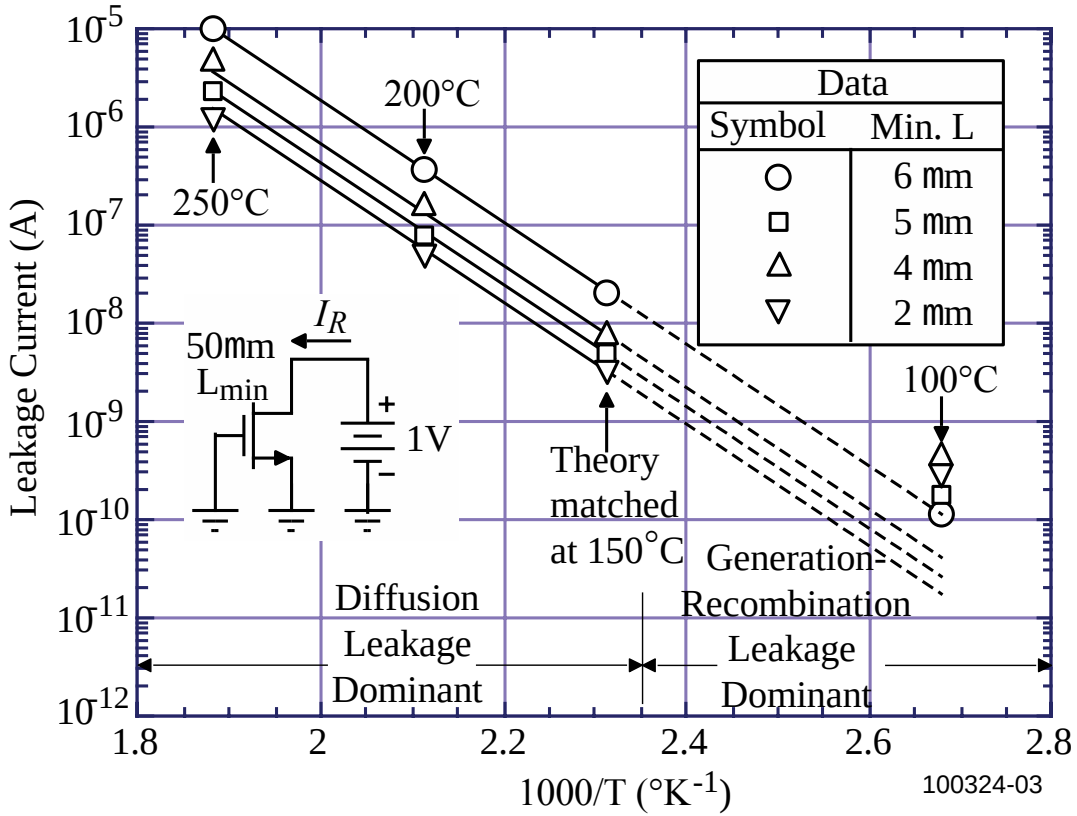
Example

Assume that the temperature is 300°K (room temperature) and calculate the reverse diode current change and the TC_F for a 5°K increase.

Solution

The TC_F can be calculated from the above expression as TC_F = 0.01 + 0.155 = 0.165. Since the TC_F is change per degree, the reverse current will increase by a factor of 1.165 for every degree K (or °C) change in temperature. Multiplying by 1.165 five times gives an increase of approximately 2. Thus, the reverse saturation current approximately doubles for every 5°C temperature increase. (Experimental is closer to 8°C.)

Experimental Verification of the PN Junction Temperature Dependence



Theory:

$$I_s(T) \propto T^3 \exp\left(\frac{V_G(T)}{kT}\right)$$

Temperature Modeling of the PN Junction – Continued

PN Junctions (Forward biased – v_D constant):

$$i_D \cong I_s \exp\left(\frac{v_D}{V_t}\right)$$

Differentiating this expression with respect to temperature and assuming that the diode voltage is a constant ($v_D = V_D$) gives

$$\frac{di_D}{dT} = \frac{i_D}{I_s}\frac{dI_s}{dT} - \frac{1}{T}\frac{V_D}{V_t} i_D$$

The fractional temperature coefficient for i_D is

$$\frac{1}{i_D}\frac{di_D}{dT} = \frac{1}{I_s}\frac{dI_s}{dT} - \frac{V_D}{TV_t} = \frac{3}{T} + \left[\frac{V_{Go} - V_D}{TV_t}\right]$$

If V_D is assumed to be 0.6 volts, then the fractional temperature coefficient is equal to 0.01+(0.155-0.077) = 0.0879. The forward diode current will approx. double for a 10°C.

PN Junctions (Forward biased – i_D constant):

$$V_D = V_t \ln(I_D/I_s)$$

Differentiating with respect to temperature gives

$$\frac{dv_D}{dT} = \frac{v_D}{T} - V_t\left(\frac{1}{I_s}\frac{dI_s}{dT}\right) = \frac{v_D}{T} - \frac{3V_t}{T} - \frac{V_{Go}}{T} = -\left[\frac{V_{Go}-v_D}{T}\right] - \frac{3V_t}{T} \approx -2.3 \text{ mV/°C if } v_D = V_D = 0.6\text{V}$$

Resistor Dependence on Temperature

Diffused Resistors:

The temperature dependence of resistors depends mostly on the doping level of diffused and implanted resistors. As the doping level or sheet resistance increases from 100 Ω/□ to 400 Ω/□, the temperature coefficient varies from about +1000 ppm/°C to +4000 ppm/°C. Diffused and implanted resistors have good thermal conduction to the substrate or well.

Polysilicon Resistors:

Typically has a sheet resistance of 20 Ω/□ to 80 Ω/□ and has poor thermal conduction because it is electrically isolated by oxide layers.

Metal:

Metal is often used for resistors and has a positive temperature coefficient.

Temperature Coefficients of Resistors:

n-well = 4000 ppm/°C

Polysilicon = 500-2000 ppm/°C

Metal = +3800 ppm/°C (aluminum)

Diffusion = +1500 ppm/°C

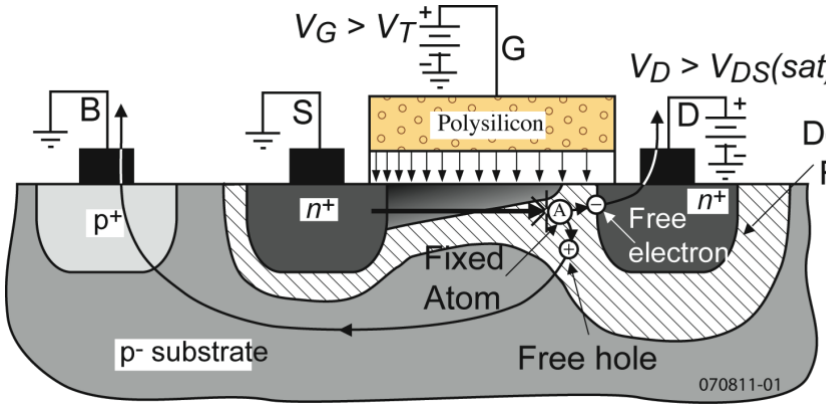
Ion implanted = +400 ppm/°C

MOSFET RELIABILITY

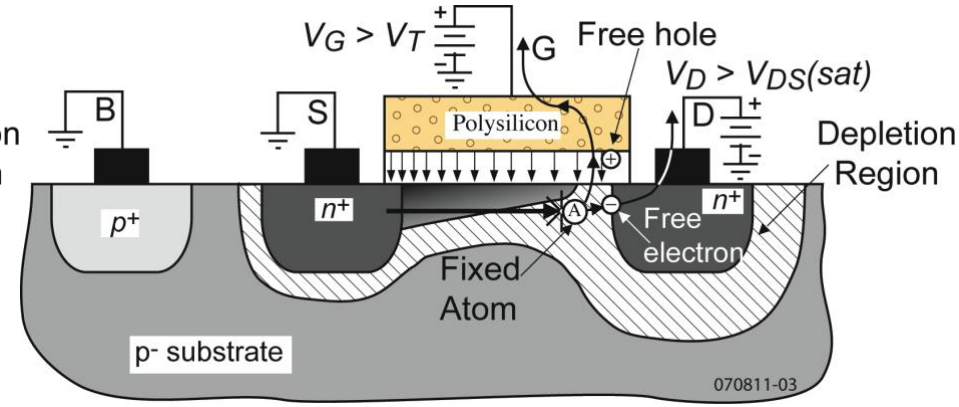
Hot Carrier Injection

Hot carriers depend on channel length. Longer channel lengths minimize hot carrier effects. The worst-case hot carrier degradation occurs in NMOS devices when the gate voltage is between V_T and $0.5V_{DS}$ and V_{DS} is large.

Substrate current-



Gate current-



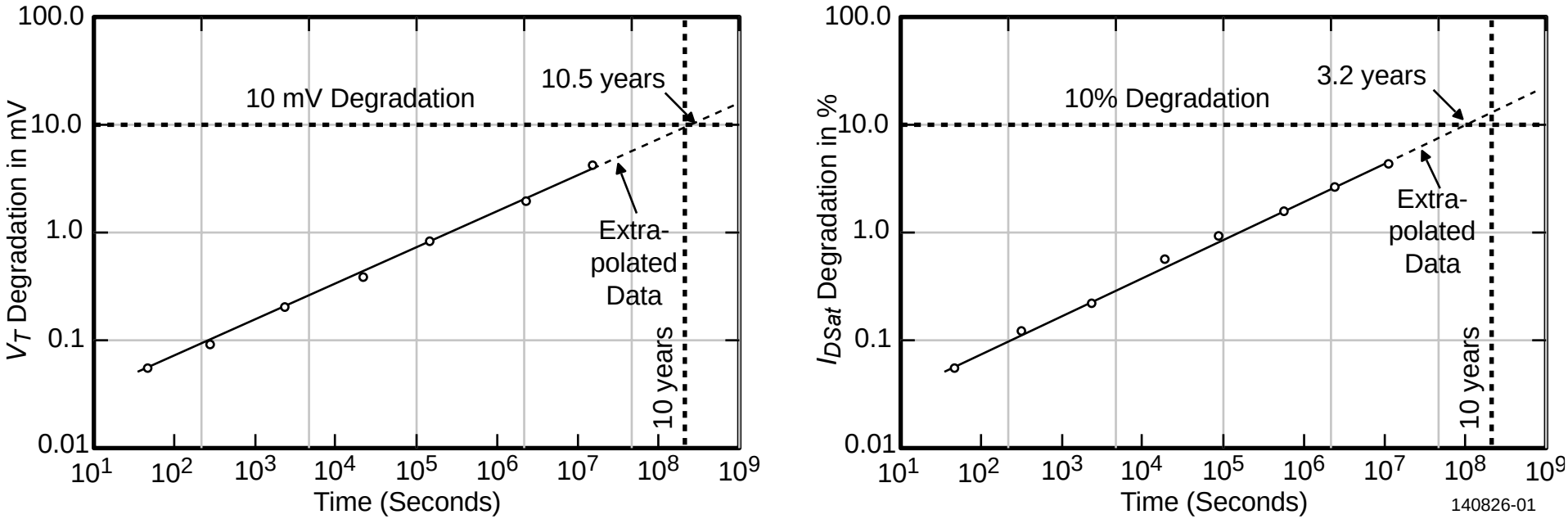
Target specifications:

1.) No more than 100mV change in V_T within a year of stress.

2.) No more than a 10% change in I_{Dsat} or R_{dson} within a year of stress.

Substrate current is a measure of hot carrier injection.

Typical NMOS Reliability Data

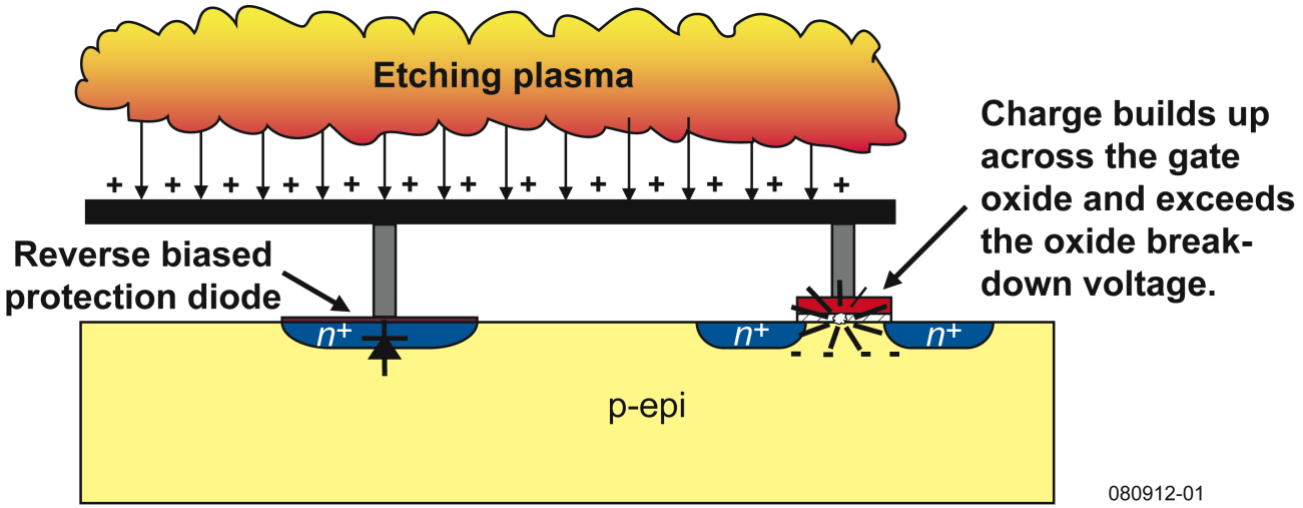


Note the extrapolation of short time data out to a year or more.

Also:

- NBTI (negative bias temperature instability) – PMOS with large gate-source voltage
- GOI (gate oxide integrity) – reliability of dielectrics

Antenna Effect



- The antenna effect is the situation during processing the charged plasmas that are used put charge on the metal and if this metal is connected to the gate of a MOSFET and the metal area is large enough, the oxide can breakdown.
- Oxide thicknesses less than 100Å are more susceptible to the antenna effect (plasma induced discharge).
- A reverse biased diode connected from the metal to the semiconductor can be used to leak this charge during processing (at high temperatures) and protect the gate oxides.
- Design rules exists to avoid having metal with large areas connected to gates (metal jumpers).

SUMMARY

- The large signal capacitance model includes depletion and parallel plate capacitors
- The depletion capacitors C_{BD} and C_{BS} vary with their reverse bias voltage
- The capacitors C_{GD}, C_{GS}, and C_{GB} have different values for the regions of cutoff, active and saturated
- The large signal model varies with process primarily through μ_o and t_{ox}
- Voltage dependence of resistors and capacitors is primarily due to the influence of depletion regions
- The temperature dependent large signal model of the MOSFET yields a gate-source voltage where the derivative of drain current with respect to temperature is zero
- Other MOSFET temperature dependence comes from the leakage currents across reverse biased *pn* junctions
- MOSFET reliability concerns degradation in performance over a specified lifetime