LECTURE 11 – LINEAR CIRCUIT MODELS

LECTURE ORGANIZATION

Outline

- Frequency independent small signal transistor models
- Frequency dependent small signal transistor model
- Noise models
- Passive component models
- Interconnects
- Substrate interference
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 86-90, 96-98 and new material

FREQUENCY INDEPENDENT SMALL SIGNAL TRANSISTOR MODELS

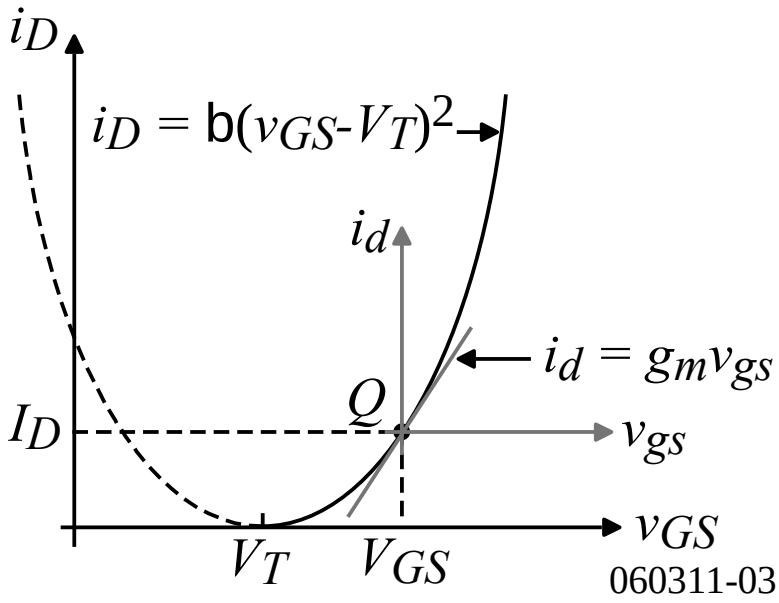
What is a Small Signal Model?

The small signal model is a linear approximation of a nonlinear model.

Mathematically:

$$i_D = \frac{\beta}{2}(v_{GS} - V_T)^2 \xrightarrow{\text{Large Signal to Small Signal}} i_d = g_m v_{gs}$$

Graphically:



The large signal curve at point Q has been approximated with a small signal model going through the point Q and having a slope of g_m.

Why Small Signal Models?

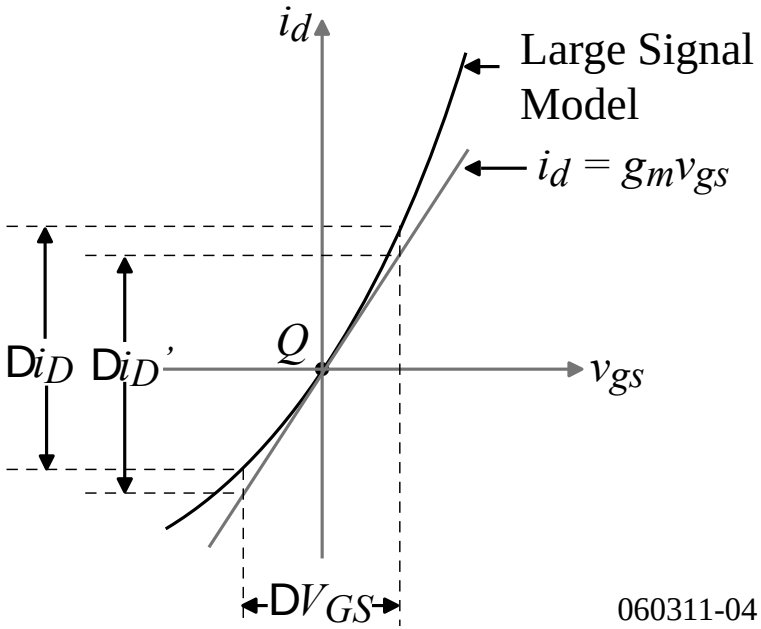
The small signal model is a linear approximation to the large signal behavior.

1.) The transistor is biased at given DC operating point (Point *Q* above)

2.) Voltage changes are made about the operating point.

3.) Current changes result from the voltage changes.

If the designer is interested in only the current changes and not the DC value, then the small signal model is a fast and simple way to find the current changes given the voltage changes.



How Good is the Small Signal Model?

It depends on how large are the changes and how nonlinear is the large signal model.

- The parameters of the small signal model will depend on the values of the large signal model.
- The model is a tradeoff in complexity versus accuracy (we will choose simplicity and give up accuracy).
- What does a simulator do? Exactly the same thing when it makes an ac analysis (i.e. frequency response)
- Regardless of the approximate nature of the small signal model, it is the primary model used to predict the signal performance of an analog circuit.

Be alert for situations where the small signal model will be in error (i.e. slide 25-27).

Small-Signal Model for the Saturation Region

The small-signal model is a linearization of the large signal model about a quiescent or operating point.

Consider the large-signal MOSFET in the saturation region ($v_{DS} \geq v_{GS} - V_T$) :

$$i_D = \frac{W\mu_o C_{ox}}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

The small-signal model is the linear dependence of i_d on v_{gs}, v_{bs}, and v_{ds}. Written as,

$$i_d \approx g_m v_{gs} + g_{mbs} v_{bs} + g_{ds} v_{ds}$$

where

$$g_m \equiv \frac{di_D}{dv_{GS}}\Big|_Q = \beta(V_{GS}-V_T) = \sqrt{2\beta I_D}$$

$$g_{ds} \equiv \frac{di_D}{dv_{DS}}\Big|_Q = \frac{\lambda I_D}{1 + \lambda V_{DS}} \approx \lambda I_D$$

and

$$g_{mbs} \equiv \frac{di_D}{dv_{BS}}\Big|_Q = \left(\frac{di_D}{dv_{GS}}\right)\left(\frac{dv_{GS}}{dv_{BS}}\right)\Big|_Q = \left(-\frac{di_D}{dV_T}\right)\left(\frac{dV_T}{dv_{BS}}\right)\Big|_Q = \frac{g_m\gamma}{2\sqrt{2|\phi_F| - V_{BS}}} = \eta g_m$$

Small-Signal Model – Continued

Complete schematic model:

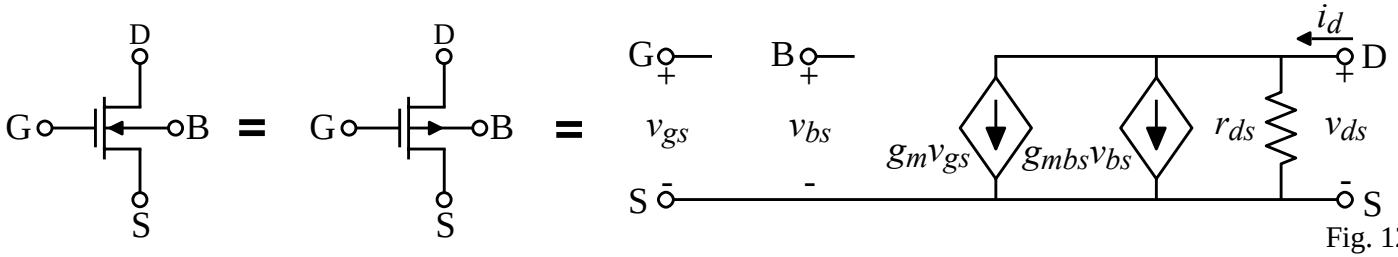


Fig. 120-01

where

$$g_m \equiv \left.\frac{di_D}{dv_{GS}}\right|_Q = \beta(V_{GS}-V_T) = \sqrt{2\beta I_D} \qquad g_{ds} \equiv \left.\frac{di_D}{dv_{DS}}\right|_Q = \frac{\lambda i_D}{1+\lambda v_{DS}} \approx \lambda i_D$$

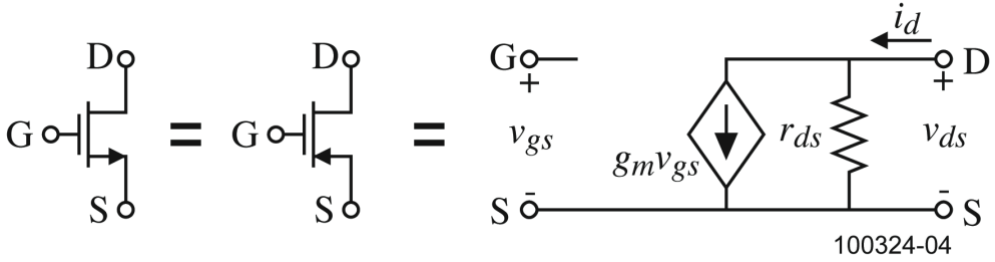
and

$$g_{mbs} = \left.\frac{\imath_D}{v_{BS}}\right|_Q = \left(\frac{i_D}{v_{GS}}\right)\left(\frac{v_{GS}}{v_{BS}}\right)\Bigg|_Q = \left(-\frac{i_D}{v_T}\right)\left(\frac{v_T}{v_{BS}}\right)\Bigg|_Q = \frac{g_m\gamma}{2\sqrt{2|\phi_F| - V_{BS}}} = \eta g_m$$

Simplified schematic model:

A very useful assumption:

$g_m \approx 10 g_{mbs} \approx 100 g_{ds}$



Small-Signal Model for other Regions

Active region:

$$g_m = \frac{i_D}{v_{GS}}\Big|_Q = \frac{K'WV_{DS}}{L}(1+\lambda V_{DS}) \approx \left(\frac{K'W}{L}\right)V_{DS} \quad g_{mbs} = \frac{i_D}{v_{BS}}\Big|_Q = \frac{K'W\gamma V_{DS}}{2L\sqrt{2\phi_F - V_{BS}}}$$

$$g_{ds} = \frac{i_D}{v_{DS}}\Big|_Q = \frac{K'W}{L}(V_{GS} - V_T - V_{DS})(1+\lambda V_{DS}) + \frac{I_D\lambda}{1+\lambda V_{DS}} \approx \frac{K'W}{L}(V_{GS} - V_T - V_{DS})$$

Note:

While the small-signal model analysis is independent of the amplitude of the signal, the small-signal parameters are not.

Weak inversion region:

If $v_{DS} > 0$, then

$$i_D = I_t \frac{W}{L}\exp\left(\frac{v_{GS}-V_T}{nV_t}\right)\left(1 + \frac{v_{DS}}{V_A}\right)$$

Small-signal model:

$$g_m = \frac{di_D}{dv_{GS}}\Big|_Q = I_t \frac{W}{L}\frac{I_t}{nV_t}\exp\left(\frac{v_{GS}-V_T}{nV_t}\right)\left(1 + \frac{v_{DS}}{V_A}\right) = \frac{I_D}{nV_t} = \frac{qI_D}{nkT} = \frac{I_D}{V_t}\frac{C_{ox}}{C_{ox}+C_{js}}$$

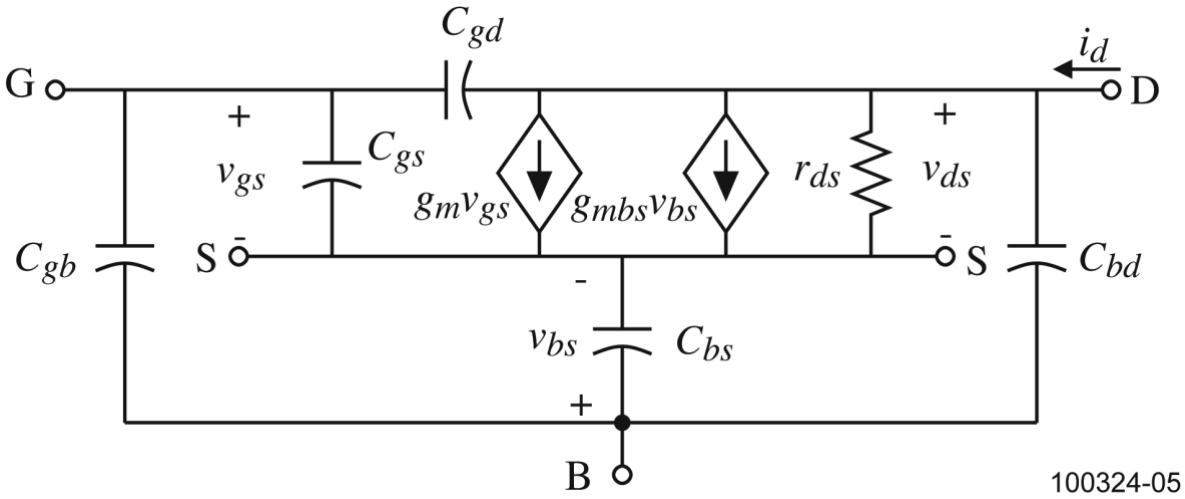
$$g_{ds} = \frac{di_D}{dv_{DS}}\Big|_Q \approx \frac{I_D}{V_A}$$

FREQUENCY DEPENDENT SMALL SIGNAL MODEL

Small-Signal Frequency Dependent Model

The depletion capacitors are found by evaluating the large signal capacitors at the DC operating point.

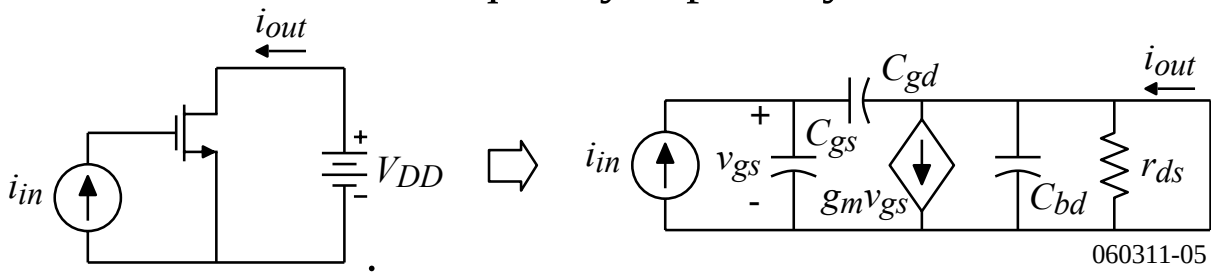
The charge storage capacitors are constant for a specific region of operation.



Gain-bandwidth of the MOSFET (f_T)

The short-circuit current gain is measure of the frequency capability of the MOSFET.

Small signal model:



Small signal analysis gives,

$$i_{out} = g_m v_{gs} - sC_{gd}v_{gs} \quad \text{and} \quad v_{gs} = \frac{i_{in}}{s(C_{gs} + C_{gd})}$$

Therefore,

$$\frac{i_{out}}{i_{in}} = \frac{g_m - sC_{gd}}{s(C_{gs} + C_{gd})} \approx \frac{g_m}{s(C_{gs} + C_{gd})}$$

Assume $V_{SB} = 0$ and the MOSFET is in saturation,

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs} + C_{gd}} \approx \frac{1}{2\pi}\frac{g_m}{C_{gs}}$$

Recalling that

$$C_{gs} \approx \frac{2}{3} C_{ox}WL \quad \text{and} \quad g_m = \mu_o C_{ox}\frac{W}{L}(V_{GS} - V_T) \quad \rightarrow \quad f_T = \frac{3}{4\pi}\frac{\mu_o}{L^2}(V_{GS} - V_T)$$

For velocity saturation, $f_T \propto 1/L$.

NOISE MODELS

Derivation of the MOSFET Thermal Noise Model

In the active region, the channel resistance of the MOSFET is given from the simple large signal model as,

$$R_{channel} = \frac{1}{\frac{\partial i_D}{\partial v_{DS}}\Big|_Q} = \frac{1}{\frac{K'W}{L}(V_{GS} - V_T - V_{DS})} \approx \frac{1}{\frac{K'W}{L}(V_{GS} - V_T)} = \frac{1}{g_m(\text{sat})}$$

The current thermal noise spectral density of a MOSFET in the active region would be

$$i_n^2(\text{active}) = \frac{4kT}{R_{channel}} = 4kTg_m(\text{sat}) \quad (\text{A}^2/\text{Hz})$$

In the saturation region, approximate the channel resistance as 2/3 the value in the active region resulting in 2/3 the noise. Therefore in saturation we have the current thermal noise spectral density as,

$$i_n^2(\text{sat}) = \frac{2}{3} i_n^2(\text{active}) = \frac{8kTg_m(\text{sat})}{3} \quad (\text{A}^2/\text{Hz})$$

Translating this drain current noise to the gate voltage noise by dividing by g_m^2 gives

$$e_n^2 = \frac{8kT}{3g_m} \quad (\text{V}^2/\text{Hz})$$

The Influence of the Back Gate on Thermal Noise

The influence of the back gate on the thermal noise can be developed by replacing g_m of the previous expressions with $g_m + g_{mbs}$

Substituting R with $R_{channel}$(sat) gives the voltage and current noise spectral densities as,

$$e_n^2 = \frac{8kT}{3(g_m + g_{mbs})}\,(\mathrm{V^2/Hz}) = \frac{8kT}{3g_m(1+\eta)}\,(\mathrm{V^2/Hz})$$

or

$$i_n^2 = \frac{8kT(g_m + g_{mbs})}{3}\,(\mathrm{A^2/Hz}) = \frac{8kTg_m(1+\eta)}{3}\,(\mathrm{A^2/Hz})$$

where

$$\eta = \frac{g_{mbs}}{g_m}$$

1/*f* Noise Model

Another significant noise contribution to MOSFETs is a noise that is typically inversely proportional to frequency called the 1/*f* noise.

This 1/*f* noise spectral density is given as,

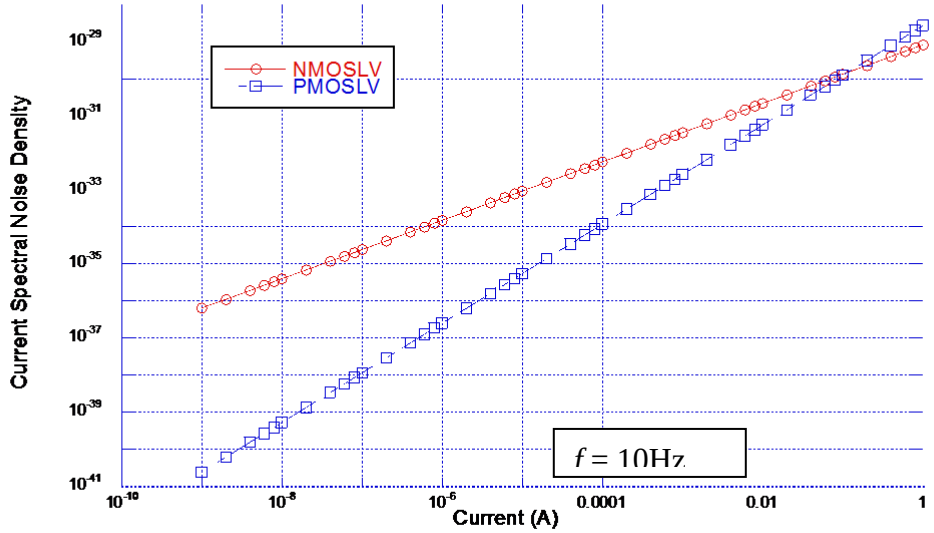
$$i_n^2 = \left[\frac{KF\, I_D^{AF}}{f^S C_{ox} L^2}\right] \qquad \text{or} \qquad e_n^2 = \frac{KF}{2f^S C_{ox} WL\, K'},$$

where

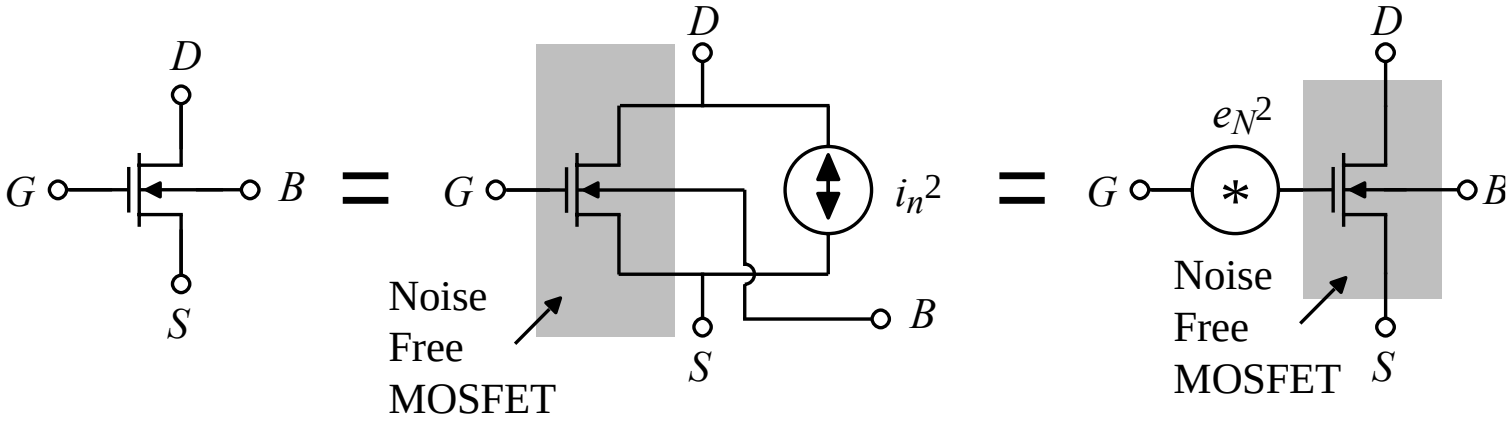
KF = Flicker noise coefficient

S = Slope factor of the 1/*f* noise

Although we do not have a good explanation for the reason why, the value of the 1/*f* noise for a PMOS is typically less than that for an NMOS for the same current and *W*/*L*.



MOS Device Noise at Low Frequencies



where

$$i_n^2 = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{KF\, I_D^{AF}}{f^S C_{ox} L^2} \right] \quad (\text{amperes}^2/\text{Hz})$$

$$\eta = \frac{g_{mbs}}{g_m}$$

k = Boltzmann's constant

KF = Flicker noise coefficient

S = Slope factor of the 1/f noise

AF = Current coefficient

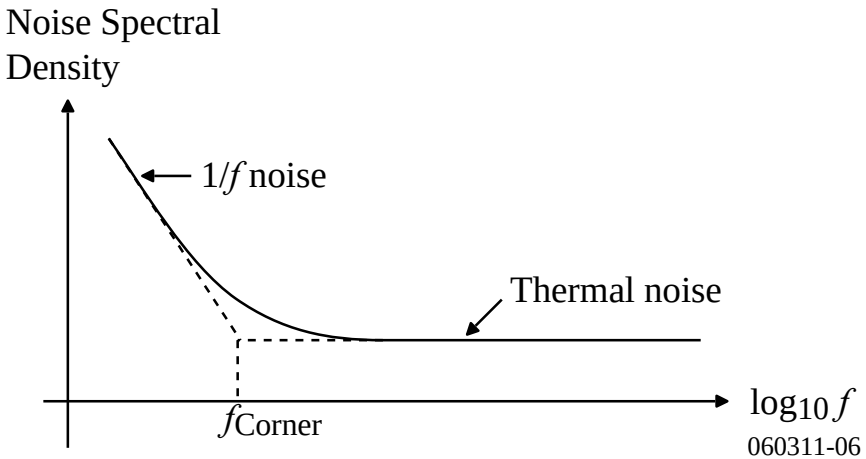
Reflecting the MOSFET Noise to the Gate

Dividing i_n^2 by g_m^2 gives the voltage noise spectral density as

$$e_n^2 = \frac{i_n^2}{g_m^2} = \left[\frac{8kT}{3g_m(1+\eta)} + \frac{KF}{2fC_{ox}WL\,K'} \right] \quad (\text{volts}^2/\text{Hz})$$

It will be convenient to use $B = \frac{KF}{2C_{ox}K'}$ to simplify the notation.

Frequency response of MOSFET noise:

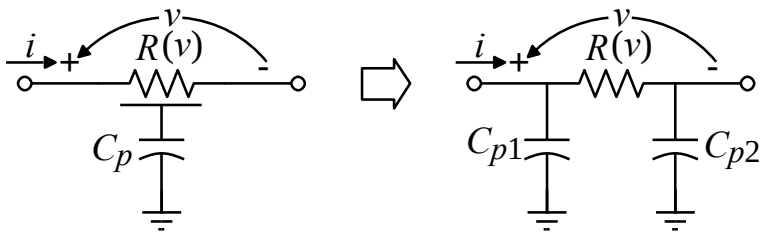


The $1/f$ corner frequency is:

$$\frac{8kT}{3g_m(1+\eta)} = \frac{KF}{2fC_{ox}WL\,K'} \quad \Rightarrow \quad f_{corner} \approx \frac{3g_mB}{8kTWL} \text{ if } g_{mbs} = 0$$

PASSIVE COMPONENT MODELS

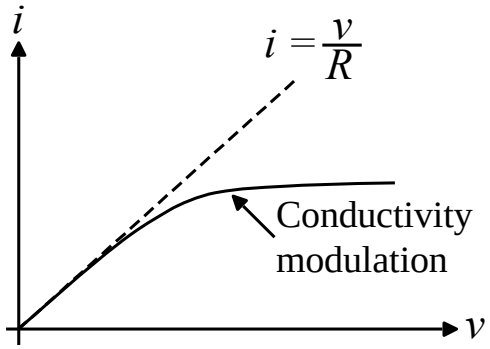
Resistor Models



Distributed Model Lumped Model

060315-01

1.) Large signal



060311-01

2.) Small signal

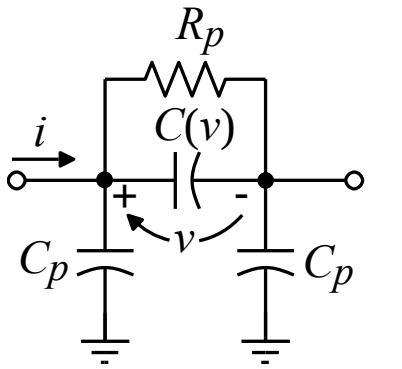
$$v = Ri$$

3.) Noise

$$e_n^2 = 4kTR \qquad \text{or} \qquad i_n^2 = 4kTG$$

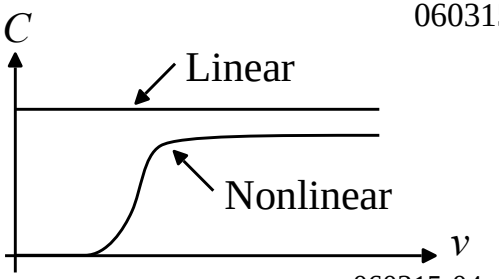
Capacitor Models

One of the parasitic capacitors is the top plate and the other is associated with the bottom plate.



060315-03

1.) Large signal



060315-04

2.) Small signal

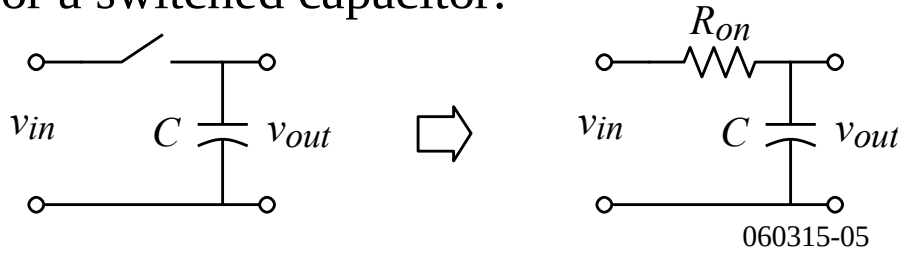
$$q = Cv \rightarrow \quad i = C(dv/dt)$$

3.) Do capacitors have noise? See next page.

Switched Capacitor Circuits - *kT/C* Noise

Capacitors and switches generate an inherent thermal noise given by *kT/C*. This noise is verified as follows.

An equivalent circuit for a switched capacitor:



The noise voltage spectral density of switched capacitor above is given as

$$e_{Ron}^2 = 4kTR_{on} \text{ Volts}^2/\text{Hz} = \frac{2kTR_{on}}{\pi} \text{ Volt}^2/\text{Rad./sec.}$$

The rms noise voltage is found by integrating this spectral density from 0 to ∞ to give

$$v_{Ron}^2 = \frac{2kTR_{on}}{\pi}\int_0^\infty \frac{\omega_1^2 d\omega}{\omega_1^2+\omega^2} = \frac{2kTR_{on}}{\pi}\left(\frac{\pi\omega_1}{2}\right) = \frac{kT}{C} \text{ Volts(rms)}^2$$

where $\omega_1 = 1/(R_{on}C)$. Note that the switch has an effective noise bandwidth of

$$f_{sw} = \frac{1}{4R_{on}C} \text{ Hz}$$

which is found by dividing the second relationship by the first.

INTERCONNECTS

Types of "Wires"

1.) Metal

Many layers are available in today's technologies:

- Lower level metals have more resistance (70 mΩ/sq.)
- Upper level metal has the less resistance because it is thicker (50 mΩ/sq.)

2.) Polysilicon

Better resistor than conductor (unpolysicided) (135Ω/sq.)

Silicided polysilicon has a lower resistance (5Ω/sq.)

3.) Diffusion

Reasonable for connections if silicided (5Ω/sq.)

Unsilicided (55Ω/sq.)

4.) Vias

Vias are vertical metal (tungsten plugs or aluminum)

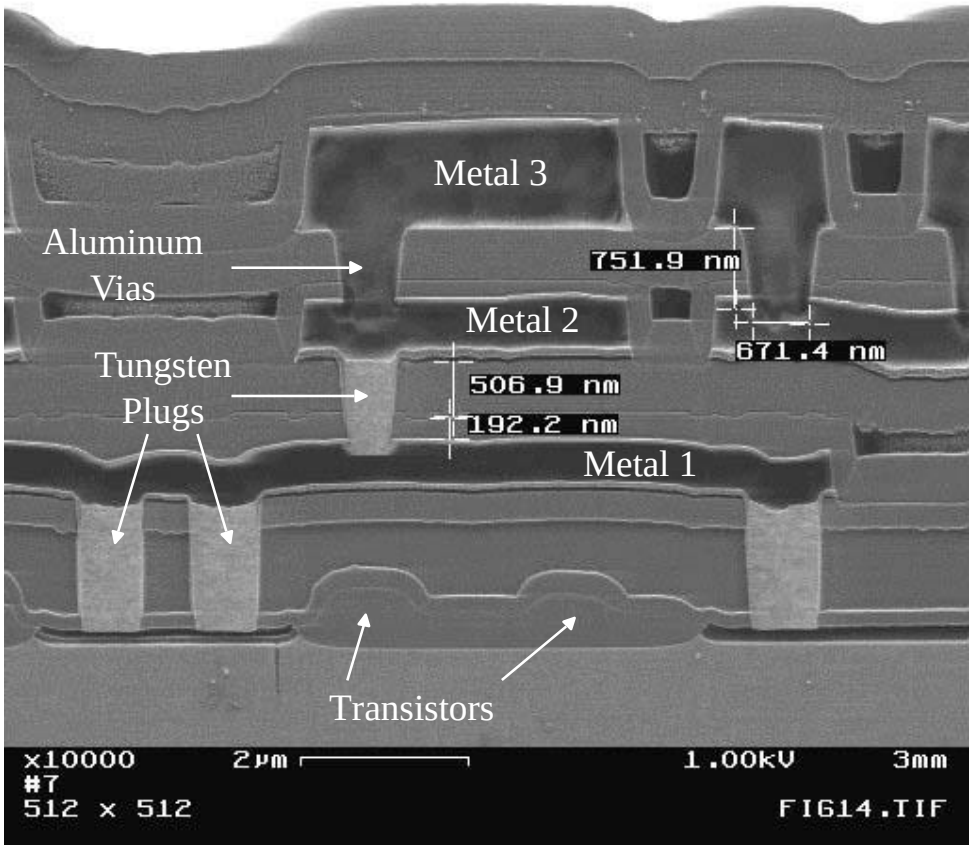
- Connect metal layer to metal layer (3.5Ω/via)
- Connect metal to silicon or polysilicon contact resistance (5Ω/contact)

Ohmic Contact Resistance

The metal to silicon contact generates resistance because of the presence of a potential barrier between the metal and the silicon.

Contact and Via Resistance:

Contact System	Contact Resistance ($\Omega/\mu m^2$)
Al-Cu-Si to 160Ω/sq. base	750
Al-Cu-Si to 5Ω/sq. emitter	40
Al-Cu/Ti-W/PtSi to 160Ω/sq. base	1250
Al-Cu/Al-Cu (Via)	5
Al-Cu/Ti-W/Al-Cu (Via)	5



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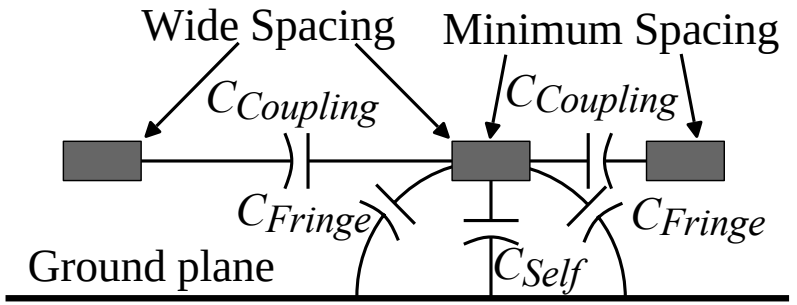
Capacitance of Wires

Self, fringing and coupling capacitances:



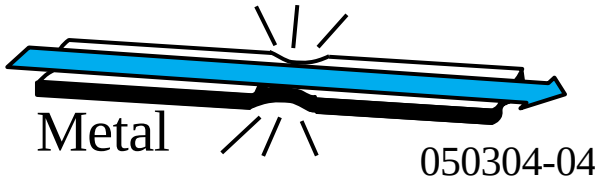
Capacitance	Typical Value	Units
Metal to diffusion, Self capacitance	33	aF/μm^2
Metal to diffusion, Fringe capacitance, minimum spacing	7	aF/μm
Metal to diffusion, Fringe capacitance, wide spacing	40	aF/μm
Metal to metal, Coupling capacitance, minimum spacing	85	aF/μm
Metal to substrate, Self capacitance	28	aF/μm^2
Metal to substrate, Fringe capacitance, minimum spacing	4	aF/μm
Metal to substrate, Fringe capacitance, wide spacing	39	aF/μm

Electromigration

Electromigration occurs if the current density is too large and the pressure of carrier collisions on the metal atoms causes a slow displacement of the metal.

Black's law:

$$\text{MTF} = \frac{1}{AJ^2} e^{(E_a/kT_j)}$$



Where

A = rate constant ($cm^4/A^2/hr$)

J = current density (A/cm^2)

E_a = activation energy in electron volts (0.5eV for Al and 0.7eV for Cu doped Al)

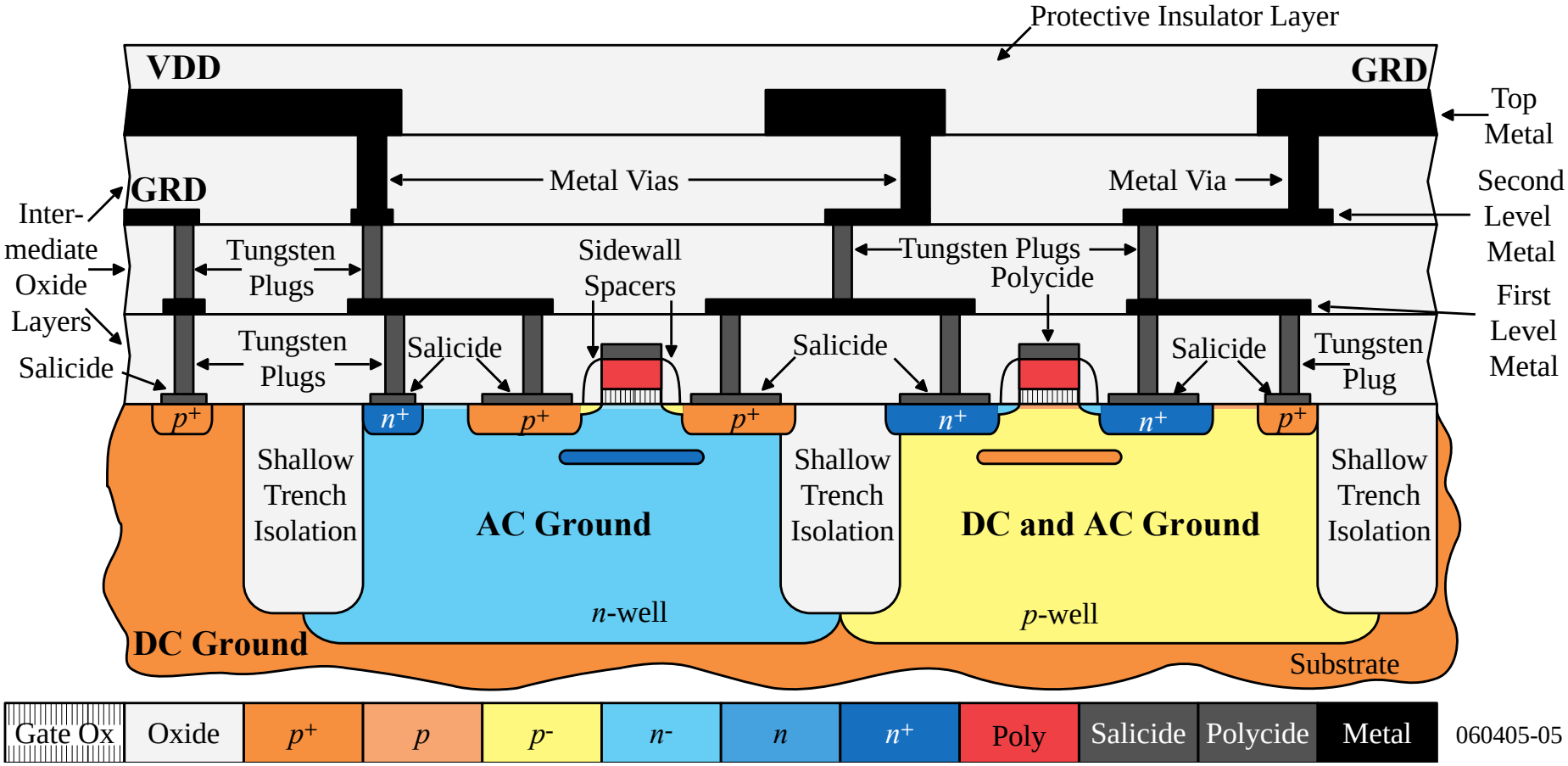
k = Boltzmann's constant (8.6×10^{-5} eV/K)

Electromigration leads to a maximum current density, J_{max}. J_{max} for copper doped aluminum is 5×10^5 A/cm^2 at 85°C.

If t = 10,000 Angstroms and $J_{max} = 5 \times 10^5$ A/cm^2, then a 10µm wide lead can conduct no more than 50mA at 85°C.

Where is AC Ground on the Chip?

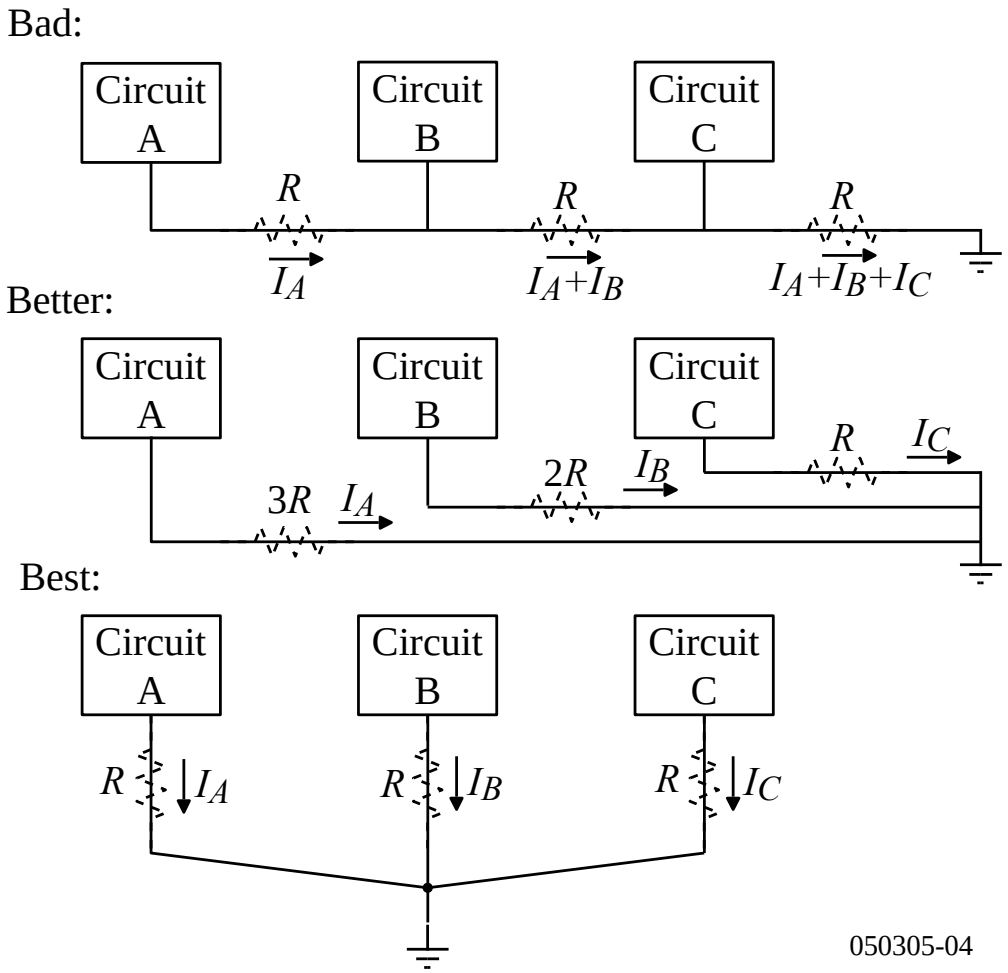
AC grounds on the chip are any area tied to a fixed potential. This includes the substrate and the wells. *All parasitic capacitances are in reference to these points.*



Grounds that are Not Grounds

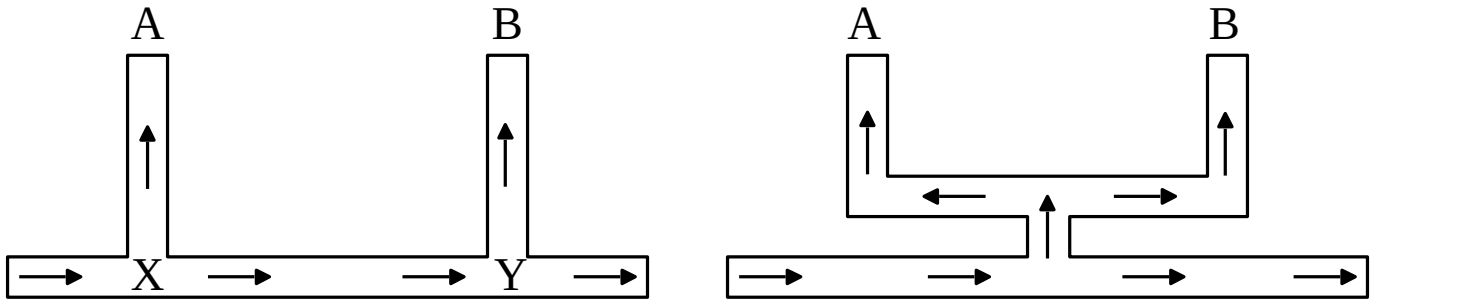
Because of the resistance of "wires", current flowing through a wire can cause a voltage drop.

An example of good and bad practice:



Kelvin Connections

Avoid unnecessary ohmic drops.



Ohmic Connection Kelvin Connection 041223-12

In the left-hand connection, an *IR* drop is experienced between *X* and *Y* causing the potentials at *A* and *B* to be slightly different.

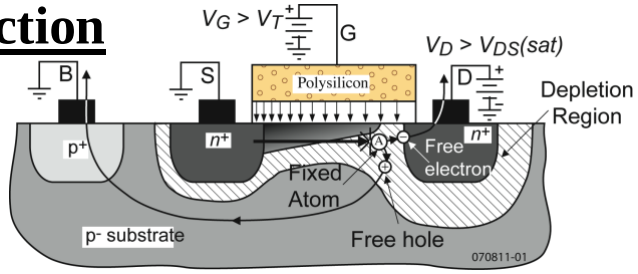
For example, let the current be 100μA and the metal be 30mΩ/sq. Suppose that the distance between *X* and *Y* is 100 squares. Therefore, the *IR* drop is

100μA x 30mΩ/sq. x 100sq. = 0.3mV

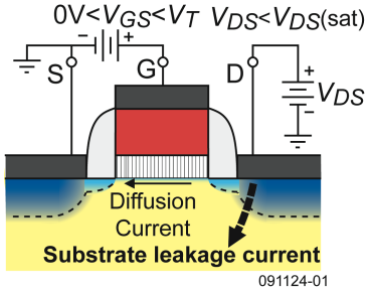
SUBSTRATE NOISE INTERFERENCE

Methods of Substrate Injection

- Hot carrier

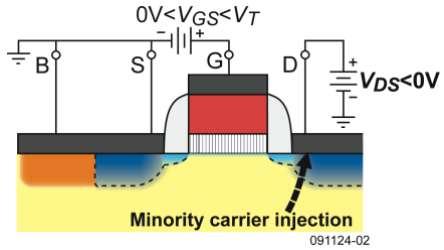


- Leakage

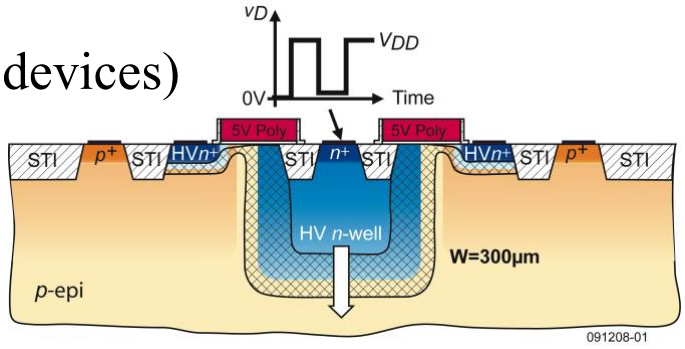


Also: The substrate BJT and the inductor create currents in the substrate.

- Minority Carrier



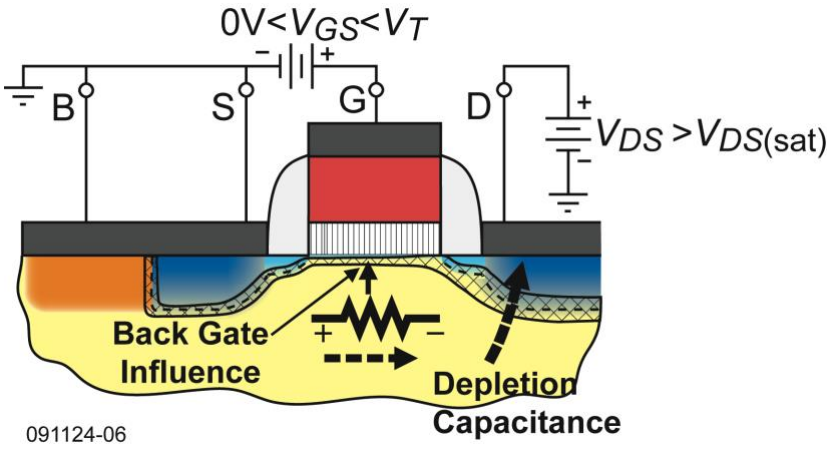
- Displacement Current (large devices)



How is Noise Injected into Components?

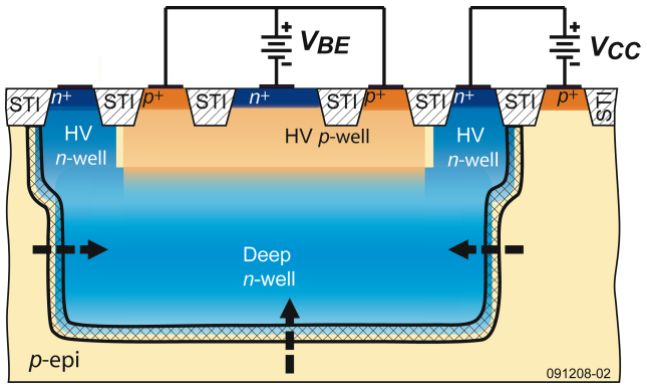
MOSFETs:

Injection occurs by the bulk effect on the threshold and across the depletion capacitance.

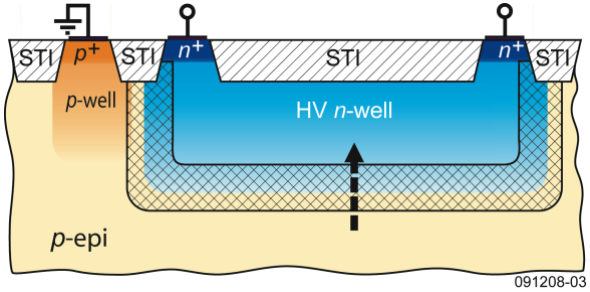


BJTs:

Injection primarily across the depletion capacitance.

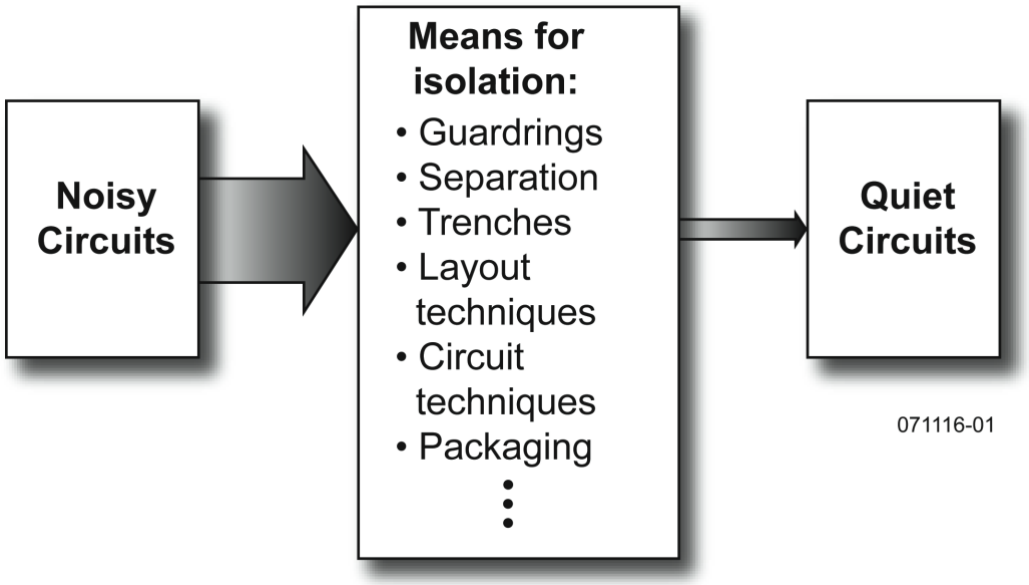


Passives:



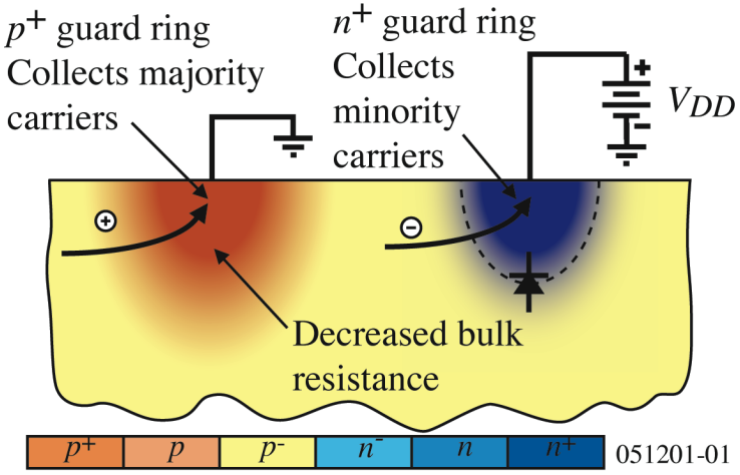
Isolation Techniques

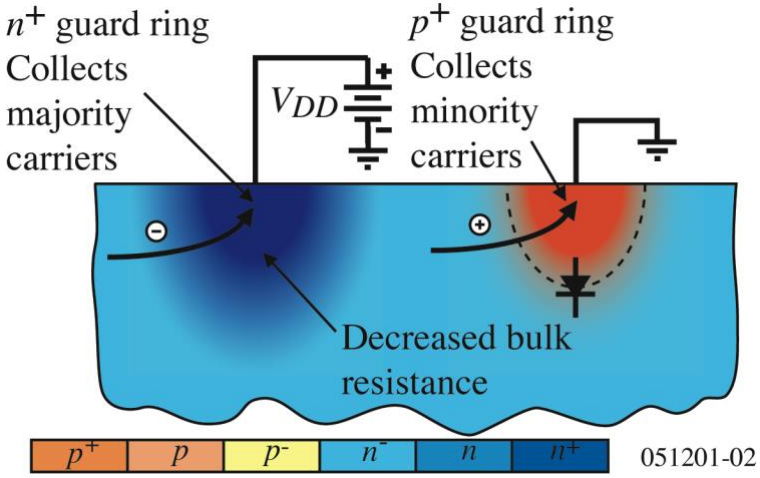
Isolation techniques include both layout and circuit approaches to isolating quiet from noisy circuits.



Isolation Techniques – Guard Rings

- Collect the majority/minority carriers in the substrate
- Connect the guard rings to external potentials through conductors with
  - Minimum resistance
  - Minimum inductance $v = L\frac{di}{dt}$





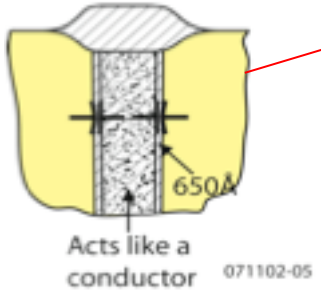
Isolation Techniques - Layout

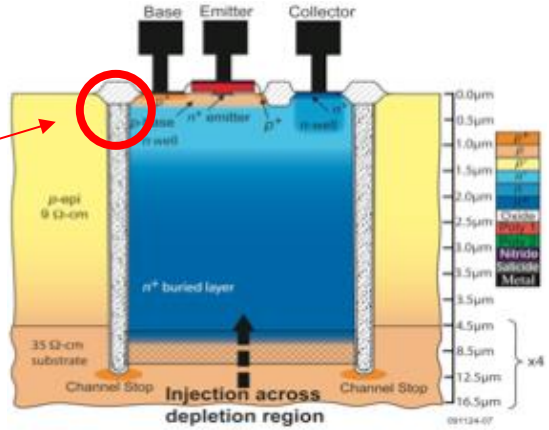
Separation:

Physical separation – works well for non-epi, less for epi

Trenches:

Good if filled with a dielectric, not good if filled with a conductor.



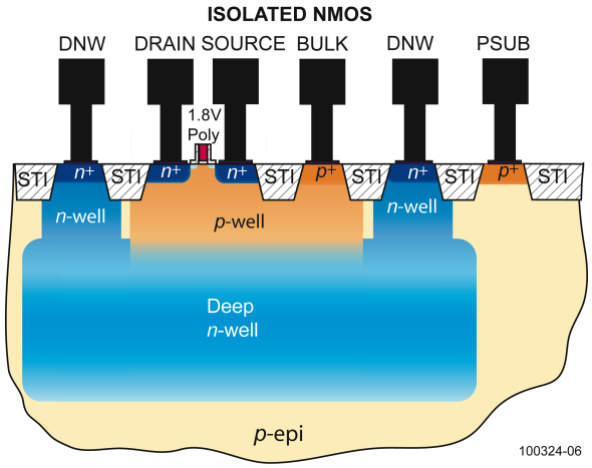


Layout:

Common centroid geometry does not help.

Keep contact and via resistance to a minimum.

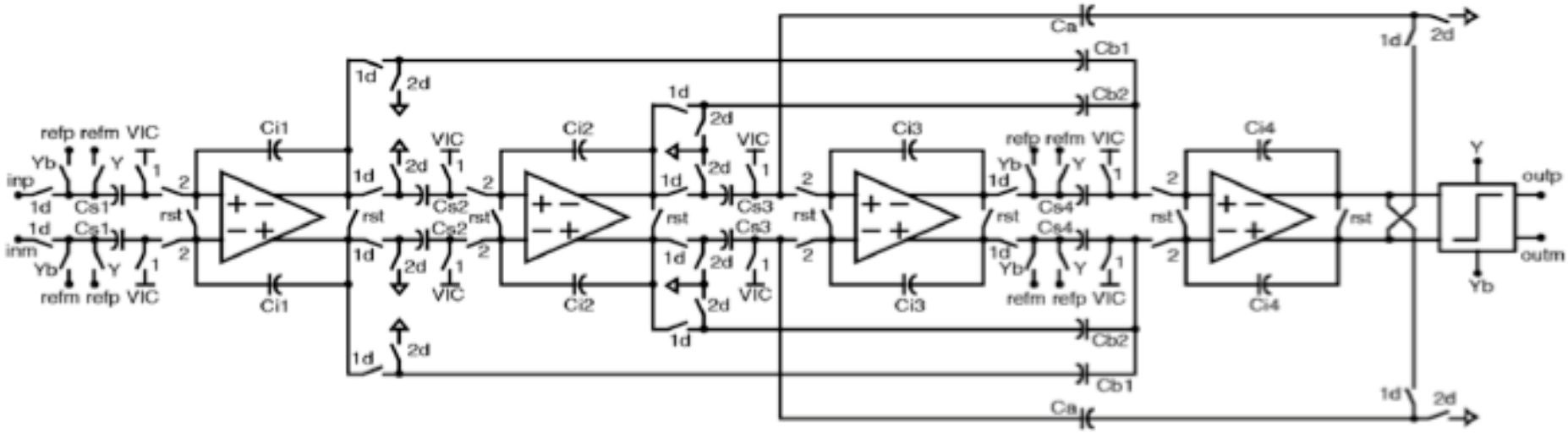
Wells help to isolate (deep *n*-well)



Isolation Techniques - Noise Insensitive Circuit Design

- Design for high power supply rejection ratio (PSRR)
- Correlated sampling techniques – eliminate low frequency noise
- Use "quiet" digital logic (power supply current remains constant)
- Use differential signal processing techniques.

Example of a 4th order Sigma Delta modulator using differential circuits:

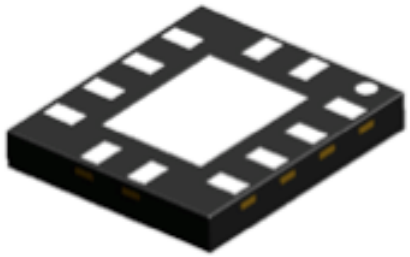


Noise Isolation Techniques - Reduction of Package Parasitics

- Keep the lead inductance to a minimum (multiple bond wires)
- Package selection†

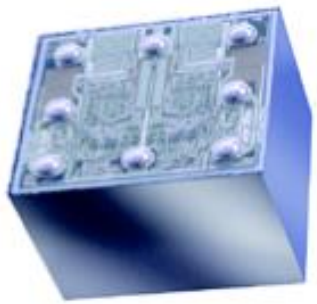
Package	Body Size (mm)	Lead Count	R (ohms)		L (nH)		M (nH)				C (pF)		C_{M12} (pF)	
			Corner	Center	Corner	Center	Corner		Center		Corner	Center	Corner	Center
							M12	M13	M12	M13				
QFP	28x28	208	0.90	0.65	12.00	8.00	8.00	6.50	5.50	4.50	0.20	0.06	1.00	0.60
	20x14	128	1.2	0.8	4.50	2.40	2.80	2.20	1.40	1.10	0.10	0.05	0.45	0.20
	12x12	80	0.36	0.28	2.90	2.40	2.30	1.60	1.30	0.90	0.15	0.10	0.27	0.20
LLP	All sizes	All	0.001	0.001	0.008	0.008	0.001	0.001	0.001	0.001	0.03	0.03	0.03	0.03
Mini SOIC	5x3	8	0.015	0.015	0.45	0.45	0.15	0.08	0.15	0.08	0.05	0.05	0.04	0.04
SC-70	2x1.25	5	0.015	-	0.045	-	0.08	0.05	-	-	0.06	-	0.06	-
SSOP	5.3x10.2	28	0.3	0.25	2.9	1.3	1.45	0.85	0.6	0.35	0.2	0.08	0.27	0.1
MDIP	19x6.35	14	0.15	0.05	7.0	3.0	2.5	1.8	1.0	0.7	0.65	0.25	1.1	0.4
μSMD (small bumps)	All sizes	All	0.003	-	0.011	-	0.002	-	-	-	0.016	-	0.012	-
μSMD (large bumps)	All sizes	All	0.002	-	0.013	-	0.002	-	-	-	0.016	-	0.012	-

Leadless lead frame:



Still has bond wires

Micro surface mount device:



Minimum inductance package

† *Electrical Performance of Packages*, National Semiconductor Application Note 1205, August 2001.

SUMMARY

- Small signal models are a linear representation of the transistor electrical behavior
- Including the transistor capacitors in the small signal model gives frequency dependence
- Noise models include thermal and $1/f$ noise voltage or current spectral density models
- Passive component models include the nonlinearity, small signal and noise models
- Interconnects include metal, polysilicon, diffusion and vias
- Electromigration occurs if the current density is too large causing a displacement of metal
- Substrate interference is due to interaction between various parts of an integrated circuit via the substrate
- Method to reduce substrate interference include:
  - Physical separation
  - Guard rings
  - Reduced inductance in the power supply and ground leads
  - Appropriate contacts to the regions of constant potential
  - Reduce the source of interfering noise
  - Use differential signal processing techniques