LECTURE 36 – CHARACTERIZATION OF ADCS AND SAMPLE AND HOLD CIRCUITS
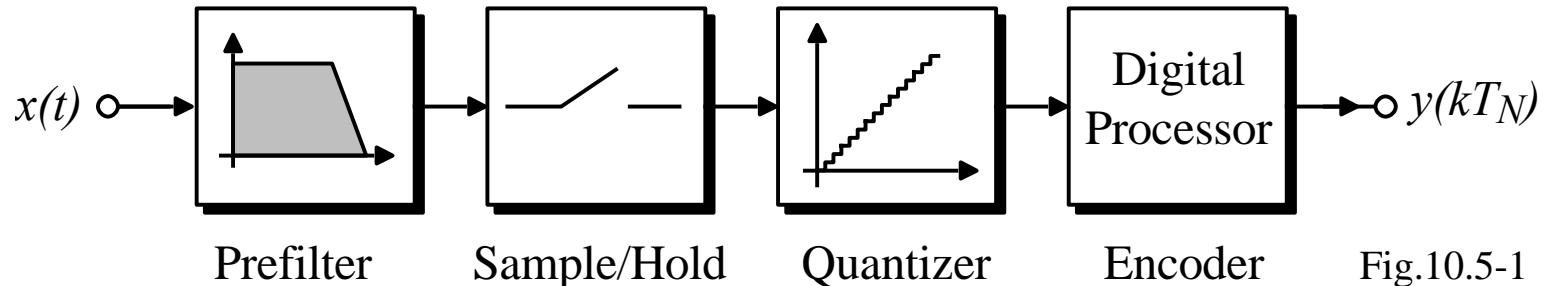## LECTURE ORGANIZATION

Outline

• Introduction to ADCs

• Static characterization of ADCs

• Dynamic characteristics of ADCs

• Sample and hold circuits

• Design of a sample and hold

• Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 539-557

INTRODUCTION

General Block Diagram of an Analog-Digital Converter

Fig.10.5-1

- Prefilter - Avoids the aliasing of high frequency signals back into the baseband of the ADC
- Sample-and-hold - Maintains the input analog signal constant during conversion
- Quantizer - Finds the subrange that corresponds to the sampled analog input
- Encoder - Encoding of the digital bits corresponding to the subrange
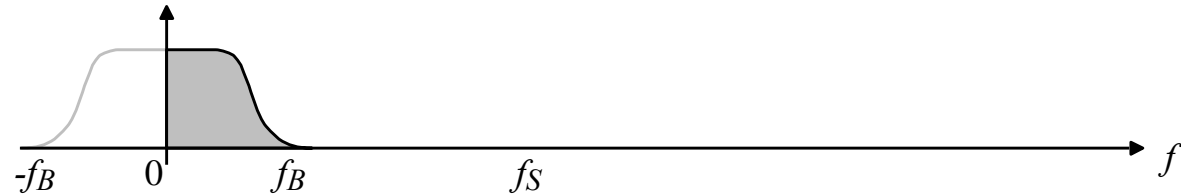
Nyquist Frequency Analog-Digital Converters

The sampled nature of the ADC places a practical limit on the bandwidth of the input signal. If the sampling frequency is f_S, and f_B is the bandwidth of the input signal, then
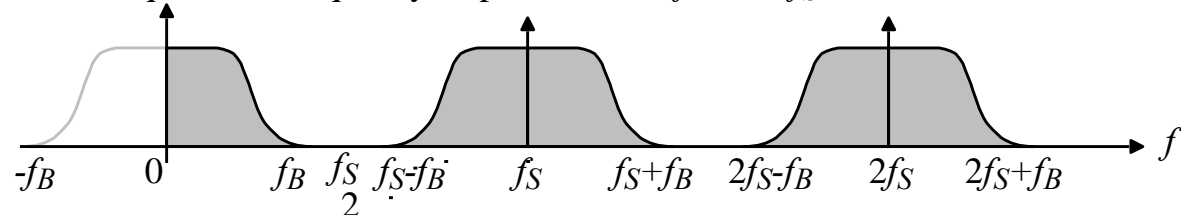
$$f_B < 0.5f_S$$

which is simply the *Nyquist* relationship which states that to avoid aliasing, the sampling frequency must be greater than twice the highest signal frequency.
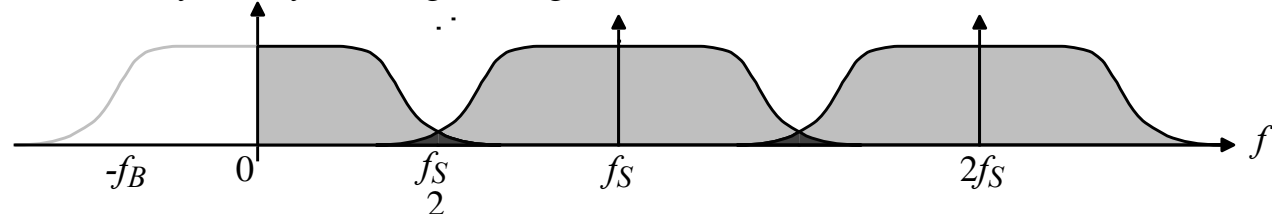
Continuous time frequency response of the analog input signal.

Sampled data equivalent frequency response where $f_B < 0.5f_S$.

Case where $f_B > 0.5f_S$ causing aliasing.

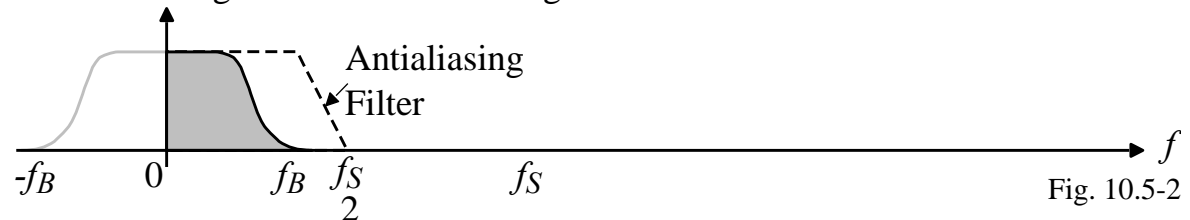Use of an antialiasing filter to avoid aliasing.

Antialiasing Filter

Fig. 10.5-2

Classification of Analog-Digital Converters

Analog-digital converters can be classified by the relationship of f_B and $0.5f_S$ and by their conversion rate.

- *Nyquist ADCs* - ADCs that have f_B as close to $0.5f_S$ as possible.
- *Oversampling ADCs* - ADCs that have f_B much less than $0.5f_S$.

Classification of Analog-to-Digital Converter Architectures

Conversion Rate	Nyquist ADCs	Oversampled ADCs
Slow	Integrating (Serial)	Very high resolution <14-16 bits
Medium	Successive Approximation 1-bit Pipeline Algorithmic	Moderate resolution <10-12 bits
Fast	Flash Multiple-bit Pipeline Folding and interpolating	Low resolution < 6-8 bits

STATIC CHARACTERIZATION OF ANALOG-TO-DIGITAL CONVERTERS

Input-Output Characteristics

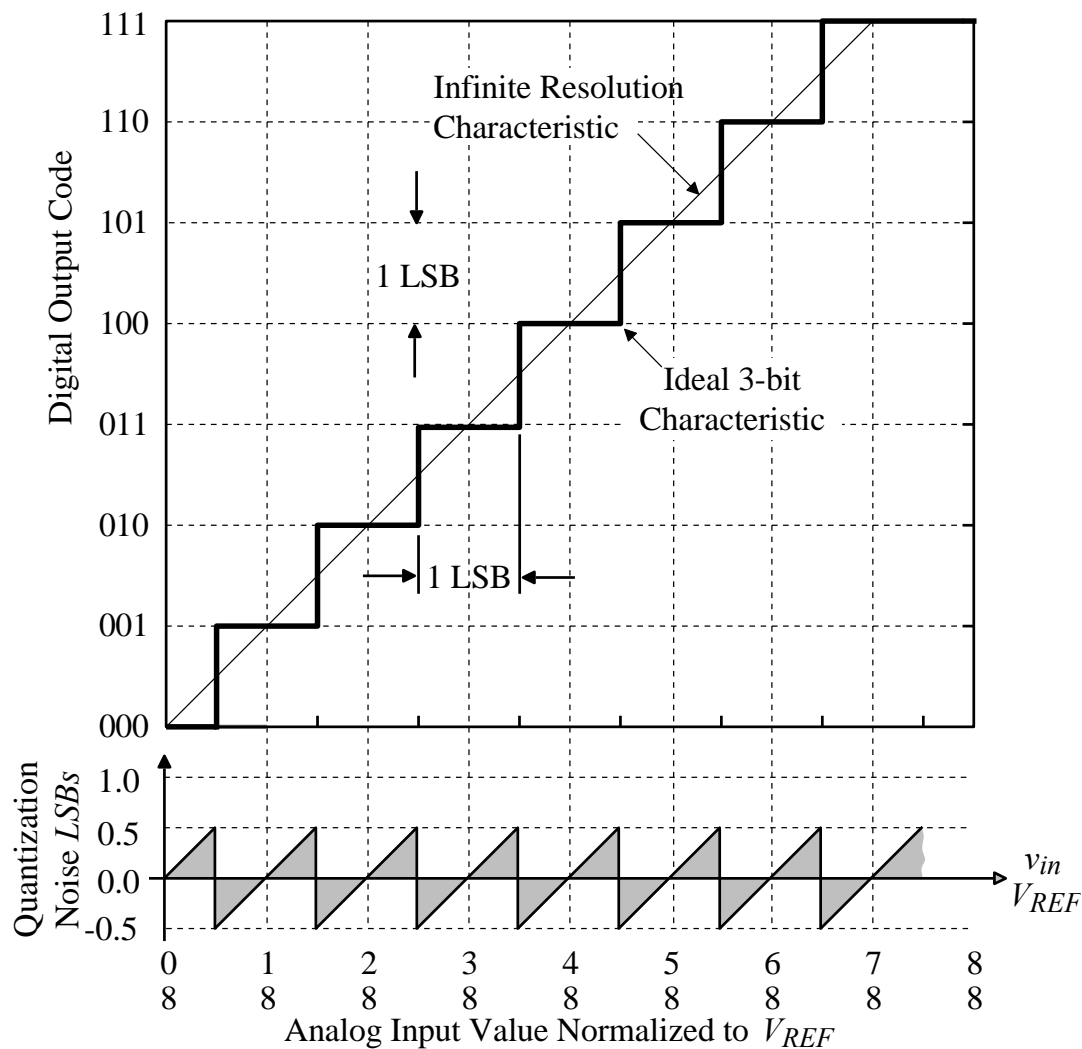Ideal input-output characteristics of a 3-bit ADC

Figure 10.5-3 Ideal input-output characteristics of a 3-bit ADC.

Definitions

- The *dynamic range, signal-to-noise ratio (SNR),* and the *effective number of bits (ENOB)* of the ADC are the same as for the DAC

- *Resolution* of the ADC is the smallest analog change that distinguishable by an ADC.

- *Quantization Noise* is the $\pm 0.5LSB$ uncertainty between the infinite resolution characteristic and the actual characteristic.

- *Offset Error* is the difference between the ideal finite resolution characteristic and actual finite resolution characteristic

- *Gain Error* is the difference between the ideal finite resolution characteristic and actual finite resolution characteristic measured at full-scale input. This difference is *proportional* to the analog input voltage.
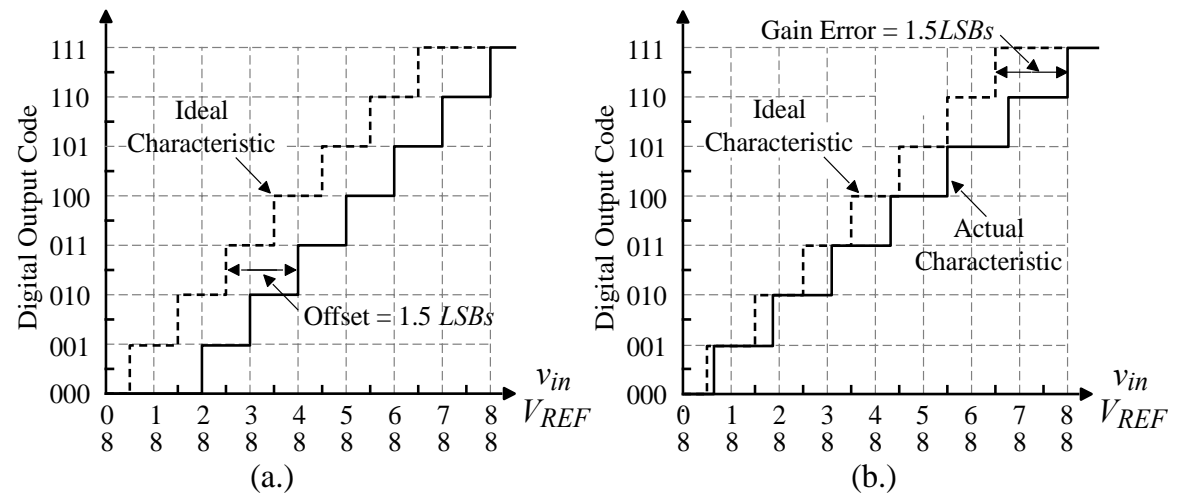

Figure 10.5-4 - (a.) Example of offset error for a 3-bit ADC. (b.) Example of gain error for a 3-bit ADC.

Integral and Differential Nonlinearity

The integral and differential nonlinearity of the ADC are referenced to the vertical (digital) axis of the transfer characteristic.

• *Integral Nonlinearity (INL)* is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*)

• *Differential Nonlinearity (DNL)* is a measure of the separation between adjacent levels measured at each vertical step (% or *LSB*).

$$DNL = (D_{cx} - 1) \; LSBs$$

where D_{cx} is the size of the actual vertical step in *LSBs*.

Note that *INL* and *DNL* of an analog-digital converter will be in terms of integers in contrast to the *INL* and *DNL* of the digital-analog converter. As the resolution of the ADC increases, this restriction becomes insignificant.

Example of *INL* and *DNL*
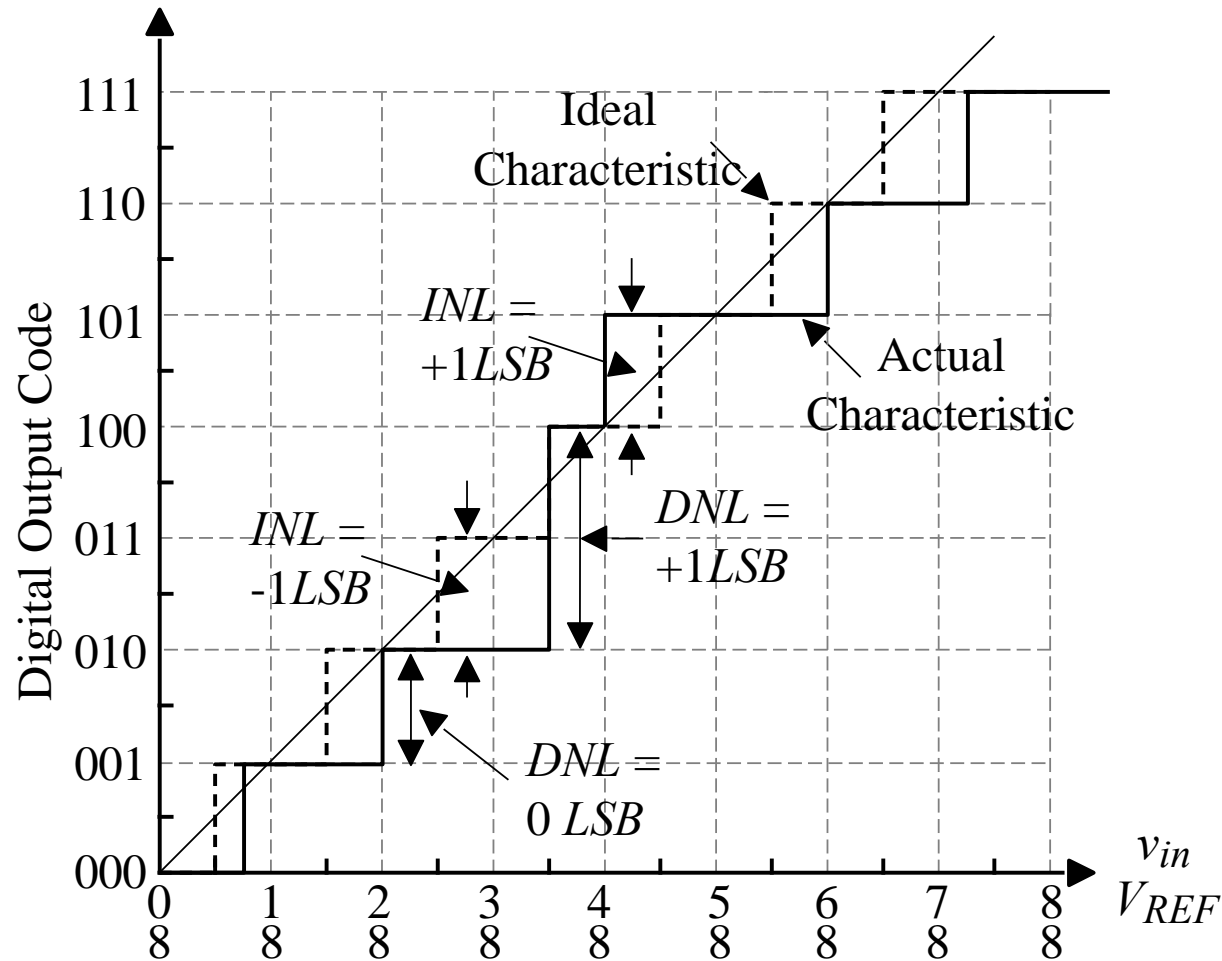
Example of *INL* and *DNL* for a 3-bit ADC.)   Fig.10.5-5

Note that the DNL and INL errors can be specified over some range of the analog input.

Monotonicity

A *monotonic* ADC has all vertical jumps positive. Note that monotonicity can only be detected by *DNL*.
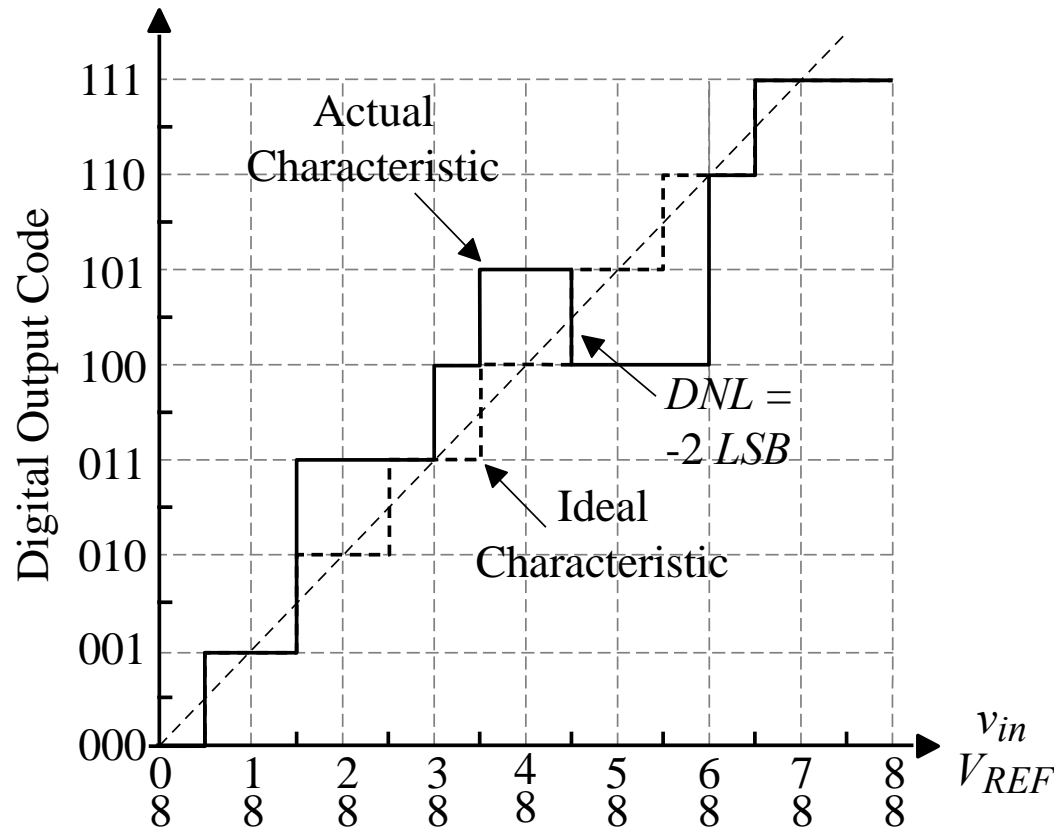
Example of a nonmonotonic ADC:

Fig. 10.5-6L

If a vertical jump is 2*LSB* or greater, missing output codes may result.

If a vertical jump is -1*LSB* or less, the ADC is not monotonic.

Example 36-1 - *INL* and *DNL* of a 3-bit ADC

Find the *INL* and *DNL* for the 3-bit ADC shown on the previous slide.

Solution

With respect to the digital axis:

1.) The largest value of *INL* for this 3-bit ADC occurs between 3/16 to 5/16 or 7/16 to 9/16 and is 1*LSB*.

2.) The smallest value of *INL* occurs between 11/16 to 12/16 and is -2*LSB*.

3.) The largest value of *DNL* occurs at 3/16 or 6/8 and is +1*LSB*.

4.) The smallest value of *DNL* occurs at 9/16 and is -2*LSB* which is where the converter becomes nonmonotonic.
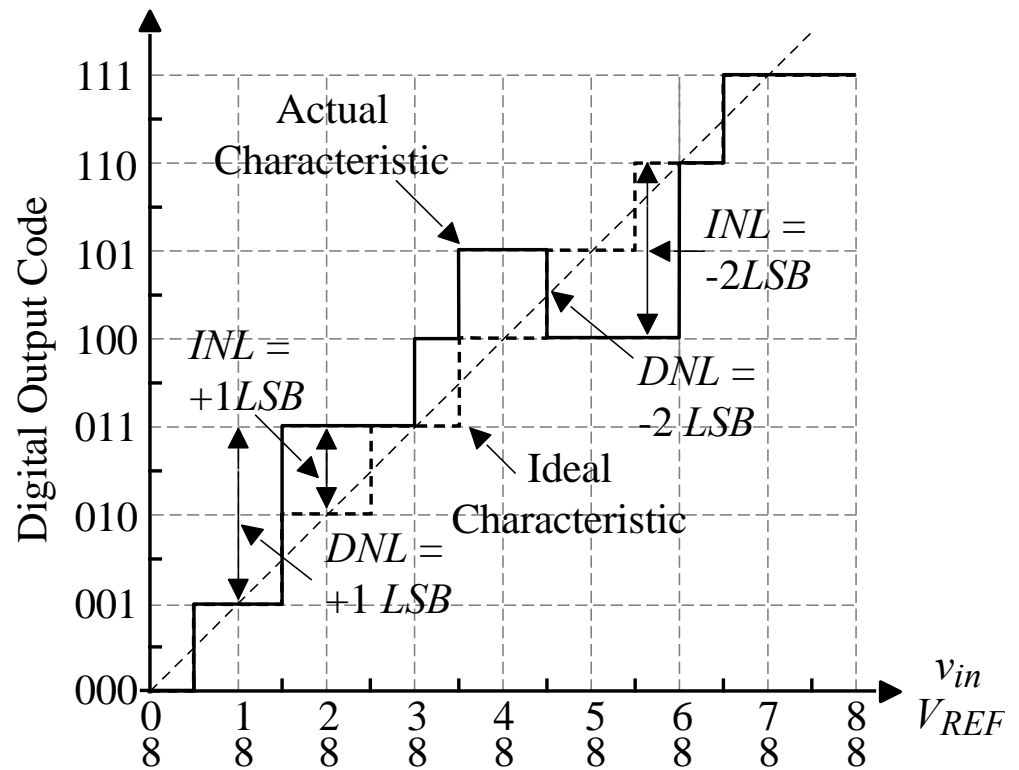

Fig. 10.5-6DL

DYNAMIC CHARACTERISTICS OF ADCs

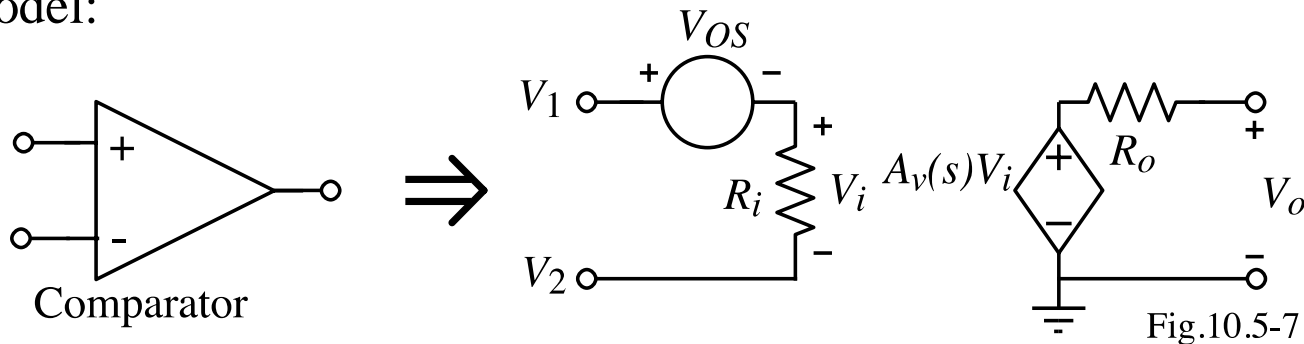### What are the Important Dynamic Characteristics for ADCs?

The dynamic characteristics of ADCs are influenced by:

• Comparators

- Linear response

- Slew response

• Sample-hold circuits

• Circuit parasitics

• Logic propagation delay

Comparator

The comparator is the quantizing unit of ADCs.

Open-loop model:

Fig.10.5-7

Nonideal aspects:

• Input offset voltage, V_{OS} (a static characteristic)

• Propagation time delay

   - Bandwidth (linear)

$$A_v(s) = \frac{A_v(0)}{\dfrac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1}$$

   - Slew rate (nonlinear)

$$\Delta T = \frac{C \cdot \Delta V}{I} \quad (I \text{ constant}) = \frac{\Delta V}{\text{Slew Rate}}$$

SAMPLE AND HOLD CIRCUITS

Requirements of a Sample and Hold Circuit

The objective of the sample and hold circuit is to sample the unknown analog signal and hold that sample while the ADC decodes the digital equivalent output.

The sample and hold circuit must:

1.) Have the accuracy required for the ADC resolution, i.e. accuracy $= \dfrac{100\%}{2^N}$

2.) The sample and hold circuit must be fast enough to work in a two-phase clock. For an ADC with a 100 Megasample/second sample rate, this means that the sample and hold must perform its function within 5 nanoseconds.

3.) Precisely sample the analog signal at the same time for each clock. An advantage of the sample and hold circuit is that it removes the precise timing requirements from the ADC itself.

4.) The power dissipation of the sample and hold circuit must be small. Unfortunately, the above requirements for accuracy and speed will mean that the power must be increased as the bits are increased and/or the clock period reduced.

Sample-and-Hold Circuit

Waveforms of a sample-and-hold circuit:

Definitions:

• *Acquisition time* (t_a) = time required to acquire the analog voltage

• *Settling time* (t_s) = time required to settle to the final held voltage to within an accuracy tolerance

Fig.10.5-9
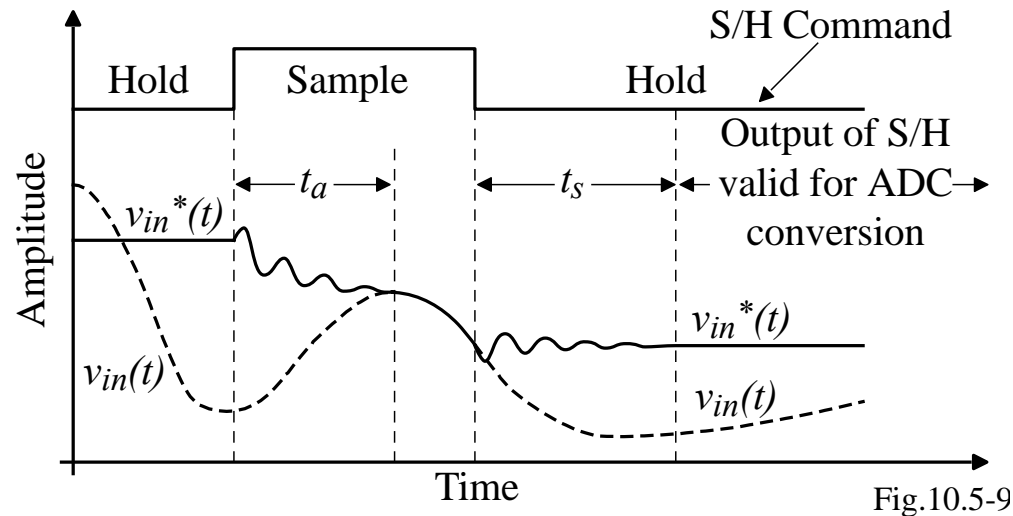
$$\therefore \quad T_{sample} = t_a + t_s \qquad \rightarrow \qquad \text{Maximum sample rate} = f_{sample}(\text{max}) = \frac{1}{T_{sample}}$$

Other consideratons:

• *Aperture time*= the time required for the sampling switch to open after the S/H command is initiated

• *Aperture jitter* = variation in the aperture time due to clock variations and noise

Types of S/H circuits:

• No feedback - faster, less accurate

• Feedback - slower, more accurate
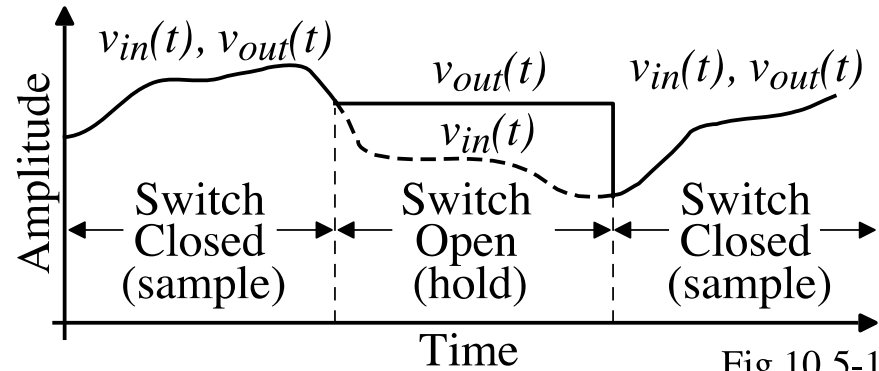
Open-Loop, Buffered S/H Circuit
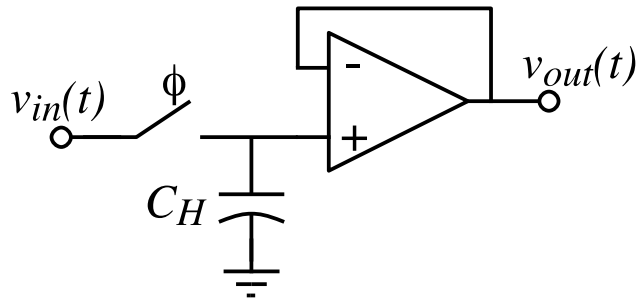
Circuit:

Fig.10.5-10

Attributes:

• Fast, open-loop

• Requires current from the input to charge C_H

• DC voltage offset of the op amp and the charge feedthrough of the switch will create dc errors

Settling Time

Assume the op amp has a dominant pole at $-\omega_a$ and a second pole at $-GB$.

The unity-gain response can be approximated as, $\quad A(s) \approx \dfrac{GB^2}{s^2 + GB \cdot s + GB^2}$

The resulting step response is, $\quad v_{out}(t) = 1 - \left(\sqrt{\dfrac{4}{3}}\, e^{-0.5GB \cdot t}\right) \sin\left(\sqrt{\dfrac{3}{4}}\, GB \cdot t + \phi\right)$

Defining the error as the difference between the final normalized value and $v_{out}(t)$, gives,

$$Error(t) = \varepsilon = 1 - v_{out}(t) = \sqrt{\dfrac{4}{3}}\, e^{-0.5GB \cdot t}$$

In most ADCs, the error is equal to $\pm 0.5LSB$. Since the voltage is normalized,

$$\dfrac{1}{2^{N+1}} = \sqrt{\dfrac{4}{3}}\, e^{-0.5GB \cdot t_s} \qquad \rightarrow \qquad e^{0.5GB \cdot t_s} = \dfrac{4}{\sqrt{3}}\, 2^N$$

Solving for the time, t_s, required to settle with $\pm 0.5LSB$ from the above equation gives

$$t_s = \dfrac{2}{GB}\, ln\left(\dfrac{4}{\sqrt{3}}\, 2^N\right) = \dfrac{1}{GB}\, [1.3863N + 1.6740]$$
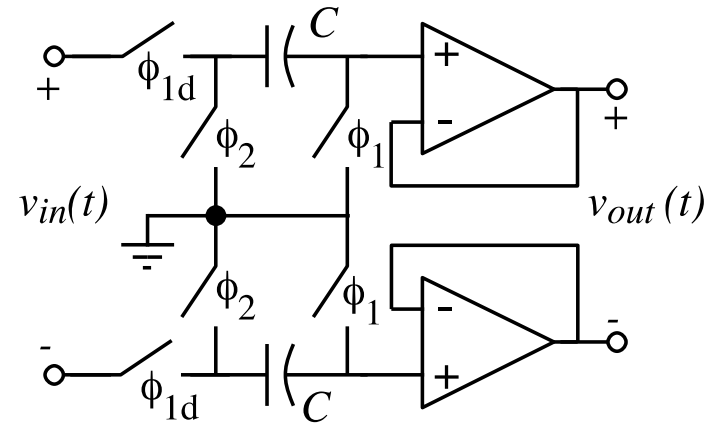
Thus as the resolution of the ADC increases, the settling time for any unity-gain buffer amplifiers will increase. For example, if we are using the open-loop, buffered S/H circuit in a 10 bit ADC, the amount of time required for the unity-gain buffer with a GB of 1MHz to settle to within 10 bit accuracy is 2.473μs.

Open-Loop, Switched-Capacitor S/H Circuit

Circuit:
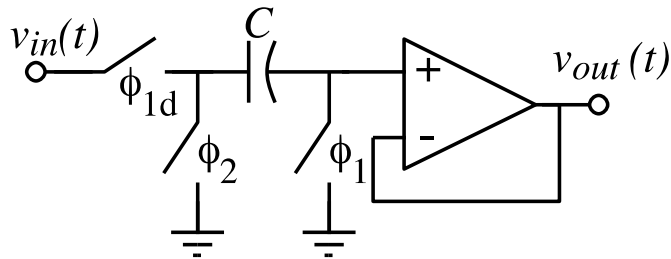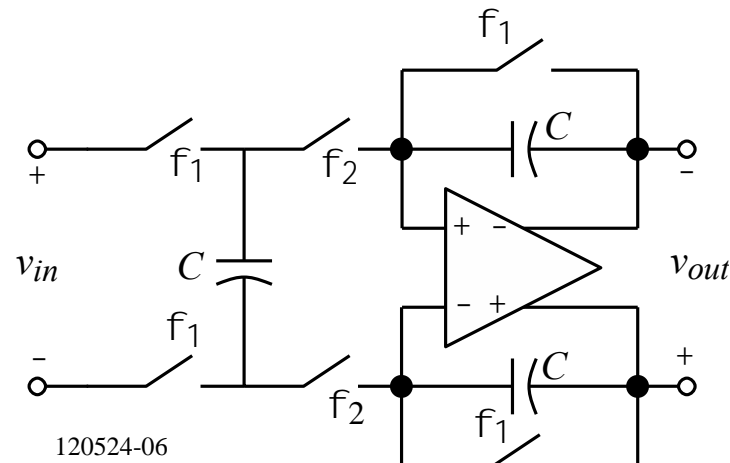

Switched capacitor S/H circuit.　　　Differential switched-capacitor S/H

Fig.10.5-11

• Delayed clock used to remove input dependent feedthrough.

• Differential version has better *CMRR*, cancellation of even harmonics, and reduction of charge injection and clock feedthrough
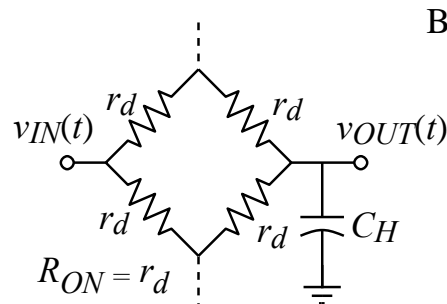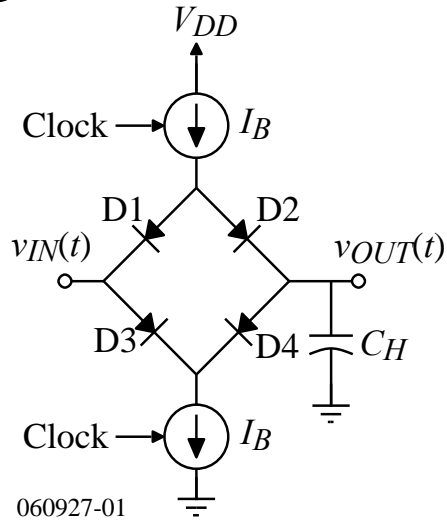
True differential version:

120524-06
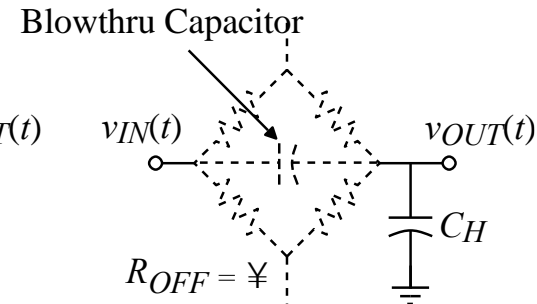
Open-Loop, Diode Bridge S/H Circuit

Diode bridge S/H circuit:

$R_{ON} = r_d$

Sample phase - diodes forward biased.

Blowthru Capacitor

$R_{OFF} = ¥$

Hold phase - diodes reversed biased.

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MOS diode bridge S/H circuit:

$R_{ON} = 1/g_m$
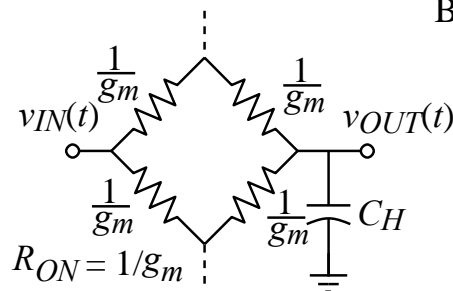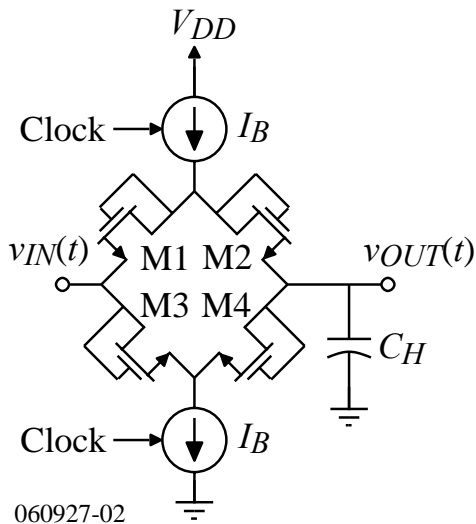
Sample phase - MOS diodes forward biased.

Blowthru Capacitor

$R_{OFF} = ¥$
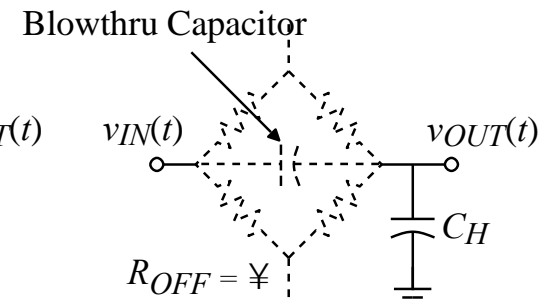
Hold phase - MOS diodes reversed biased.

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Practical Implementation of the Diode Bridge S/H Circuit
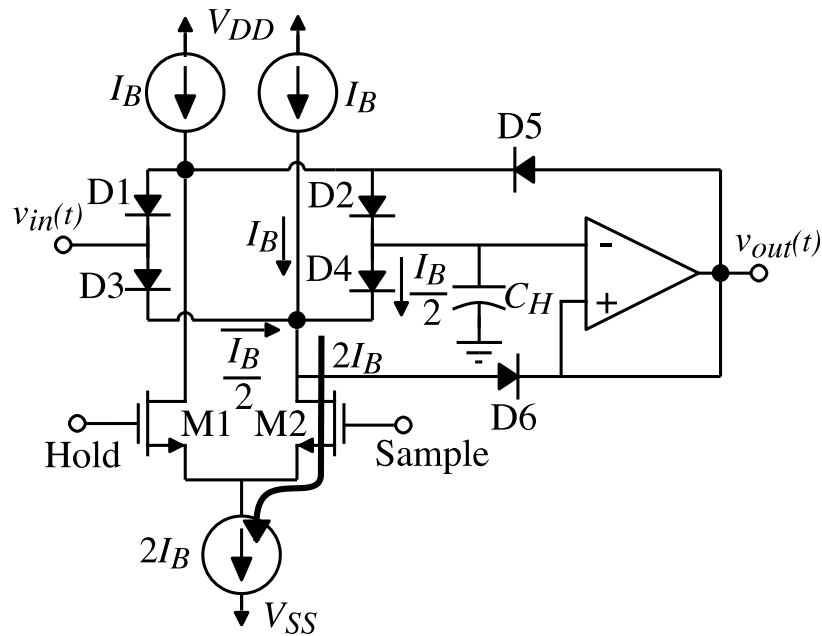
Practical implementation of the diode bridge sample and hold (sample mode).
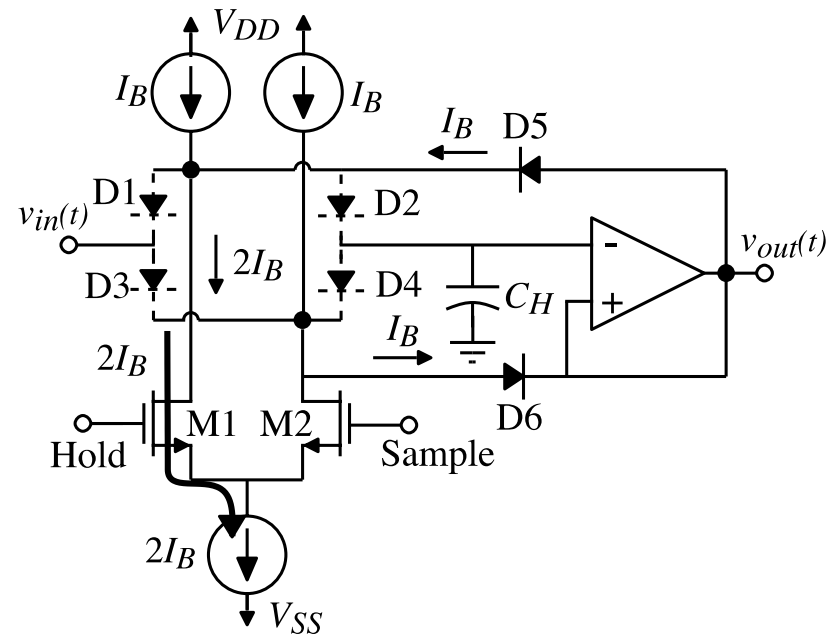
Hold mode.

150619-01

During the hold mode, the diodes D5 and D6 become forward biased and clamp the upper and lower nodes of the sampling bridge to the sampled voltage.

Closed-Loop S/H Circuit

Circuit:
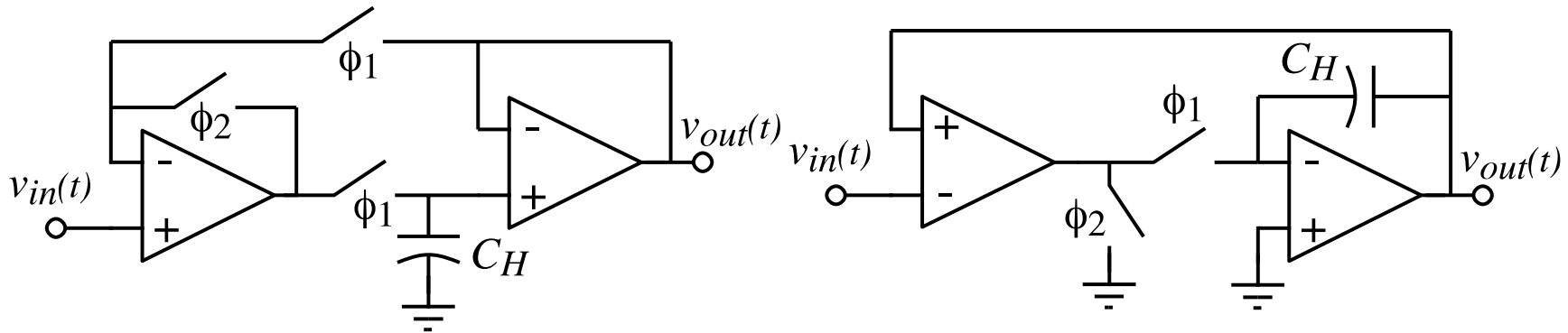
Closed-loop S/H circuit. ϕ_1 is the sample phase and ϕ_2 is the hold phase.

An improved version.

Fig.10.5-13

Attributes:

• Accurate

• First circuit has signal-dependent feedthrough

• Slower because of the op amp feedback loop

Closed-Loop, Switched Capacitor S/H Circuits

Circuit:
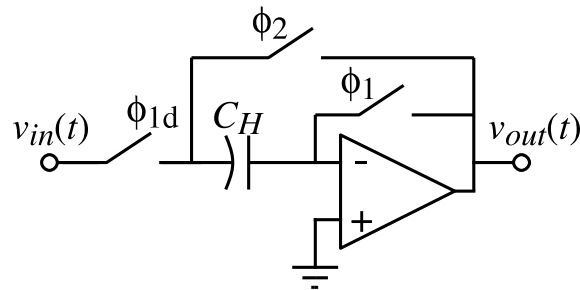
Switched capacitor S/H circuit which autozeroes the op amp input offset voltage.
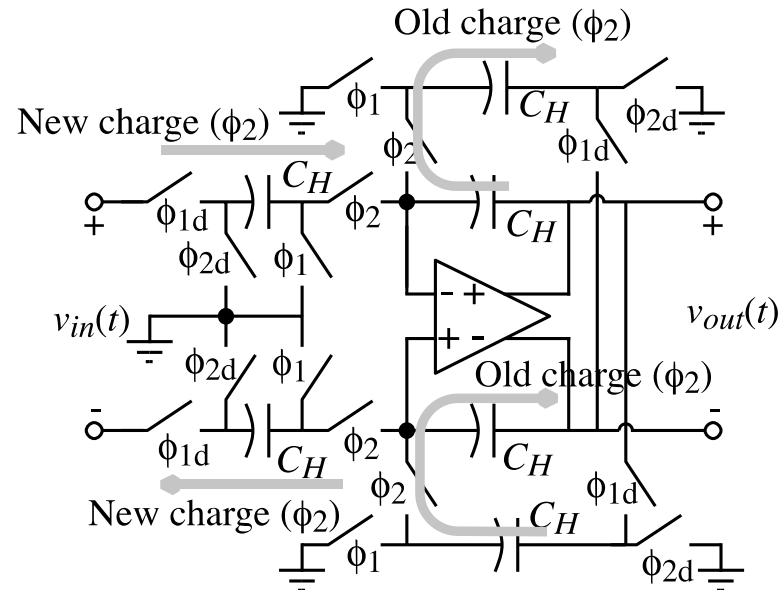
A differential version that avoids large changes at the op amp output

Attributes:

• Accurate

• Signal-dependent feedthrough eliminated by a delayed clock

• Differential circuit keeps the output of the op amps constant during the ϕ_1 phase avoiding slew rate limits

Current-Mode S/H Circuit

Circuit:

Fig.10.5-15
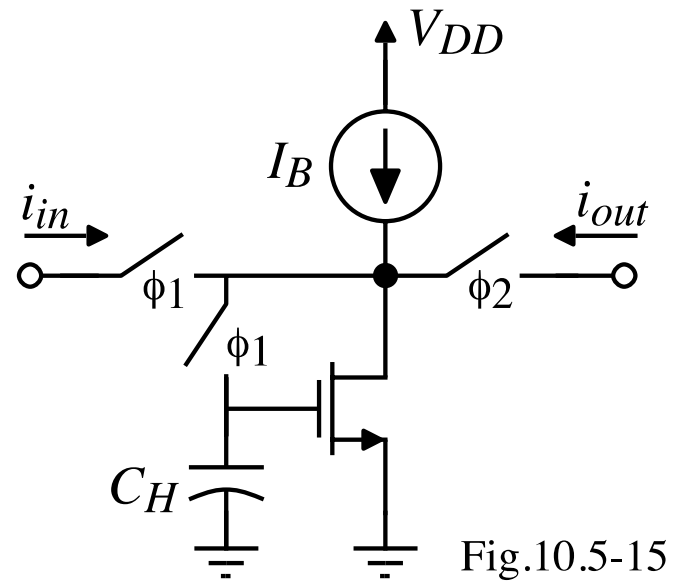
Attributes:

- Fast

- Requires current in and out

- Good for low voltage implementations

Aperature Jitter in S/H Circuits

Illustration:

If we assume that $v_{in}(t) = V_p sin\,\omega t$, then the maximum slope is equal to ωV_p.

Figure 10.5-14 - Illustration of aperature jitter in an ADC.

Therefore, the value of ΔV is given as

$$\Delta V = \left|\frac{dv_{in}}{dt}\right| \Delta t = \omega V_p \Delta t .$$

The rms value of this noise is given as

$$\Delta V(\text{rms}) = \left|\frac{dv_{in}}{dt}\right| \Delta t = \frac{\omega V_p \Delta t}{\sqrt{2}} .$$

The aperature jitter can lead to a limitation in the desired dynamic range of an ADC. For example, if the aperature jitter of the clock is 100ps, and the input signal is a full scale peak-to-peak sinusoid at 1MHz, the rms value of noise due to this aperature jitter is $111\mu V(\text{rms})$ if the value of $V_{REF} = 1V$.

DESIGN OF A SAMPLE AND HOLD AMPLIFIER

Specifications

Accuracy = 10 bits

Clock frequency is 10 MHz

Power dissipation $\leq$ 1mW

Signal level is from 0 to 1V

Slew rate $\geq$ 100V/μs with C_L = 1pF

Use 0.25μm CMOS

Technology Parameters (C_{ox} = 60.6x10^{-4} F/m^2):

Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		N-Channel	P-Channel	
V_{T0}	Threshold Voltage (V$_{BS}$ = 0)	0.5± 0.15	-0.5 ± 0.15	V
K'	Transconductance Para-meter (in saturation)	120.0 ± 10%	25.0 ± 10%	μA/V^2
γ	Bulk threshold parameter	0.4	0.6	(V)$^{1/2}$
λ	Channel length modulation parameter	0.32 ($L=L_{min}$) 0.06 ($L \geq 2L_{min}$)	0.56 ($L=L_{min}$) 0.08 ($L \geq 2L_{min}$)	(V)$^{-1}$
$2|\phi_F|$	Surface potential at strong inversion	0.7	0.8	V

Op Amp Design

Gain:

$$\text{Gain error} = \frac{1}{1+\text{Loop Gain}} \leq 0.5 \text{ LSB} = \frac{1}{2^{11}}$$

Therefore, the op amp gain $\geq 2^{11} = 2048$ V/V

Choose the op amp gain as ≥ 5000 V/V

Gainbandwidth:

For a dominant pole op amp with unity-gain feedback, the relationship between the gain-bandwidth (GB), accuracy (N) and speed (t_s) is

$$t_s = \left(\frac{N+1}{GB}\right) ln(2) = 0.693 \left(\frac{N+1}{GB}\right)$$

Therefore, if $t_s \leq 0.5\ T_{clock} = 50$ ns (choose $t_s = 10$ ns). For $N = 10$, the gain-bandwidth is

$$GB = 0.762 \times 10^9 = 120 \text{ MHz}$$

Dominant pole is 24 kHz and with an output capacitance of 1pF this means the output resistance of the op amp must be ≥ 6.6 MΩ.

Op Amp Design – Continued

The previous specifications suggest a self-compensated op amp. The gain and output resistance should be easy to achieve with a cascaded output. A folded-cascode op amp is proposed for the design. In order to have the 0-1V signal range, a *p*-channel, differential input is selected. This will give the input 0-1V range. The output will effectively be 0-1V with the unity gain feedback around the op amp.

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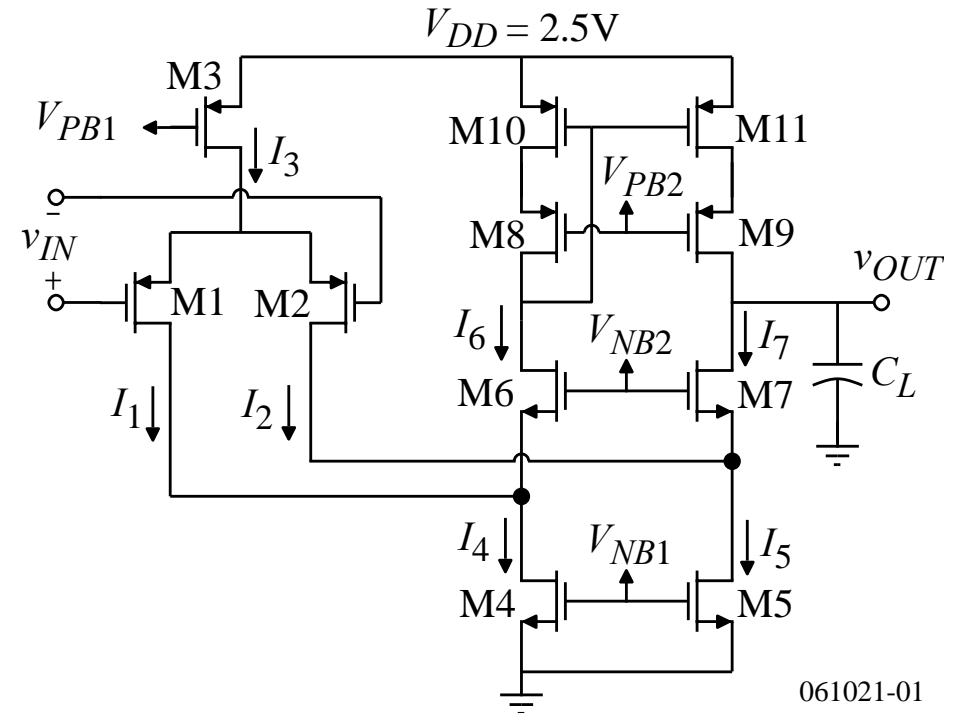
Bias Currents:

The 100V/µs slew rate requires $I_3 = 100µA$. Setting $I_4 = I_5 = 125µA$ gives a power dissipation of 0.875mW with $V_{DD} = 2.5V$.

Op Amp Design – Continued

Transistor sizes:

Design M4-M7 to give a saturation voltage of 0.1V with 125µA.

$$\therefore \quad \frac{W_4}{L_4} = \frac{W_5}{L_5} = \frac{W_6}{L_6} = \frac{W_7}{L_7} = \frac{2I_D}{K_n' \cdot V_{DS}(\text{sat})^2} = \frac{2 \cdot 125}{120 \cdot 0.01} \approx \underline{\underline{200}}$$

Since the upper swing is not as important, choose a saturation voltage of 0.25 for M8 – M11.

$$\therefore \quad \frac{W_8}{L_8} = \frac{W_9}{L_9} = \frac{W_{10}}{L_{10}} = \frac{W_{11}}{L_{11}} = \frac{2I_D}{K_p' \cdot V_{DS}(\text{sat})^2} = \frac{2 \cdot 125}{25 \cdot 0.0625} = \underline{\underline{160}}$$

To get the GB of 120 MHz, this implies the g_m of M1 and M2 is

$$g_m = GB \cdot C_L = (120 \text{x} 10^6 \cdot 2\pi)(10^{-12}) = 762 \ \mu S$$

$$\therefore \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_m^2}{2I_D K_p'} = \frac{762 \cdot 762}{2 \cdot 25 \cdot 50} = \underline{\underline{232}}$$

Let the upper input common mode voltage be 1.5V which gives the W/L of M3 as,

$$1V = V_{SG1} + V_{SD3} = 0.631 + V_{SD3} \quad \Rightarrow \quad V_{SD3} = 0.369V \quad \Rightarrow \quad \frac{W_3}{L_3} \approx \underline{\underline{60}}$$

Op Amp Design – Continued

We now need to check the output resistance and the gain to make sure the specifications are satisfied. Let us choose twice minimum channel length to keep the capacitive parasitics minimized and not have the output resistance too small. Therefore at quiescent conditions,

$$r_{ds5} = 133\text{k}\Omega, \ r_{ds7} = 222\text{k}\Omega, \ g_{m7} = 1.935\text{mS and } r_{ds2} = 250\text{k}\Omega$$

$$\therefore \quad R_{outdown} \approx (r_{ds5} \| r_{ds2}) g_{m7} r_{ds7} = 37.29\text{M}\Omega$$

$$r_{ds9} = r_{ds11} = 167\text{k}\Omega, \text{ and } g_{m11} = 1.697\text{mS}$$

$$\therefore \quad R_{outup} \approx r_{ds11} g_{m9} r_{ds9} = 47.33\text{M}\Omega$$
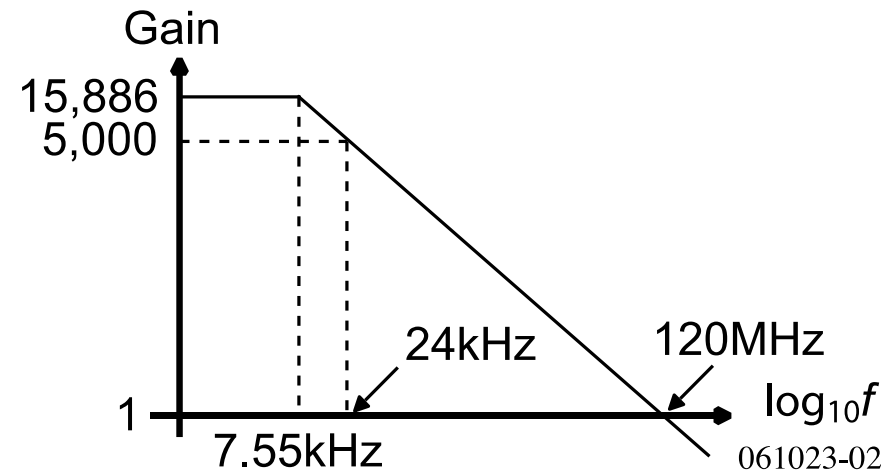
$$\therefore \quad R_{out} \approx 20.86\text{M}\Omega$$

The low frequency gain is,

$$A_v \approx g_{m1} R_{out}$$

$$= 762\mu\text{S} \cdot 20.86\text{M}\Omega = 15{,}886 \text{ V/V}$$

The frequency response will be as shown:

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Op Amp Bias Voltages

We also need to design the bias voltages V_{NB1}, V_{NB2}, V_{PB1} and V_{PB2}. This can be done using the following circuit:

Note, the W/L of M3, M4 and M7 will be 6 so that a current of 10µA gives 100µA in M3 of the op amp. Also, W/L of M1 and M5 will be 16 so a current of 10µA gives 125µA in M4 and M5 of the op amp.

If M2 is 4 times larger than M1, which gives a W/L of 64 for M2. Under these conditions,

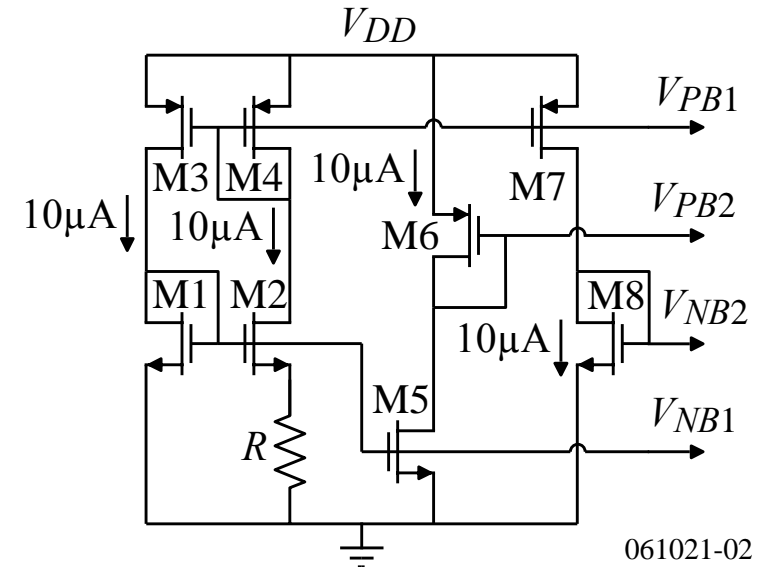$$I_2 = I_1 = \frac{1}{2\beta_1 R^2} \implies R = \frac{10^6}{\sqrt{2 \cdot 120 \cdot 16 \cdot 10}} = 5.1\text{k}\Omega$$

The extra 40µA brings the power dissipation to 0.975mW which is still in specification.

The W/L of M6 and M8 are designed as follows:

$$V_{GS8} = V_T + 2V_{ON} \implies V_{GS8} - V_T = 0.2\text{V} = \sqrt{\frac{2 \cdot 10}{120 \cdot (W_8/L_8)}} \implies \frac{W_8}{L_8} =$$

4.167

$$V_{SG6} = |V_T| + 2V_{ON} \Rightarrow \quad V_{SG6} - |V_T| = 0.5\text{V} = \sqrt{\frac{2 \cdot 10}{25 \cdot (W_6/L_6)}} \quad \Rightarrow \quad \frac{W_6}{L_6} \quad =$$

3.20

Switch and Hold Capacitor Design

Switch:

Since the signal amplitude is from 0 to 1V, a single NMOS switch should be satisfactory. The resistance of a minimum size NMOS switch is,

$$R_{ON}(\text{worst case}) \approx \frac{1}{K_n'(W/L)(V_{GS}-V_T)} = \frac{10^6}{120(1)(1.5-0.5)} = 8.33\text{k}\Omega$$

For a $C_H = 1$pf, the time constant is 8 ns. This is too close to the 50 ns so let us increase the switch size to 0.5μm/0.25μm which gives a time constant of 4ns.

Therefore, the W/L ratio of the NMOS switch is 0.5μm/0.25μm and the hold capacitor is 1pf.

Check the error due to channel injection and clock feedthrough–

If we assume the clock that rises and falls in 1ns, then a 0.5μm/0.25μm switch works in the fast transition region. The channel/clock error can be calculated as:

$$V_{error} = -\left(\frac{W{\cdot}CGDO + \dfrac{C_{channel}}{2}}{C_L}\right)\left(V_{HT} - \frac{\beta V_{HT}^3}{6U{\cdot}C_L}\right) - \frac{W{\cdot}CGDO}{C_L}(V_S+2V_T-V_L)$$

Switch and Hold Capacitor Design – Continued

Assuming $CGDO$ is $200\text{x}10^{-12}$ F/m we can calculate V_{HT} as 0.8131V. Thus,

$V_{error} =$

$$-\left(\frac{100\text{x}10^{-18}+0.5(7.57\text{x}10^{-16})}{1\text{x}10^{-12}}\right)\left(0.8131-\frac{0.105\text{x}10^{-3}}{15\text{x}10^{-3}}\right) - \frac{100\text{x}10^{-18}}{1\text{x}10^{-12}}(1+1-0) = -0.586\text{mV}$$

For a 1volt signal with 10 bit accuracy, the error must be less than 1LSB which is 0.967mV. The channel/clock error is close to this value and one may have to consider using a CMOS switch or a dummy switch to reduce the error.

Summary:

At this point, the analog designer understands the weaknesses and strengths of the design. The next steps will not be done but are listed below:

    1.) Simulation to confirm and explore the hand-calculated performance
    2.) Layout of the op amp, hold capacitor and switch.
    3.) Verification of the layout
    4.) Extraction of the parasitics from the layout
    5.) Resimulation of the design.
    6.) Check for sensitivity to ESD and latchup.
    7.) Select package and include package parasitics in simulation.

SUMMARY

- An ADC is by nature a sampled data circuit (cannot continuously convert analog into digital)
- Two basic types of ADCs are:
  - Nyquist – analog bandwidth is as close to the Nyquist frequency as possible
  - Oversampled – analog bandwidth is much smaller than the Nyquist frequency
- The active components in an ADC are the comparator and the sample and hold circuit
- A sample and hold circuit must have at least the accuracy of $100\%/2^N$
- Sample and hold circuits are divided into two types:
  - Open loop which are fast but not as accurate
  - Close loop which are slower but more accurate
- An example of designing a sample and hold amplifier was given to illustrate the electrical design process for CMOS analog circuits