```
.cseg
.org 0

        ldi r16, 0b10101010
        sts DDRL, r16
        ldi r16, 0b00001010
        out DDRB, r16

        ; Turn on LEDs
        ldi r16, 0b10101010
        sts PORTL, r16
        ldi r16, 0b00001010
        out PORTB, r16

        ldi r17, 0xFF           ; Toggle mask
        ldi r18, 0b10101010 ; AND mask for PORTL
        ldi r19, 0b00001010 ; AND mask for PORTB

main_loop:

        ; Nested delay loop
        ldi r20, 0x3D
x1:
                ldi r21, 0xFF
x2:
                        ldi r22, 0xFF
x3:
                                dec r22
                                brne x3
                        dec r21
                        brne x2
                dec r20
                brne x1

        ; Toggle LEDs
        lds r16, PORTL
        eor r16, r17
        and r16, r18
        sts PORTL, r16
        in r16, PORTB
        eor r16, r17
        and r16, r19
        out PORTB, r16

        jmp main_loop
```