數位系統設計 HW3: Single-cycle MIPS

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1. Simulated timing

本次合成出的電路能通過 testbench 的 cycle time T 最低可到 3.52：

```
`timescale 1 ns/10 ps
`define H_CYCLE 1.76
`define CYCLE 3.52

module SingleCycle_tb;
```

由於本次的 testbench 需要的 cycle 數為 18.5 個 cycle，通過模擬花費的時間為：

```
Loading snapshot worklib.SingleCycle_tb:v ..................... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
Your lw instruction is correct!
Your lw instruction is correct!
Your add instruction is correct!
Your sub instruction is correct!
Your and instruction is correct!
Your beq instruction is correct!
Your or instruction is correct!
Your slt instruction is correct!
Your sw instruction is correct!
Your jump instruction is correct!
Your jal instruction is correct!
Your jr instruction is correct!
Your beq instruction is correct!

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  Congratulations!! Your design has passed all the test!!

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Simulation complete via $finish(1) at time 65120 PS + 0
./DSDHW3_tb_gate.v:225          $finish;
ncsim> exit
```

65.12 ns，即 3.52 ns x 18.5。模擬結果的花費時間正確。

另外在 `report_timing` 中可以看到 slack (MET)：

```
 U3126/Y (NOR2X1)                         0.06       2.95 f
 U3127/Y (NOR2X1)                         0.10       3.05 r
 U3130/Y (NOR2X1)                         0.05       3.09 f
 U1225/Y (AOI21XL)                        0.21       3.30 r
 U1104/Y (OAI2BB1X4)                      0.06       3.36 f
 U1103/Y (AOI21X2)                        0.18       3.53 r
 U1158/Y (OAI21X1)                        0.05       3.59 f
 U1183/Y (XNOR2XL)                        0.09       3.67 f
 U2046/Y (AOI222XL)                       0.21       3.89 r
 pc_r_reg[30]/D (DFFSX1)                  0.00       3.89 r
 data arrival time                                   3.89

 clock CLK (rise edge)                    4.00       4.00
 clock network delay (ideal)              0.00       4.00
 pc_r_reg[30]/CK (DFFSX1)                 0.00       4.00 r
 library setup time                      -0.11       3.89
 data required time                                  3.89
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 data required time                                  3.89
 data arrival time                                  -3.89
 -----------------------------------------------------------
 slack (MET)                                        0.00
```

2. **Area** (from `report_area`)

```
Number of ports:                          296
Number of nets:                          4314
Number of cells:                         4032
Number of combinational cells:           2944
Number of sequential cells:              1057
Number of macros/black boxes:               0
Number of buf/inv:                        436
Number of references:                     149

Combinational area:              24878.791410
Buf/Inv area:                     1828.099778
Noncombinational area:           27273.823448
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 52152.614858
Total area:                 undefined
```

顯示的 total cell area 約為 52152.61。

3. **Cost** (A x T)

$A \times T \approx 52152.61 \times 3.52 \approx 183577.19$

- **其他細節**

本次作業中用來合成的 script 寫在 DSDHW3.v 的註解中。

實作部分滿足 MIPS 的規格和功能要求（32x32b REG, 32b PC, 11 required instructions）。