

The figure is a timing diagram for a Verilog testbench named `TestGlitchy`. It displays six signals over a 10 ns time interval. The signals are:

- `/glitch_tb/TestGlitchy/go`: A signal that transitions from 0 to 1 at approximately 2.5 ns and back to 0 at approximately 3.5 ns.
- `/glitch_tb/TestGlitchy/ws`: A signal that transitions from 0 to 1 at approximately 3.5 ns and back to 0 at approximately 4.5 ns.
- `/glitch_tb/TestGlitchy/clk`: A periodic square wave with a period of 2 ns, starting at 0.
- `/glitch_tb/TestGlitchy/reset_n`: A signal that is 1 until approximately 1 ns, then transitions to 0 and remains there.
- `/glitch_tb/TestGlitchy/no_glitch_ps`: A signal that is 1 until approximately 1 ns, then transitions to 0 and remains there.
- `/glitch_tb/TestGlitchy/no_glitch_ns`: A signal that is 1 until approximately 1 ns, then transitions to 0 and remains there.

The diagram includes a message window on the left showing the following messages:

- `1'h0`
- `1'h1`
- `1'h1`
- `1'h1`
- `DLY`
- `READ`

The bottom of the diagram shows a time scale from 0 ns to 10 ns with major grid lines every 1 ns and minor grid lines every 100 ps. A cursor is positioned at 0.00 ns.