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ECE 474

Glitch/Glitchy State Machine

Section 1:
I noticed that my waveform is behaving kind of strange compared to the one in the slides. In mine rd drops for some strange reason. Although the glitchy (sv) code is the same, I believe that it might have synthesized a different gate level. This means that it would consider other sorts of timing delays.

Now, the odd behavior of ds can be noted in the waveform by the random “ticks” or “highs”. This is due to propagation delays in the gates used. This is why it happens pico-seconds after the rising edge, and not during it. I know this is gate related because it does not happen in the RTL simulation.
Note: the first picture in the submission is named “Glitch Waveform”.

Section 2:
The second code named no_glitch corrects the strange behavior of rd and ds by utilizing latches. In the schematic for the glitchless code, one can see that the output ds is connected directly to a latch. This makes it so that regardless of the timing delays introduced by the logic gates, the output is decided upon that latch. Although it can have some slight delay, it will be incredibly minimal and prevent us from receiving data at different times.

Submission Notes:
My script in the root folder named RUN_THIS_ONE.sh runs the scripts located in “Glitch” and “no_glitch” folders. These sub-scrips run design vision and other modelsim commands such as vlog and vsim. At the moment, they are set to operate in quiet-Gui-less mode. If you wish to see direct wave output, open and edit both the “bash.sh” files in these folders and delete “-c”.