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ECE 474
April 17th, 2020

Questions:

a. Total area = 1463.446 μm^2

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Report : area
Design : alu
Version: L-2016.03-SP2
Date   : Fri Apr 17 17:53:41 2020
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Library(s) Used:

    saed90nm_typ (File: /nfs/guille/a1/cadlibs/synop_lib/SAED_EDK90nm/Digital_Standard_Cell_Library/synopsys/models/saed90nm_typ_pg.db)

Number of ports:                           60
Number of nets:                           198
Number of cells:                          144
Number of combinational cells:            141
Number of sequential cells:                 2
Number of macros/black boxes:               0
Number of buf/inv:                         24
Number of references:                      20

Combinational area:               1372.608000
Buf/Inv area:                      132.720005
Noncombinational area:              22.118000
Macro/Black Box area:                0.000000
Net Interconnect area:              68.720055

Total cell area:                  1394.726000
Total area:                       1463.446055
1
```

b. # of Different Gates Used = 21

```
alu
    AND2X1                     saed90nm_typ
    AND3X1                     saed90nm_typ
    AO221X1                    saed90nm_typ
    AOI222X1                   saed90nm_typ
    INVX0                      saed90nm_typ
    LATCHX1                    saed90nm_typ
    MUX21X1                    saed90nm_typ
    NAND2X0                    saed90nm_typ
    NAND3X0                    saed90nm_typ
    NAND4X0                    saed90nm_typ
    NOR2X0                     saed90nm_typ
    NOR4X0                     saed90nm_typ
    OA21X1                     saed90nm_typ
    OA22X1                     saed90nm_typ
    OAI21X1                    saed90nm_typ
    OAI22X1                    saed90nm_typ
    OR2X1                      saed90nm_typ
    OR4X1                      saed90nm_typ
    XOR2X1                     saed90nm_typ
    alu_DW01_addsub_0
        FADDX1                 saed90nm_typ
        XOR2X1                 saed90nm_typ
        XOR3X1                 saed90nm_typ
```

NOTE: XOR2X1 was listed twice, so I counted it as one

c. NAND2X1 = $5.5296\ \mu m^2$

Number of cells (gates) = $\frac{Total\ Area}{NAND\ Gate\ Area}$ = $\frac{1463.446\ \mu m^2}{5.5296\ \mu m^2}$ = 265

d. After running the report_hierarchy command, I was able to notice that the other block added is alu_DW01_addsub_0. This appears to be another alu, and was implemented because it noticed my design had add/sub capability. Based on my generated schematic, they're configured to be in series from one another.

e. The longest delay starts from the external input to data output. It's delay value is 2.58

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Design : alu
Version: L-2016.03-SP2
Date   : Fri Apr 17 18:11:40 2020
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Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

  Startpoint: opcode[1] (input port)
  Endpoint: alu_zero (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  alu                8000                  saed90nm_typ
  alu_DW01_addsub_0  8000                  saed90nm_typ

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  opcode[1] (in)                           0.00       0.00 r
  U239/QN (INVX0)                          0.03       0.03 f
  U238/QN (NAND2X0)                        0.12       0.14 r
  U211/QN (NAND2X0)                        0.56       0.71 f
  r32/ADD_SUB (alu_DW01_addsub_0)          0.00       0.71 f
  r32/U8/Q (XOR2X1)                        0.24       0.94 r
  r32/U1_0/CO (FADDX1)                     0.15       1.09 r
  r32/U1_1/CO (FADDX1)                     0.14       1.23 r
  r32/U1_2/CO (FADDX1)                     0.13       1.36 r
  r32/U1_3/CO (FADDX1)                     0.13       1.49 r
  r32/U1_4/CO (FADDX1)                     0.13       1.62 r
  r32/U1_5/CO (FADDX1)                     0.13       1.75 r
  r32/U1_6/CO (FADDX1)                     0.13       1.89 r
  r32/U1_7/S (FADDX1)                      0.20       2.08 f
  r32/SUM[7] (alu_DW01_addsub_0)           0.00       2.08 f
  U205/QN (AOI222X1)                       0.23       2.32 r
  U207/QN (NAND2X0)                        0.08       2.40 f
  U210/Q (OR4X1)                           0.14       2.54 f
  U208/QN (NOR2X0)                         0.04       2.58 r
  alu_zero (out)                           0.00       2.58 r
  data arrival time                                   2.58
  -----------------------------------------------------------
  (Path is unconstrained)
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Server Issues: My issues included .modelsimlock. I couldn't do anything and had to wait a whole night for it to work.

Assignment Issues: The hardest part of this assignment was detecting X values and flagging when I had to. For a solution, I always checked for a change in the output and ran if statements to check what flags should be triggered.