

TM60N03DF
N-Channel Enhancement Mosfet
General Description

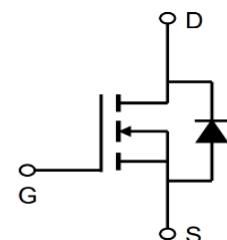
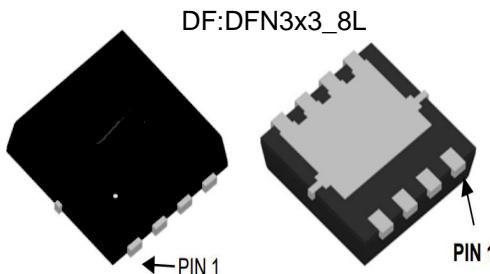
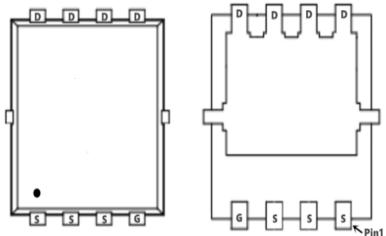
- Low R_{DS(ON)}
- RoHS and Halogen-Free Compliant

Applications

- Load switch
- PWM

General Features

$V_{DS} = 30V$ $I_D = 60A$
 $R_{DS(ON)} = 4.7m\Omega$ (typ.) @ $V_{GS}=10V$
 100% UIS Tested
 100% R_g Tested



Marking: 60N03

Absolute Maximum Ratings ($T_A = 25^\circ C$ Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	60	A
$I_D@T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	30	A
I_{DM}	Pulsed Drain Current ²	160	A
EAS	Single Pulse Avalanche Energy ³	58	mJ
I_{AS}	Avalanche Current	60	A
$P_D@T_c=25^\circ C$	Total Power Dissipation ⁴	25	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	30	---	---	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	---	4.7	6.0	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=10\text{A}$	---	6.5	9	
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	1.2	---	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=24\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=24\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_D=30\text{A}$	---	43	---	S
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=4.5\text{V}$, $I_D=15\text{A}$	---	34	---	nC
Q_{gs}	Gate-Source Charge		---	6	---	
Q_{gd}	Gate-Drain Charge		---	9	---	
$T_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DD}}=15\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$ $I_D=15\text{A}$	---	8.5	---	ns
T_r	Rise Time		---	103	---	
$T_{\text{d}(\text{off})}$	Turn-Off Delay Time		---	37.3	---	
T_f	Fall Time		---	105	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1600	---	pF
C_{oss}	Output Capacitance		---	245	---	
C_{rss}	Reverse Transfer Capacitance		---	215	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,6}	$V_G=V_D=0\text{V}$, Force Current	---	---	60	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	140	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=25\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=48\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Performance Characteristics

Figure 1: Output Characteristics

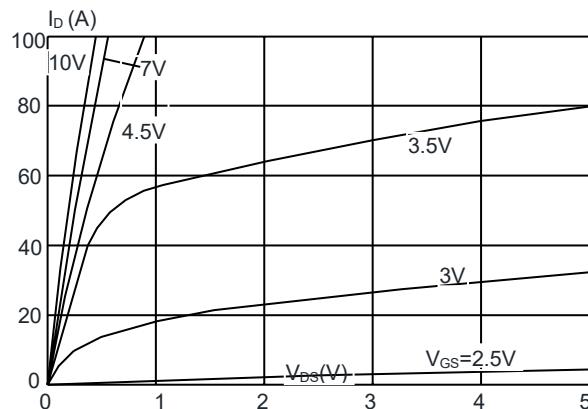


Figure 3: On-resistance vs. Drain Current

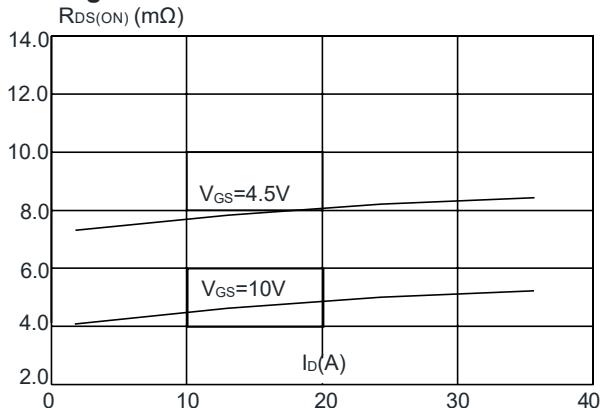


Figure 5: Gate Charge Characteristics

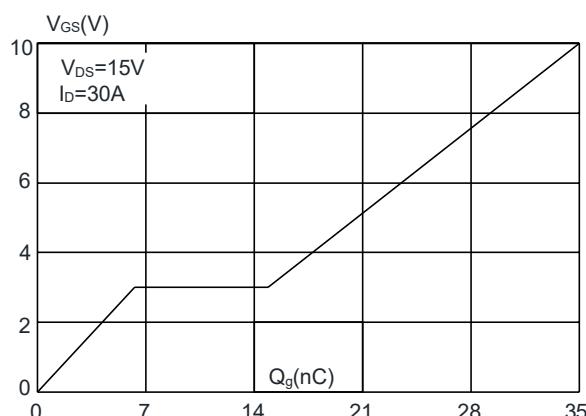


Figure 2: Typical Transfer Characteristics

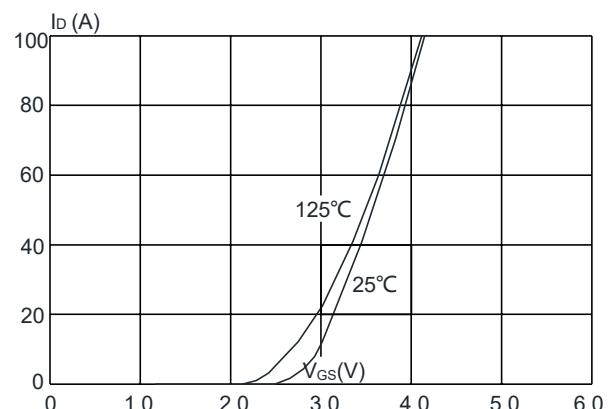


Figure 4: Body Diode Characteristics

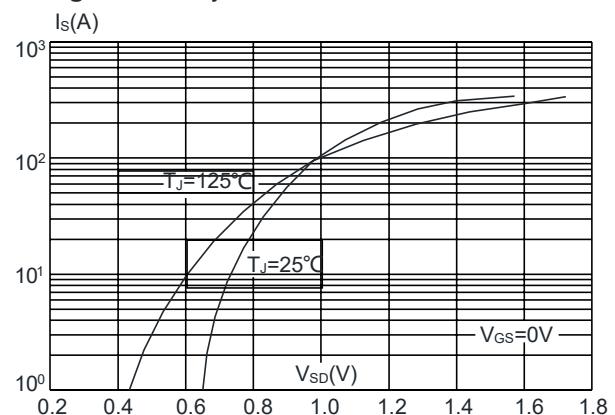
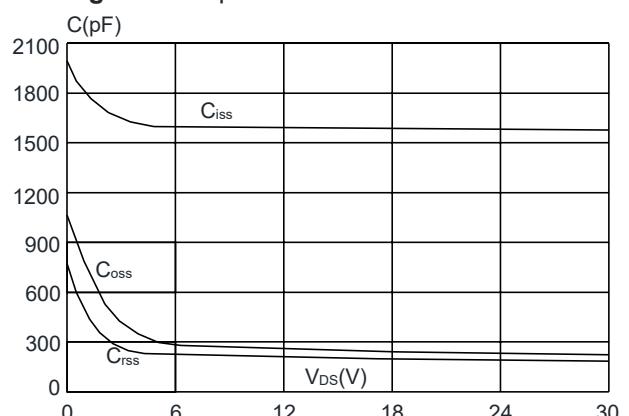


Figure 6: Capacitance Characteristics



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Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

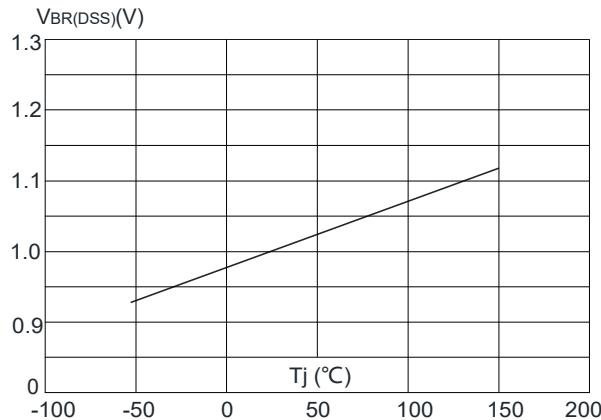


Figure 8: Normalized on Resistance vs. Junction Temperature

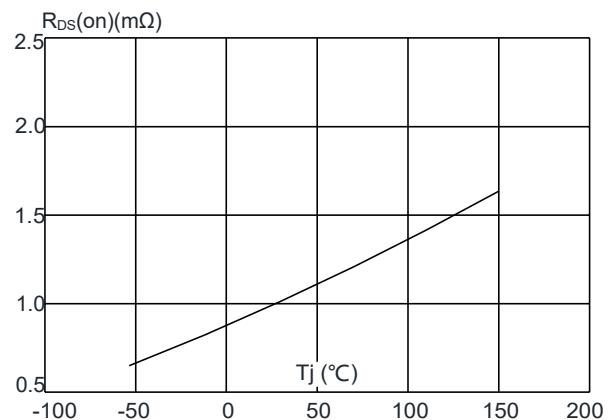


Figure 9: Maximum Safe Operating Area

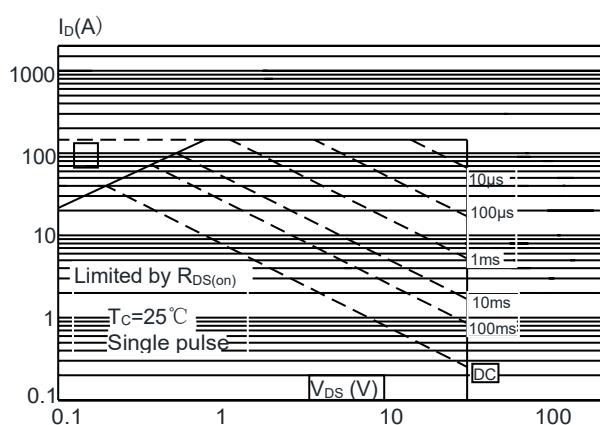


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

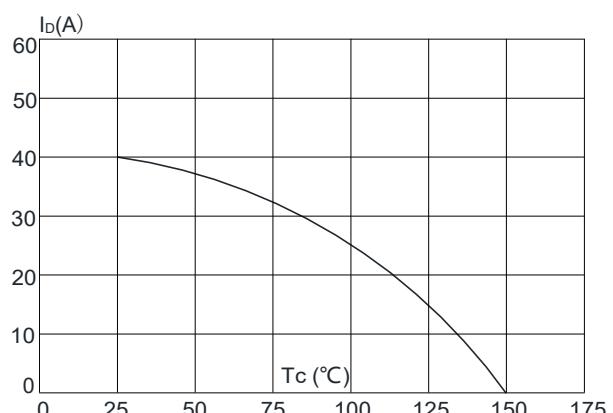
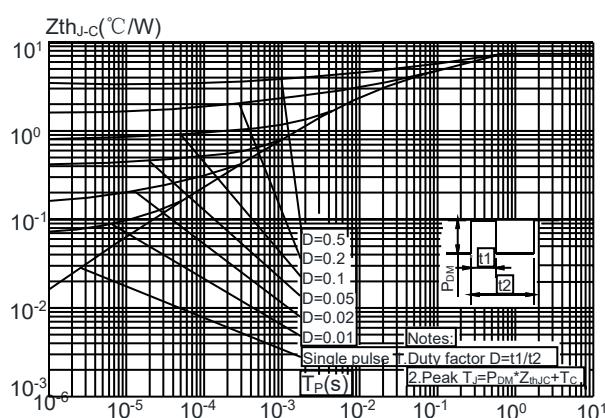


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

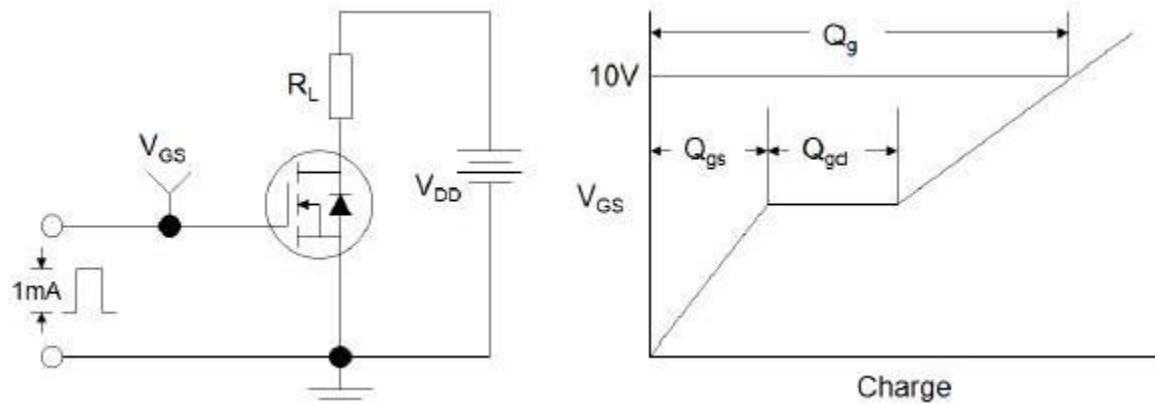


Figure 1: Gate Charge Test Circuit & Waveform

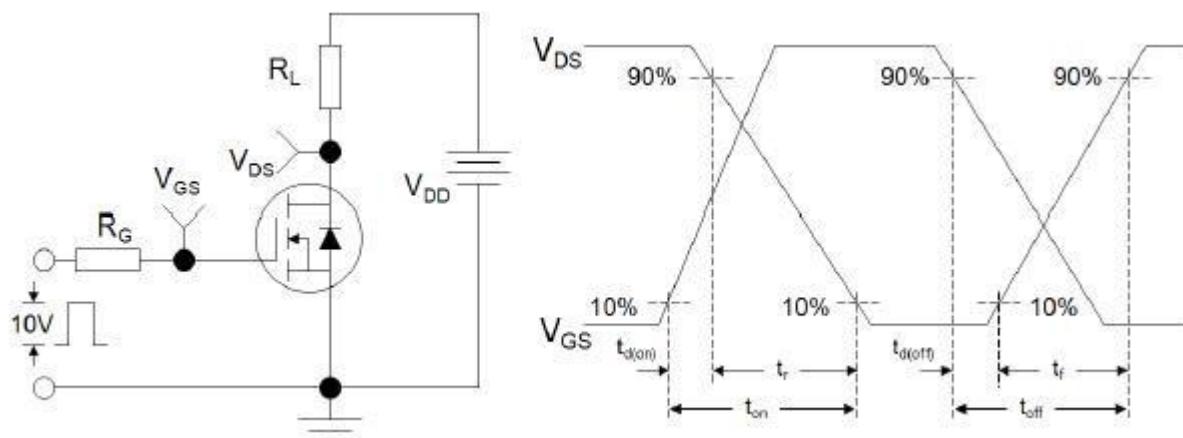


Figure 2: Resistive Switching Test Circuit & Waveforms

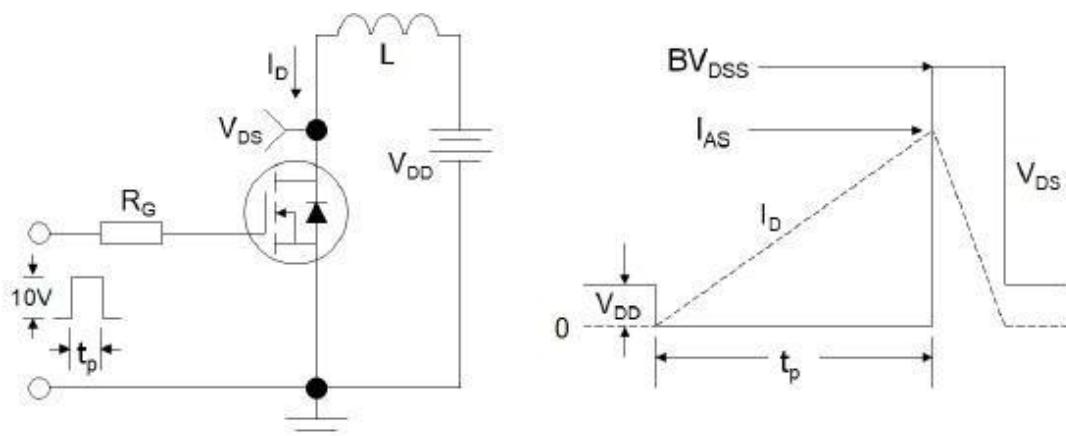
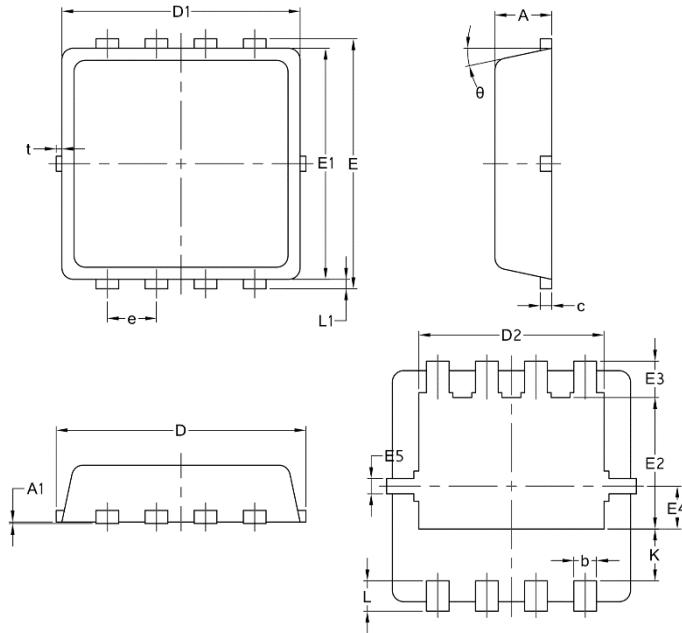


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms

Package Mechanical Data: DFN3x3-8L



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14