



CY74FCT16244T/2244T CY74FCT16444T/2H244T

16 Bit Buffers/Line Drivers

Features

- Low power, pin-compatible replacement for ABT functions
- FCT-E speed at 3.2 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5V \pm 10\%$

CY74FCT16244T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^{\circ}\text{C}$

CY74FCT162244T Features:

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5V$, $T_A = 25^{\circ}\text{C}$

CY74FCT16444T Features:

- 64 mA sink current, 32 mA source current
- Reduced system loading

CY74FCT162H244T Features:

- Bus hold on data inputs
- Eliminates the need for external pull-up or pull-down resistors

Functional Description

These 16-bit buffers/line drivers are designed for use in memory driver, clock driver, or other bus interface applications, where high-speed and low power are required. With flow-through pinout and small shrink packaging board layout is simplified. The three-state controls are designed to allow 4-bit, 8-bit or combined 16-bit operation. The outputs are designed with a power-off disable feature to allow for live insertion of boards.

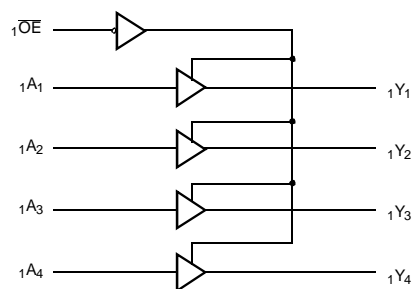
The CY74FCT16244T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162244T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162244T is ideal for driving transmission lines.

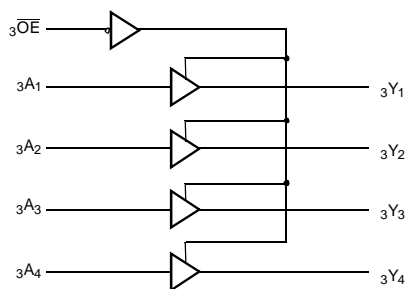
The CY74FCT16444 is designed for 16-bit operation, reducing control lines from four \overline{OE} to one \overline{OE} to reduce input loading.

The CY74FCT162H244T is a 24-mA balanced output part that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

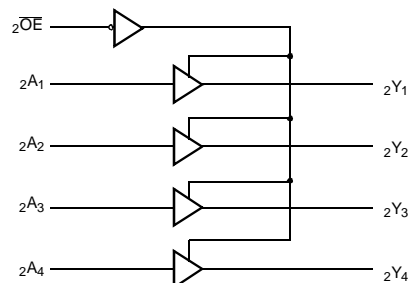
Logic Block Diagrams CY74FCT16244T, CY74FCT162244T, CY74FCT162H244T



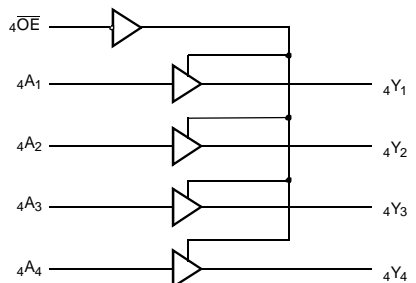
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FCT16244-2



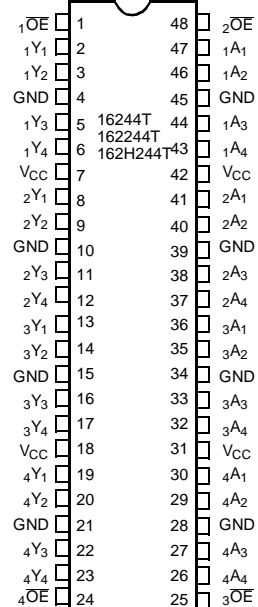
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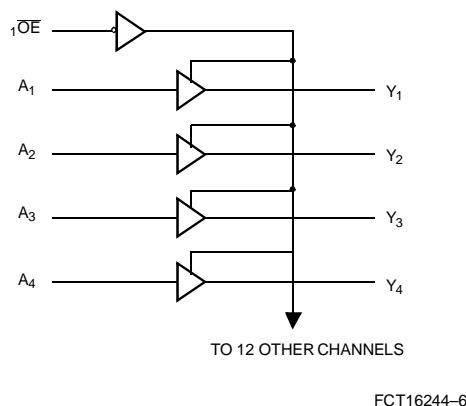
Pin Configuration

SSOP/TSSOP Top View

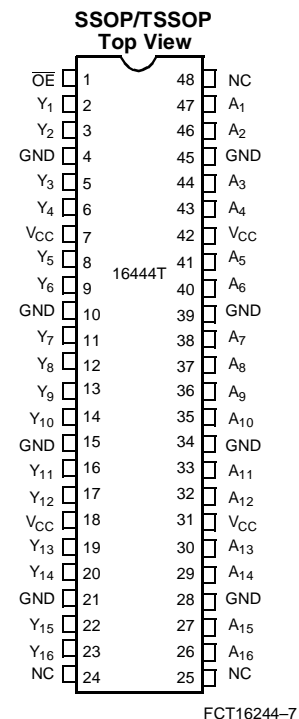


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Logic Block Diagram CY74FCT16444T



Pin Configuration



Pin Description

Name	Description
\overline{OE}	Three-State Output Enable Inputs (Active LOW)
A	Data Inputs ^[1]
Y	Three-State Outputs

Function Table^[2]

Inputs		Outputs
\overline{OE}	A	Y
L	L	L
L	H	H
H	X	Z

Maximum Ratings^[3,4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... -55°C to +125°C

Ambient Temperature with
Power Applied -55°C to +125°C

DC Input Voltage -0.5V to +7.0V

DC Output Voltage -0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) -60 to +120 mA

Power Dissipation..... 1.0W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Ordering Range

Range	Ambient Temperature	V _{CC}
Commercial	- 40°C to +85°C	5V ± 10%

Notes:

- On CY74FCT162H244T these pins have "bus hold."
- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[6]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	Standard	V _{CC} =Max., V _I =V _{CC}		±1	μA
		Bus Hold			±100	
I _{IL}	Input LOW Current	Standard	V _{CC} =Max., V _I =GND		±1	μA
		Bus Hold			±100	
I _{BBH} I _{BBL}	Bus Hold Sustain Current on Bus Hold Input ^[7]	V _{CC} =Min. V _I =2.0V V _I =0.8V	-50 +50			μA
I _{BHHO} I _{BHLO}	Bus Hold Overdrive Current on Bus Hold Input ^[7]	V _{CC} =Max., V _I =1.5V			TBD	mA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[8]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[8]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V ^[9]			±1	μA

Output Drive Characteristics for CY74FCT16244T, CY74FCT16444T

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162244T, CY74FCT162H244T

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
I _{ODL}	Output LOW Current ^[8]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[8]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Notes:

- Typical values are at V_{CC}=5.0V, T_A = +25°C ambient.
- This parameter is guaranteed but not tested.
- Pins with bus hold are described in Pin Description.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Tested at +25°C.



Capacitance^[6] ($T_A = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	4.5	6.0	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \leq 0.2\text{V}$, $V_{IN} \leq V_{CC} - 0.2\text{V}$	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}$ ^[10]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ^[11]	$V_{CC} = \text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = \text{GND}$ $V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	60	100	$\mu\text{A}/\text{MHz}$
I_C	Total Power Supply Current ^[12]	$V_{CC} = \text{Max.}$, $f_1 = 10\text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE} = \text{GND}$ $V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	0.6	1.5	mA
		$V_{IN} = 3.4\text{V}$ or $V_{IN} = \text{GND}$	0.9	2.3	mA
		$V_{CC} = \text{Max.}$, $f_1 = 2.5\text{ MHz}$, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE} = \text{GND}$ $V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	2.4	4.5 ^[13]	mA
		$V_{IN} = 3.4\text{V}$ or $V_{IN} = \text{GND}$	6.4	16.5 ^[13]	mA

Notes:

10. Per TTL driven input ($V_{IN} = 3.4\text{V}$); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 I_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4\text{V}$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Switching Characteristics Over the Operating Range^[14]

Parameter	Description	CY74FCT16244T CY74FCT162244T CY74FCT16444T CY74FCT162H244T		CY74FCT16244AT CY74FCT162244AT CY74FCT16444AT CY74FCT162H244AT		Unit	Fig. No. ^[15]
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	1.5	6.5	1.5	4.8	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	8.0	1.5	6.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	7.0	1.5	5.6	ns	1, 7, 8
t _{SK(O)}	Output Skew ^[16]		0.5		0.5	ns	—

Switching Characteristics Over the Operating Range^[14] (continued)

Parameter	Description	CY74FCT16244CT CY74FCT162244CT CY74FCT16444CT CY74FCT162H244CT		CY74FCT16244ET CY74FCT162244ET CY74FCT162H244ET		Unit	Fig. No. ^[15]
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	1.5	4.1	1.5	3.2	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	5.8	1.5	4.4	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.2	1.5	3.6	ns	1, 7, 8
t _{SK(O)}	Output Skew ^[16]		0.5		0.5	ns	—

Notes:

14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information section.
16. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.



Ordering Information CY74FCT16244

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.2	CY74FCT16244ETPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16244ETPVC	O48	48-Lead (300-Mil) SSOP	
4.1	CY74FCT16244CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16244CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT16244ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16244ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16244TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16244TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162244

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.2	CY74FCT162244ETPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162244ETPVC	O48	48-Lead (300-Mil) SSOP	
4.1	CY74FCT162244CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162244CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT162244ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162244ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT162244TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162244TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT16444

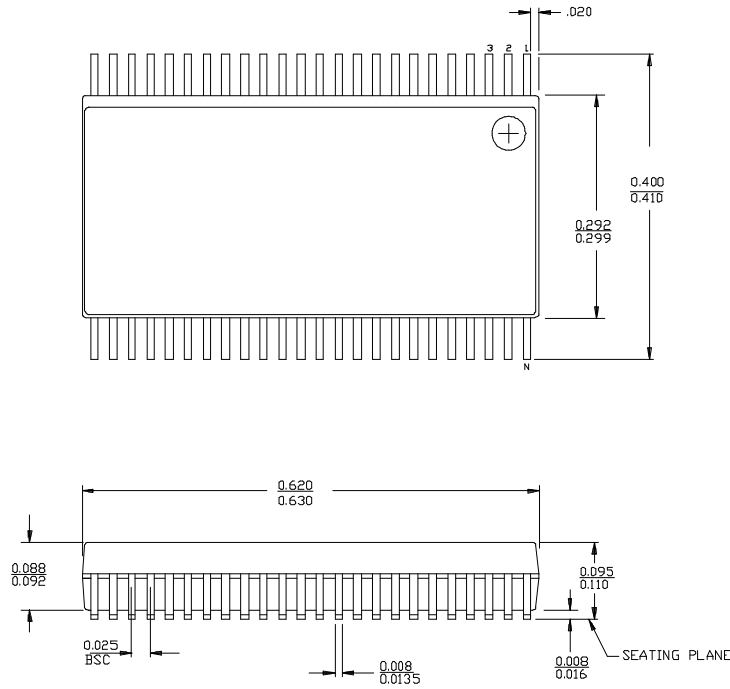
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16444CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16444CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT16444ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16444ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16444TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16444TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H244

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.2	CY74FCT162H244ETPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H244ETPVC	O48	48-Lead (300-Mil) SSOP	
4.1	CY74FCT162H244CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H244CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT162H244ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H244ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT162H244TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H244TPVC	O48	48-Lead (300-Mil) SSOP	

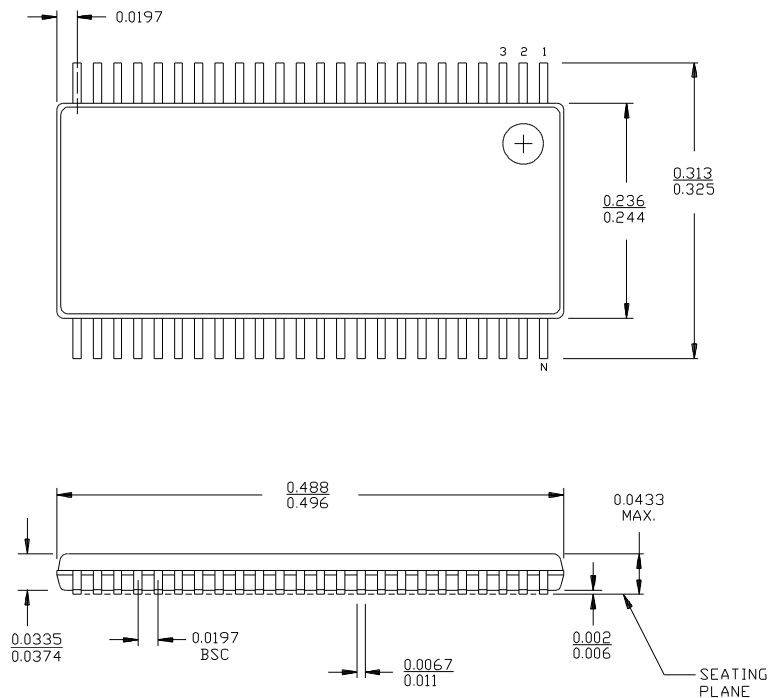
Package Diagrams

48-Lead Shrunk Small Outline Package O48



DIMENSIONS IN INCHES MIN.
MAX.

48-Lead Thin Shrunk Small Outline Package Z48



DIMENSIONS IN INCHES MIN.
MAX.