a)

LUT:

Used: 1

Available: 9312

IOB:

Used: 3

Available: 232

b)

Delay: 5.753ns

c)

RTL View

Viewing an RTL schematic opens an NGR file that can be viewed as a gate-level schematic.

This schematic is generated after the HDL synthesis phase of the synthesis process. It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device.

Technology View

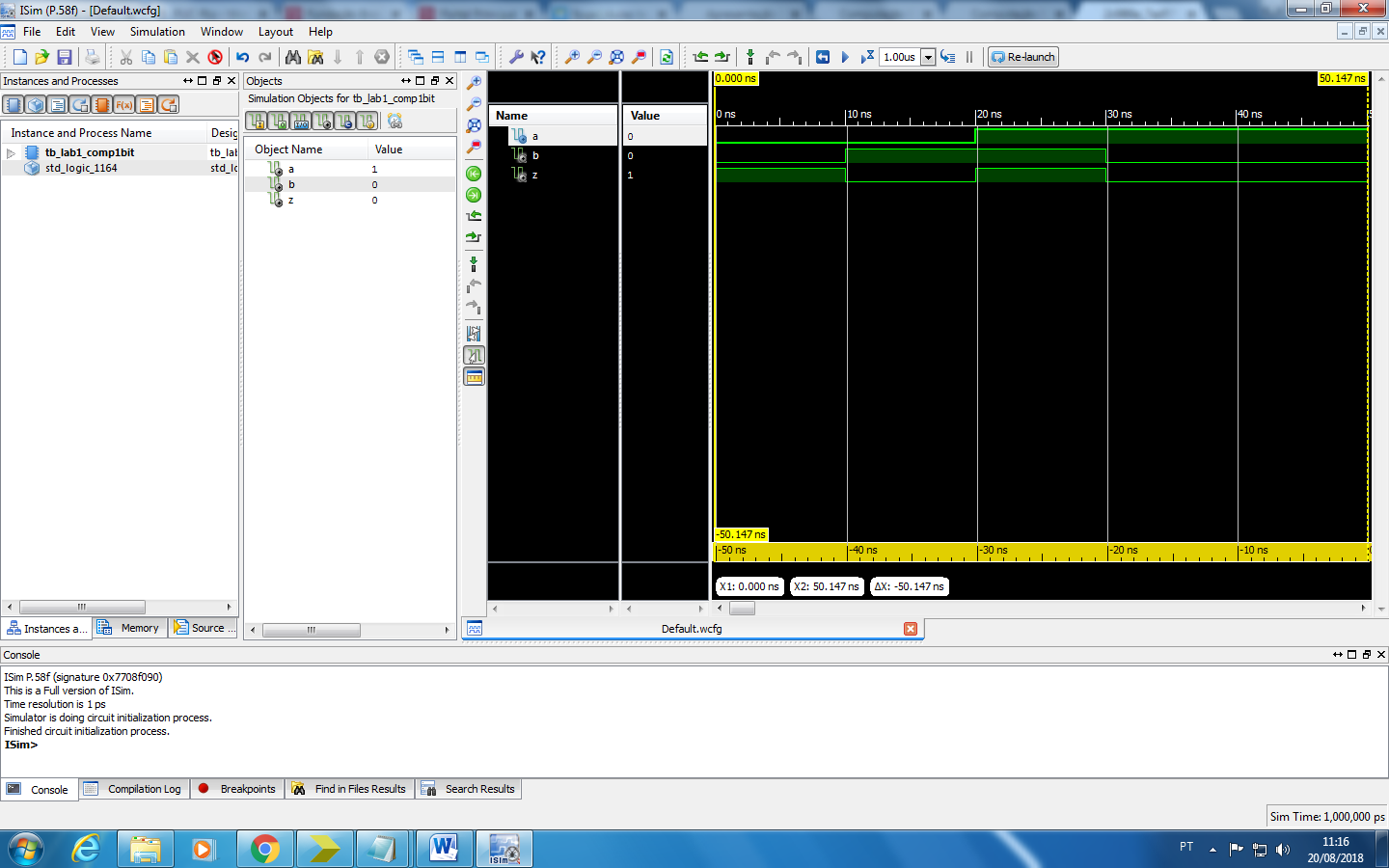
Viewing a Technology schematic opens an NGC file that can be viewed as an architecture-specific schematic.

This schematic is generated after the optimization and technology targeting phase of the synthesis process. It shows a representation of the design in terms of logic elements optimized to the target Xilinx device or "technology"; for example, in terms of of LUTs, carry logic, I/O buffers, and other technology-specific components. Viewing this schematic allows you to see a technology-level representation of your HDL optimized for a specific Xilinx architecture, which might help you discover design issues early in the design process.

You should always refer to technology schematic for synthesized result.

To disable RTL schematic generation to speed up synthesis, you can set XST property Generate RTL Schematic (-rtlview) to "No".

c)



A simulação do comparador funciona corretamente e, como foi demonstrado na imagem acima, não apresenta atraso significativo na saída.

3)

z <= S1 or S2;

S2 <= (not a and not b);

S1 <= (a and b);

Nenhuma diferença foi detectada, como esperado.

6)