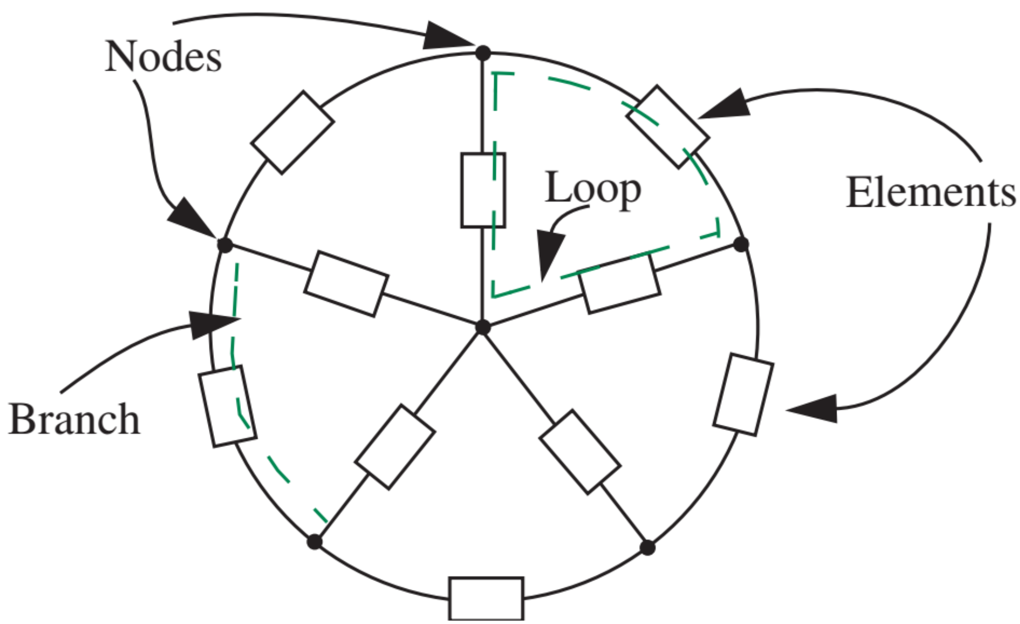
Lecture 2
Basic Laws & Circuit Analysis

Outline

- Terminology: Branches, Nodes, and Loops
- Kirchhoff's Laws
  - KCL
  - KVL
- Circuit Analysis
  - Nodal Analysis
  - Mesh Analysis

Terminology: Branches, Nodes, and Loops

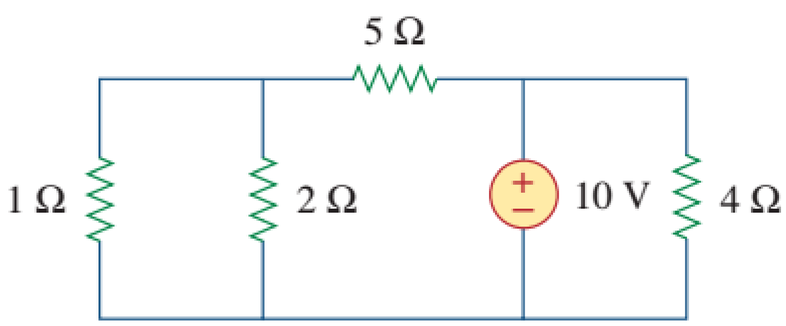
- **Branch**: represents a single element;
- **Node**: a point of connection between two or more branches;
- **Loop**: **Any** closed path in a circuit.



[Source: MIT]

Loop, Independent Loop, Mesh

- A loop is a closed path with no node passed more than once.
- A loop is independent if it contains at least one branch which is not a part of any other independent loop.
- A mesh is a loop that does not contain any other loop within it.

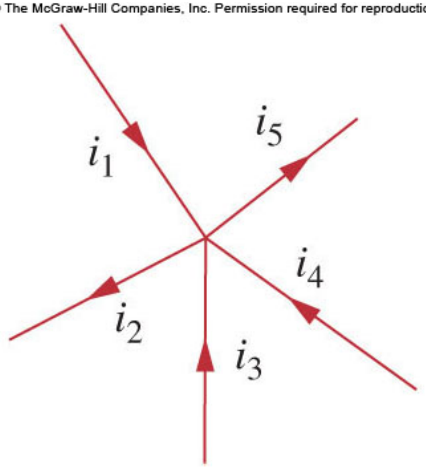


- b – number of branches
- n – number of nodes
- l_{ind} – number of ind. loops

$$l_{ind} = b - (n - 1)$$

Kirchhoff's Laws

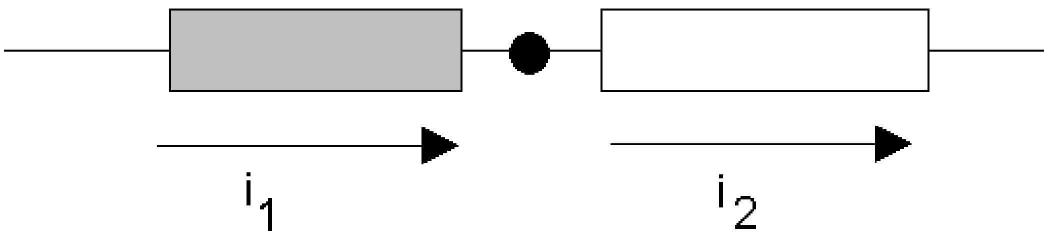
- Kirchhoff's Current Law (KCL):
  - The algebraic sum of all the **currents** entering any **node** in a circuit equals zero.
  - Why?



Gustav Robert Kirchhoff
1824-1887

A Major Implication of KCL

- KCL tells us that **all of the elements that are connected *in series* carry the same current**.

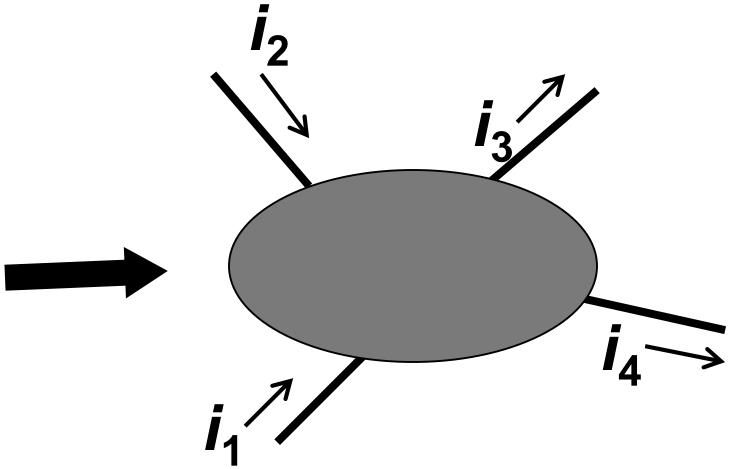


Current entering node = Current leaving node

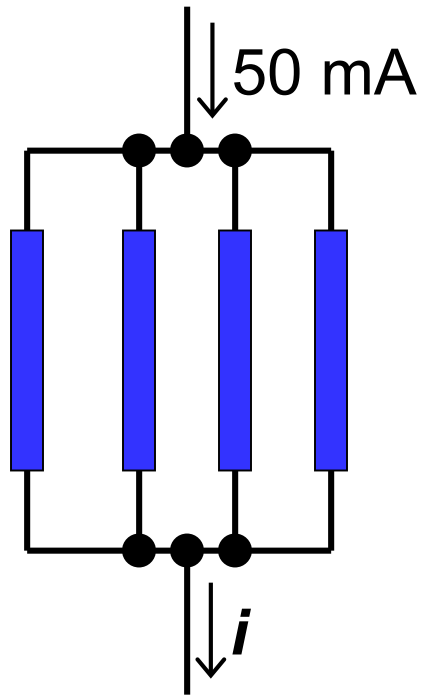
Generalization of KCL

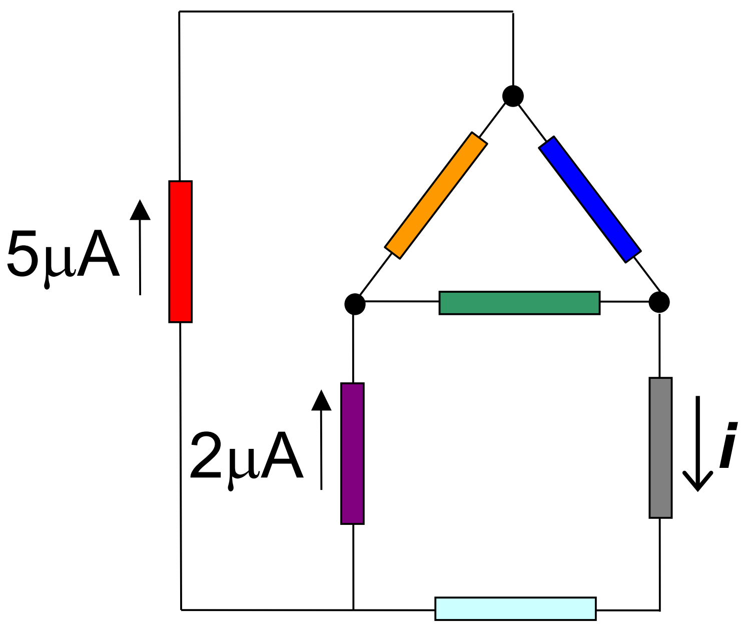
- The sum of currents entering/leaving a **closed surface** is zero.
  - Circuit branches can be inside this surface, *i.e.* the surface can enclose more than one node!

This could be a big chunk of a circuit, *e.g.* a "black box"

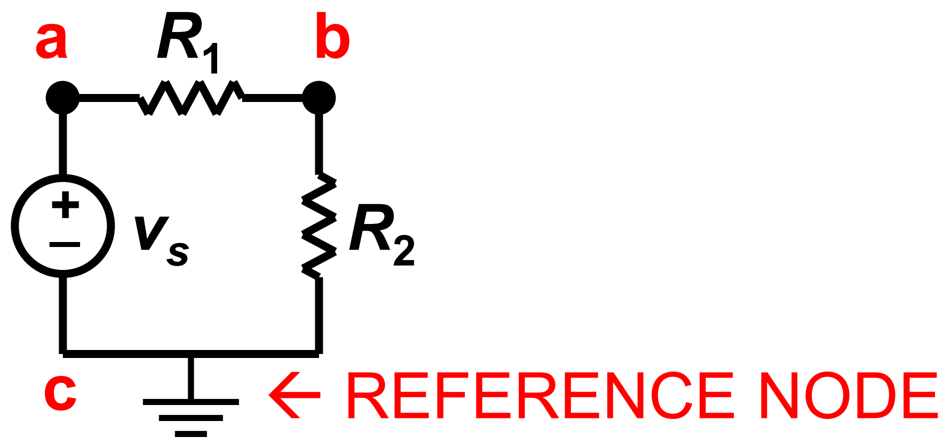


Generalized KCL Examples





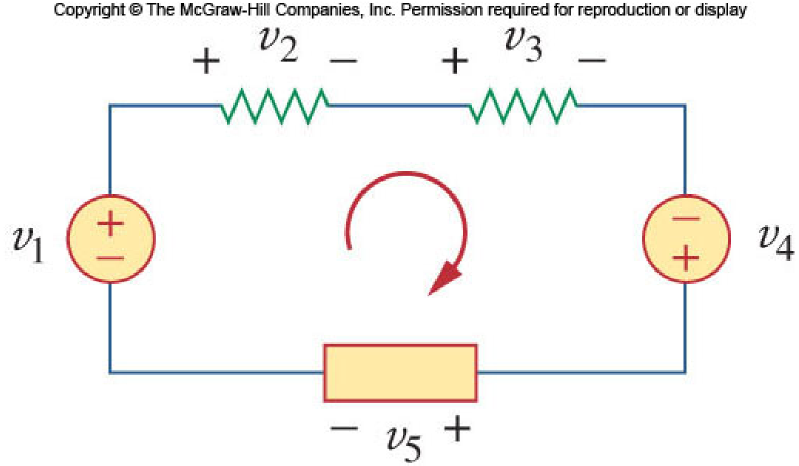
Notation: Node and Branch Voltages



- Use one node as the reference (the "common" or "ground" node) – label it with a symbol.
- The voltage drop from node $\boldsymbol{x}$ to the reference node is called the **node voltage** $\boldsymbol{V_x}$.
- The voltage across a circuit element is defined as the difference between the node voltages at its terminals.

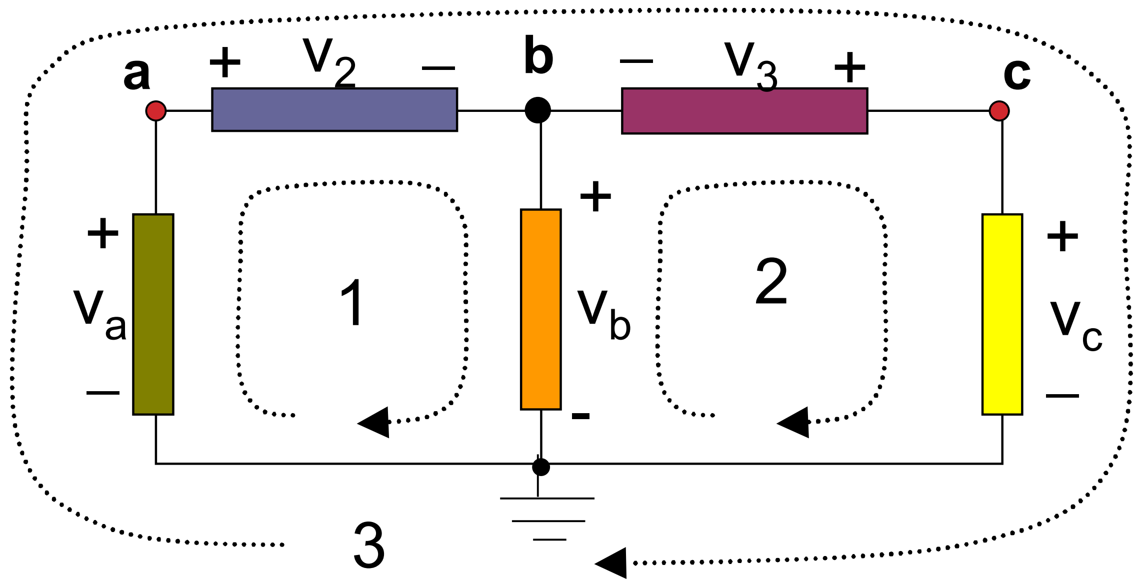
Kirchhoff's Voltage Law (KVL)

- The algebraic sum of all the **voltages** around any **loop** in a circuit equals zero.
- Why?



KVL Example

Three closed paths:



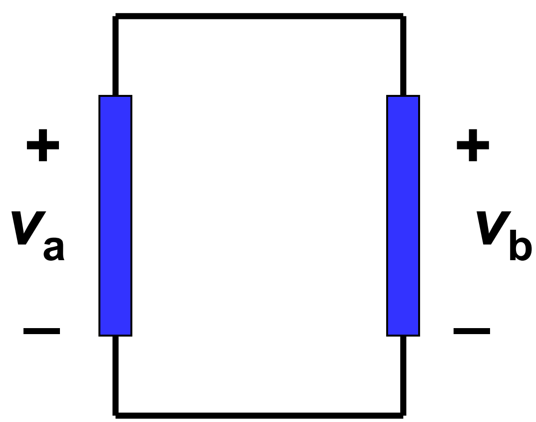
Path 1:

Path 2:

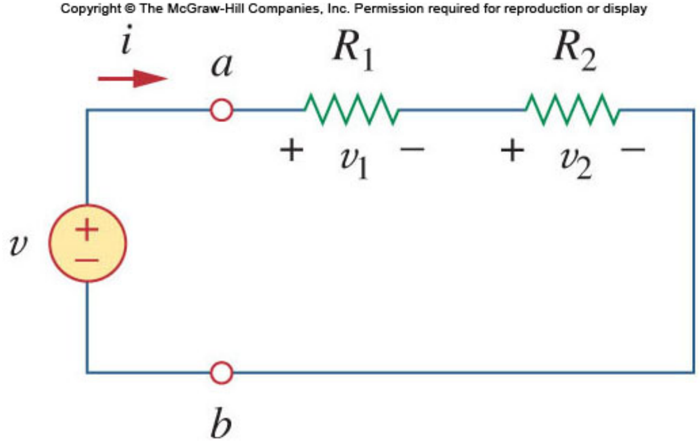
Path 3:

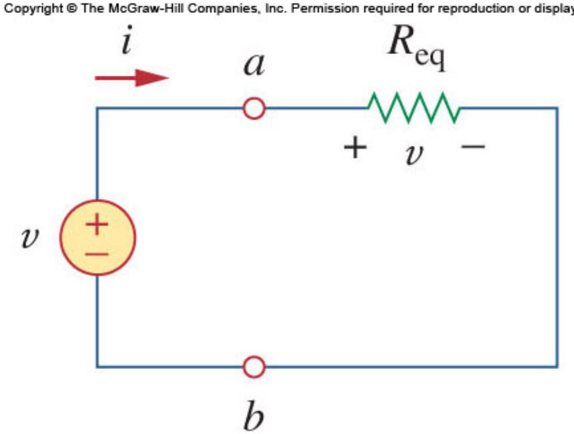
A Major Implication of KVL

- KVL tells us that **any set of elements which are connected at both ends carry the same voltage**.
- We say these elements are connected **in parallel**.



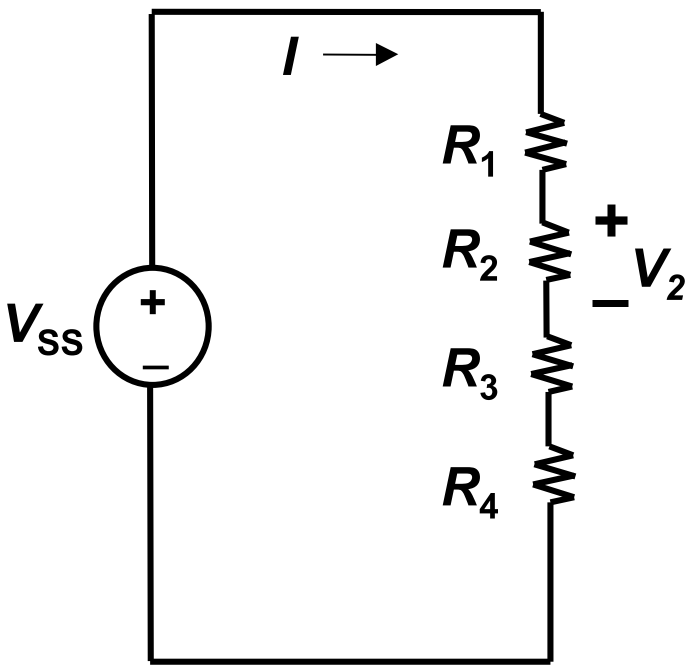
Voltage Division

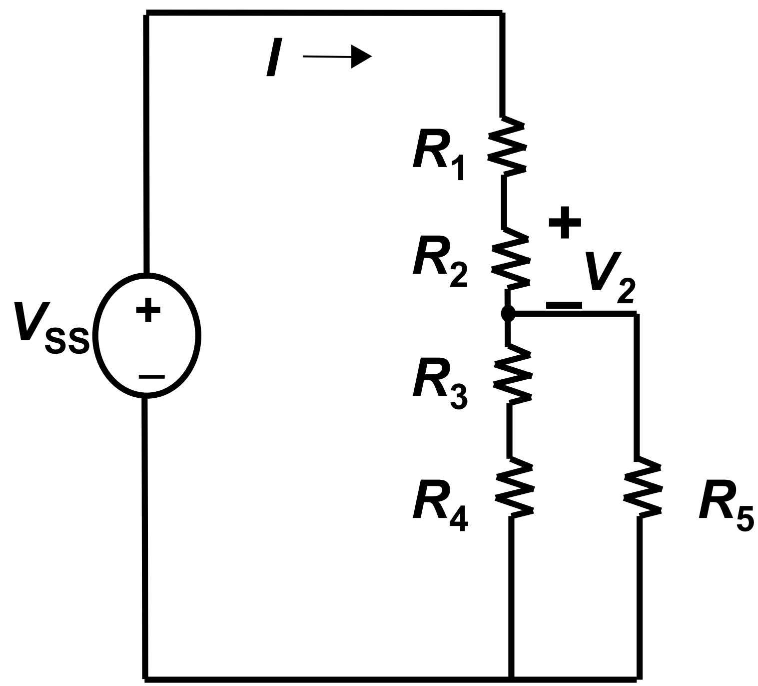




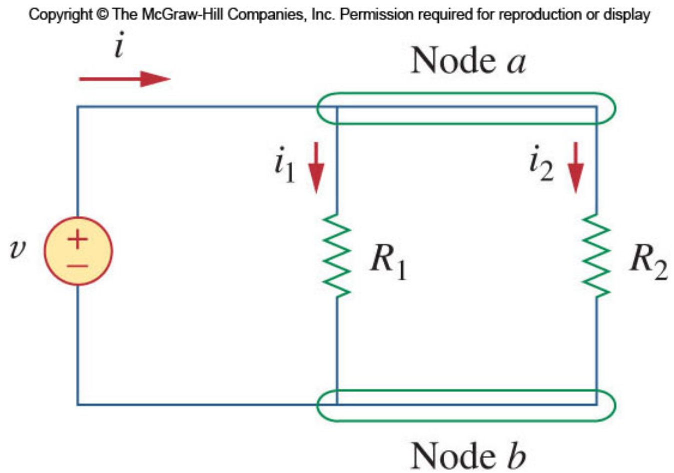
Three-terminal rheostat

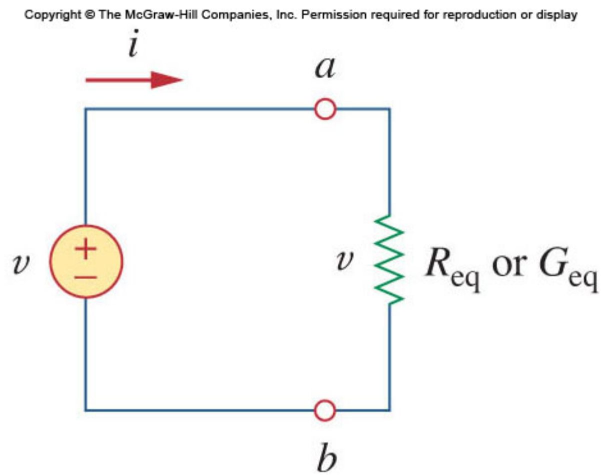
Voltage Divider





Parallel Resistors/Current Division

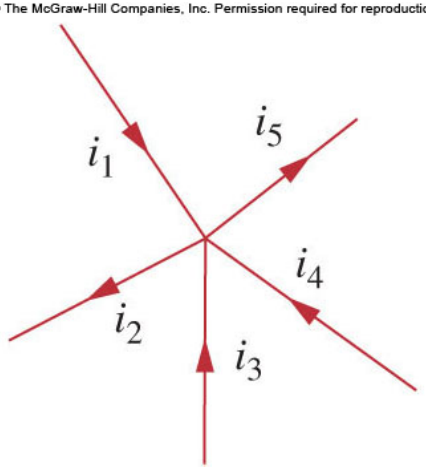


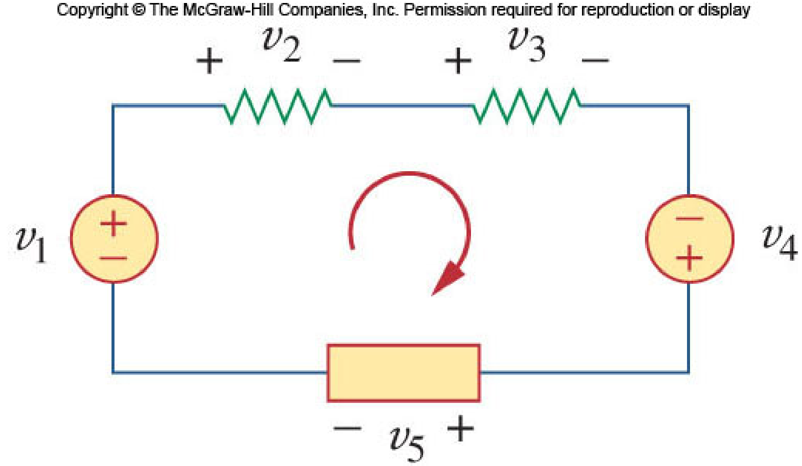


Summary

- KCL and KVL

$$\sum_{n=1}^{N} i_n = 0 \qquad\qquad \sum_{m=1}^{M} v_m = 0$$





Circuit Analysis

- Two techniques will be presented in this part:
  - Nodal analysis, which is based on **KCL**
    - Used in SPICE, the internal engine of circuit simulators.
  - Mesh analysis, which is based on **KVL**

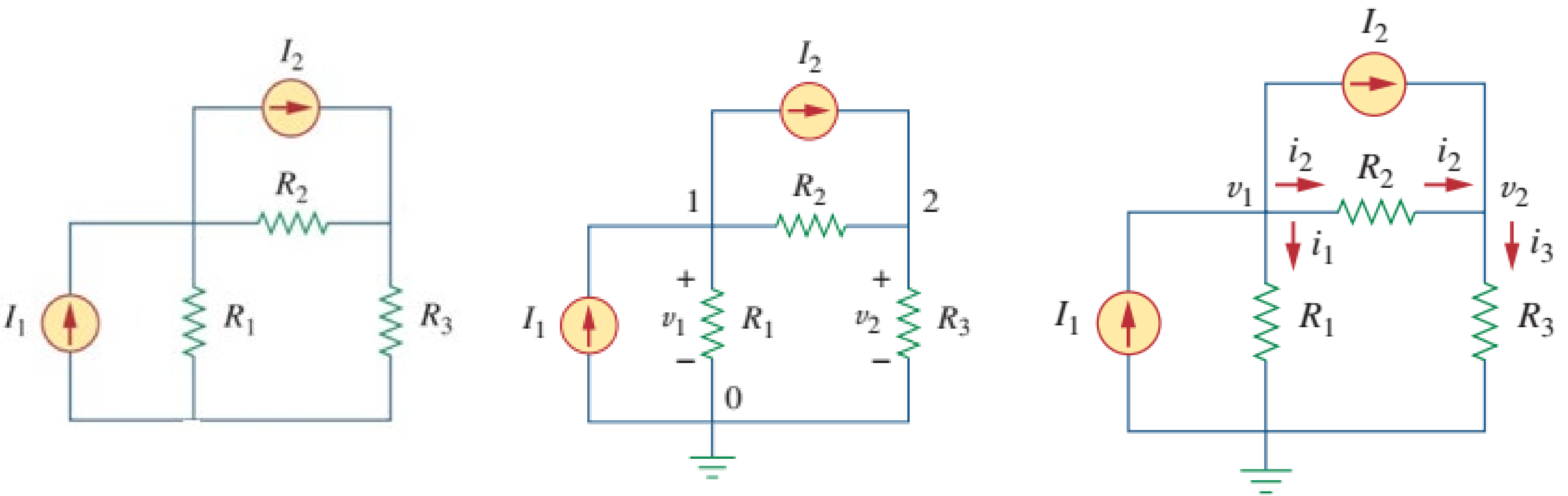
- The analysis will result in a set of simultaneous equations

http://bwrcs.eecs.berkeley.edu/Classes/IcBook/SPICE/
http://www.ni.com/white-paper/5413/zhs/

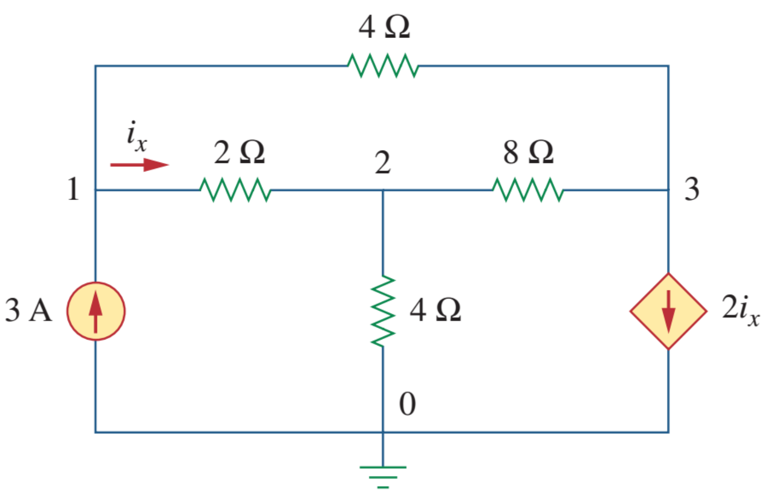
Nodal Analysis – Three Steps

- Given a circuit with *n* nodes, the nodal analysis is accomplished via three steps:
  1. Select a node as the reference (i.e., ground) node. Assign the node voltages to the remaining ***(n-1)*** nodes. Voltages are relative to the reference node.
  2. Apply KCL to the ***(n-1)*** nodes, expressing branch current in terms of the node voltages (using the *I*-*V* relationships of branch elements).
  3. Solve the resulting simultaneous equations to obtain the unknown node voltages.

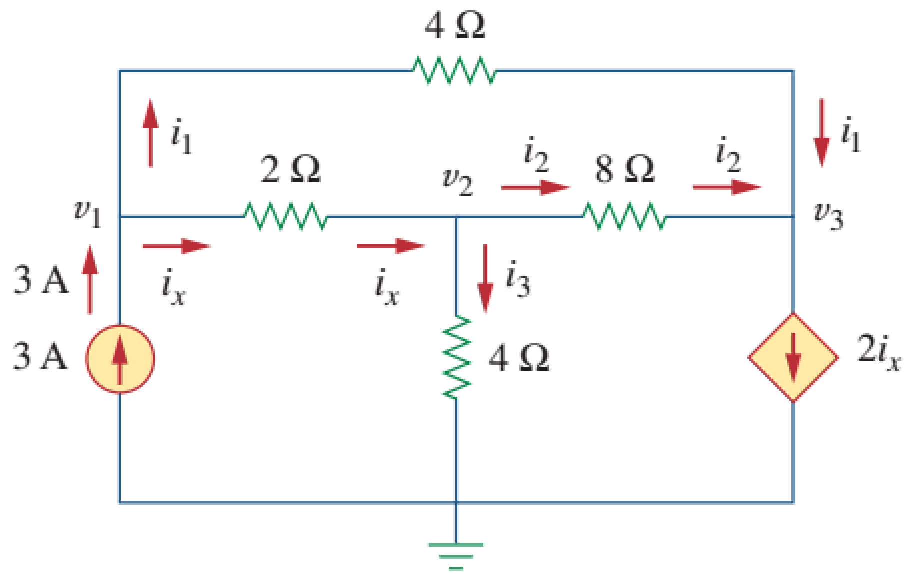
Nodal Analysis Example #1



Nodal Analysis: Example #2

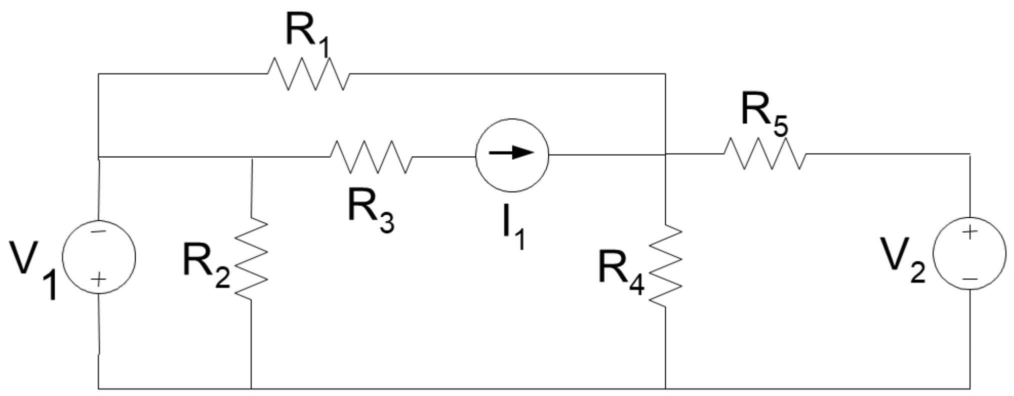


(a)



Nodal Analysis with Voltage Sources

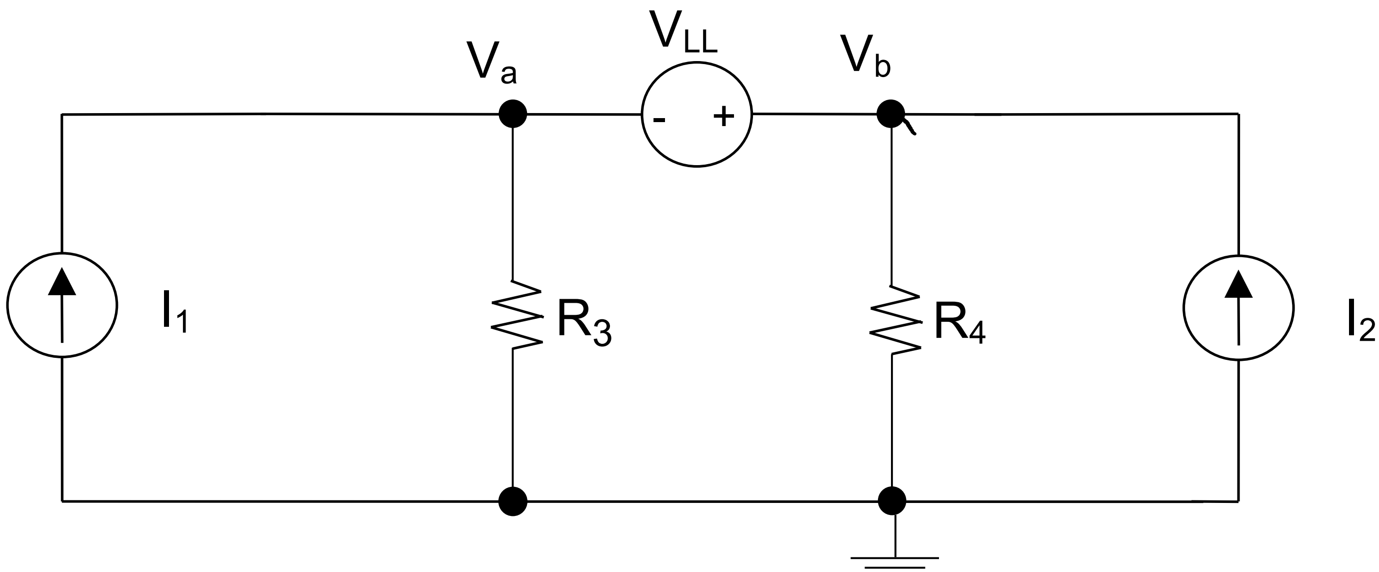
Case I:



Nodal Analysis: Supernode

Case II

A "floating" voltage source is one for which neither side is connected to the reference node, e.g. V_{LL} in the circuit below:

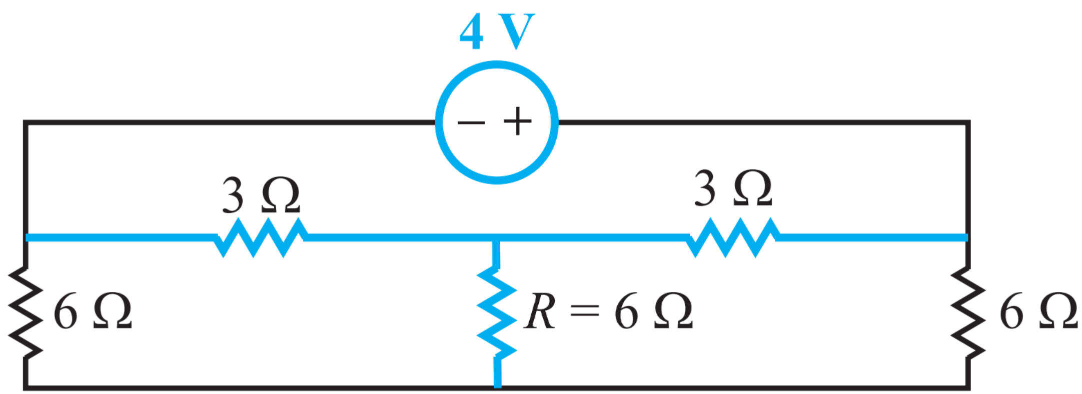


A supernode is formed by enclosing a (dependent or independent) voltage source connected between two nonreference nodes and any elements connected in parallel with it.

[Source: Berkeley]

Exercise

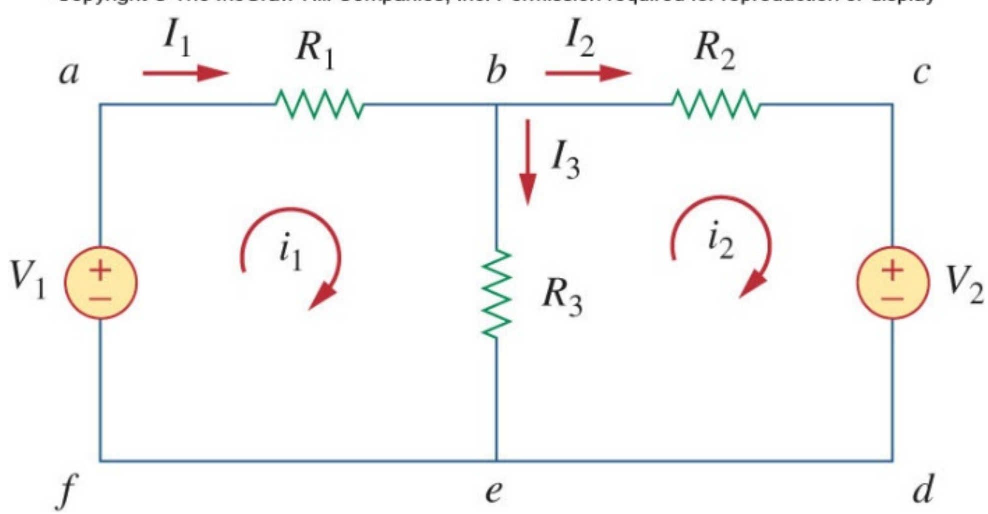
- Find the power supplied by the voltage source.



[Source: Berkeley]

Mesh Analysis

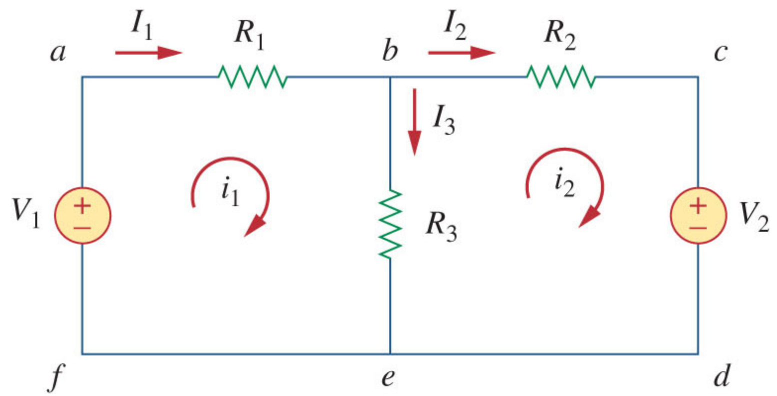
- Another general procedure for analyzing circuits is to use the mesh currents as the circuit variables.



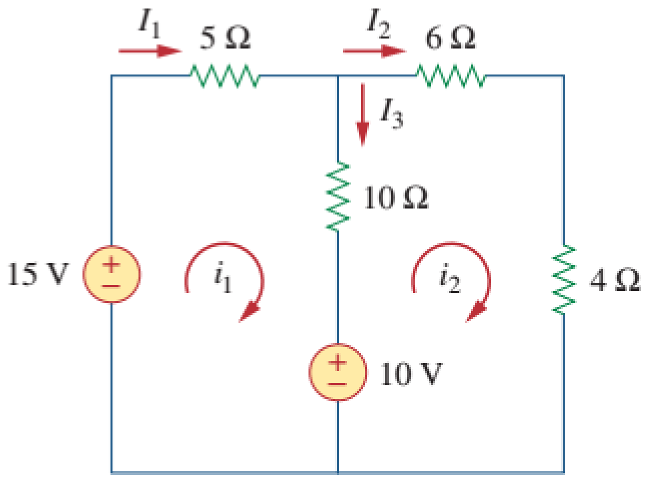
- Mesh analysis uses KVL to find unknown currents.

Mesh Analysis Steps

- Mesh analysis follows these steps:
  1. Assign mesh currents $i_1, i_2, \ldots i_x$ to the x meshes
  2. Apply KVL to each of the x mesh currents.
  3. Solve the resulting x simultaneous equations to get the mesh currents.

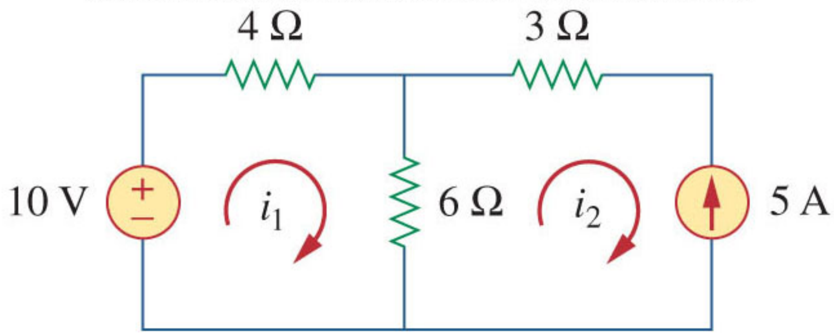


Example

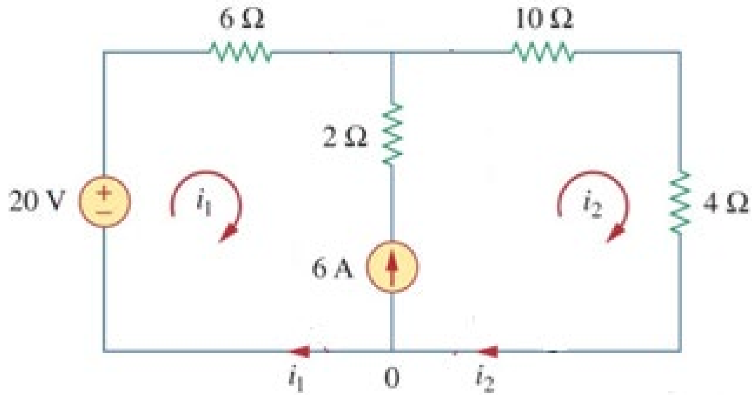


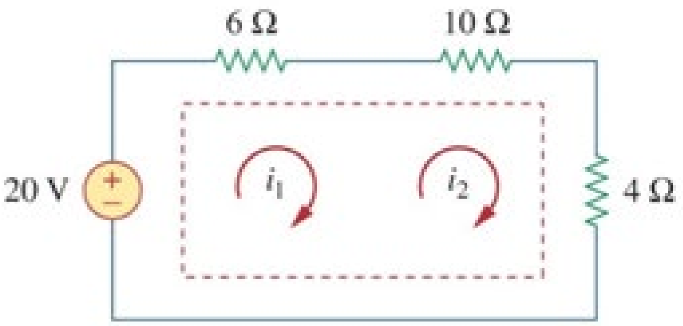
Mesh Analysis with Current Sources

- The presence of a current source makes the mesh analysis simpler in that it reduces the number of equations.
  - If the current source is located on only one mesh, the current for that mesh is defined by the source. For example:



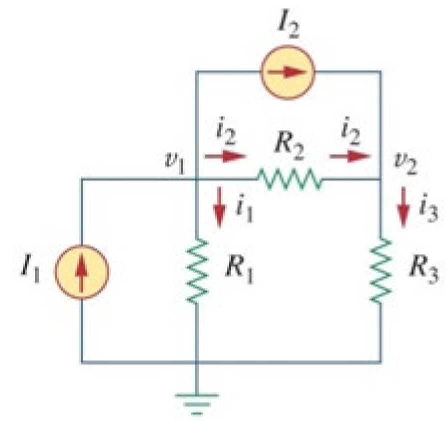
Supermesh



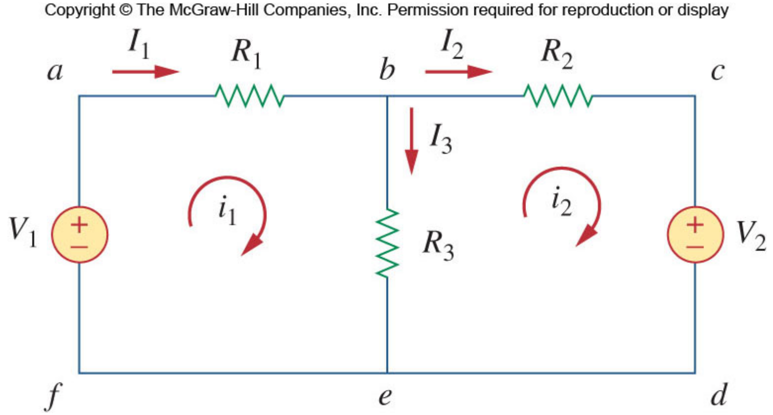


Summary

- Node Analysis
  - Node voltage is the unknown
  - Solve by KCL
  - Special case: Floating voltage source

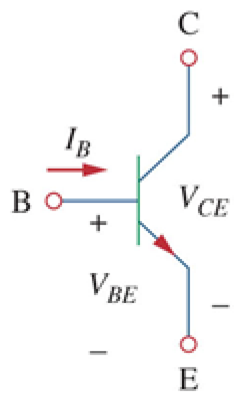


- Mesh Analysis
  - Loop current is the unknown
  - Solve by KVL
  - Special case: Current source

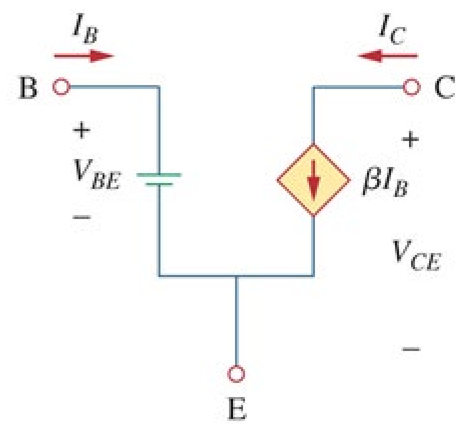


DC model of a BJT

- The figure below shows the equivalent DC model for a BJT in active mode.



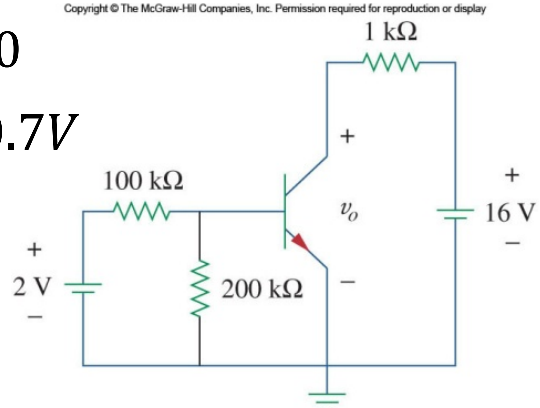
$$I_C = \beta I_B$$



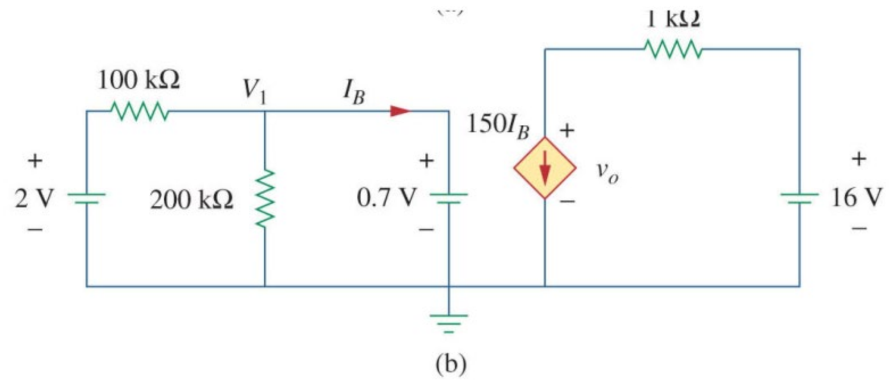
Setting up a BJT circuit

$\beta = 150$

$v_{BE} = 0.7V$



Original circuit



Circuit for nodal analysis