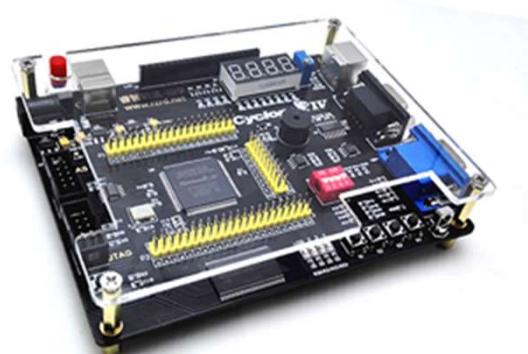




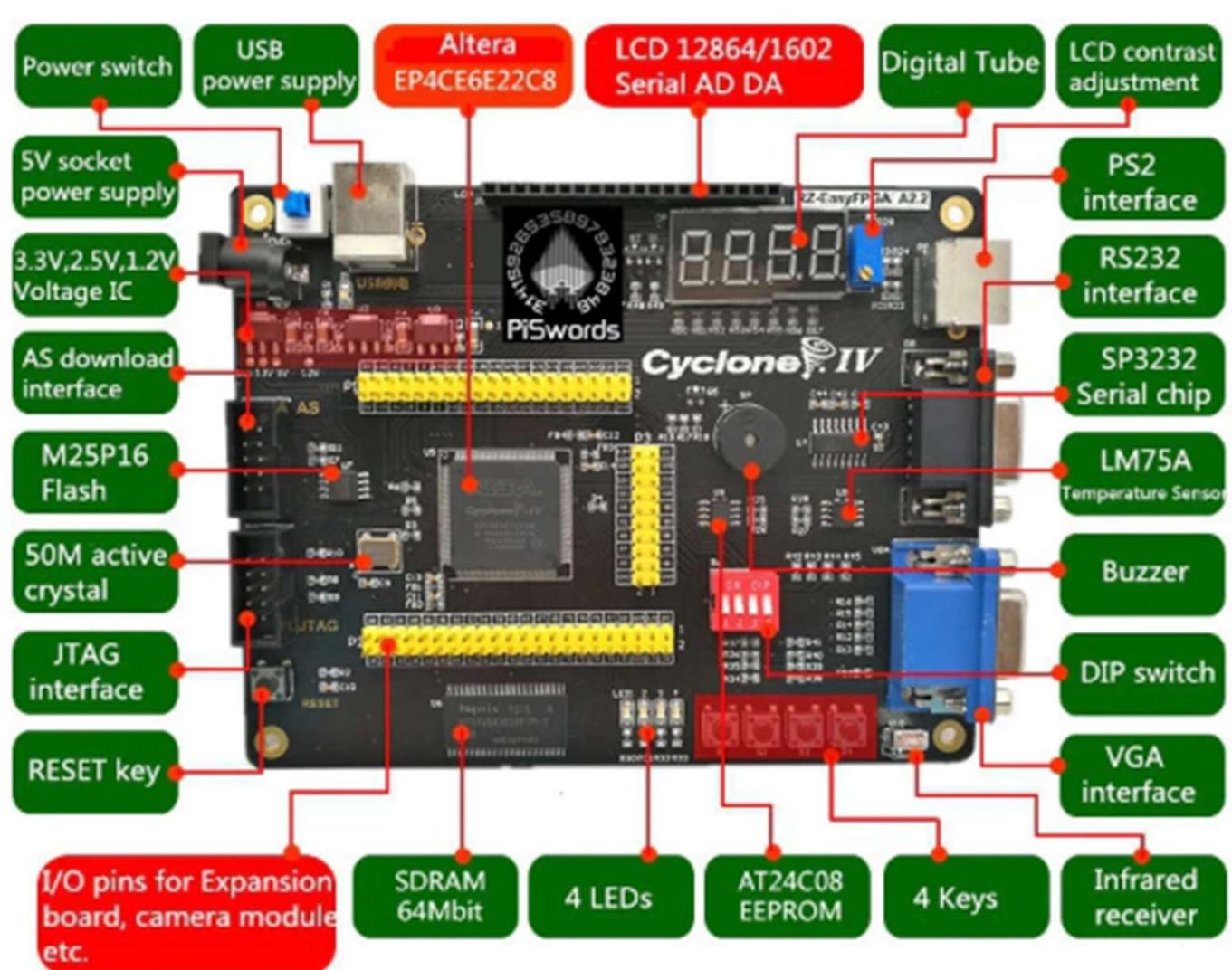
Tutorial

Placa de Desenvolvimento com FPGA Altera Cyclone IV



ITA – IEEA – EEA21
2019

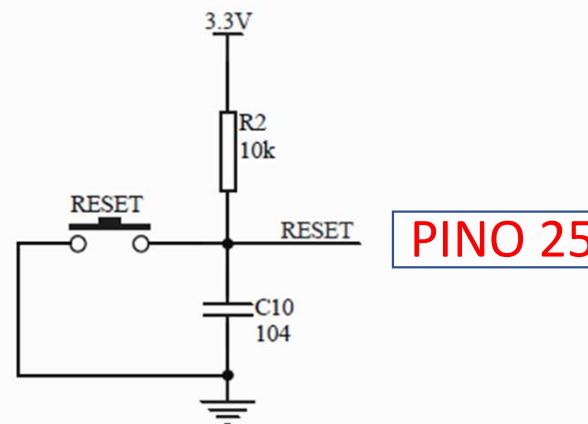
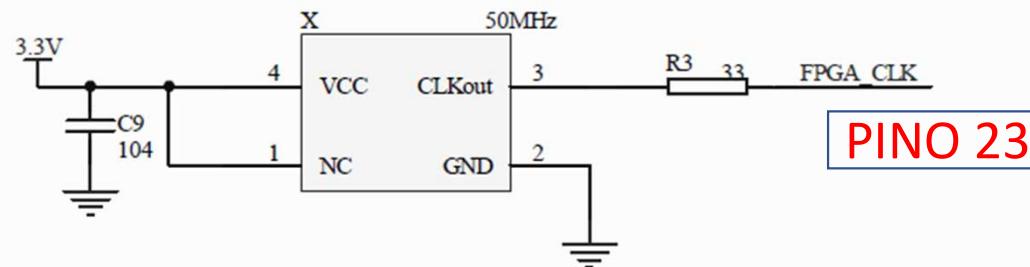
Altera EP4CE6 FPGA开发板



Crystal and reset

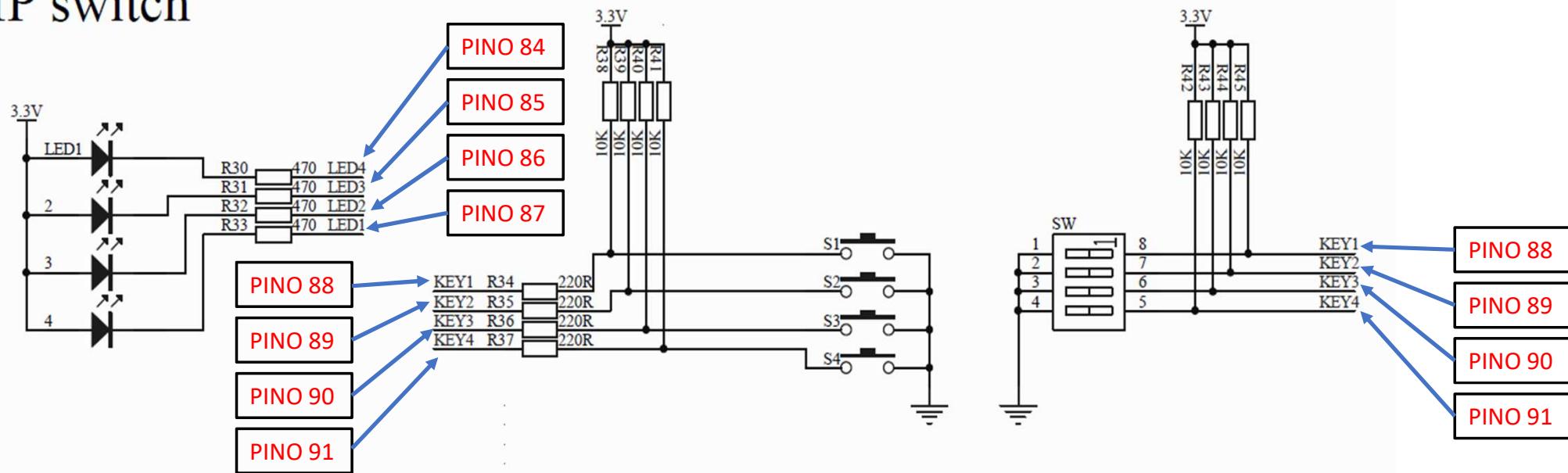
晶振及复位电路

OSCILADOR DE 50MHz

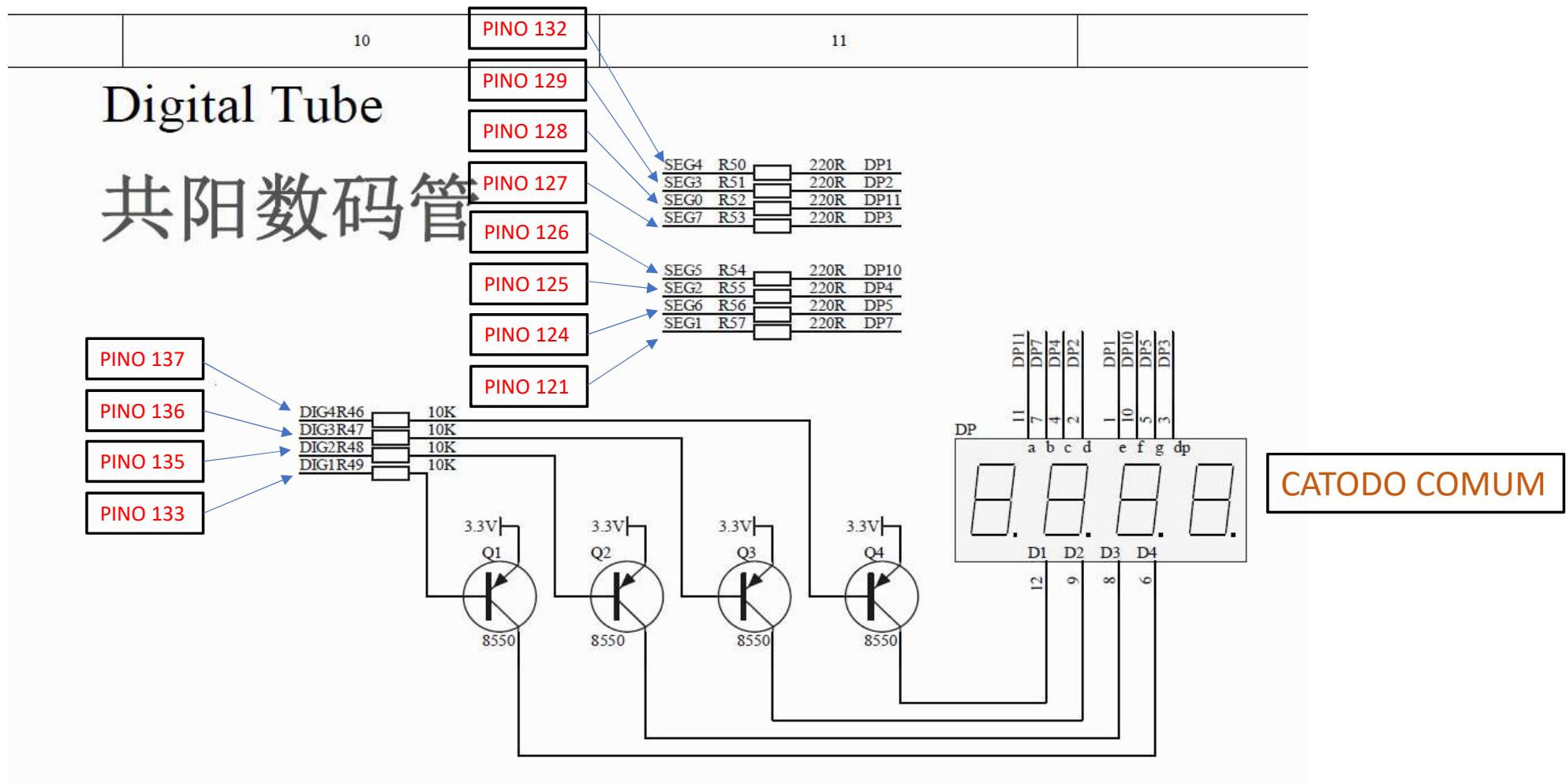


Button, LED,
DIP switch

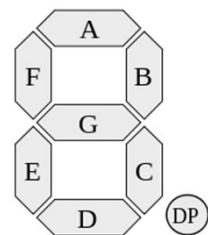
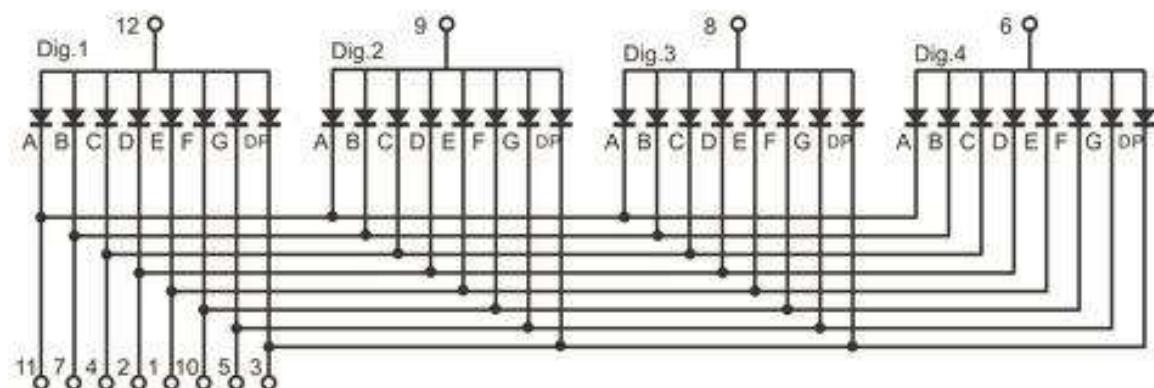
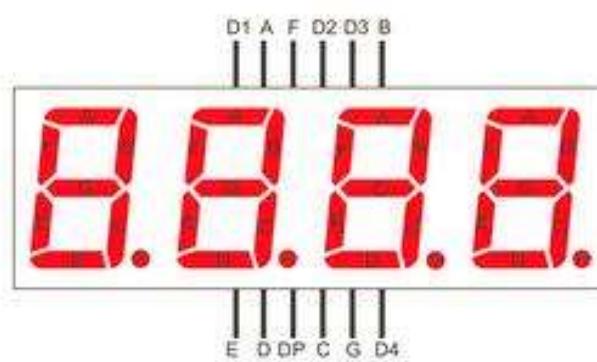
独立按键及LED 拨码开关



- LEDS ACENDEM COM '0'
- CHAVE PRESSIONADA = '0'
- 'TACT SWITCHES' E 'DIP SWITCHES' ESTÃO EM PARALELO

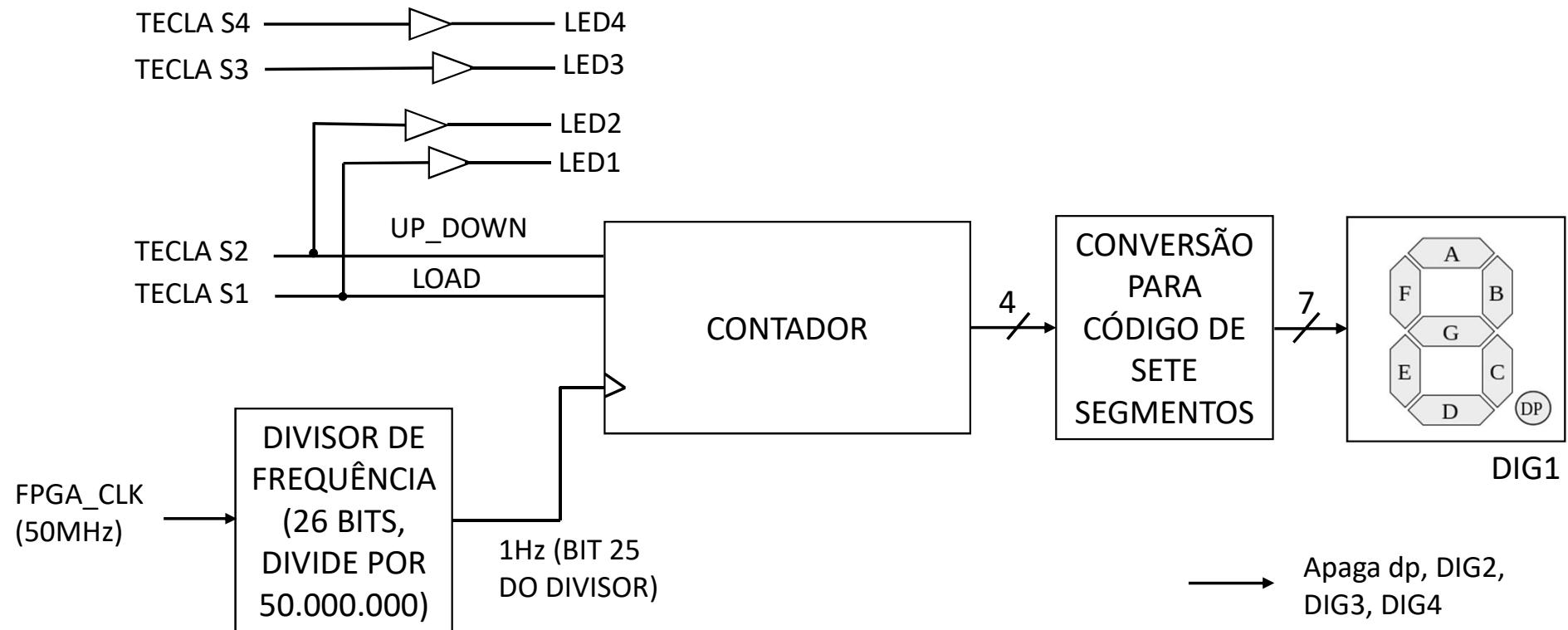


- LEDS DOS SEGMENTOS ACENDEM COM '0'
- OS DÍGITOS SÃO SELECIONADOS COM '0'



EXPERIMENTO

- Implementar um contador decimal de 9 a 0 ou de 0 a 9, com 'clock' a cada 1s;
- Normalmente conta de forma decrescente e mostra a saída no dígito mais à direita do 'display' de 7 segmentos (DIG1);
- Quando mantida pressionada a tecla S2, conta de forma crescente, mostra a saída em DIG1 e acende LED2;
- Pressionar a tecla S1 faz com que o contador seja carregado com 9 e o LED3 seja aceso;
- S3 e S4 pressionados fazem acender LED3 e LED4, respectivamente.



3 PROJETOS:

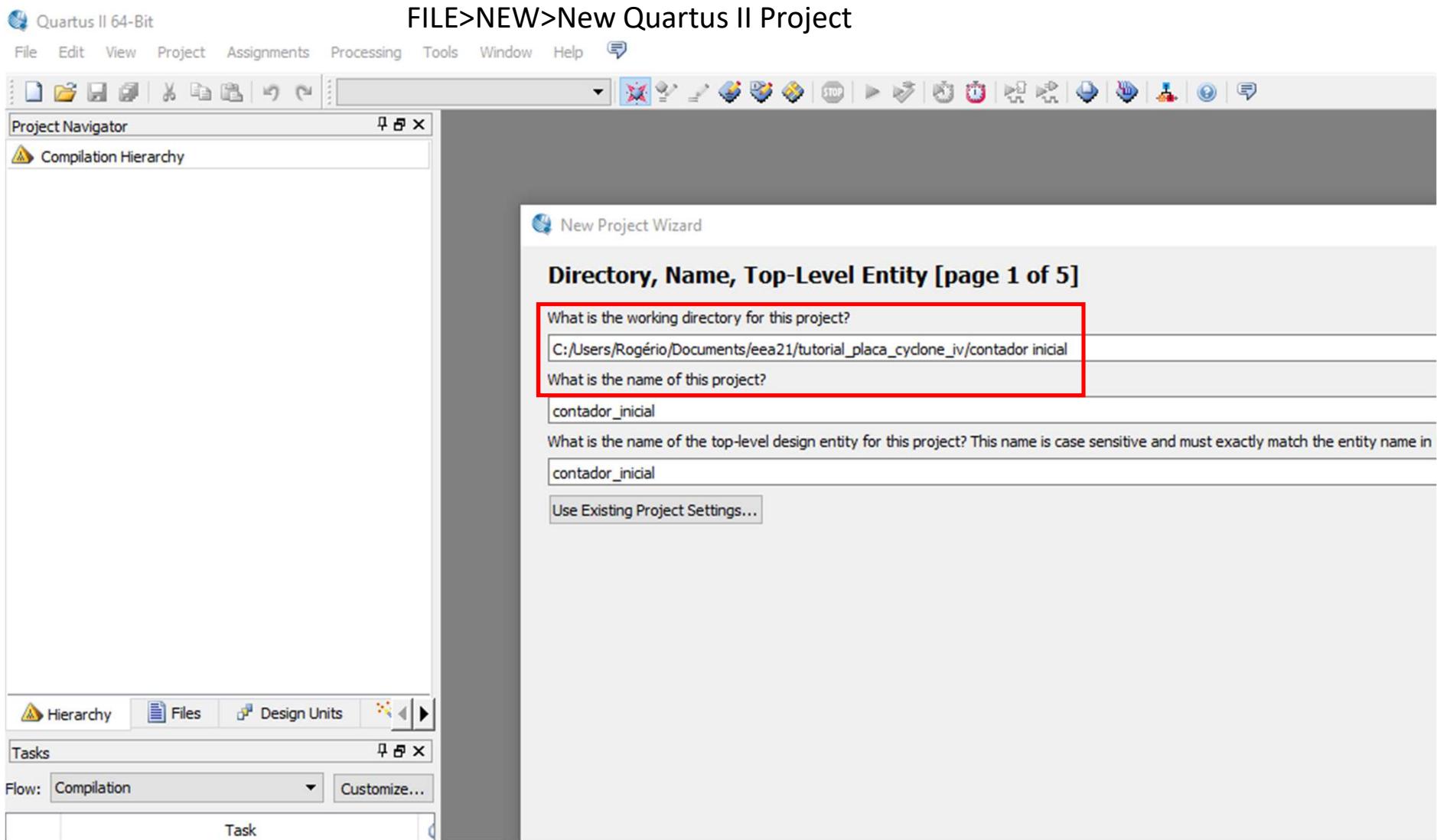
- Contador (bdf)
- Conversão para 7 segmentos (VHDL)
- Final (bdf, integrando os projetos anteriores e um divisor de frequência)

OBJETIVOS:

- Integração de Projetos
- Atribuição de Pinos
- Programação da FPGA

PROJETO 1: CONTADOR

FILE>NEW>New Quartus II Project



New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

Device family

Family: Cyclone IV E
Devices: All

Target device

Auto device selected by the Fitter
 Specific device selected in 'Available devices' list
 Other: n/a

Show in 'Available devices' list

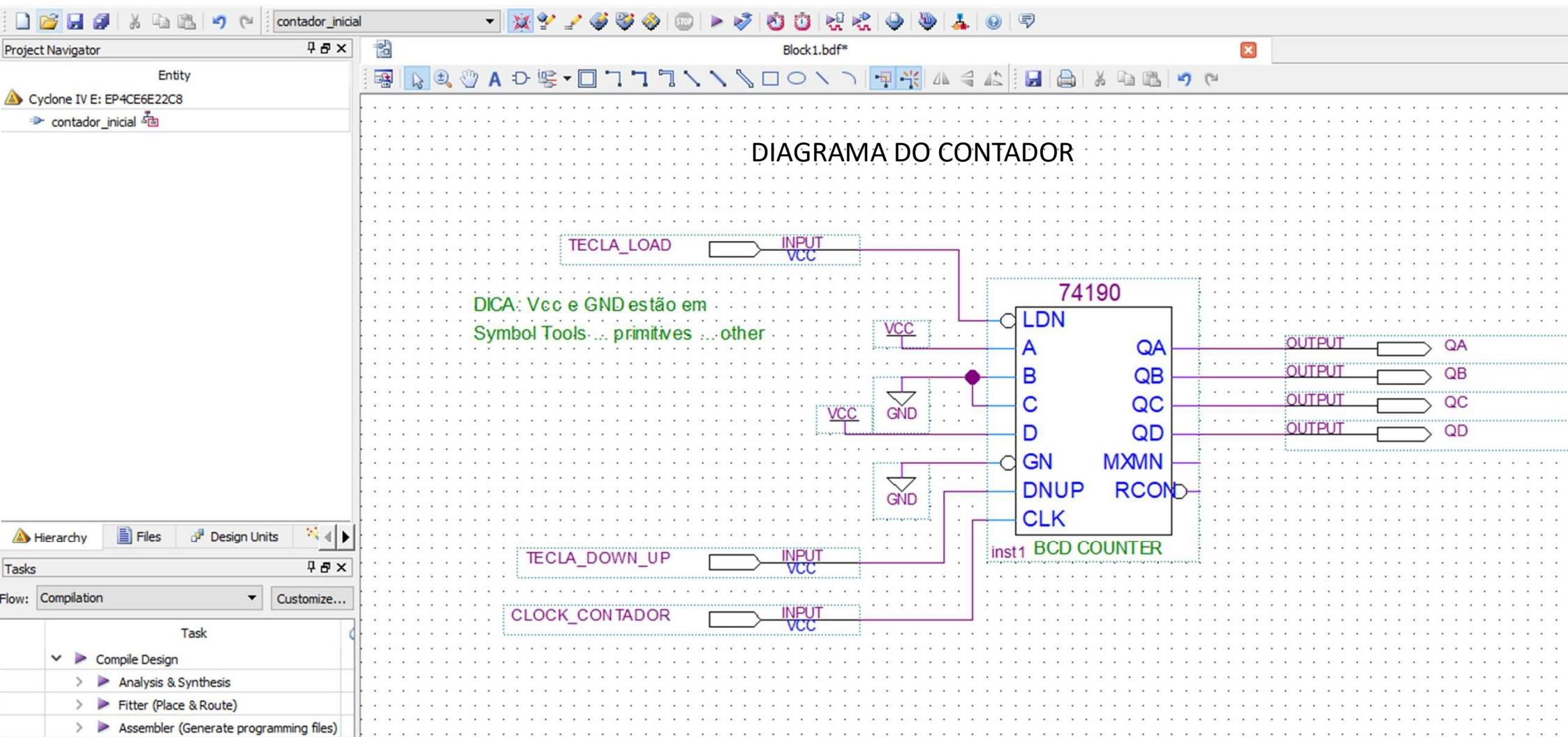
Package: Any
Pin count: Any
Speed grade: Any
Name filter:
 Show advanced devices HardCopy compatible only

Available devices:

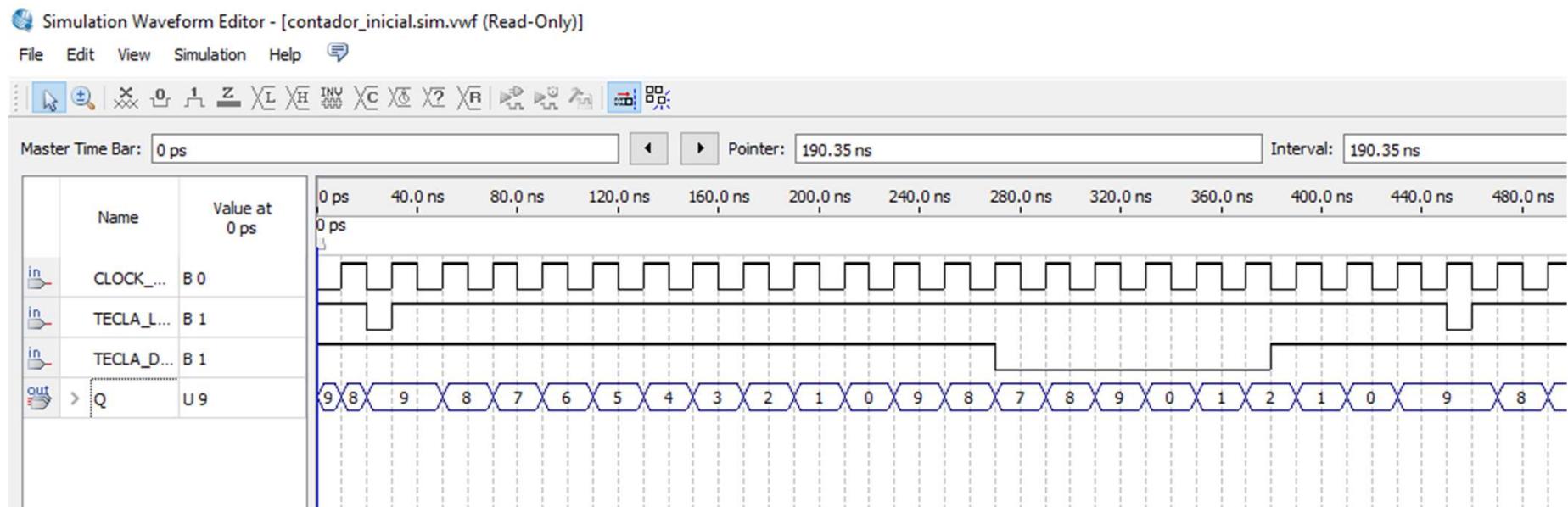
Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	GI
EP4CE6E22A7	1.2V	6272	92	276480	30	2	10
EP4CE6E22C6	1.2V	6272	92	276480	30	2	10
EP4CE6E22C7	1.2V	6272	92	276480	30	2	10
EP4CE6E22C8	1.2V	6272	92	276480	30	2	10
EP4CE6E22C8L	1.0V	6272	92	276480	30	2	10
EP4CE6E22C9L	1.0V	6272	92	276480	30	2	10
EP4CE6E22I7	1.2V	6272	92	276480	30	2	10

Companion device

HardCopy:

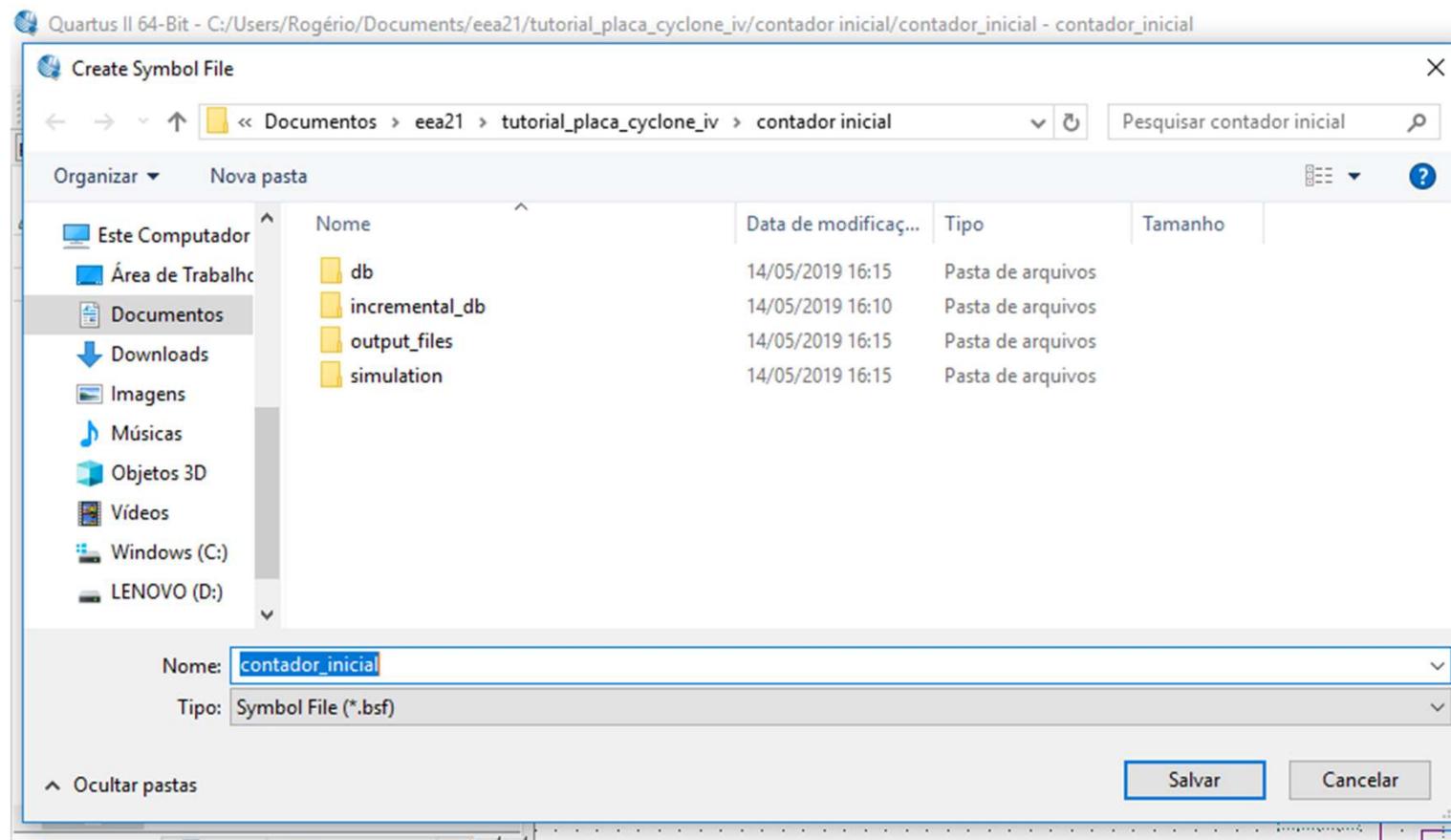


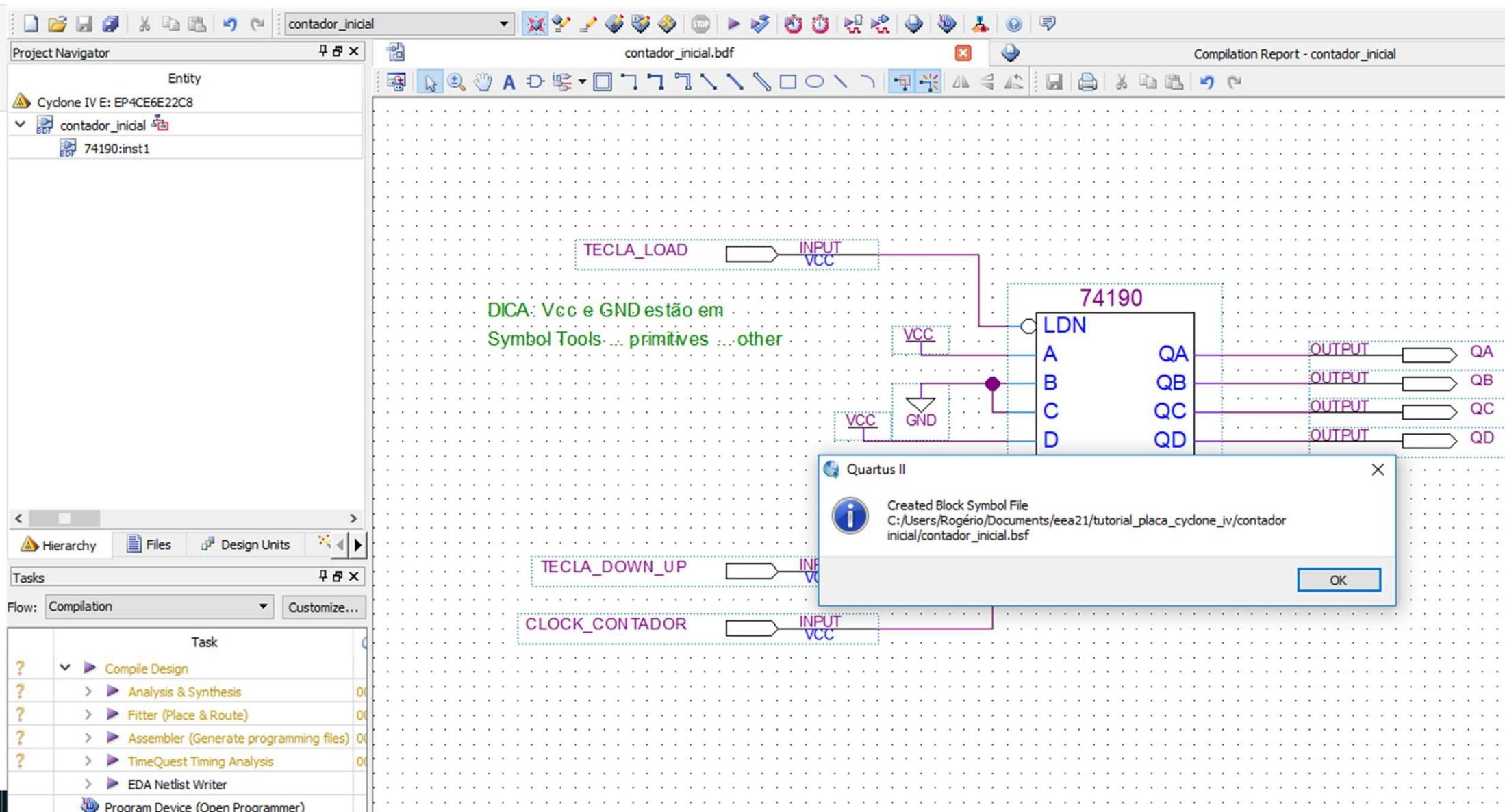
TESTE DO CONTADOR



CRIANDO O SÍMBOLO PARA USAR NO FINAL

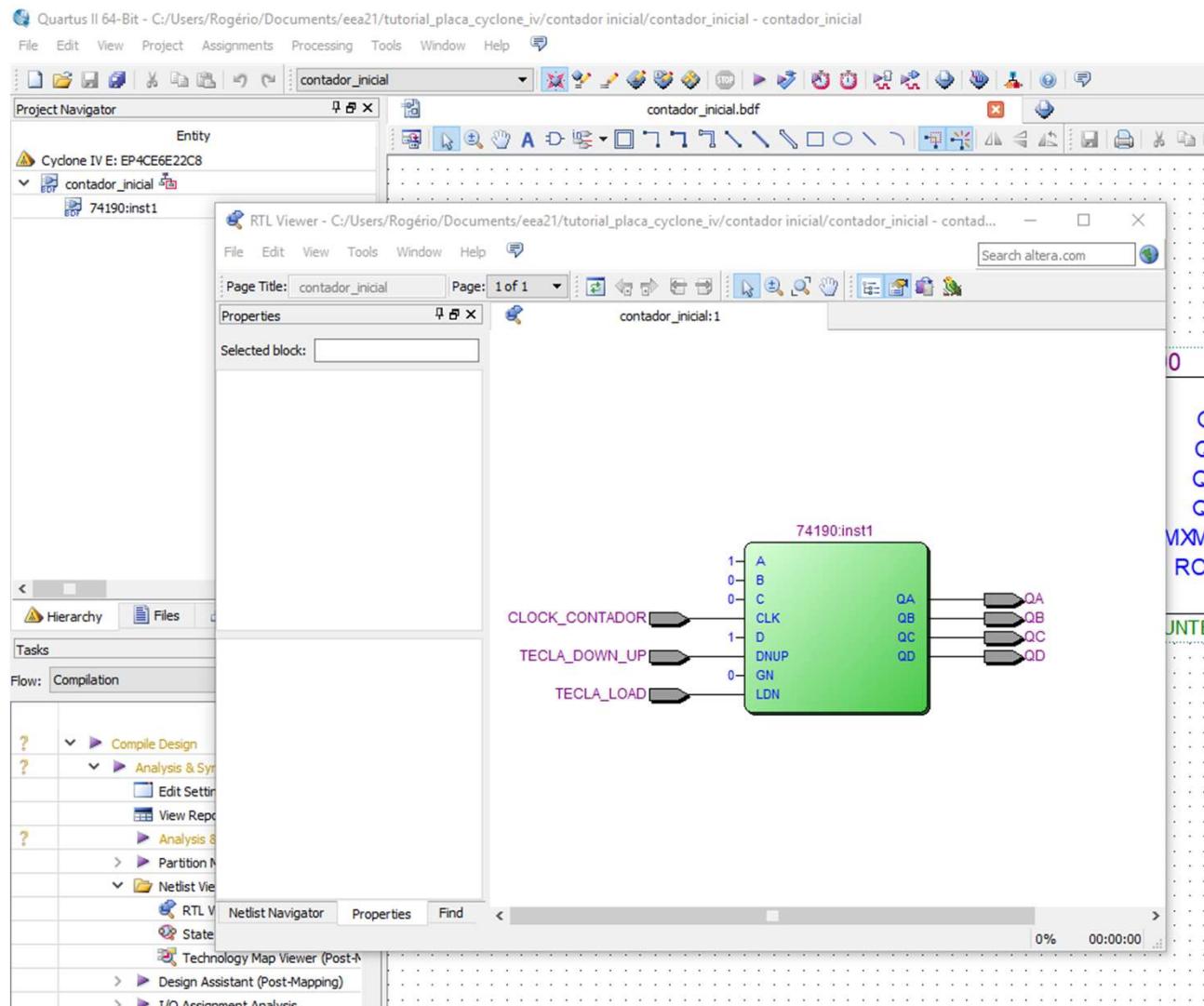
FILE>Create / Update>Create Symbol Files for Current File



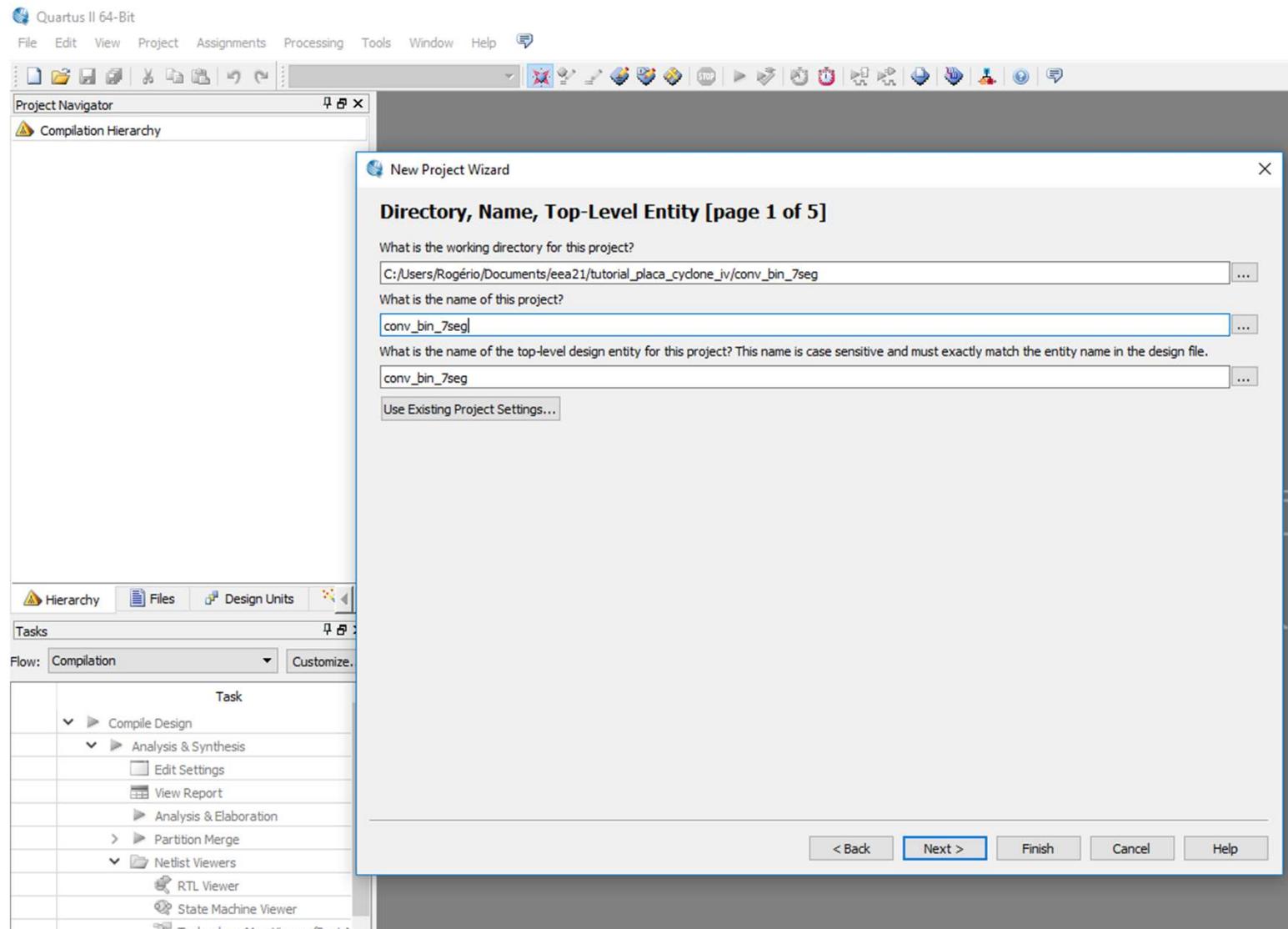


Vendo o Símbolo Criado

Tools>Netlist Viewers>RTL Viewer



PROJETO 2: CONVERSÃO PARA CÓDIGO DE 7 SEGMENTOS



File>New>VHDL File

Quartus II 64-Bit - C:/Users/Rogério/Documents/eea21/tutorial_placa_cyclone_iv/conv_bin_7seg/conv_bin_7seg - conv_bin_7seg

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity Cyclone IV E: EP4CE6E22C8 conv_bin_7seg

conv_bin_7seg.vhd Compilation Report - conv_bin_7seg

```
-- Tutorial da Placa Cyclone IV
library ieee;
use ieee.std_logic_1164.all;

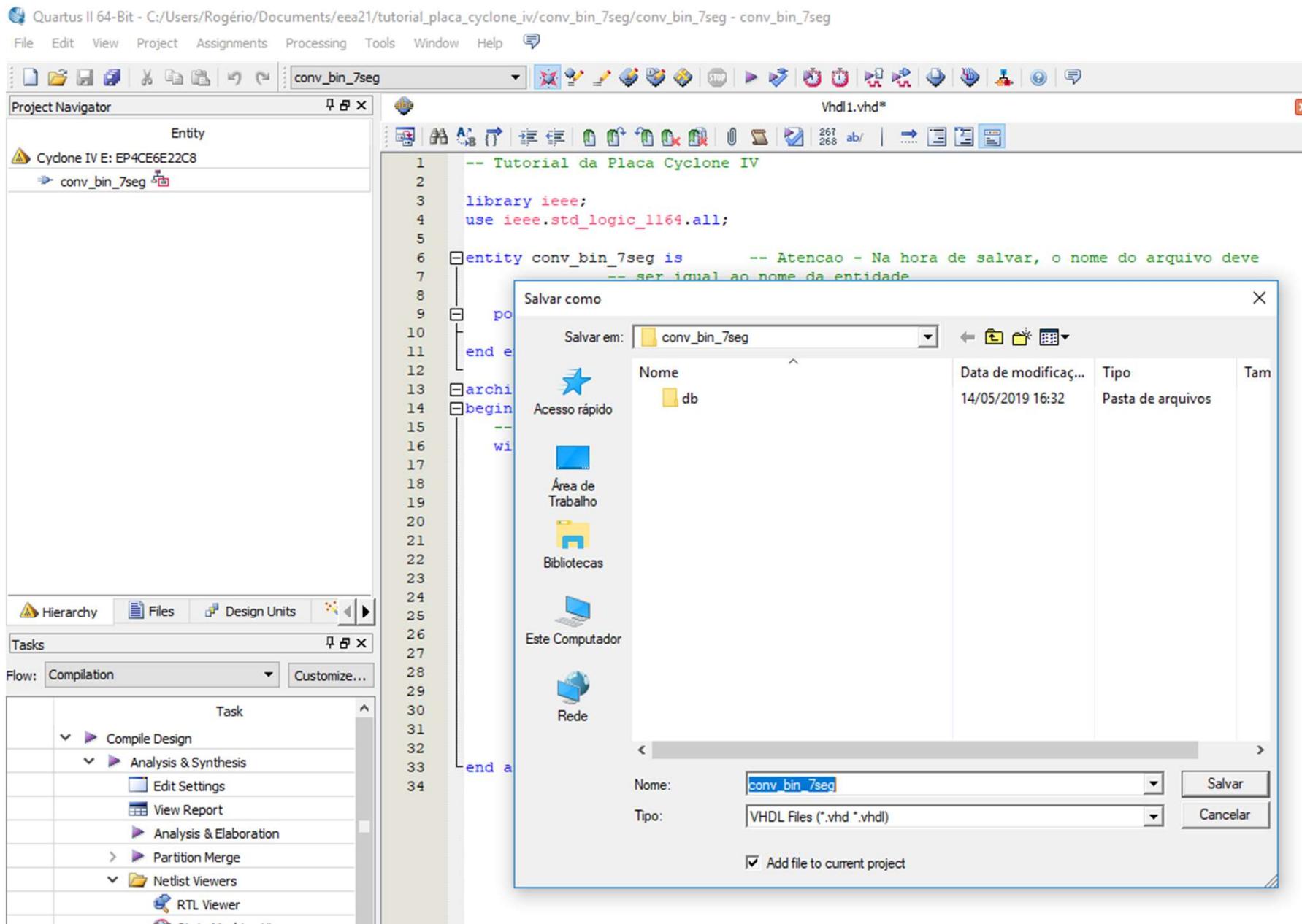
entity conv_bin_7seg is      -- Atenção - Na hora de salvar, o nome do arquivo deve
                           -- ser igual ao nome da entidade
  port(d: in std_logic_vector (3 downto 0);
       q: out std_logic_vector (6 downto 0));
end entity;

architecture conv_arch of conv_bin_7seg is
begin
  -- saída = leds abcdefg do display de 7 segmentos (ordem) = acendem com 0
  with d select
    q <= "0000001" when "0000",   -- 0 -> 01
           "1001111" when "0001",   -- 1 -> 4F
           "0010010" when "0010",   -- 2 -> 12
           "0000110" when "0011",   -- 3 -> 06
           "11001100" when "0100",  -- 4 -> 4C
           "0100100" when "0101",   -- 5 -> 24
           "0100000" when "0110",   -- 6 -> 20
           "0000111" when "0111",   -- 7 -> 0F
           "0000000" when "1000",   -- 8 -> 00
           "0000100" when "1001",   -- 9 -> 04
           "0001000" when "1010",   -- A -> 08
           "1100000" when "1011",   -- B -> 60
           "0110001" when "1100",   -- C -> 31
           "1000010" when "1101",   -- D -> 42
           "0110000" when "1110",   -- E -> 30
           "0111000" when "1111";  -- F -> 38
end architecture;
```

Hierarchy Files Design Units Tasks Flow: Compilation Customize... Task Compile Design Analysis & Synthesis Filter (Place & Route) Assembler (Generate programming files) TimeQuest Timing Analysis EDA Netlist Writer Program Device (Open Programmer)

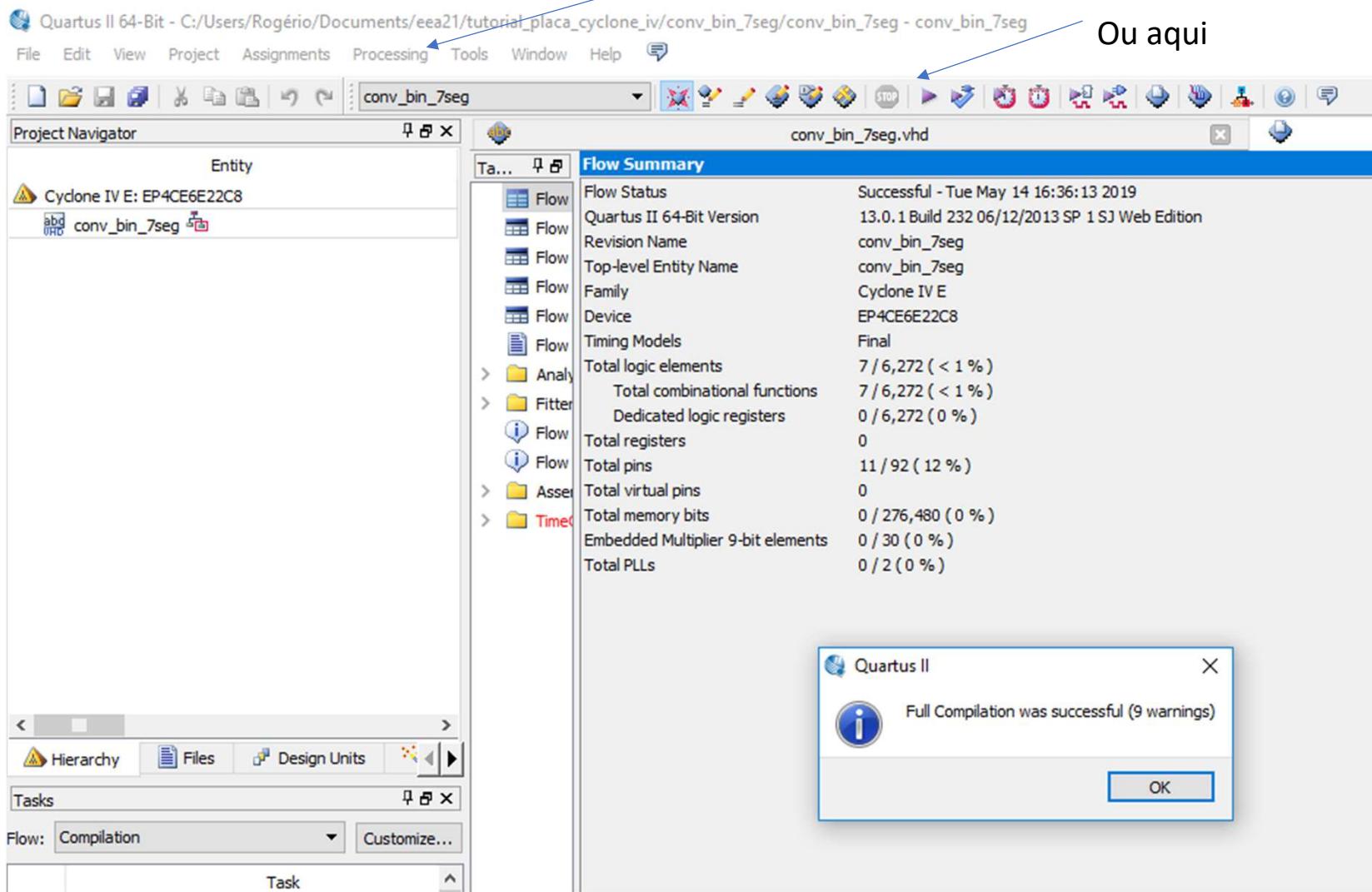
All <<Search>>

Type ID Message



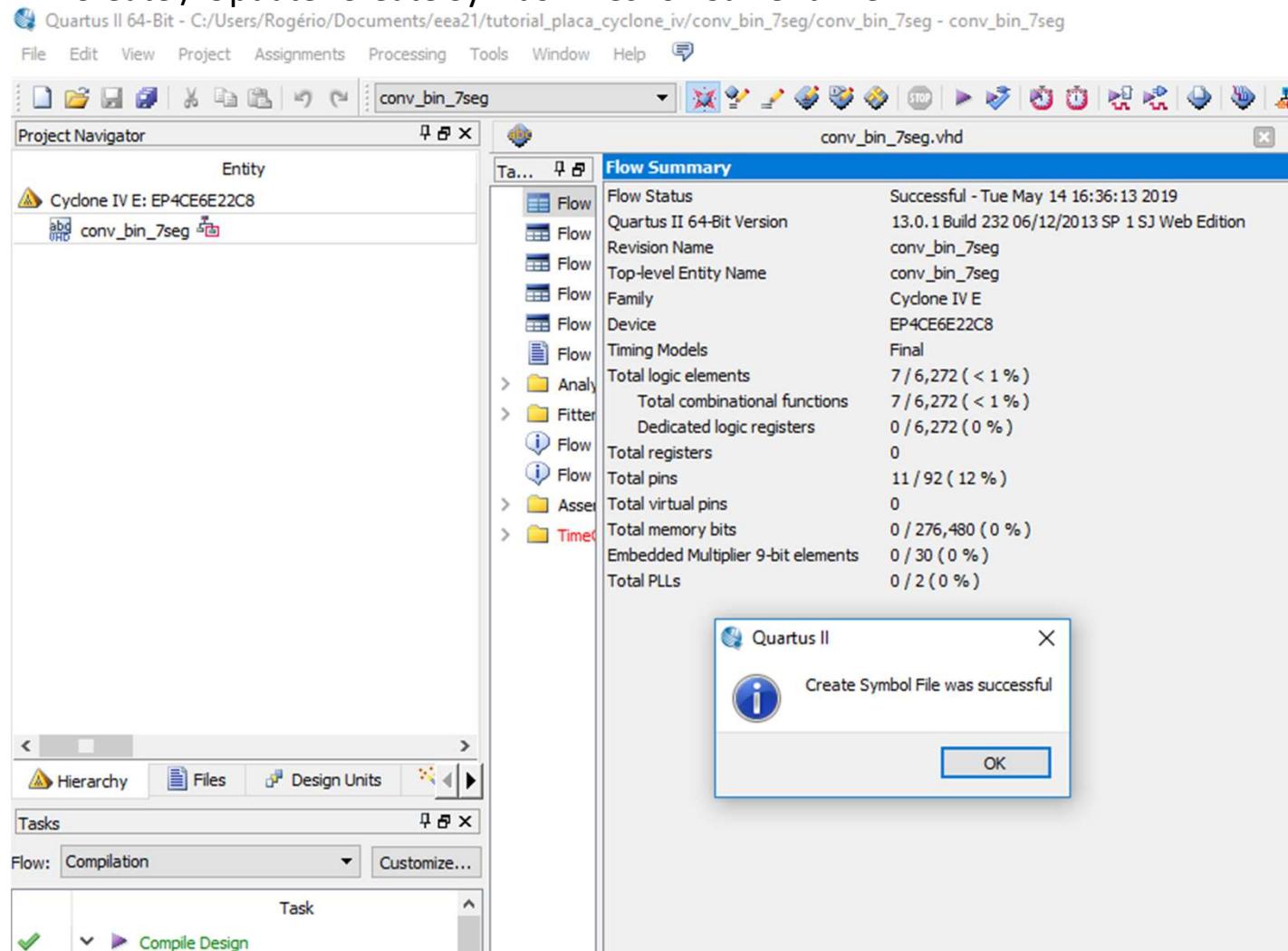
Compilar

Processing>Start Compilation

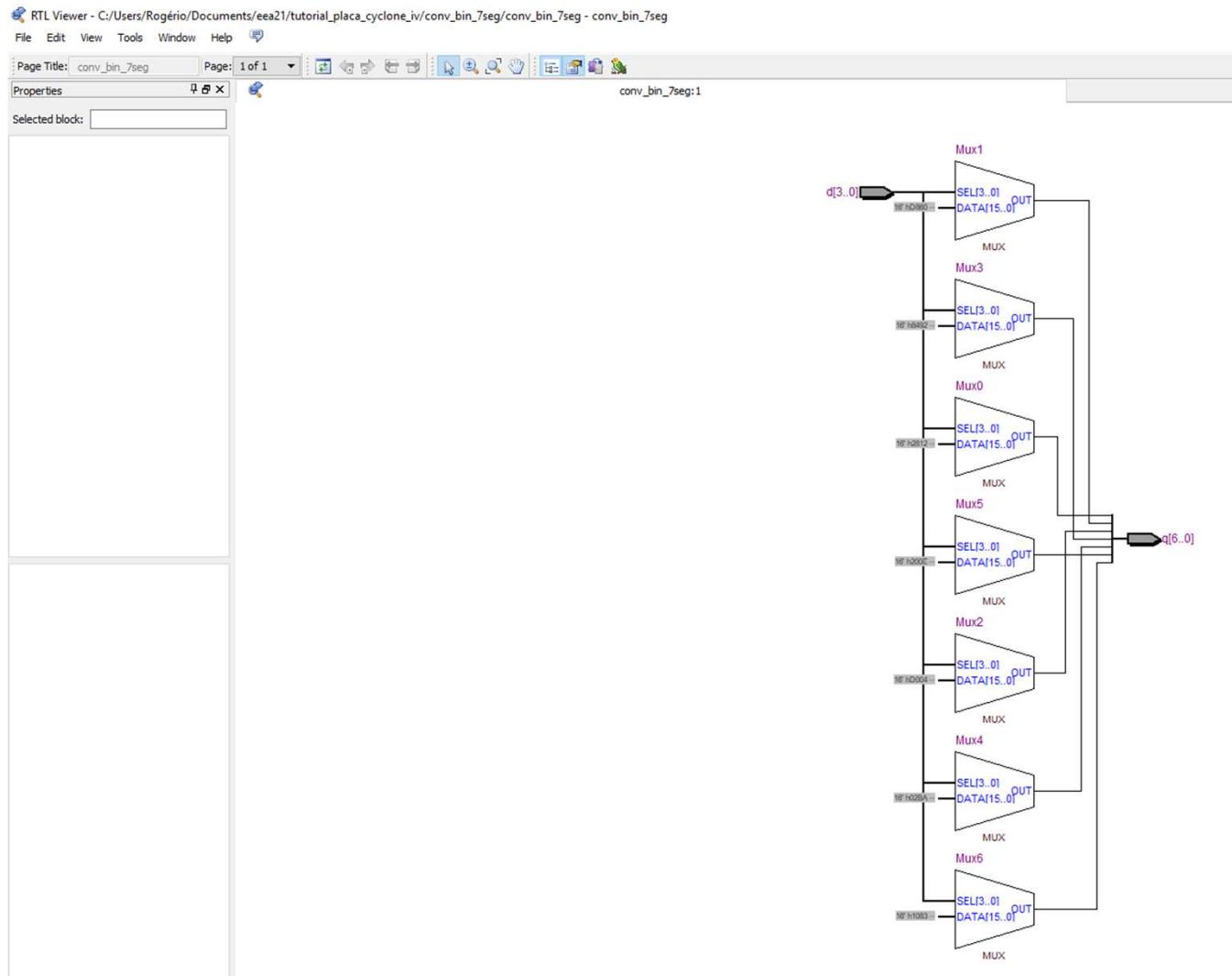


CRIANDO O SÍMBOLO PARA USAR NO FINAL

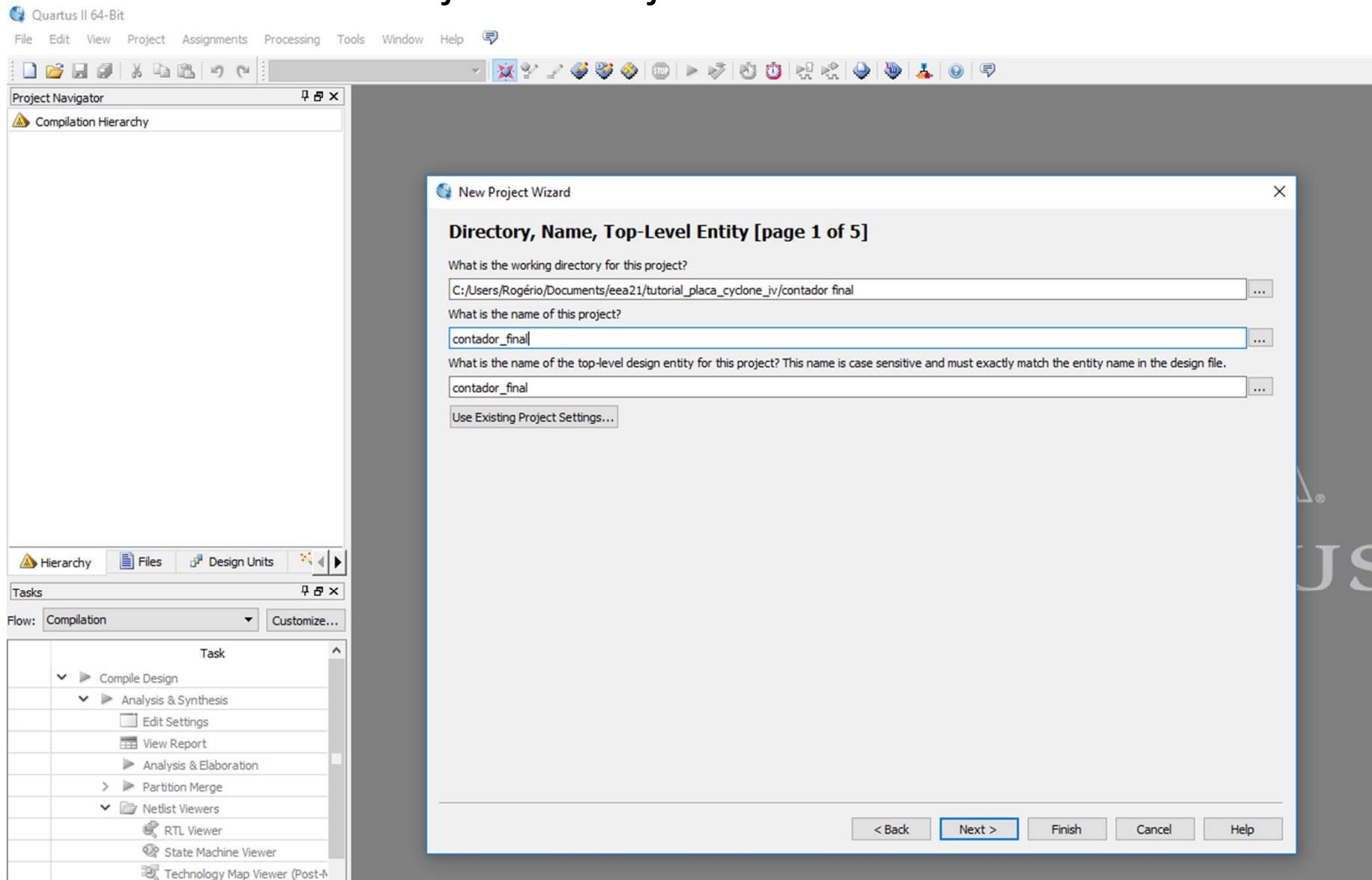
FILE>Create / Update>Create Symbol Files for Current File

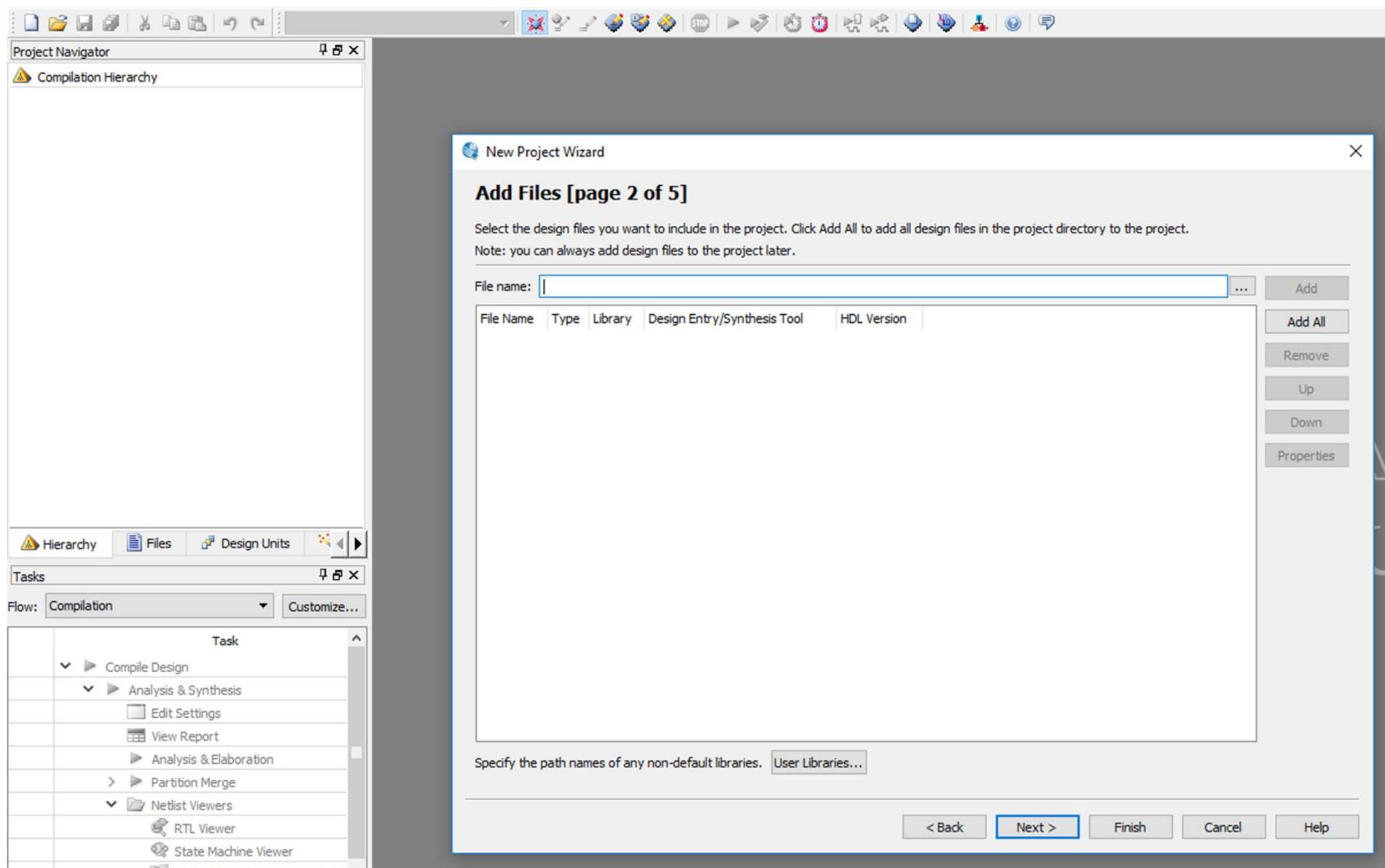


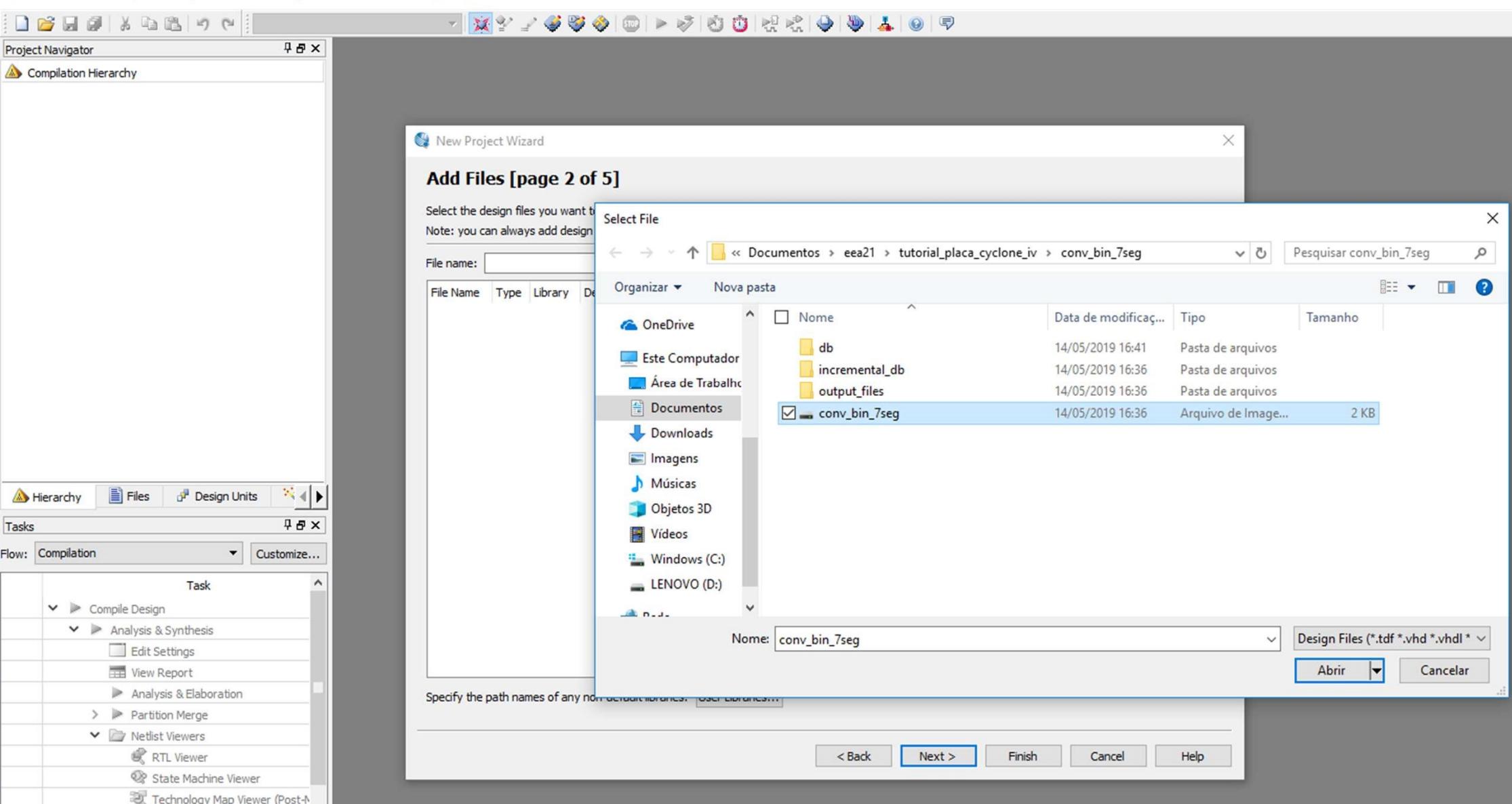
Tools>Netlist Viewers>RTL Viewer

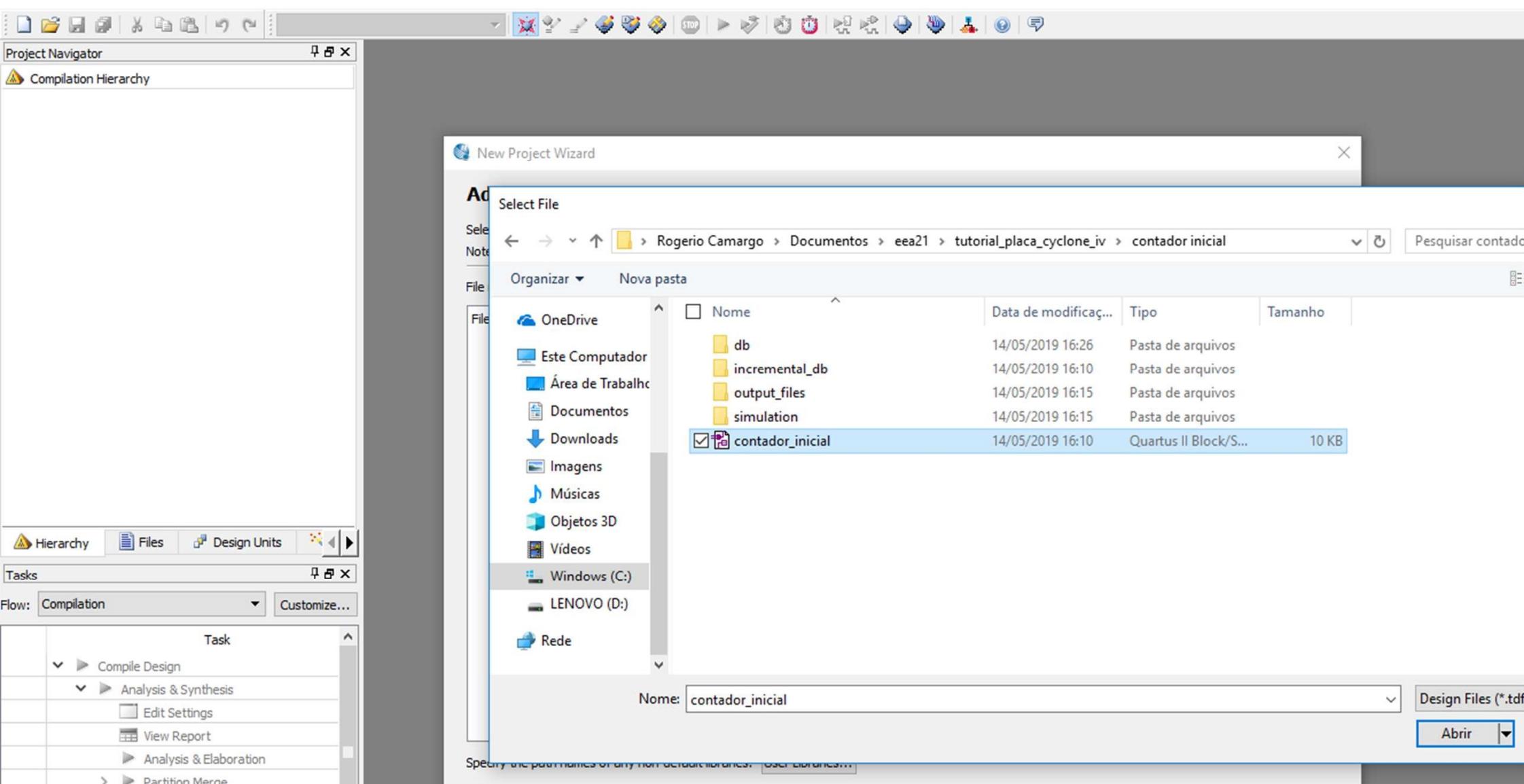


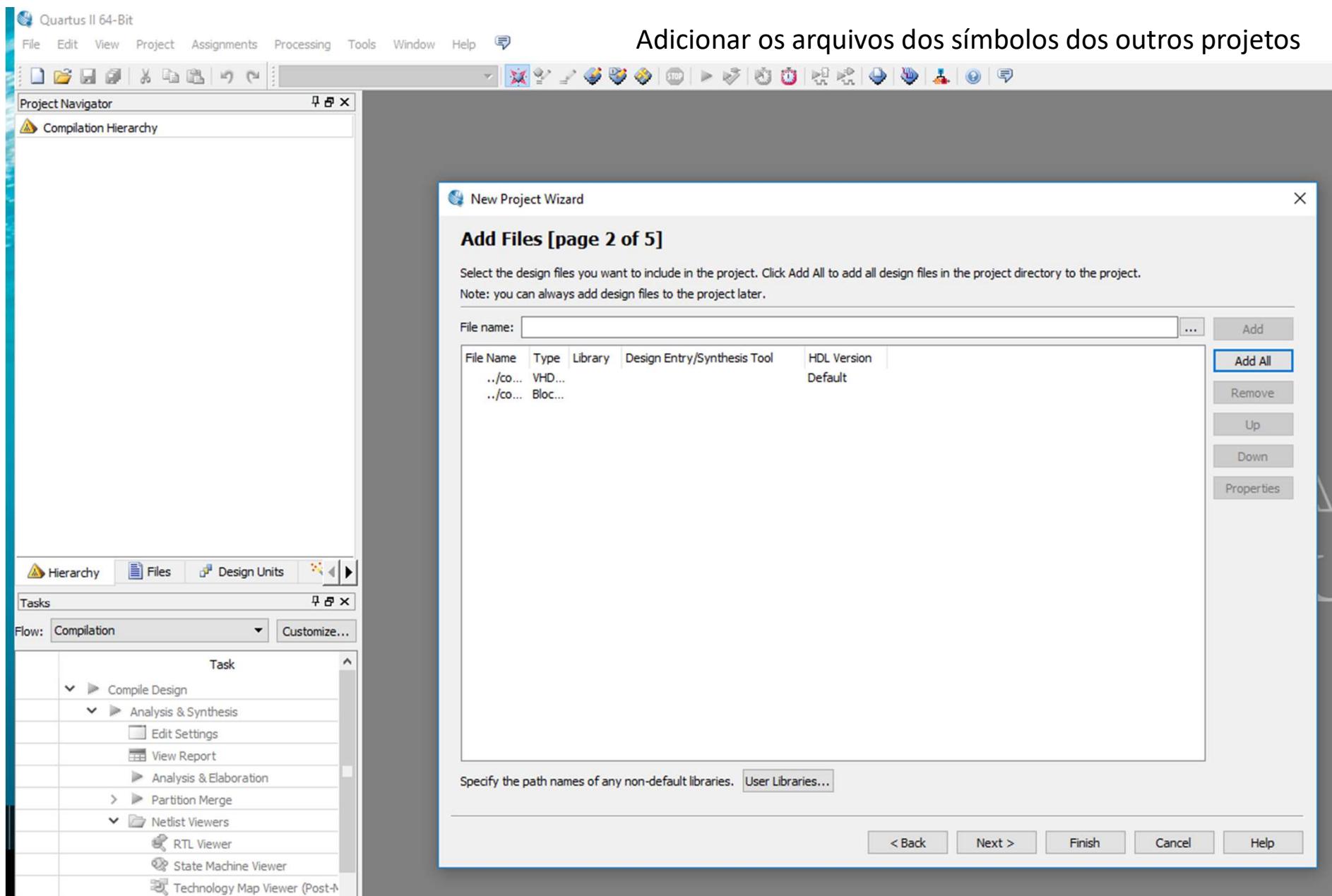
Projeto 3: Projeto Final





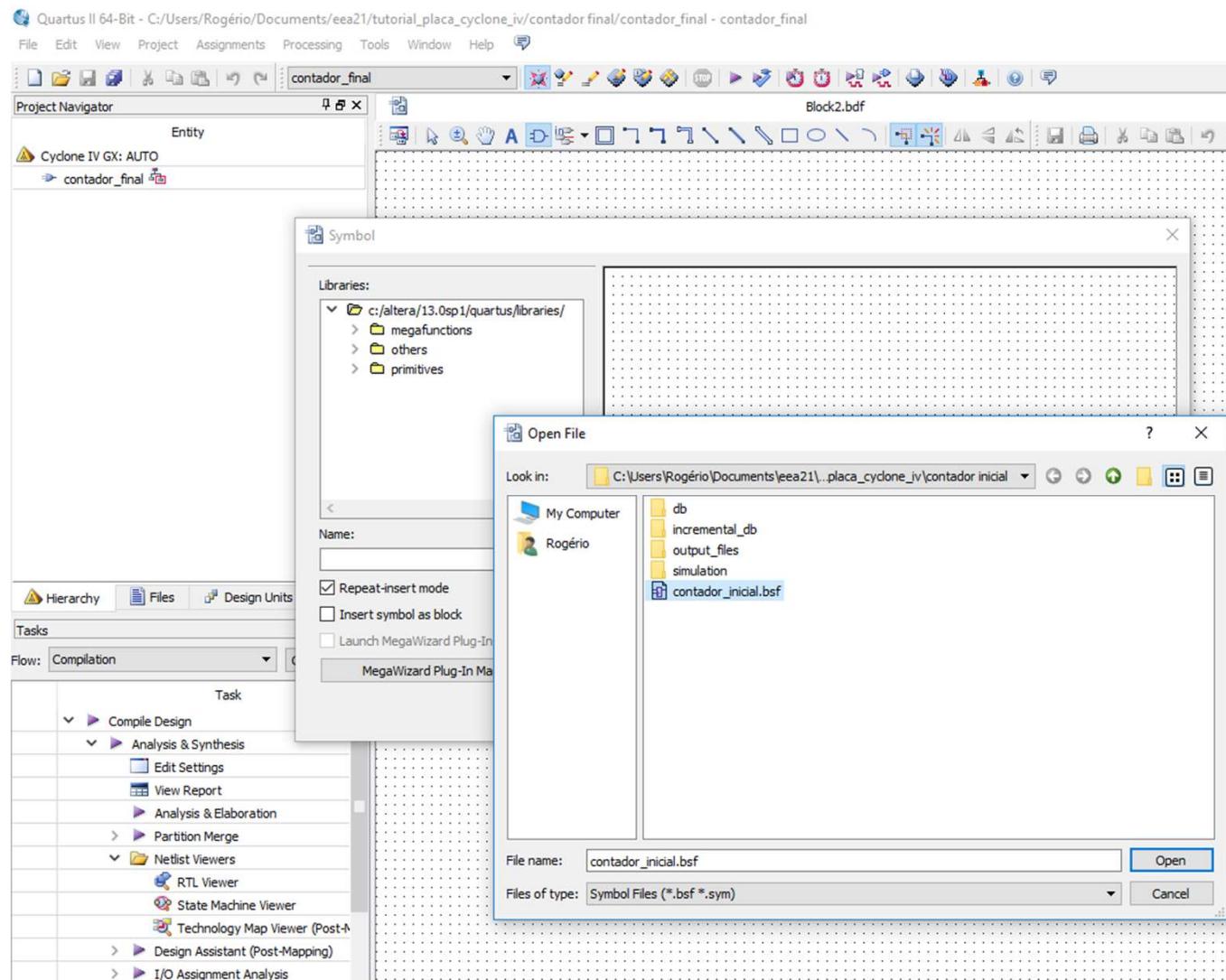




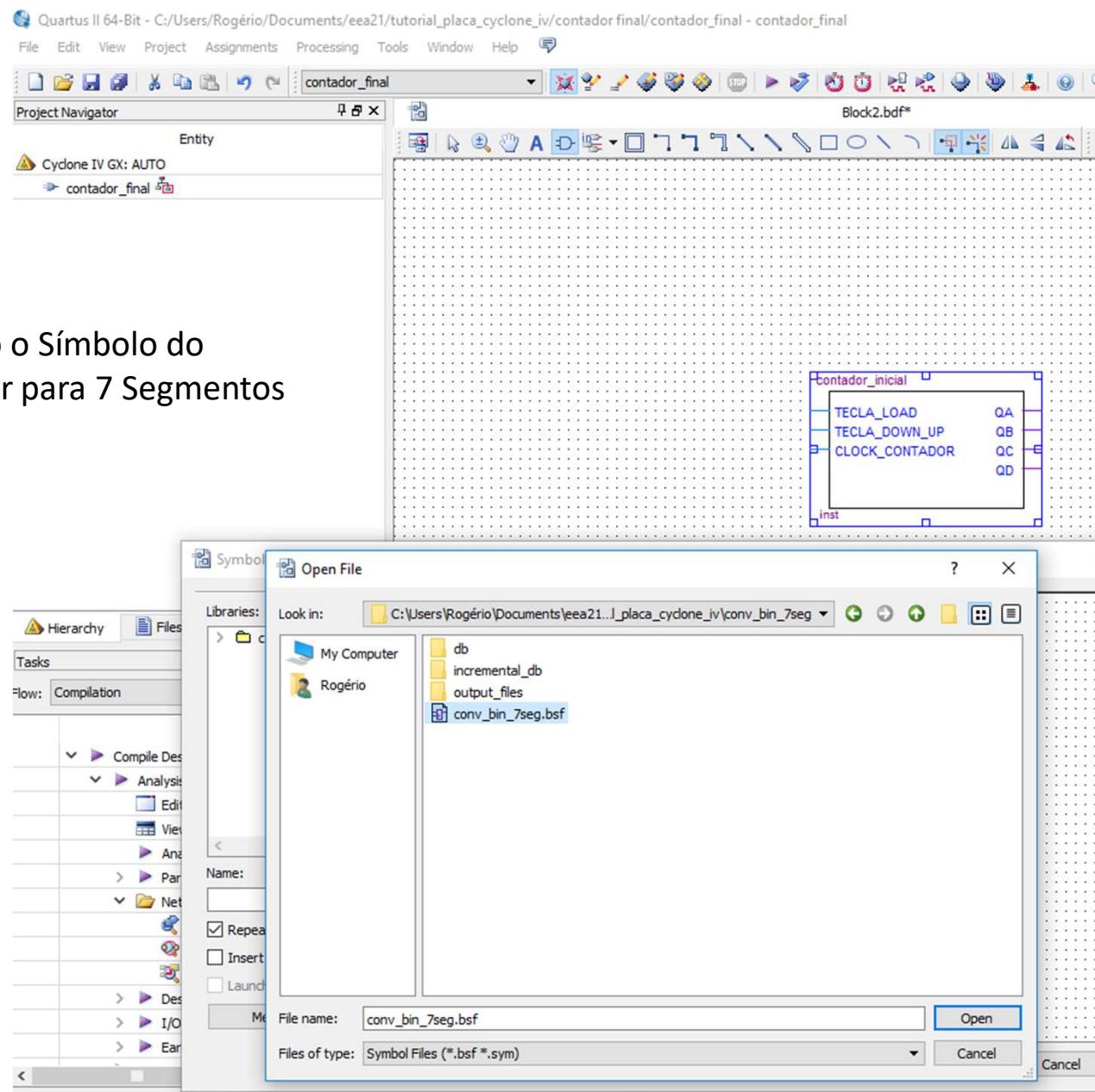


File>New>Block Diagram/Schematic File
Symbol Tool>...

Inserir o contador

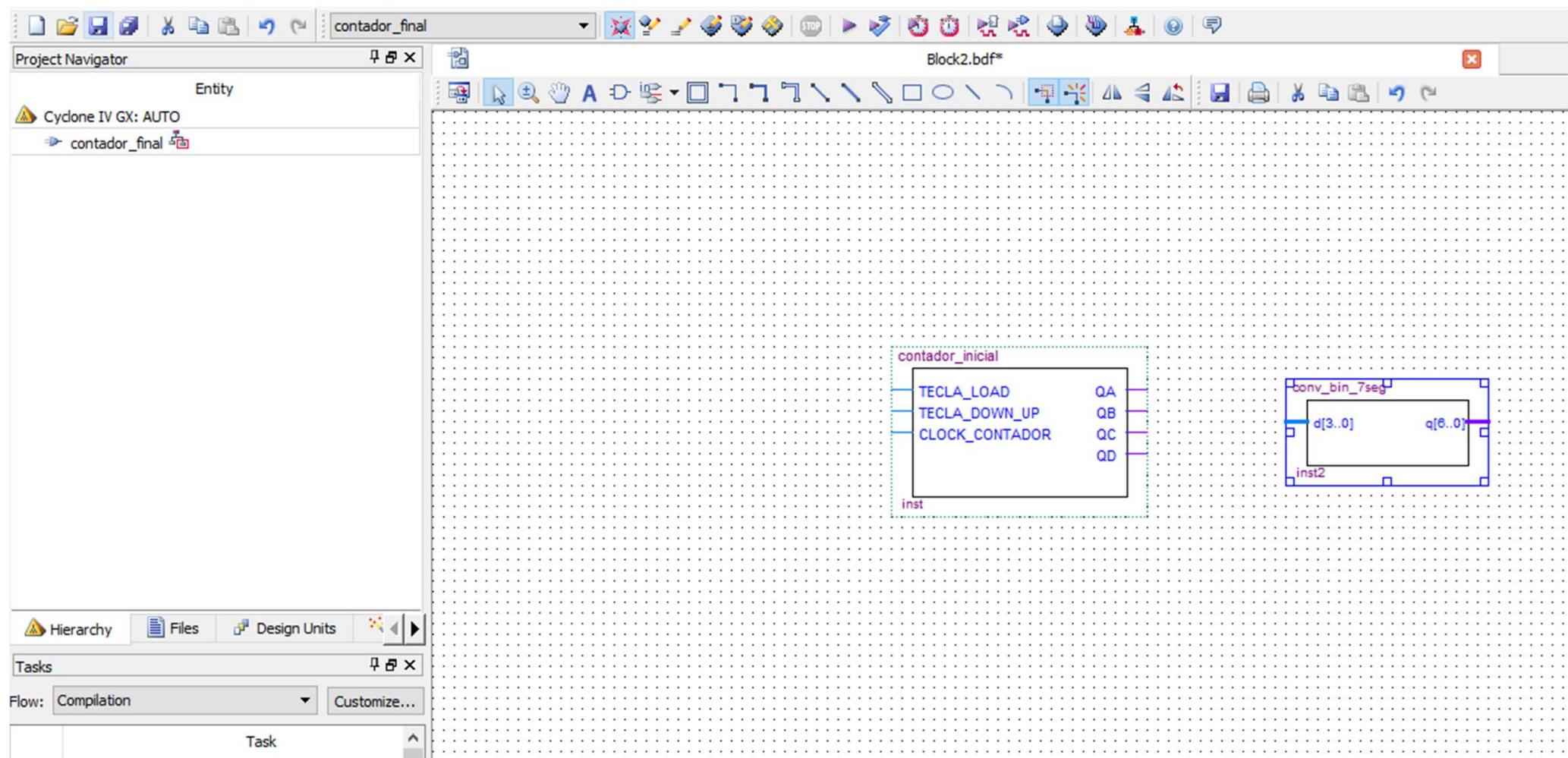


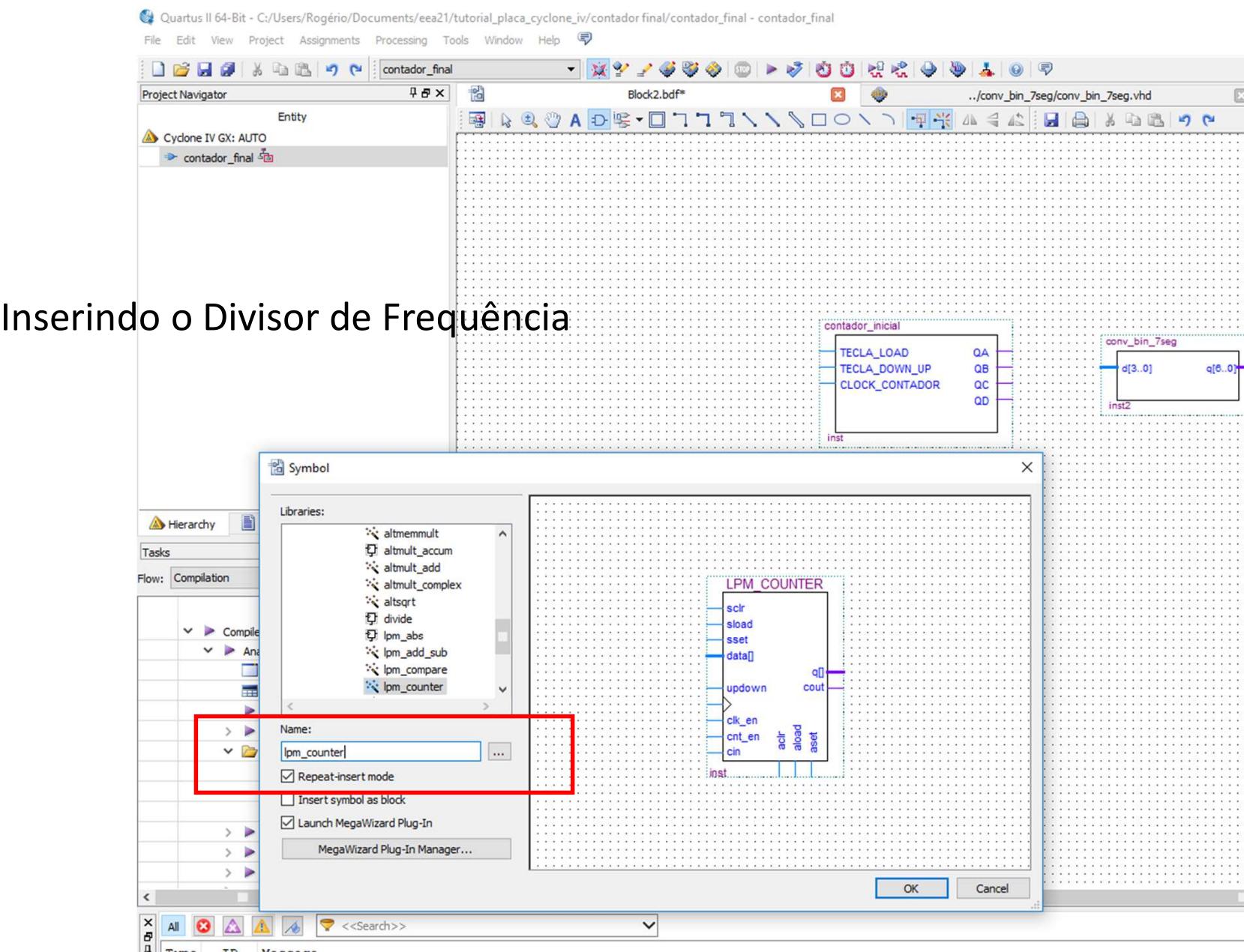
Inserindo o Símbolo do Conversor para 7 Segmentos

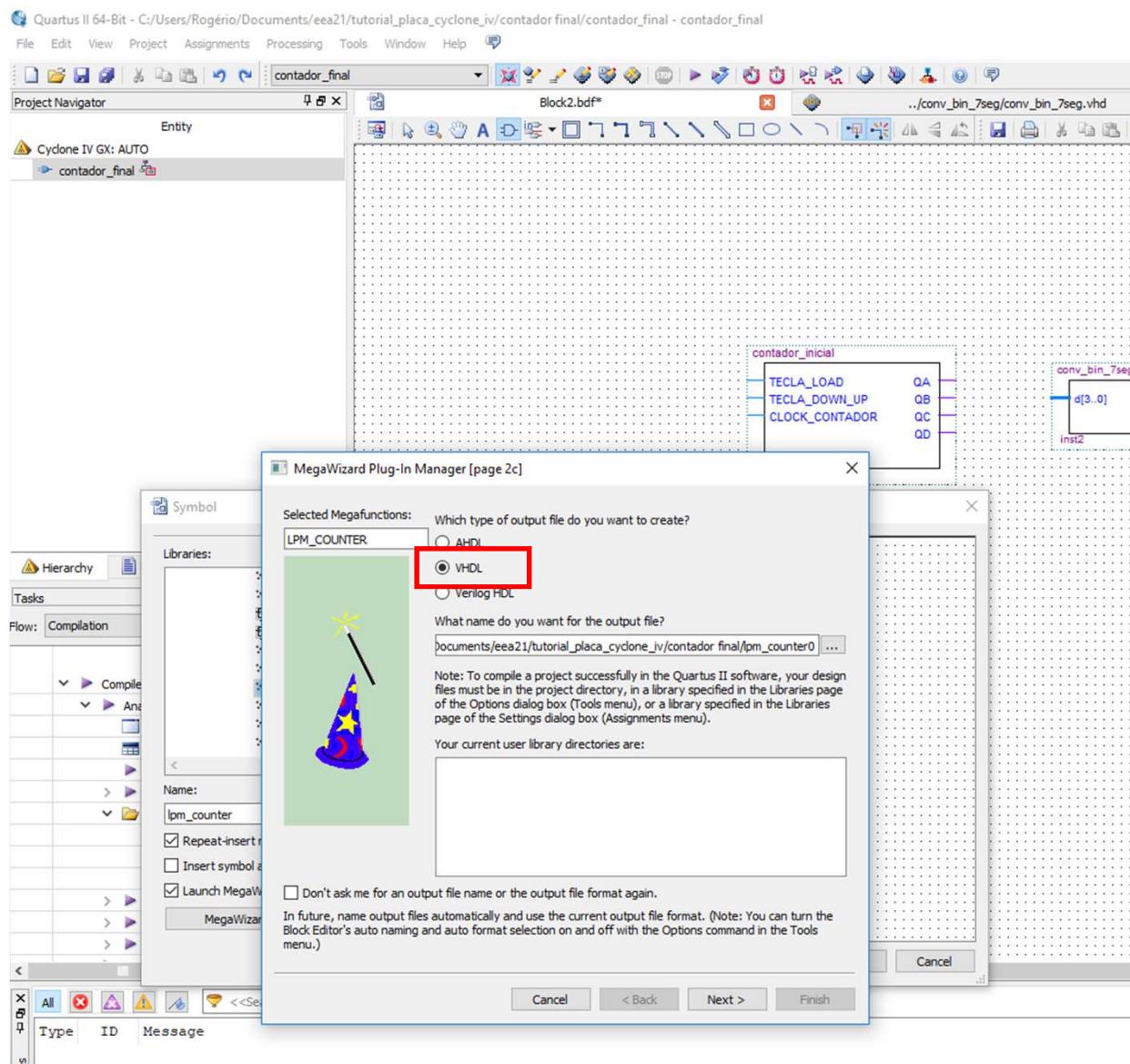


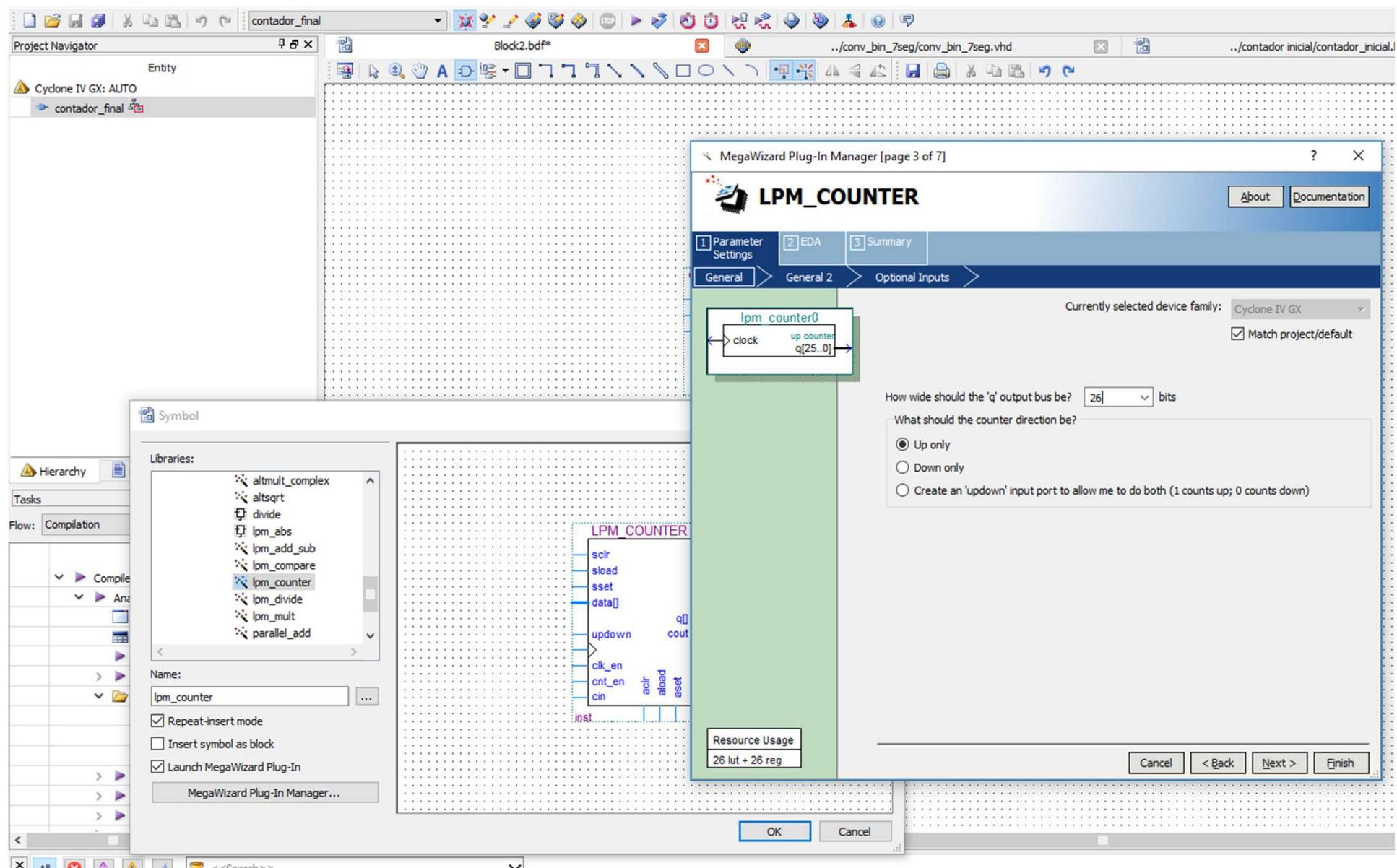
Quartus II 64-Bit - C:/Users/Rogério/Documents/eea21/tutorial_placa_cyclone_iv/contador_final/contador_final - contador_final

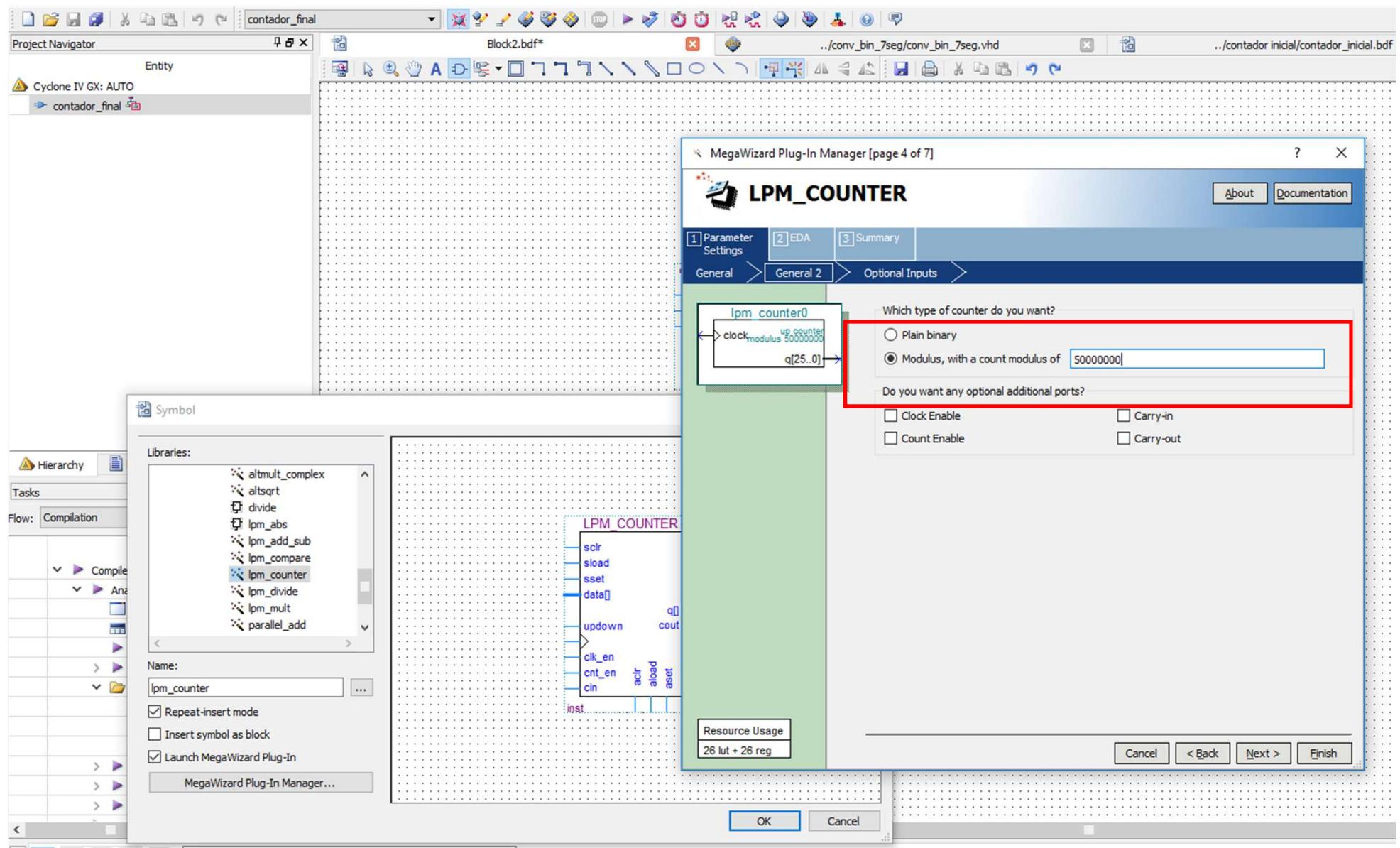
File Edit View Project Assignments Processing Tools Window Help











Project Navigator Entity Cyclone IV GX: AUTO contador_final

Block2.bdf/conv_bin_7seg/conv_bin_7seg.vhd/contador inicial/contador_inicial.bdf

MegaWizard Plug-In Manager [page 7 of 7]

LPM_COUNTER

1 Parameter Settings 2 EDA 3 Summary

Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.

The MegaWizard Plug-In Manager creates the selected files in the following directory:
C:\Users\Rogério\Documents\eea21\tutorial_placa_cyclone_iv\contador final\

File	Description
<input checked="" type="checkbox"/> lpm_counter0.vhd	Variation file
<input type="checkbox"/> lpm_counter0.inc	AHDL Include file
<input checked="" type="checkbox"/> lpm_counter0.cmp	VHDL component declaration file
<input checked="" type="checkbox"/> lpm_counter0.bsf	Quartus II symbol file
<input type="checkbox"/> lpm_counter0_inst....	Instantiation template file

Cancel < Back Next > Finish

Symbol

Hierarchy

Libraries:

- almult_complex
- altsqrt
- divide
- lpm_abs
- lpm_add_sub
- lpm_compare
- lpm_counter
- lpm_divide
- lpm_mult
- parallel_add

Name: lpm_counter

Repeat-insert mode

Insert symbol as block

Launch MegaWizard Plug-In

MegaWizard Plug-In Manager...

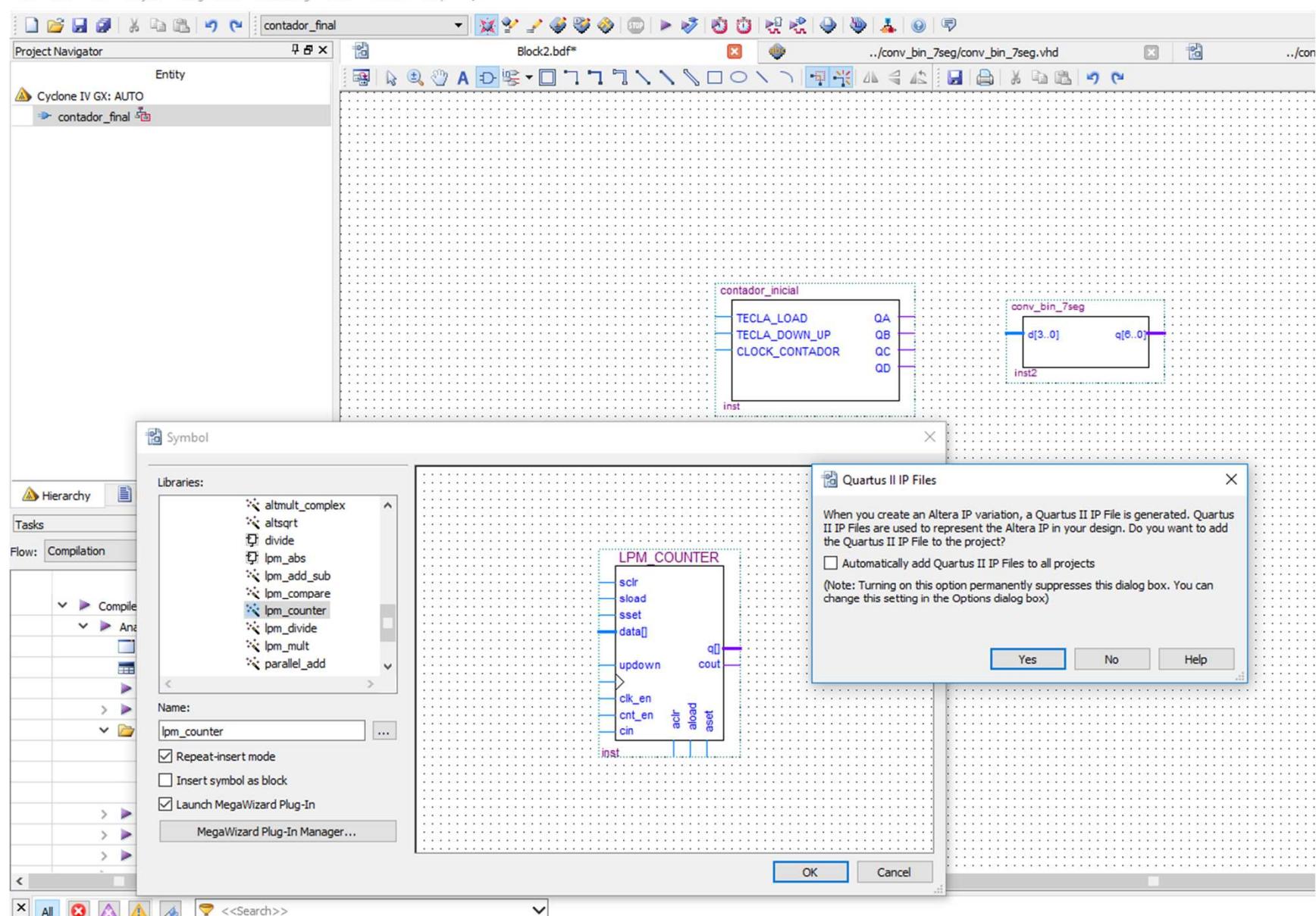
LPM_COUNTER

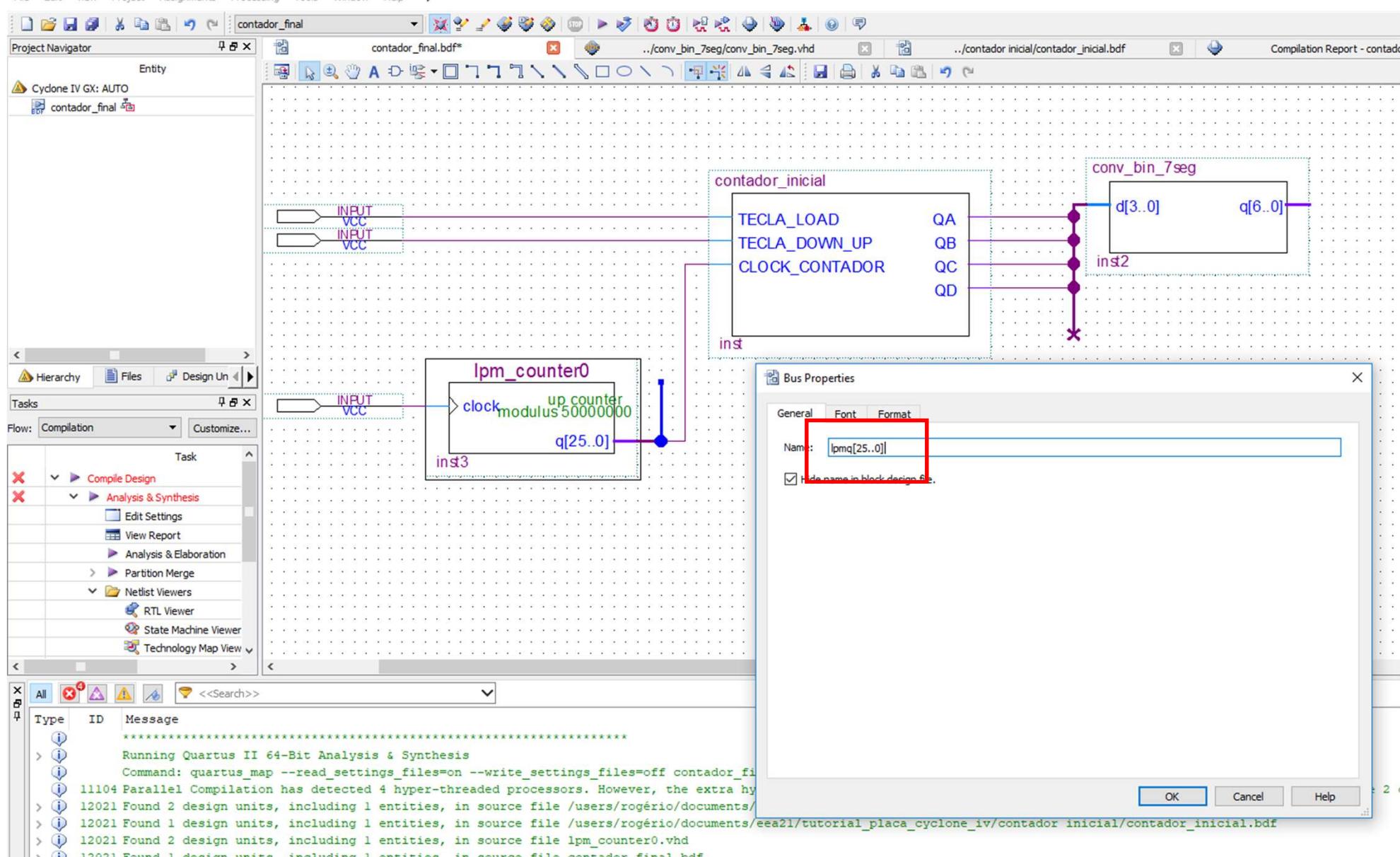
Resource Usage
26 lut + 26 reg

inst sclr sload sset data[] updown clk_en cnt_en cin aclr aload asset cout

Quartus II 64-Bit - C:/Users/Rogério/Documents/eea21/tutorial_placa_cyclone_iv/contador_final/contador_final - contador_final

File Edit View Project Assignments Processing Tools Window Help





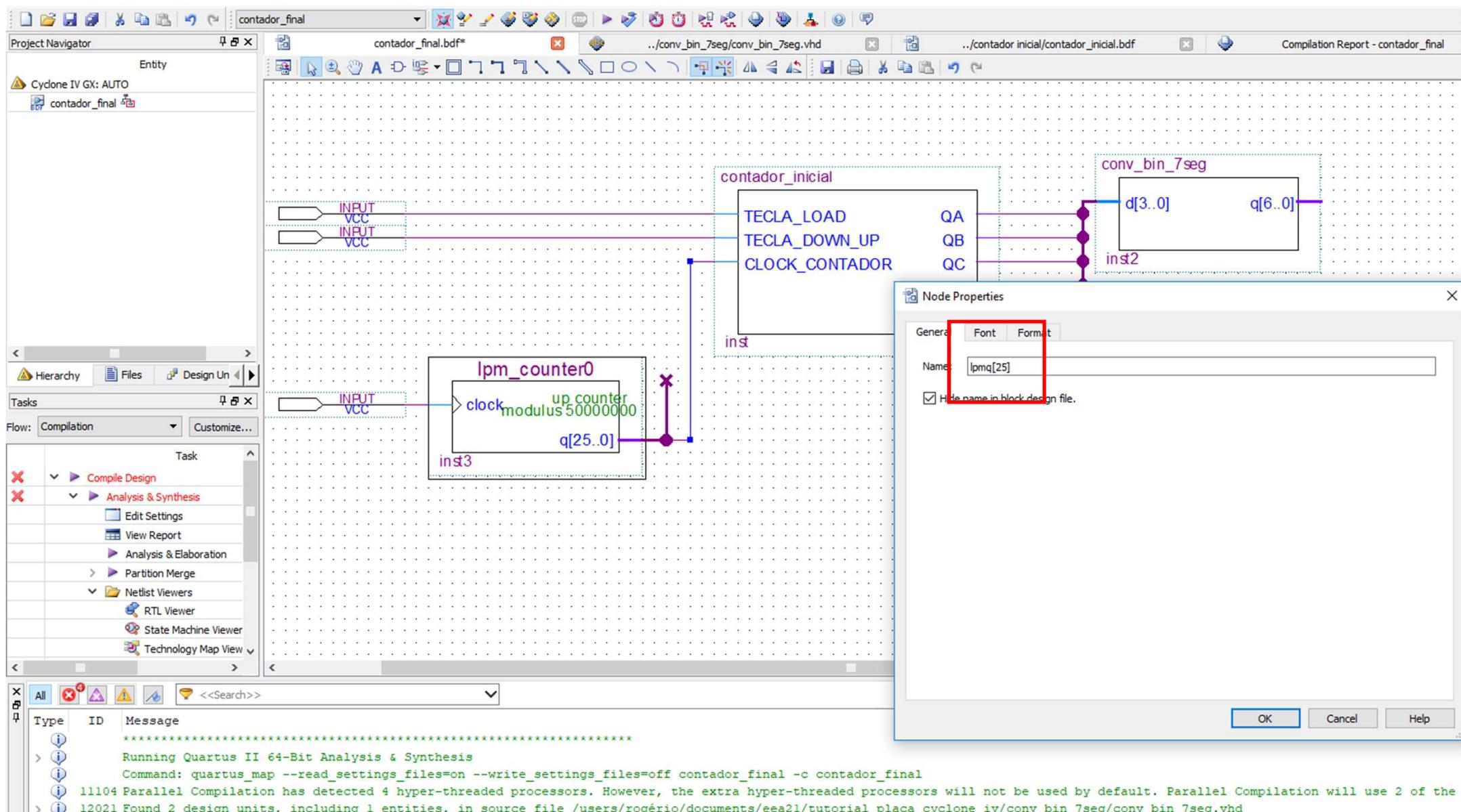
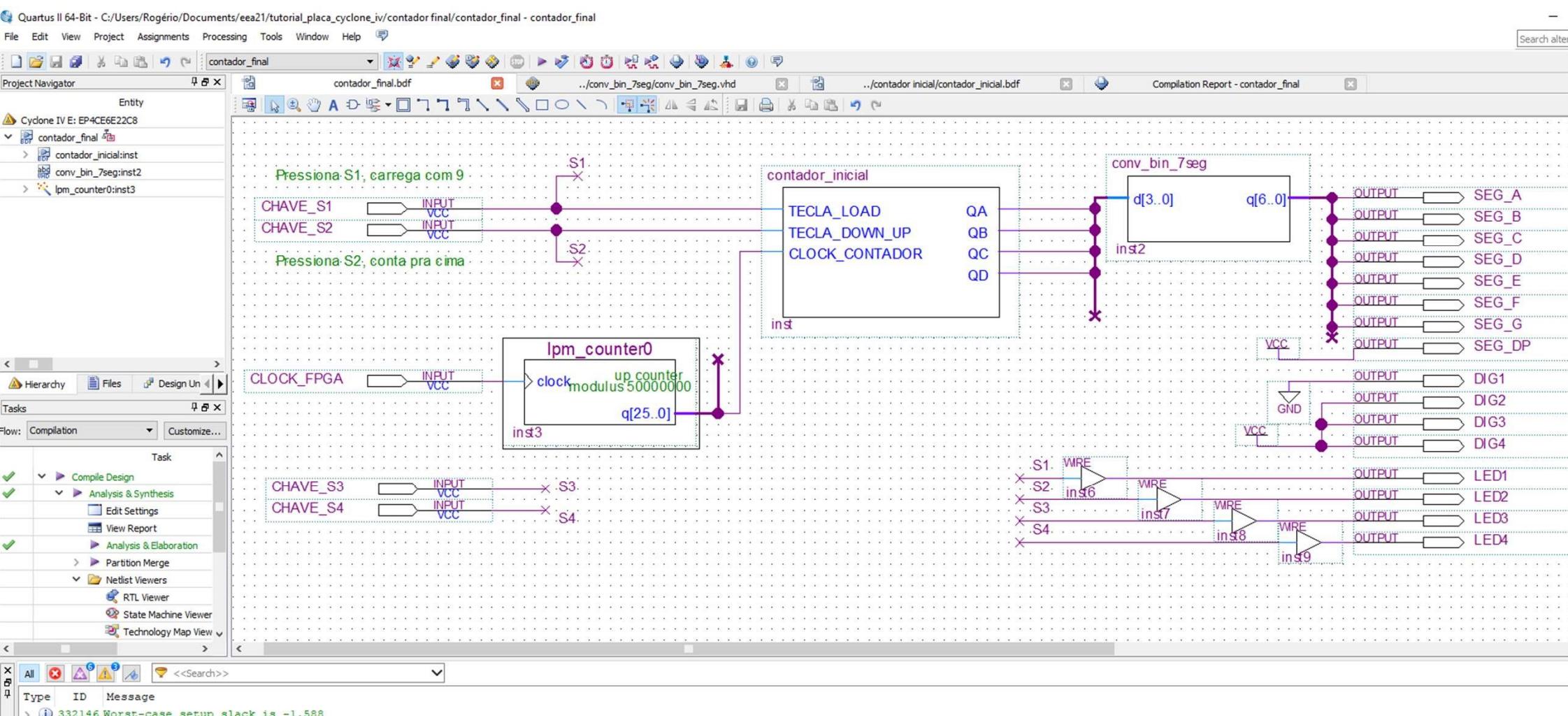


DIAGRAMA FINAL, APÓS LIGAR TODOS OS COMPONENTES



Atribuição dos Números dos Pinos

Pin Planner - C:/Users/Rogério/Documents/eea21/tutorial_placa_cyclone_iv/contador final/contador_final - contador_final

File Edit View Processing Tools Window Help

Groups

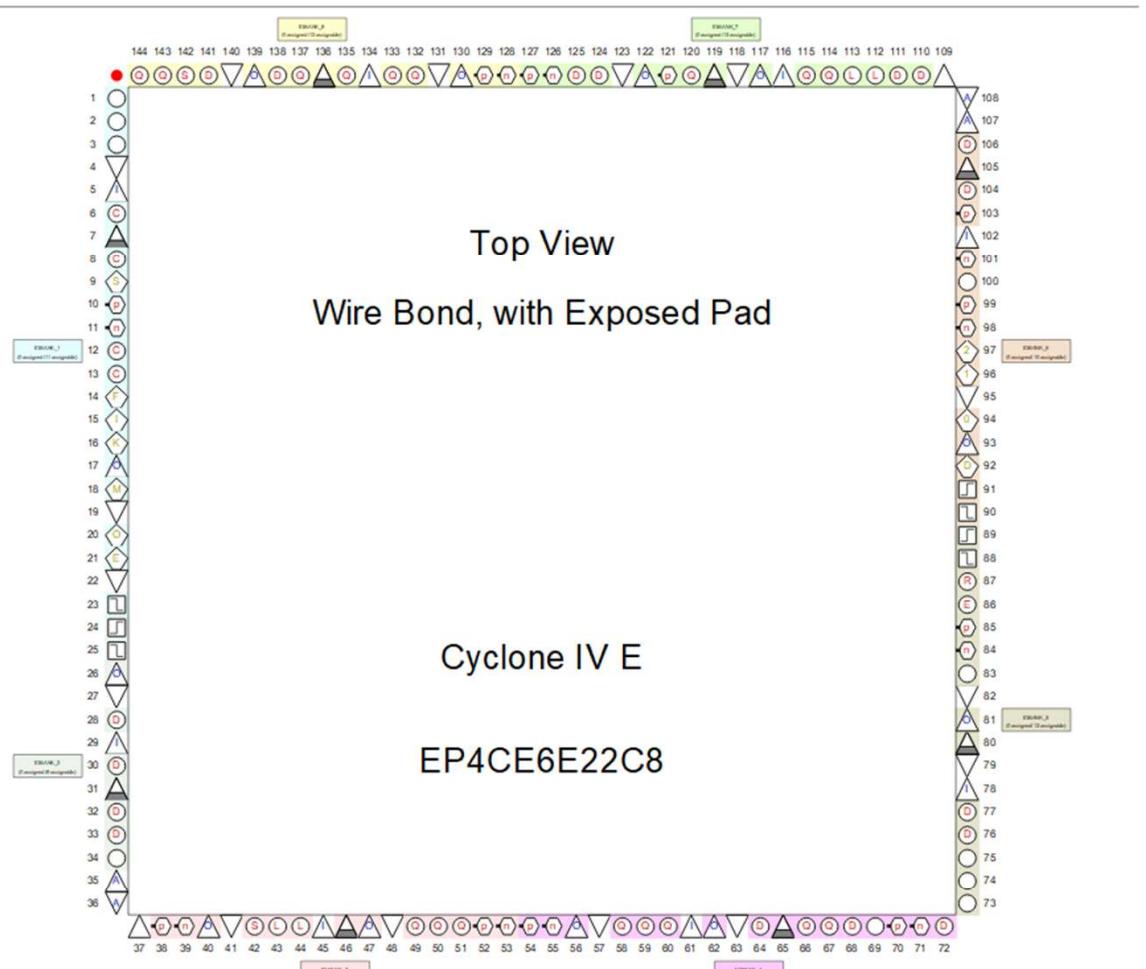
Named: *

Node Name	Direction
<<new group>>	

Tasks

- Run Analysis and Elaboration
- Early Pin Planning
 - Early Pin Planning...
 - Run I/O Assignment Analysis
 - Export Pin Assignments...
- Change View
 - Show I/O Banks
 - Show VREF Groups
 - Show Edges
 - Show DQ/DQS Pins
 - x4 Mode
 - x8 Mode
 - x16 Mode
 - x32 Mode
 - Show Clock Region Input Pins

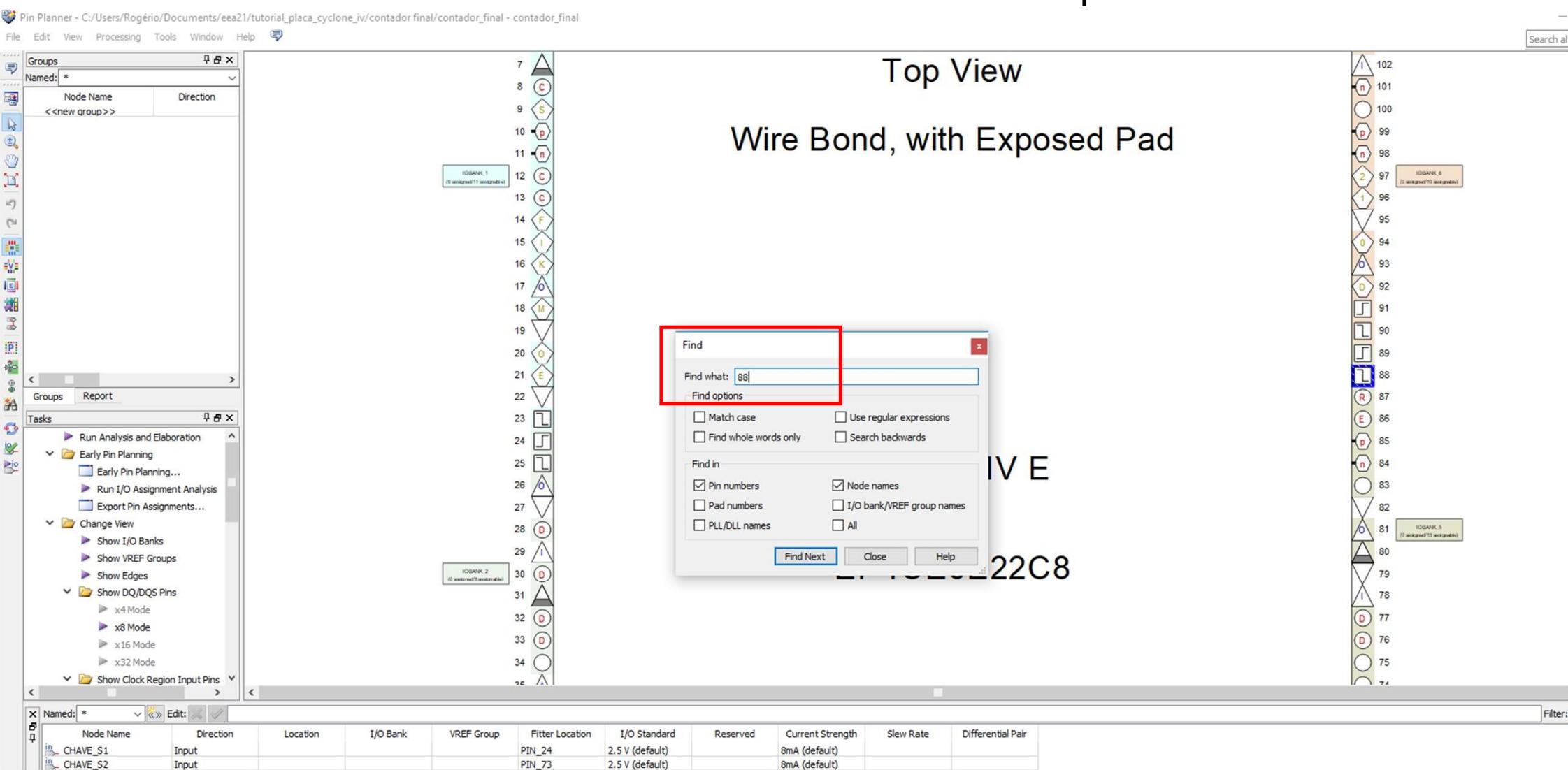
Assignements>Pin Planner



Named: * **Edit:**

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair
in_CHAVE_S1	Input				PIN_24	2.5 V (default)		8mA (default)		
in_CHAVE_S2	Input				PIN_73	2.5 V (default)		8mA (default)		
in_CHAVE_S3	Input				PIN_55	2.5 V (default)		8mA (default)		
in_CHAVE_S4	Input				PIN_132	2.5 V (default)		8mA (default)		
in_CLOCK_FPGA	Input				PIN_23	2.5 V (default)		8mA (default)		
out_DIG1	Output				PIN_44	2.5 V (default)		8mA (default)	2 (default)	
out_DIG2	Output				PIN_100	2.5 V (default)		8mA (default)	2 (default)	

Edit>Find ou clica direto no número do pino



Top View

Wire Bond, with Exposed Pad

Pin Properties
 Pin number: PIN_88
 Node name: CHAVE_S1
 I/O Standard: 2.5 V (default)
 Reserved:

Name	Value
I/O bank	5
VREF group	B5_N0
Edge	RIGHT
General function	Dedicated Clock
Special function	
Pad ID	CLK7
VREF pad ID	DIFFCLK_3n
Input only	Yes
Input of	
PLL_2	Global
Input of	

Find

Find what: 88

Find options

Match case Use regular expressions

Find whole words only Search backwards

Find in

Pin numbers Node names

Pad numbers I/O bank/VREF group names

PLL/DLL names All

Find Next Close Help

Groups

Named: *

Node Name Direction

<<new group>>

Tasks

- Run Analysis and Elaboration
- Early Pin Planning
 - Early Pin Planning...
 - Run I/O Assignment Analysis
 - Export Pin Assignments...
- Change View
 - Show I/O Banks
 - Show VREF Groups
 - Show Edges
- Show DQ/DQS Pins
 - x4 Mode
 - x8 Mode
 - x16 Mode
 - x32 Mode
- Show Clock Region Input Pins

Node Name	Direction	Location	I/O Bank	VREF Group	Filter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair
CHAVE_S1	Input	PIN_88	5	B5_N0	PIN_24	2.5 V (default)		8mA (default)		
CHAVE_S2	Input				PIN_73	2.5 V (default)		8mA (default)		

Todos os pinos assinalados

Project Navigator Entity

- Cyclone IV E: EP4CE6E22C8
 - contador_final
 - contador_inicial:inst
 - conv_bin_7seg:inst2
 - lpm_counter0:inst3

Flow Summary

Flow Status	Successful - Thu May 16 15:35:57 2019
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	contador_final
Top-level Entity Name	contador_final
Family	Cyclone IV E
Device	EP4CE6E22C8
Timing Models	Final
Total logic elements	51 / 6,272 (< 1 %)
Total combinational functions	51 / 6,272 (< 1 %)
Dedicated logic registers	30 / 6,272 (< 1 %)
Total registers	30
Total pins	21 / 92 (23 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)

Hierarchy Files Design Unit

Tasks

Flow: Compilation Customize...

Task

- Compile Design
 - Analysis & Synthesis
 - Edit Settings
 - View Report
 - Analysis & Elaboration
 - Partition Merge
 - Netlist Viewers
 - RTL Viewer

Analizar se a atribuição dos pinos está OK

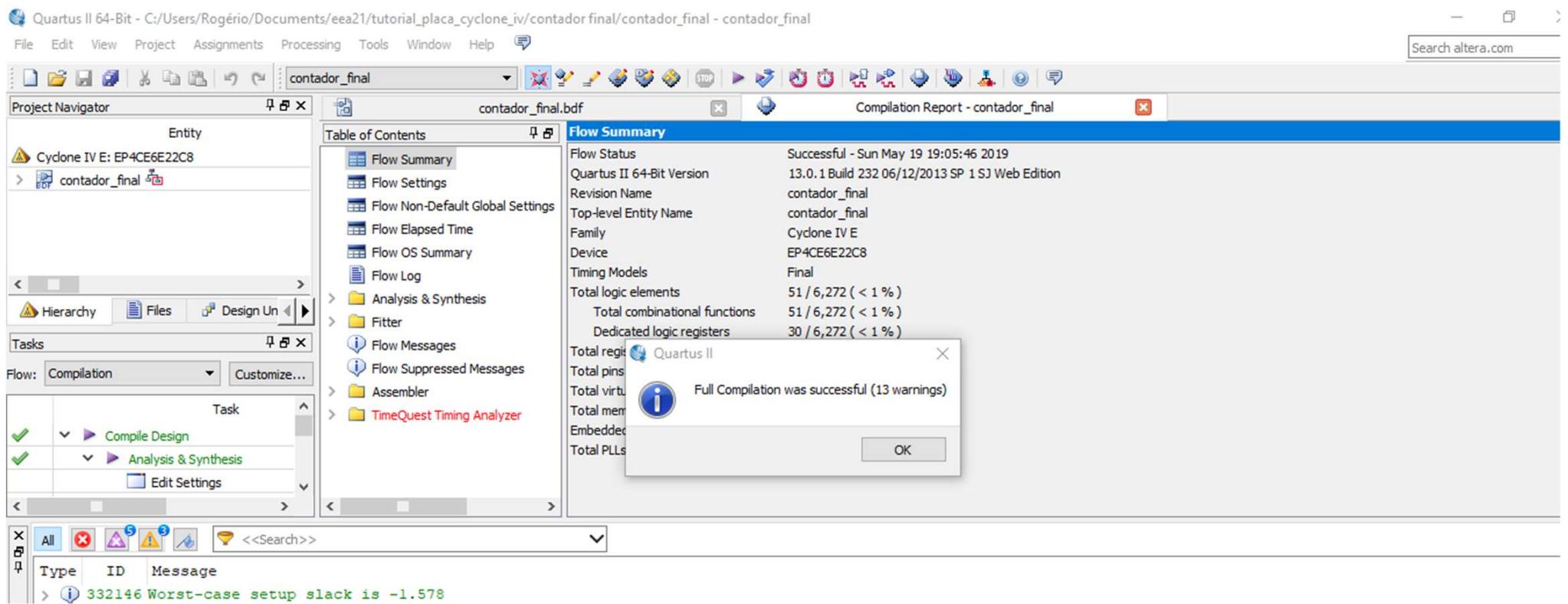
Processing>Start I/O Assignments Analysis

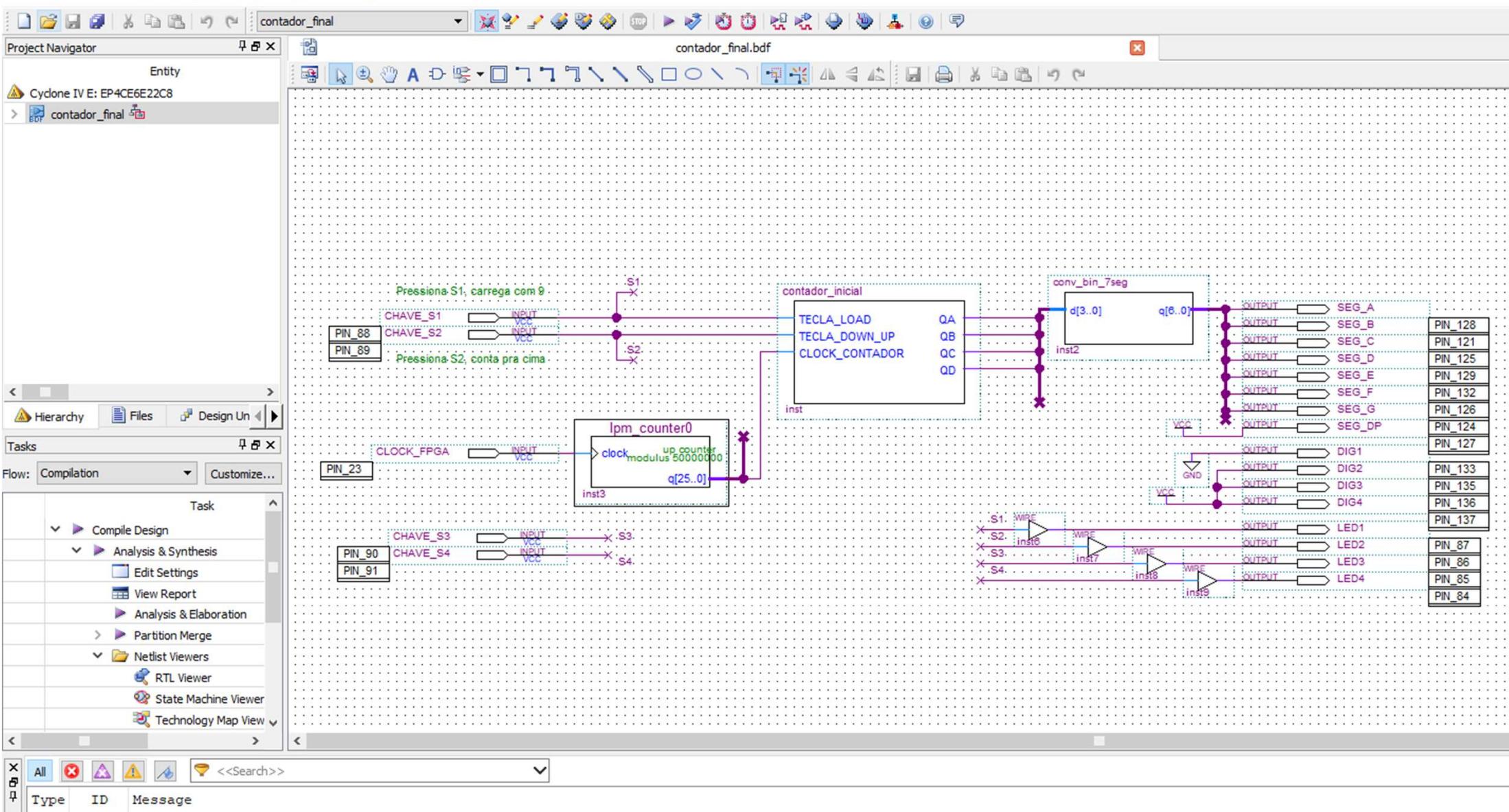
Quartus II

I/O Assignment Analysis was successful (2 warnings)

OK

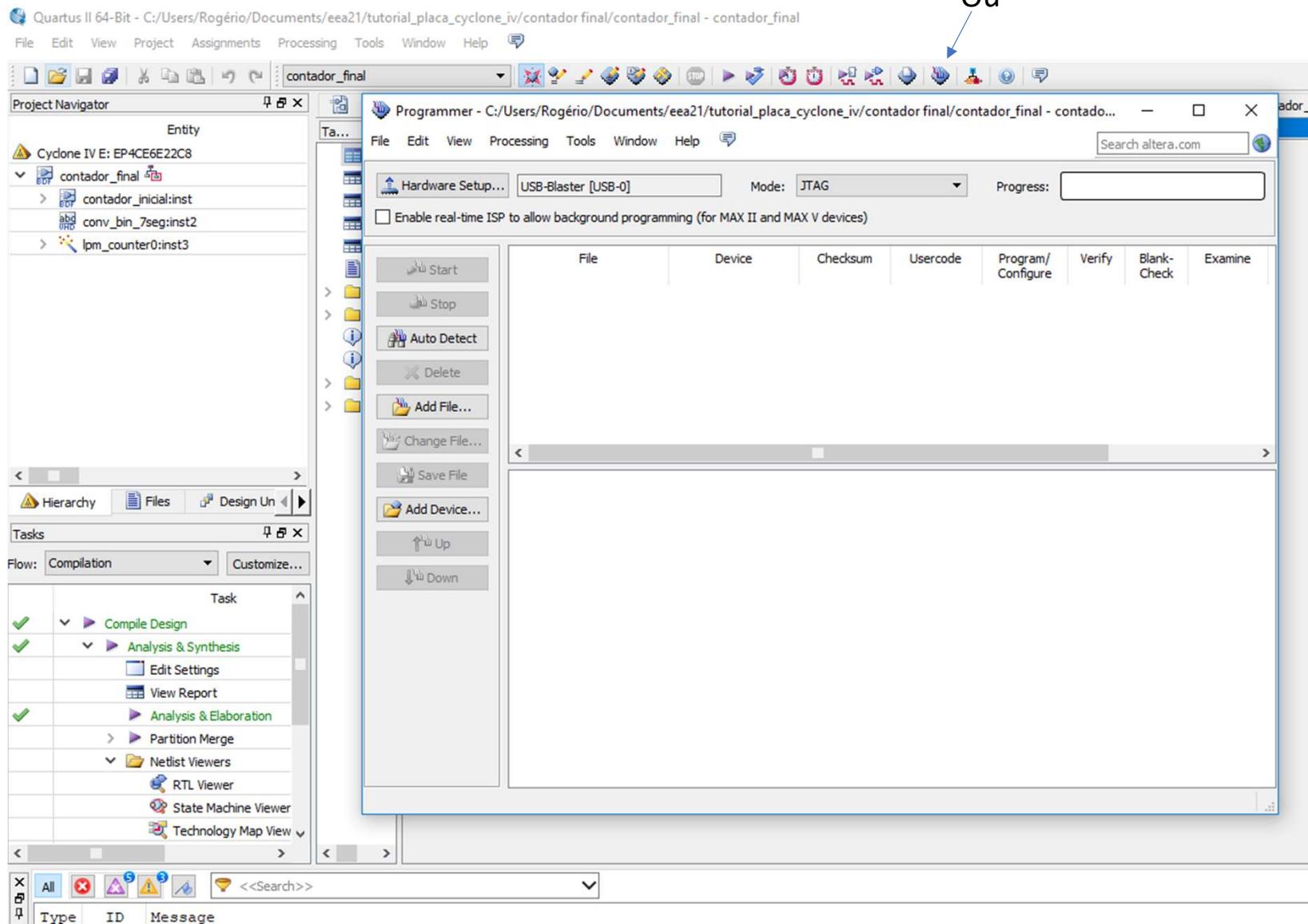
COMPILAR APÓS ASSINALAR/ANALISAR OS PINOS

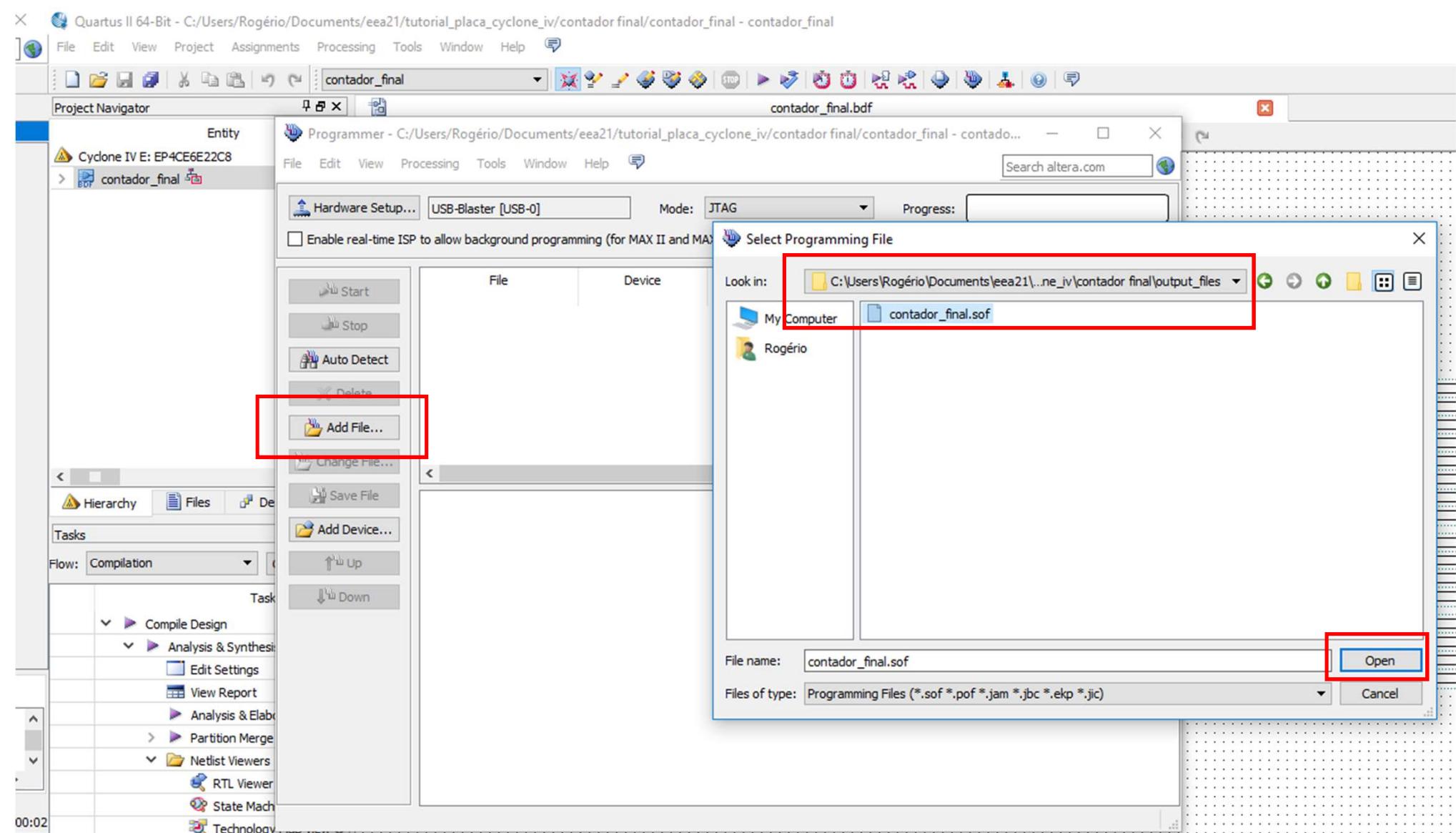




PROGRAMAR A FPGA

Tools>Programmer





Quartus II 64-Bit - C:/Users/Rogério/Documents/eea21/tutorial_placa_cyclone_iv/contador final/contador_final - contador_final

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity
Cyclone IV E: EP4CE6E22C8
contador_final

Programmer - C:/Users/Rogério/Documents/eea21/tutorial_placa_cyclone_iv/contador final/contador_final - contador_final.bdf

File Edit View Processing Tools Window Help Search altera.com

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress:

Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine
output_files/contador_fin...	EP4CE6E22	000997C8	000997C8	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

Hierarchy Files Devices Tasks Flow: Compilation

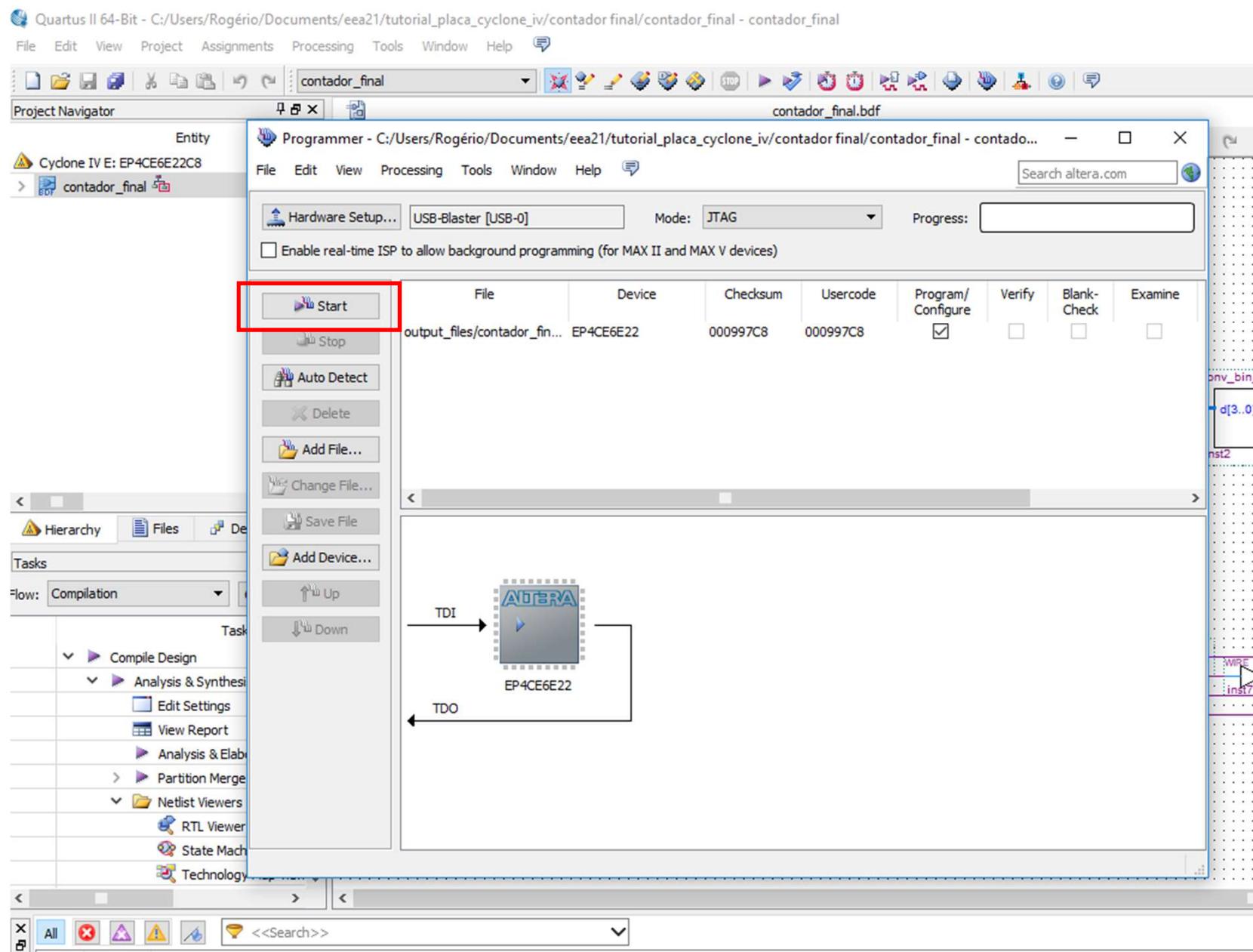
Compile Design Analysis & Synthesis Edit Settings View Report Analysis & Elab Partition Merge Netlist Viewers RTL Viewer State Machine Technology

TDI TDO

ALTERA EP4CE6E22

All <>Search>>

bnv_bin
d[3..0]
inst2
WIRE
inst7



Quartus II 64-Bit - C:/Users/Rogério/Documents/eea21/tutorial_placa_cyclone_iv/contador final/contador_final - contador_final

File Edit View Project Assignments Processing Tools Window Help

