This set of Computer Fundamentals Problems focuses on “Parallel Processing Systems”.

1. Execution of several activities at the same time.
a) processing
b) parallel processing
c) serial processing
d) multitasking
View Answer

Answer: b
Explanation: Execution of several activities at the same time is referred to as parallel processing. Like, Two multiplications at the same time on 2 different processes.
2. Parallel processing has single execution flow.
a) True
b) False
View Answer

Answer: b
Explanation: The statement is false. Sequential programming specifically has single execution flow.
3. A term for simultaneous access to a resource, physical or logical.
a) Multiprogramming
b) Multitasking
c) Threads
d) Concurrency
View Answer

Answer: d
Explanation: Concurrency is the term used for the same. When several things are accessed simultaneously, the job is said to be concurrent.
4. _____ leads to concurrency.
a) Serialization
b) Parallelism
c) Serial processing
d) Distribution
View Answer

Answer: b
Explanation: Parallelism leads naturally to Concurrency. For example, Several processes trying to print a file on a single printer.
5. A parallelism based on increasing processor word size.
a) Increasing
b) Count based
c) Bit based

d) Bit level
View Answer

Answer: d
Explanation: Bit level parallelism is based on increasing processor word size. It focuses on hardware capabilities for structuring.
6. A type of parallelism that uses micro architectural techniques.
a) instructional
b) bit level
c) bit based
d) increasing
View Answer

Answer: a
Explanation: Instructional level uses micro architectural techniques. It focuses on program instructions for structuring.
7. MIPS stands for?
a) Mandatory Instructions/sec
b) Millions of Instructions/sec
c) Most of Instructions/sec
d) Many Instructions / sec
View Answer

Answer: b
Explanation: MIPS stands for Millions of Instructions/sec. MIPS is a way to measure the cost of computing.
8. The measure of the “effort” needed to maintain efficiency while adding processors.
a) Maintainablity
b) Efficiency
c) Scalabilty
d) Effectiveness
View Answer

Answer: c
Explanation: The measure of the “effort” needed to maintain efficiency while adding processors is called as scalabilty.
9. The rate at which the problem size need to be increased to maintain efficiency.
a) Isoeffciency
b) Efficiency
c) Scalabilty
d) Effectiveness
View Answer

Answer: a

Explanation: Isoefficiency is the rate at which the problem size need to be increased to maintain efficiency.
10. Several instructions execution simultaneously in _____
a) processing
b) parallel processing
c) serial processing
d) multitasking
View Answer

Answer: b
Explanation: In parallel processing, the several instructions are executed simultaneously.

PIPELINING

1. _____ have been developed specifically for pipelined systems.
a) Utility software
b) Speed up utilities
c) Optimizing compilers
d) None of the mentioned
View Answer

Answer: c
Explanation: The compilers which are designed to remove redundant parts of the code are called as optimizing compilers.
2. The pipelining process is also called as _____
a) Superscalar operation
b) Assembly line operation
c) Von Neumann cycle
d) None of the mentioned
View Answer

Answer: b
Explanation: It is called so because it performs its operation at the assembly level.
3. The fetch and execution cycles are interleaved with the help of _____
a) Modification in processor architecture
b) Clock
c) Special unit
d) Control unit
View Answer

Answer: b
Explanation: The time cycle of the clock is adjusted to perform the interleaving.
4. Each stage in pipelining should be completed within _____ cycle.

a) 1
b) 2
c) 3
d) 4
View Answer

Answer: a
Explanation: The stages in the pipelining should get completed within one cycle to increase the speed of performance.
5. In pipelining the task which requires the least time is performed first.
a) True
b) False
View Answer

Answer: b
Explanation: This is done to avoid starvation of the longer task.
6. If a unit completes its task before the allotted time period, then _____
a) It'll perform some other task in the remaining time
b) Its time gets reallocated to a different task
c) It'll remain idle for the remaining time
d) None of the mentioned
View Answer

Answer: c
Explanation: None.
7. To increase the speed of memory access in pipelining, we make use of _____
a) Special memory locations
b) Special purpose registers
c) Cache
d) Buffers
View Answer

Answer: c
Explanation: By using the cache we can reduce the speed of memory access by a factor of 10.
8. The periods of time when the unit is idle is called as _____
a) Stalls
b) Bubbles
c) Hazards
d) Both Stalls and Bubbles
View Answer

Answer: d
Explanation: The stalls are a type of hazards that affect a pipelined system.
9. The contention for the usage of a hardware device is called _____

a) Structural hazard
b) Stalk
c) Deadlock
d) None of the mentioned
View Answer

Answer: a
Explanation: None.
10. The situation wherein the data of operands are not available is called _____
a) Data hazard
b) Stock
c) Deadlock
d) Structural hazard
View Answer

Answer: a
Explanation: Data hazards are generally caused when the data is not ready on the destination side.

Which of the following is not a solution of branch difficulties?

(A) Prefetch target instruction
(B) Loop buffer
(C) Delayed branch
(D) Branch buffer

Answer

(D)

Delayed load & Delayed branch can be solutions of pipeline conflict in which two pipelines?

(A) Instruction pipeline & Arithmetic pipeline
(B) RISC pipeline & Instruction pipeline
(C) RISC pipeline & Arithmetic pipeline
(D) Only RISC pipeline

Answer

(B)

Which is one of the major characteristics of RISC in concept of pipelining?

(A) Overlapped register window
(B) Few addressing modes
(C) Single-cycle instruction execution

(D) Hardwired control

Answer

(C)

Which is used in the field of Medical diagnosis, Seismic data analysis & Image processing?

(A) Scalar processing
(B) Vector processing
(C) RISC pipeline
(D) All of above

Answer

(B)

HAZARDS

This set of Computer Organization online quiz focuses on “Hazards of Processor Architecture”.

1. Any condition that causes a processor to stall is called as _____
a) Hazard
b) Page fault
c) System error
d) None of the mentioned
View Answer

Answer: a
Explanation: An hazard causes a delay in the execution process of the processor.
2. The periods of time when the unit is idle is called as _____
a) Stalls
b) Bubbles
c) Hazards
d) Both Stalls and Bubbles
View Answer

Answer: d
Explanation: The stalls are a type of hazards that affect a pipe-lined system.
3. The contention for the usage of a hardware device is called _____
a) Structural hazard
b) Stalk
c) Deadlock
d) None of the mentioned
View Answer

Answer: a
Explanation: The processor contends for the usage of the hardware and might enter into a deadlock state.
4. The situation wherein the data of operands are not available is called _____
a) Data hazard
b) Stock
c) Deadlock
d) Structural hazard
View Answer

Answer: a
Explanation: Data hazards are generally caused when the data is not ready on the destination side.
5. The stalling of the processor due to the unavailability of the instructions is called as _____
a) Control hazard
b) structural hazard
c) Input hazard
d) None of the mentioned
View Answer

Answer: a
Explanation: The control hazard also called as instruction hazard is usually caused by a cache miss.
6. The time lost due to the branch instruction is often referred to as _____
a) Latency
b) Delay
c) Branch penalty
d) None of the mentioned
View Answer

Answer: c
Explanation: This time also retards the performance speed of the processor.
7. The pipeline bubbling is a method used to prevent data hazard and structural hazards.
a) True
b) False
View Answer

Answer: a
Explanation: The periods of time when the unit is idle is called a Bubble.
8. _____ method is used in centralized systems to perform out of order execution.
a) Scorecard
b) Score boarding

c) Optimizing
d) Redundancy
View Answer

Answer: b
Explanation: In a scoreboard, the data dependencies of every instruction are logged. Instructions are released only when the scoreboard determines that there are no conflicts with previously issued and incomplete instructions.
9. The algorithm followed in most of the systems to perform out of order execution is _____
a) Tomasulo algorithm
b) Score carding
c) Reader-writer algorithm
d) None of the mentioned
View Answer

Answer: a
Explanation: The Tomasulo algorithm is a hardware algorithm developed in 1967 by Robert Tomasulo from IBM. It allows sequential instructions that would normally be stalled due to certain dependencies to execute non-sequentially (out-of-order execution).
10. The problem where process concurrency becomes an issue is called as _____
a) Philosophers problem
b) Bakery problem
c) Bankers problem
d) Reader-writer problem
View Answer

Answer: d
Explanation: None.

MULTIPROCESSOR

Multiprocessors are classified as _____.

(A) SIMD
(B) MIMD
(C) SISD
(D) MISD

Answer

(B)

Full-form of VLSI?

(A) Very large scale integration

(B) Very least scale instructions
(C) Variety of large & small instructions
(D) Very long scalable integration

Answer

(A)

Which one is not benefit of multiprocessors?

(A) Multiple independent jobs can be made to operate in parallel
(B) A single job can be partitioned into multiple parallel tasks
(C) Multiple jobs can be made to operate in serial
(D) All are benefits

Answer

(C)

What is another name of tightly coupled multiprocessor?

(A) Distributed memory processors
(B) Mutually coupled processors
(C) Binding memory processors
(D) Shared memory processors

Answer

(D)

What is another name of loosely coupled multiprocessor?

(A) Distributed memory processors
(B) Shared memory processors
(C) Mutually coupled processors
(D) Binding memory processors

Answer

(A)

Which of the following is not characteristics of tightly coupled multiprocessors?

(A) Each processor has its own cache memory
(B) One global common memory that all CPUs can access
(C) Each processor has its own local memory
(D) Shared memory processors

Answer

(C)

Which of the following is not characteristics of loosely coupled multiprocessors?

(A) Processors are tied together by a switching scheme
(B) They don’t use packets to transfer data
(C) Distributed memory processors
(D) Each processor has its own local memory

Answer

(B)

Which of the following is not one of the interconnection structures?

(A) Crossbar switch
(B) Hypercube system
(C) Single port memory
(D) Time-shared common bus

Answer

(C)

In time-shared common bus, when one processor is communicating with the memory, what all other processors do?

(A) busy with internal operations
(B) must be idle waiting for the bus
(C) interrupt the working processor
(D) either A or B

Answer

(D)

Full-form of MM in multiport memory & crossbar switch?

(A) Memory module
(B) Multiport module
(C) Multiport memory
(D) Main Memory

Answer

(A)

A processor does not require _____ bus to communicate with memory.

(A) address
(B) interrupt
(C) data

(D) control

Answer

(B)

What is the advantage of multiport memory organization?

(A) Simple construction
(B) Less hardware needed
(C) High transfer rate
(D) None of above

Answer

(C)

Disadvantage of multiport memory organization is that it has _____.

(A) low transfer rate
(B) non-priority based system
(C) small number of connectors
(D) expensive memory control

Answer

(D)

How many buses/cables are required to establish multiport memory organization between 7 CPUs & 5 MMs?

(A) 35
(B) 42
(C) 40
(D) 37

Answer

(B)

Which combinational device is used in crossbar switch for selecting proper memory from multiple addresses?

(A) Multiplexer
(B) Decoder
(C) Encoder
(D) Demultiplexer

Answer

(A)

How many switch points are there in crossbar switch network that connects 9 processors to 6 memory modules?

(A) 50
(B) 63
(C) 60
(D) 54

Answer

(D)

Which method is used as an alternative way of snooping-based coherence protocol?

(A) Directory protocol
(B) Memory protocol
(C) Compiler based protocol
(D) None of above

Answer

(A)

Which of the following is not proper method for the solution of cache coherence problem?

(A) Write through with update protocol
(B) Write through with invalidation protocol
(C) Write through with deletion protocol
(D) All are valid

Answer

(C)

Which mechanism performs an analysis on the code to determine which data items may become unsafe for caching, and they mark those items accordingly?

(A) Directory protocol
(B) Snoopy protocol
(C) Server based cache coherence
(D) Compiler based cache coherence

Answer

(D)

1. What is the high speed memory between the main memory and the CPU called?
a) Register Memory
b) Cache Memory
c) Storage Memory

d) Virtual Memory
View Answer

Answer: b
Explanation: It is called the Cache Memory. The cache memory is the high speed memory between the main memory and the CPU.
2. Cache Memory is implemented using the DRAM chips.
a) True
b) False
View Answer

Answer: b
Explanation: The Cache memory is implemented using the SRAM chips and not the DRAM chips. SRAM stands for Static RAM. It is faster and is expensive.
3. Whenever the data is found in the cache memory it is called as _____
a) HIT
b) MISS
c) FOUND
d) ERROR
View Answer

Answer: a
Explanation: Whenever the data is found in the cache memory, it is called as Cache HIT. CPU first checks in the cache memory since it is closest to the CPU.
4. LRU stands for _____
a) Low Rate Usage
b) Least Rate Usage
c) Least Recently Used
d) Low Required Usage
View Answer

Answer: c
Explanation: LRU stands for Least Recently Used. LRU is a type of replacement policy used by the cache memory.
5. When the data at a location in cache is different from the data located in the main memory, the cache is called _____
a) Unique
b) Inconsistent
c) Variable
d) Fault
View Answer

Answer: b
Explanation: The cache is said to be inconsistent. Inconsistency must be avoided as it leads to serious data bugs.
6. Which of the following is not a write policy to avoid Cache Coherence?
a) Write through
b) Write within
c) Write back

d) Buffered write
View Answer

Answer: b
Explanation: There is no policy which is called as the write within policy. The other three options are the write policies which are used to avoid cache coherence.
7. Which of the following is an efficient method of cache updating?
a) Snoopy writes
b) Write through
c) Write within
d) Buffered write
View Answer

Answer: a
Explanation: Snoopy writes is the efficient method for updating the cache. In this case, the cache controller snoops or monitors the operations of other bus masters.
8. In _____ mapping, the data can be mapped anywhere in the Cache Memory.
a) Associative
b) Direct
c) Set Associative
d) Indirect
View Answer

Answer: a
Explanation: This happens in the associative mapping. In this case, a block of data from the main memory can be mapped anywhere in the cache memory.
9. The number of sign bits in a 32-bit IEEE format is ____
a) 1
b) 11
c) 9
d) 23
View Answer

Answer: a
Explanation: There is only 1 sign bit in all the standards. In a 32-bit format, there is 1 sign bit, 8 bits for the exponent and 23 bits for the mantissa.
10. The transfer between CPU and Cache is _____
a) Block transfer
b) Word transfer
c) Set transfer
d) Associative transfer
View Answer

Answer: b
Explanation: The transfer is a word transfer. In the memory subsystem, word is transferred over the memory data bus and it typically has a width of a word or half-word.

1) A collection of lines that connects several devices is called .....

A. bus
B. peripheral connection wires
C. Both a and b
D. internal wires

Answer: A. bus

2) A complete microcomputer system consist of .....

A. microprocessor
B. memory
C. peripheral equipment
D. all of the above

Answer: D. all of the above

3) PC Program Counter is also called .....

A. instruction pointer
B. memory pointer
C. data counter
D. file pointer

Answer: A. instruction pointer

4) In a single byte how many bits will be there?

A. 8
B. 16
C. 4
D. 32

Answer: A. 8

5) CPU does not perform the operation .....

A. data transfer
B. logic operation
C. arithmetic operation
D. all of the above

Answer: A. data transfer

6) The access time of memory is ..... the time required for performing any single CPU operation.

A. Longer than
B. Shorter than
C. Negligible than
D. Same as

Answer: A. Longer than

7) Memory address refers to the successive memory words and the machine is called as .....

A. word addressable
B. byte addressable
C. bit addressable
D. Terra byte addressable

Answer: A. word addressable

8) A microprogram written as string of 0's and 1's is a .....

A. Symbolic microinstruction
B. binary microinstruction
C. symbolic microinstruction
D. binary micro-program

Answer: D. binary micro-program

9) A pipeline is like .....

A. an automobile assembly line
B. house pipeline
C. both a and b
D. a gas line

Answer: A. an automobile assembly line

10) Data hazards occur when .....

A. Greater performance loss
B. Pipeline changes the order of read/write access to operands
C. Some functional unit is not fully pipelined
D. Machine size is limited

Answer: B. Pipeline changes the order of read/write access to operands

11) Processors of all computers, whether micro, mini or mainframe must have

A. ALU
B. Primary Storage
C. Control unit
D. All of above

Answer: D. All of above

12) What is the control unit's function in the CPU?

A. To transfer data to primary storage
B. to store program instruction
C. to perform logic operations
D. to decode program instruction

Answer: D. to decode program instruction

13) What is meant by a dedicated computer?

A. which is used by one person only
B. which is assigned to one and only one task
C. which does one kind of software
D. which is meant for application software only

Answer: B. which is assigned to one and only one task

14) The most common addressing techiniques employed by a CPU is

A. immediate
B. direct
C. indirect
D. register
E. all of the above

Answer: E. all of the above

15) Pipeline implement

A. fetch instruction
B. decode instruction
C. fetch operand
D. calculate operand
E. execute instruction
F. all of abve

Answer: F. all of abve

16) Which of the following code is used in present day computing was developed by IBM corporation?

A. ASCII
B. Hollerith Code
C. Baudot code
D. EBCDIC code

Answer: D. EBCDIC code

17) When a subroutine is called, the address of the instruction following the CALL instructions stored in/on the

A. stack pointer
B. accumulator
C. program counter
D. Stack

Answer: D. Stack

18) A microprogram written as string of 0's and 1's is a

A. symbolic microinstruction
B. binary microinstruction
C. symbolic microprogram
D. binary microprogram

Answer: D. binary microprogram

19) Interrupts which are initiated by an instruction are

A. internal
B. external
C. hardware
D. Software

Answer: B. external

20) Memory access in RISC architecture is limited to instructions

A. CALL and RET
B. PUSH and POP
C. STA and LDA
D. MOV and JMP

Answer: C. STA and LDA

21) From where interrupts are generated?

A) Central processing unit
B) Memory chips
C) Registers
D) I/O devices

Answer: D) I/O devices

22) The output of a gate is low when at least one of its input is low . It is true for

A) AND gate
B) OR gate
C) NAND gate
D) NOR gate

Answer: A)AND gate

23) Which one of the following is most suitable to make a parity checker

A) AND gate
B) OR gate
C) Exclusive- OR gate
D) None of the above

Answer: C) Exclusive- OR gate

24) What is the minimum number of flip-flops required in a counter to count 100 pulses?

A) Five
B) seven
C) Ten
D) hundred

Answer: B) seven

25. For a RS flip-flop constructed with NAND gates and input R=1 and s=1 the state is

A) Memory state
B) Set state
C) Reset state
D) Unused state

Answer: D) Unused state

26. The advantage of RISC processor over CISC processor is that

A) The hardware architecture is simpler
B) An instruction can be executed in one cycle
C) Less number of registers accommodate in chip
D) Parallel execution capabilities

Answer: B) An instruction can be executed in one cycle

27. Which of the following is true about interrupts?

A) They are generated when memory cycles are stolen
B) They are used in place of data channels
C) They can be generated by arithmetic operation
D) They can indicate completion of an I/O operation

Answer: A) They are generated when memory cycles are stolen

28. Te devices connected to a microprocessor can use the data bus:

A) all the time
B) at regular interval of time
C) only when it's sending or receiving data
D) when the microprocessor is reset

Answer: C) only when it's sending or receiving data

29. Intel 8080 microprocessor has an instruction set of 91 instruction. The opcode to implement this instruction set should be at least

A) 3 bit long
B) 5 bit long
C) 7 bit long
D) 9 bit long

Answer: C) 7 bit long

30. Dynamic RAMs are best suited to

A) slow system
B) large system
C) one bit system
D) none of the above

Answer: A) slow system

31. Intel Pentium CPU is a

A. RISC based
B. CISC based
C. Both of the above
D. None of the above

Answer: A. RISC based

32. A modem is used to link up two computers via

A. telephone line
B. dedicated line
C. Both of the above
D. None of the above

Answer: C. Both of the above

33. The maximum integer which can be stored on a 8 bit accumulator is
A. 112
B. 200
C. 255

D. 224

Answer: C. 255

34. In a system with a 16 bit address bus, what is the maximum number of 1K byte memory devices it could contain

A. 16
B. 64
C. 256
D. 65536

Answer: C. 256

35. Which of the following memories in a computer is volatile?

A. RAM
B. ROM
C. EPROM
D. ALL

Answer: A. RAM

36. A peripheral is

A. any drives installed in the computer
B. tapedrive connected to a computer
C. any physical device connected to the computer
D. None of above

Answer: C. any physical device connected to the computer

37. How many bits do you think will be adequate to encode individual character in Devnagari script

A. 12
B. 16
C. 64
D. 10

Answer: D. 10

38. Which of the following bus is used to transfer data from main memory to peripheral device?

A. DMA bus
B. Output bus
C. Data bus
D.All of the above

Answer: C. Data bus

39. To provide increased memory capacity for operating system, the

A. virtual memory is created
B. cache memory is increased
C. memory for OS is reserved
D. Additional memory is installed

Answer: A. virtual memory is created

40. CD -RAW is

A. Input device only
B. output device only
C. Both of the above
D. None of the above

Answer: B. output device only

41. Which of the following require large computer memory?

A. Imaging
B. Graphics
C. Voice
D. All of the above

Answer: D. All of the above

42. Which major development led to the production of microcomputers?

A. Magnetic disks
B. floppy disks
C. Logic gates
D. Integrated Circuits

Answer: D. Integrated Circuits

43. In immediate addressing the operand is placed

A. in the CPU register
B. after opcode in the instruction
C. in the memory
D. in the stack

Answer: B. after opcode in the instruction

44. Micro instructions are stored in

A. computer memory

B. primary storage
C. secondary storage
D. control memory
E. cache memory

Answer: D. control memory

45. Pipeline processing implement

A. fetch instruction
B. decode instruction
C. fetch operand
D. calculate operand
E. execute instruction
F. all of the above

Answer: F. all of the above

46. The 16- bit registers in 8085 is

A. general purpose register
B. accumulator
C. stack pointer and program counter
D. all of the above

Answer: C. stack pointer and program counter

47. Instruction pipelining has minimum stages

A. 4
B. 2
C. 3
D. 6

Answer: B. 2

48. Systems that do not have parallel processing capabilities are

A. SISD
B. SIMD
C. MIMD
D. All of the above

Answer: A. SISD

49. The word size of the microprocessor refers to

A. the amount of a information that can be stored in a byte
B. the amount of a information that can be stored in a cycle

C. The number of machine operations performed in a second
D. the maximum length of an English word that can be input to a computer

Answer: B. the amount of a information that can be stored in a cycle

50. How many address lines are needed to address each memory location in a 2048X 4 memory chip?

A. 10
B. 11
C. 8
D. 12

Answer: B. 11

51. Who is regarded as the founder of Computer Architecture?

A. Alan Turing
B. Konrad Zuse
C. John von Neumann
D. John William Mauchly
E. None of the answers above is correct

Answer: C. John von Neumann

52. What is characteristic for the organization of a computer architecture?

A. Size
B. Dynamic behaviour
C. Static behaviour
D. Speed
E. None of the answers above is correct

Answer: B. Dynamic behaviour

53. What is usually regarded as the von Neumann Bottleneck?

A. Processor/memory interface
B. Control unit
C. Arithmetic logical unit
D. Instruction set
E. None of the answers above is correct

Answer: A. Processor/memory interface

54. How does the number of transistors per chip increase according to Moore ´s law?

A. Quadratically
B. Linearly
C. Cubicly

D. Exponentially
E. None of the answers above is correct

Answer: D. Exponentially

55. Who is regarded as the founder of Computer Science?

A. Alan Turing
B. Konrad Zuse
C. J. Presper Eckert
D. John William Mauchly
E. None of the answers above is correct

Answer: A. Alan Turing

56. Which is the fastest storage unit in a usual memory hierarchy?

A. Cache
B. Main memory
C. Hard disk
D. Register
E. None of the answers above is correct

Answer: D. Register

57. Which cache miss does not occur in case of a fully associative cache ?

A. Conflict miss
B. Capacity miss
C. Compulsory miss
D. Cold start miss
E. None of the answers above is correct

Answer: A. Conflict miss

58. Which miss even occurs in infinite caches?

A. Coherence miss
B. Capacity miss
C. Conflict miss
D. Cold start miss
E. None of the answers above is correct

Answer: D. Cold start miss

59. What is stored in a Translation Lookaside Buffer?

A. System dumps
B. Physical addresses

C. rogram data
D. Operating system log files
E. None of the answers above is correct

Answer: B. Physical addresses

60. Which value has the speedup of a parallel program that achieves an efficiency of 75% on 32 processors?

A. 18
B. 24
C. 16
D. 20
E. None of the answers above is correct

Answer: B. 24

61. Pipelining strategy is called implement

A. instruction execution
B. instruction prefetch
C. instruction decoding
D. instruction manipulation

Answer: B. instruction prefetch

62. The concept of pipelining is most effective in improving performance if the tasks being performed in different stages :

A. require different amount of time
B. require about the same amount of time
C. require different amount of time with time difference between any two tasks being same
D. require different amount with time difference between any two tasks being different

Answer: B. require about the same amount of time

63) Which Algorithm is better choice for pipelining?

A. Small Algorithm
B. Hash Algorithm
C. Merge-Sort Algorithm
D. Quick-Sort Algorithm

Answer: C. Merge-Sort Algorithm

64. The expression 'delayed load' is used in context of

A. processor-printer communication
B. memory-monitor communication
C. pipelining

D. none of the above

Answer: C. pipelining

65. Parallel processing may occur

A. in the instruction stream
B. in the data stream
C. both[A] and [B]
D. none of the above

Answer: C. both[A] and [B]

66. The cost of a parallel processing is primarily determined by :

A. Time Complexity
B. Switching Complexity
C. Circuit Complexity
D. None of the above

Answer: C. Circuit Complexity

67. An instruction to provide small delay in program

A. LDA
B. NOP
C. BEA
D. None of the above

Answer: B. NOP

68. Characteristic of RISC (Reduced Instruction Set Computer) instruction set is

A. three instructions per cycle
B. two instructions per cycle
C. one instruction per cycle
D. none of the

Answer: C. one instruction per cycle

69. In daisy-chaining priority method, all the devices that can request an interrupt are connected in

A. parallel
B. serial
C. random
D. none of the above

Answer: B. serial

70. Which one of the following is a characteristic of CISC (Complex Instruction Set Computer)

A. Fixed format instructions
B. Variable format instructions
C. Instructions are executed by hardware
D. None of the above

Answer: B. Variable format instructions

71. During the execution of the instructions, a copy of the instructions is placed in the _____ .

A. Register
B. RAM
C. System heap
D. Cache

Answer: D. Cache

72. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster ?

A. A
B. B
C. Both take the same time
D. Insuffient information

Answer: A. A

73. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ .

A. Super-scaling
B. Pipe-lining
C. Parallel Computation
D. None of these

Answer: B. Pipe-lining

74. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution ?

A. ISA
B. ANSA
C. Super-scalar
D. All of the above

Answer: C. Super-scalar

75. The clock rate of the processor can be improved by,

A. Improving the IC technology of the logic circuits
B. Reducing the amount of processing done in one step
C. By using overclocking method
D. All of the above

Answer: D. All of the above

76. An optimizing Compiler does,

A. Better compilation of the given piece of code.
B. Takes advantage of the type of processor and reduces its process time.
C. Does better memory managament.
D. Both a and c

Answer: B. Takes advantage of the type of processor and reduces its process time.

77. The ultimate goal of a compiler is to,

A. Reduce the clock cycles for a programming task.
B. Reduce the size of the object code.
C. Be versatile.
D. Be able to detect even the smallest of errors.

Answer: A. Reduce the clock cycles for a programming task.

78. SPEC stands for,

A. Standard Performance Evaluation Code.
B. System Processing Enhancing Code.
C. System Performance Evaluation Corporation.
D. Standard Processing Enhancement Corporation.

Answer: C. System Performance Evaluation Corporation.

79. As of 2000, the reference system to find the performance of a system is _____ .

A. Ultra SPARC 10
B. SUN SPARC
C. SUN II
D. None of these

Answer: A. Ultra SPARC 10

80. When Performing a looping operation, the instruction gets stored in the _____.

A. Registers
B. Cache

C. System Heap
D. System stack

Answer: B. Cache

81. The average number of steps taken to execute the set of instructions can be made to be less than one by following _____ .

A. ISA
B. Pipe-lining
C. Super-scaling
D. Sequential

Answer: C. Super-scaling

82. If a processor clock is rated as 1250 million cycles per second, then its clock period is _____ .

A. 1.9 * 10 ^ -10 sec
B. 1.6 * 10 ^ -9 sec
C. 1.25 * 10 ^ -10 sec
D. 8 * 10 ^ -10 sec

Answer: D. 8 * 10 ^ -10 sec

83. If the instruction, Add R1,R2,R3 is executed in a system which is pipe-lined, then the value of S is (Where S is term of the Basic performance equation)

A. 3
B. ~2
C. ~1
D. 6

Answer: C. ~1

84. CISC stands for,

A. Complete Instruction Sequential Compilation
B. Computer Integrated Sequential Compiler
C. Complex Instruction Set Computer
D. Complex Instruction Sequential Compilation

Answer: C. Complex Instruction Set Computer

85. As of 2000, the reference system to find the SPEC rating are built with _____ Processor.

A. Intel Atom SParc 300Mhz
B. Ultra SPARC -IIi 300MHZ
C. Amd Neutrino series
D. ASUS A series 450 Mhz

Answer: B. Ultra SPARC -IIi 300MHZ

86. The CISC stands for

A. Computer Instruction Set Compliment
B. Complete Instruction Set Compliment
C. Computer Indexed Set Components
D. Complex Instruction set computer

Answer: D. Complex Instruction set computer

87. The computer architecture aimed at reducing the time of execution of instructions is _____.

A. CISC
B. RISC
C. ISA
D. ANNA

Answer: B. RISC

88. The Sun micro systems processors usually follow _____ architecture.

A. CISC
B. ISA
C. ULTRA SPARC
D. RISC

Answer: D. RISC

89. The RISC processor has a more complicated design than CISC.

A. True
B. False

Answer: B. False

90. The iconic feature of the RISC machine among the following are

a) Reduced number of addressing modes
b) Increased memory size
c) Having a branch delay slot
d) All of the above

Answer: c) Having a branch delay slot

91. Both the CISC and RISC architectures have been developed to reduce the_____.

A. Cost

B. Time delay
C. Semantic gap
D. All of the above

Answer: C. Semantic gap

92. Out of the following which is not a CISC machine.

A. IBM 370/168
B. VAX 11/780
C. Intel 80486
D. Motorola A567

Answer: D. Motorola A567

93. Pipe-lining is a unique feature of _____.

A. RISC
B. CISC
C. ISA
D. IANA

Answer: A. RISC

94. In CISC architecture most of the complex instructions are stored in _____.

A. Register
B. Diodes
C. CMOS
D. Transistors

Answer: D. Transistors

95. Which of the architecture is power efficient?

A. CISC
B. RISC
C. ISA
D. IANA

Answer: B. RISC

96. To which class of systems does the von Neumann computer belong?

A. SIMD (Single Instruction Multiple Data)
B. MIMD (Multiple Instruction Multiple Data)
C. MISD (Multiple Instruction Single Data)
D. SISD (Single Instruction Single Data)
E. None of the answers above is correct.

Answer: D. SISD (Single Instruction Single Data)

97. Parallel programs: Which speedup could be achieved according to Amdahl´s law for infinite number of processors if 5% of a program is sequential and the remaining part is ideally parallel?

A. Infinite speedup
B. 5
C. 20
D. 50
E. None of the answers above is correct.

Answer: C. 20

98. Itanium processor: Which hazard can be circumvented by register rotation?

A. Control hazards
B. Data hazards
C. Structural hazards
D. None
E. None of the answers above is correct.

Answer: B. Data hazards

99. Which MIMD systems are best scalable with respect to the number of processors?

A. Distributed memory computers
B. ccNUMA systems
C. nccNUMA systems
D. Symmetric multiprocessors
E. None of the answers above is correct

Answer: A. Distributed memory computers

100. Cache coherence: For which shared (virtual) memory systems is the snooping protocol suited?

A. Crossbar connected systems
B. Systems with hypercube network
C. Systems with butterfly network
D. Bus based systems
E. None of the answers above is correct.

Answer: D. Bus based systems

MEMORY HIERARCHY

The last on the hierarchy scale of memory devices is _____
a) Main memory

b) Secondary memory
c) TLB
d) Flash drives
View Answer

Answer: b
Explanation: The secondary memory is the slowest memory device.
9. In the memory hierarchy, as the speed of operation increases the memory size also increases.
a) True
b) False
View Answer

10. If we use the flash drives instead of the harddisks, then the secondary storage can go above primary memory in the hierarchy.
a) True
b) False
View Answer

Answer: b
Explanation: The flash drives will increase the speed of transfer but still it

_____ have been developed specifically for pipelined systems.

A.
Utility softwares

B.
Speed up utilities

C.
Optimizing compilers

D.
None of the mentioned

Solution:
Answer: c
Explanation: The compilers which are designed to remove redundant parts of the code are called as optimizing compilers.

QUESTION: 2
The pipelining process is also called as _____

A.
Superscalar operation

B.
Assembly line operation

C.
Von neumann cycle

D.
None of the mentioned

Solution:
Answer: b
Explanation: It is called so because it performs its operation at assembly level.

QUESTION: 3
The fetch and execution cycles are interleaved with the help of _____

A.
Modification in processor architecture

B.
Clock

C.
Special unit

D.
Control unit

Solution:
Answer: b
Explanation: The time cycle of the clock is adjusted to perform the interleaving.

QUESTION: 4
Each stage in pipelining should be completed within ____ cycle.

A.
1

B.
2

C.
3

D.
4

Solution:
Answer: a
Explanation: The stages in the pipelining should get completed within one cycle to increase the speed of performance.

QUESTION: 5
In pipelining the task which requires the least time is performed first.

A.
True

B.
False

Solution:
Answer: b
Explanation: This is done to avoid starvation of the longer task.

QUESTION: 6
If a unit completes its task before the allotted time period, then

A.
It'll perform some other task in the remaining time

B.
Its time gets reallocated to different task

C.
It'll remain idle for the remaining time

D.
None of the mentioned

Solution:
QUESTION: 7
To increase the speed of memory access in pipelining, we make use of _____

A.
Special memory locations

B.
Special purpose registers

C.
Cache

D.

Buffers

Solution:
Answer: c
Explanation: By using the cache we can reduce the speed of memory access by a factor of 10.

QUESTION: 8
The periods of time when the unit is idle is called as _____

A.
Stalls

B.
Bubbles

C.
Hazards

D.
Both Stalls and Bubbles

Solution:
Answer: d
Explanation: The stalls are a type of hazards that affect a pipelined system.

QUESTION: 9
The contention for the usage of a hardware device is called as _____

A.
Structural hazard

B.
Stalk

C.
Deadlock

D.
None of the mentioned

Solution:
QUESTION: 10
The situation where in the data of operands are not available is called _____

A.
Data hazard

B.
Stock

C.
Deadlock

D.
Structural hazard

Solution:
Answer: a
Explanation: Data hazards are generally caused when the data is not ready on the destin