6

GENERATOR AND ANALYSER

6.1 STANDARD SIGNAL GENERATOR

It produces a sine wave, the amplitude or frequency of which can be adjusted over a wide range with high degree of accuracy. The output signal may be amplitude modulated or frequency modulated.

The carrier frequency is produced by a stable RF oscillator using LC tank circuit. The frequency of oscillations can be controlled by the frequency range control. In the output amplifier modulation is done, the output of this amplifier is a modulated wave.

Temperature compensating circuits and regulated power supplies are used to increase the frequency stability. Buffer amplifiers are used to provide isolation.

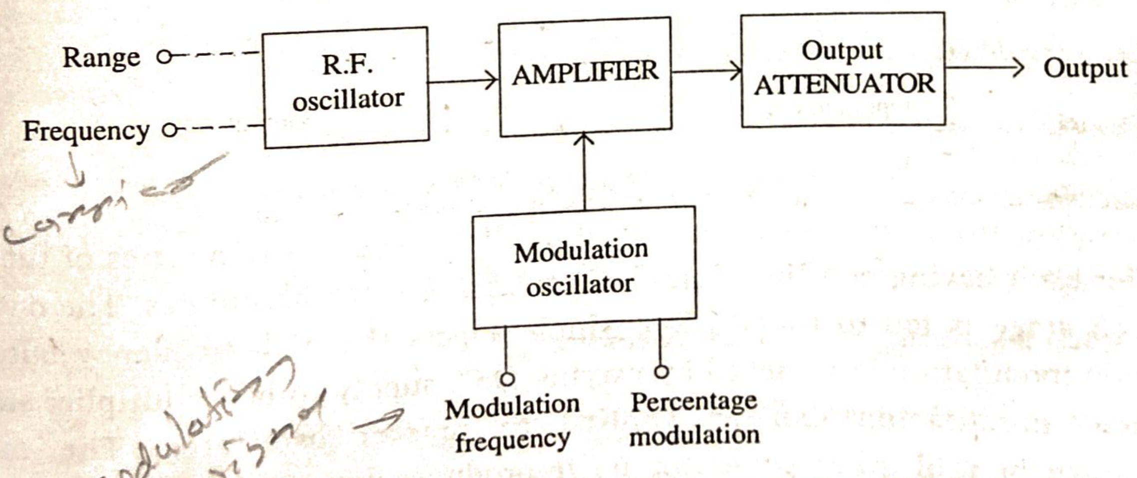


Fig. 6.1 Standard signal generator

Frequency Range : The frequency range of a oscillator can be increased using two techniques.

(a) Heterodyne principle

(b) Multiplier and divider techniques

(a) Heterodyne principle : We can get a wide frequency range using heterodyne principle. We use two oscillators. The output of both the oscillator is given to mixer circuit whose output is equal to difference of two oscillator frequency. Attenuator is used at the output to give a low level output signal.

The signal quality is good but it has poor frequency stability. The output has considerable amount of noise and spurious signal.

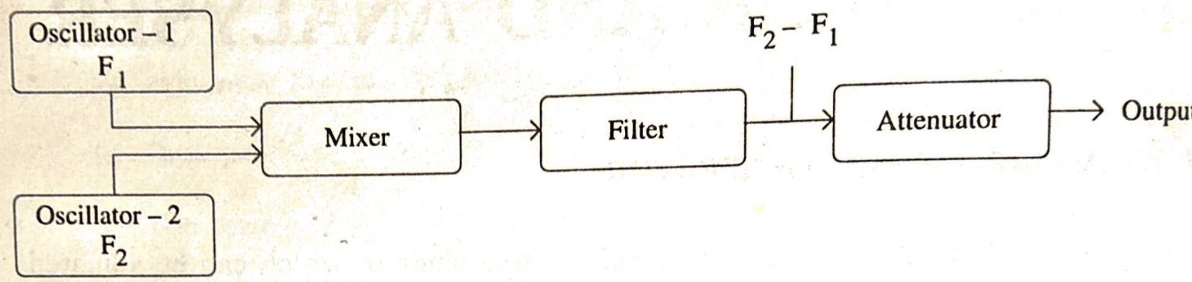


Fig. 6.2 Heterodyne oscillator

Multiplier and divider techniques : This can used to extend the frequency range.

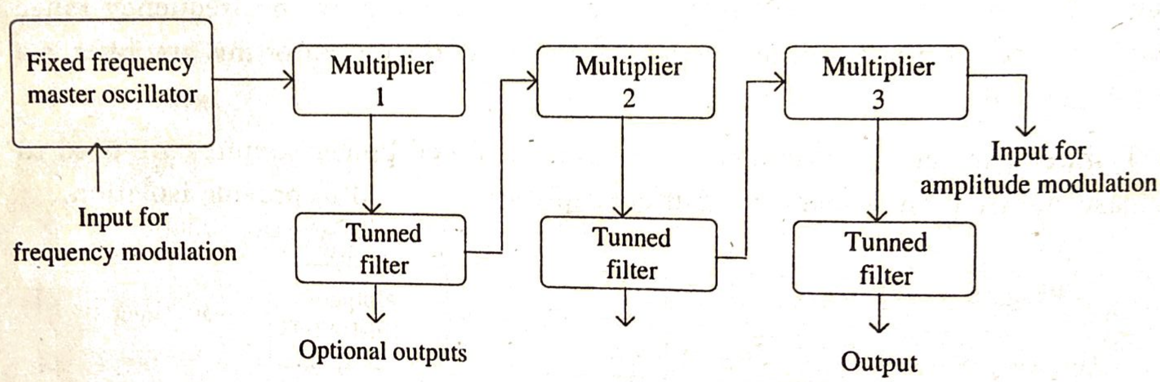


Fig. 6.3 Multiplier frequency generator

The output from fixed frequency tuned oscillator is given to a series of tunned multiplier each having non linear amplifier which produce harmonics. The output from each stage is fed to tuned filter which selects the high frequency output. Amplitude modulation is achieved by varying D.C. supply to last multiplier stage. Frequency modulation can be applied to master oscillator. The main disadvantage of multiplier generator is, it produces large amount of spurious signal around desired frequency.

In divider signal generator high frequency master oscillator is used instead of fixed frequency oscillator. The output of oscillator is divided down by series of electronic stages. The output of divider stage is square wave which when filtered gives sine wave. In this technique frequency modulation is applied to main oscillator while amplitude modulation is obtained by diode modulation in output amplifier. It does not produce any spurious signal around desired frequency.

6.2 SPECTRUM ANALYSER

The study of energy distribution across the frequency spectrum of a electrical signal is called as spectrum analysis. The spectrum analysis gives information about bandwidth, effects of different types of modulation and spurious signal generation. It is useful in design and testing of ratio frequency (RF) and pulse circuitry.

Spectrum analysis is divided into two categories :

(a) Audio frequency (AF) analysis

(b) Radio frequency (RF) analysis

They are capable of portraying graphically the amplitude as a function of frequency. It finds wide application in measurement of attenuation, FM deviation and frequency in pulse studies.

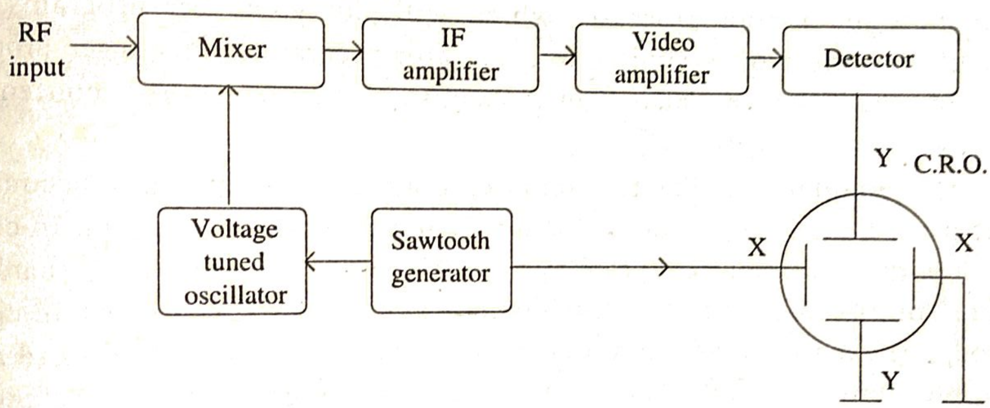


Fig. 6.4 Spectrum analyser

The circuit incorporates sawtooth generator which supplies ramp voltage to frequency control element of voltage tunned local oscillator. Local oscillator sweeps through its frequency band at recurring linear rate. The same sawtooth is applied to horizontal plates of CRO. The RF signal which is to be tested is applied to the input of mixer stage.

The sawtooth generator makes the local oscillator sweep through its frequency band to beat with input signal to produce intermediate frequency to drive IF amplifier. The output of IF amplifier is amplified and detected. After that they are applied to vertical plates of CRO. Hence on CRO screen we get display of amplitude versus frequency.

Emulator : It is a device that allows user program written for one kind of computer system to be run on another system.

A micro programmed control provides a simple, flexible and inexpensive control of a computer. A micro programmed control also provides flexibility in handling of resources and allows implementation of diverse classes of instructions.

Necessity of emulator : A user can create his own instruction set by the use of micro program. Let us consider we add to the instruction set of computer C_1 an entirely new set of instructions which is in fact a instruction set of computer C_2. In this way we could run programs written in the machine language of C_2 on C_1, so we can say C_1 emulates C_2. This is very useful as it allows replacement of absolute equipment with more upto date machines. If the replacement computer fully emulates the original one, then no software changes have to be made to run the existing programs. Emulation is easier when the machine involved have similar architecture.

We may say Emulator is a hardware, microprograms and software added to computer C_1 so that it can execute programs written for a different computer C_2. If only software is used for implementing the above mentioned process then it is called as simulation.

The hardware of emulator consists of control circuitry, memory to store the trace data after each instruction executes and a cable with a plug at the end. The emulator contains a microprocessor which will run your test programs. The software of the emulator is similar to a monitor program or debugger program. Using a emulator we can also debug, examine and change the contents of register and memory locations.

In-circuit Emulator : The in-circuit emulation technique has become an essential part of the design process for microprocessor based products. In-circuit emulation is the execution of a prototype software program in prototype hardware under the control of a software development system. To perform an in-circuit emulation, the microprocessor is removed from the prototype design board and a 40 pin cable from in-circuit emulator is plugged into the previously occupied by the microprocessor. The in-circuit emulator performs all the functions of the replaced microprocessor; in addition, it allows the prototype hardware to share all its resources, such as software, memory and I/Os . It provides a window for looking into the dynamic, real-time operation of the prototype hardware.

Emulation process : To test subsystems (such as I/O and memory) using an in-circuit emulator, the minimum prototype hardware required is a 40 pm microprocessor socket, without the microprocessor, and a power supply.

Features of in-circuit Emulator :

1. An in-circuit emulator is a software/hardware troubleshooting instrument.
2. It can be a stand alone unit or part of a software development system.
3. A small program can be entered directly into the emulator, or a program can be transferred into the emulator from a host computer system through an RS-232 serial link.
4. Once a program is loaded, a user can interact with the emulator through its keyboard or a terminal.
5. The emulator has its own software commands to perform various debugging functions.

Capabilities of Emulator : The main capabilities of emulator are listed as :

1. Down loading
2. Resource sharing
3. Debugging tools : such as
   (a) Break points
   (b) Mnemonic display
   (c) Real-time track
   (d) In-Line Assembly
   (e) Disassembly
   (f) Register Display/Modifications.

Down Loading : Facilities are provided to transfer programs between a software development system or a host computer and in-circuit emulator.

Resource Sharing : The in-circuit emulator allows the system being tested to share its memory and I/O parts. The memory and I/O parts of in-circuit emulator can be assigned any addresses, thus avoiding conflict with memory and I/Os of the prototype; This is called memory and I/O mapping.

Debugging Tools : The debugging tools listed above are used in troubleshooting programs.

Real-Time Trace : The in-circuit emulator has R/W memory used as a buffer to store the last several bus operations, and these can be displayed on the screen. The display is like a snapshot of all bus operations in real time.

In-Line Assembly : This allows the user to change data or instructions while the software is in the in-circuit emulator.

Disassembly : After instructions are changed in the in-circuit emulator, this facility can write mnemonics in software.

Register Display : This display the register contents after the execution of instructions.

ICE 85 Control Board :

The emulator executes the test program and in the case of ICE 85, stores 4 bytes of information for each machine cycle executed in a RAM on the trace board. The 4 bytes stored are status, address byte high, address byte law and data. They are sometimes called **snap data**. For the ICE 85, the snap data for the last 44 machine cycles before a breakpoint is saved in the trace RAM. These snap bytes can be read out or printed to trace the program flow on the address and data buses. Emulator commands allow breakpoints to be set at any point. Programs can be executed at full speed or one step at a time.

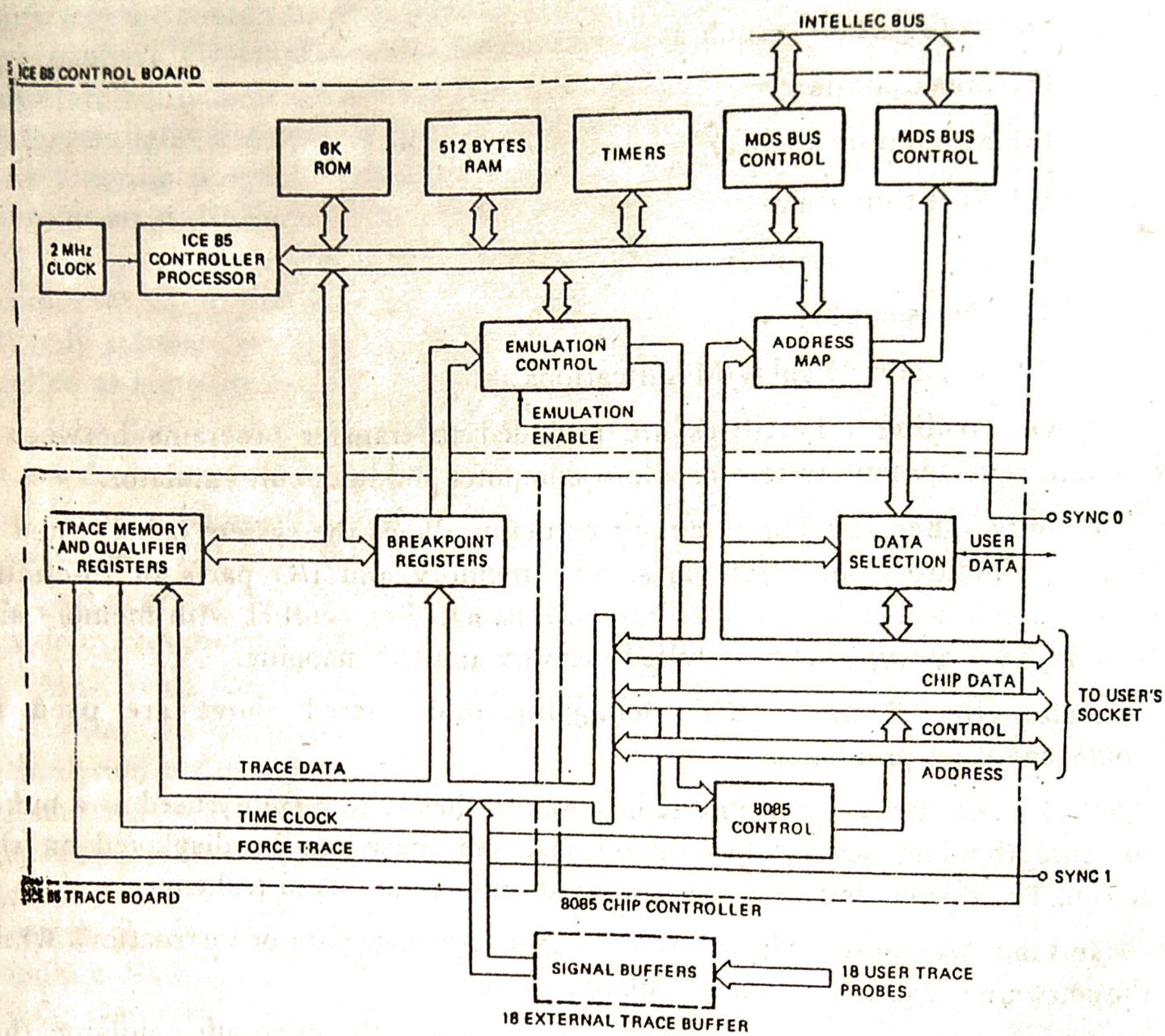


Fig.6.5 Block diagram of ICE 85

Logic analyser : It is a multitrace digital oscilloscope which is used for microprocessor related products. It is also known as logic static analyser. In a multitrace oscilloscope, the timing relationships of several signals can be observed with respect to some other events, for example, in a four trace oscilloscope, we observe the relationship of four signals at a time.

A logic analyser allows to see signals on 16 to 64 signal lines at once. Using a logic analyser one can see the signals on address bus, data bus and control bus of a microcomputer.

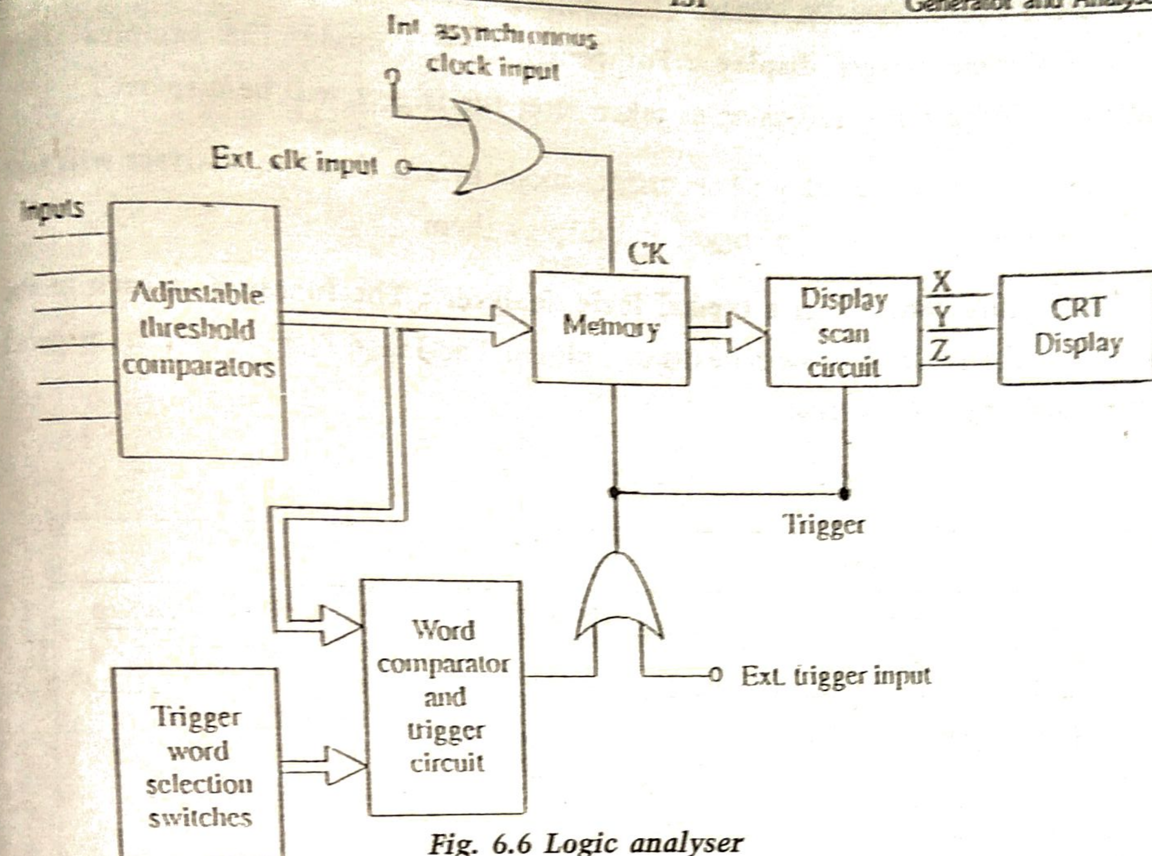


Fig. 6.6 Logic analyser

Logic analysers are used to detect and display only 1's and 0's, a comparator is used for each input. The reference input of the comparator can be adjusted to the logic threshold of the devices in the system. The analyser takes snapshots of the logic level of the input signals and stores them in the internal RAM. The clock signal tells the analyser how often to take the samples. The word recognizer circuit compares the incoming data with the word programmed by the user and it produces a trigger when the two words matches. Snapshots of input data are being taken and written into memory as long as trigger occurs and simultaneously the stored samples are displayed on the CRT.

Types of trigger display : There are three types of trigger display employed in logic analyser.

(a) Pre trigger display

(b) Centre trigger display

(c) Post trigger display.

(a) Pre trigger display : For an analyser that displays 256 samples, pre trigger means that the display will show the 256 samples that were taken just before the trigger occurred.

(b) Centre trigger display : For centre trigger mode, 128 samples taken before the trigger and 128 samples taken after the trigger will be displayed.

(c) Post trigger display : Post trigger mode means that the analyser will take 256 more samples after the trigger and display them.

Operating controls in a typical logic analyser : The function of each of the front panel push button switches is as follows. The Fig. 6.7 shows the front panel of typical logic analyser.

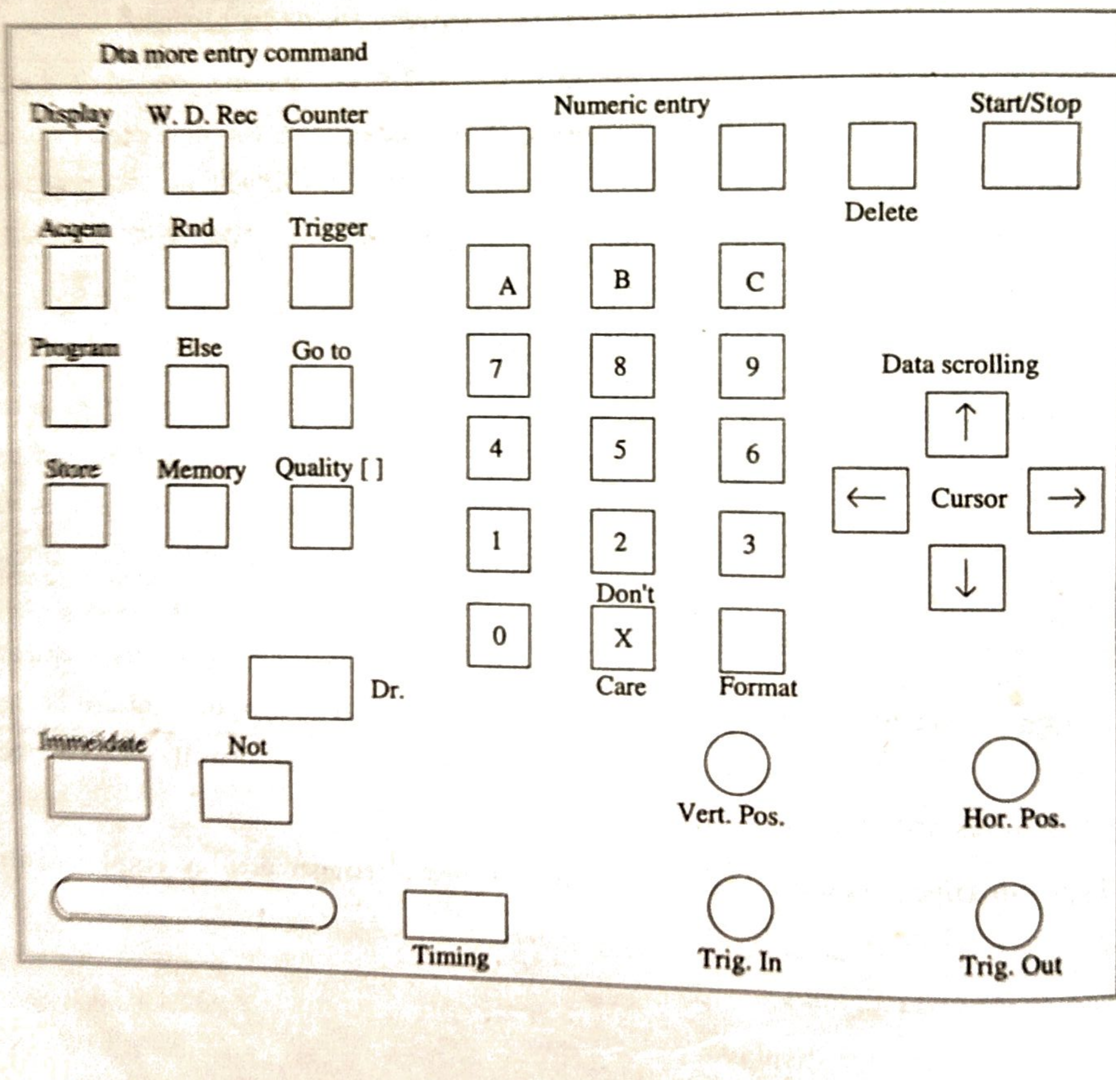


Fig. 6.7

1. "Data movement keys" are used to move information among the equipment memories and to form the display.

2. "EVENT, COMMAND AND STRUCTURE" keys together with the [ ], OR and NOT keys are used to enter the user's programme.

3. "DELETE" key removes unwanted items from the programmes.

4. "START/STOP" keys are used to run or abort execution of the current programme.

5. "DATA SCROLLING" keys are used to move a display "window" through the acquired data or a stored programme.

6. "CURSOR" keys is used to move the blinking cursor around the screen, allowing programs to be entered/detected and parameters to be changed.

7. "Display" key is used to specify the CRT as destination of a data movement command in IMMEDIATE mode. It indicates that the contents of the memory selected as the source of the move are to be displayed in the central display area of the screen. The display key is only valid in the following key stroke sequences :

IMMEDIATE DISPLAY ACQ MEN

IMMEDIATE DISPLAY PROGRAM

IMMEDIATE DISPLAY STORE MEM

The last key stroke in each sequence is the source for the more. As soon as source key is pressed, the source memory is displayed on the screen and a mode change takes place.

QUESTIONS • 6

1. Explain standard signal generator.
2. Explain how we can increase the frequency range of signal generator.
3. Explain the working of spectrum analyser and give its applications.
4. Write short notes on :
   (a) Emulator
   (b) Logic analyser.
5. Explain the working principle of Emulator.
6. Draw block diagram of spectrum Analyser and explain its functioning.

7. Draw block diagram of Logic Analyser and explain its functioning.
8. Explain the working principles of Logic Analyser with the help of a heat diagram.
9. Draw block diagram of Signal Generator and explain its functioning.
10. List specifications of spectrum Analyser.
11. Explain operational features of Emulator.
12. What is Logic Analyser? List its specification where it is used?
13. Explain working principle of spectrum analyser.
14. List specifications of Logic analyser.

7

STUDY OF STANDARD BUSES

7.1 COMMUNICATION

Communication is necessary for the efficient utilization of resources and exchange of information. A computer system may be accessed from terminals placed in user convenient locations. Sometimes the computer may be accessed from different points in a city or even different cities. Sometimes it is necessary to transfer data from one computer to another and sometimes to access the specialized resources of other computers so in all such cases communication is required. Communication can be done in :

(a) Serial form : The data is transferred between the two devices on a single wire. It is economical but the speed of transmission is very less. For long distance communications one should go for serial type.

(b) Parallel form : The data is transferred between the two devices using multiple wires. It is costly but the speed of transmission is more. For short distance communication it is more preferable.

Depending upon the transmission format serial communication is classified into two types :

(a) Synchronous transmission

(b) Asynchronous transmission

(a) Synchronous transmission : In this type of transmission the receiver and transmitter are synchronized. A block of characters is transmitted along with the synchronization information. The speed of transmission is very high. Instead of the start and stop bits, synchronous pluses are transmitted. The time interval between two word is same.

(b) Asynchronous transmission : It is character oriented. Each character carries the information of start and stop bits. When no data is transmitted a receives stays at logic 1 (Mark), logic 0 (space) starts the communication followed by characters and one or two stop bits (high). The speed of transmission is less and time interval between two words is not same.

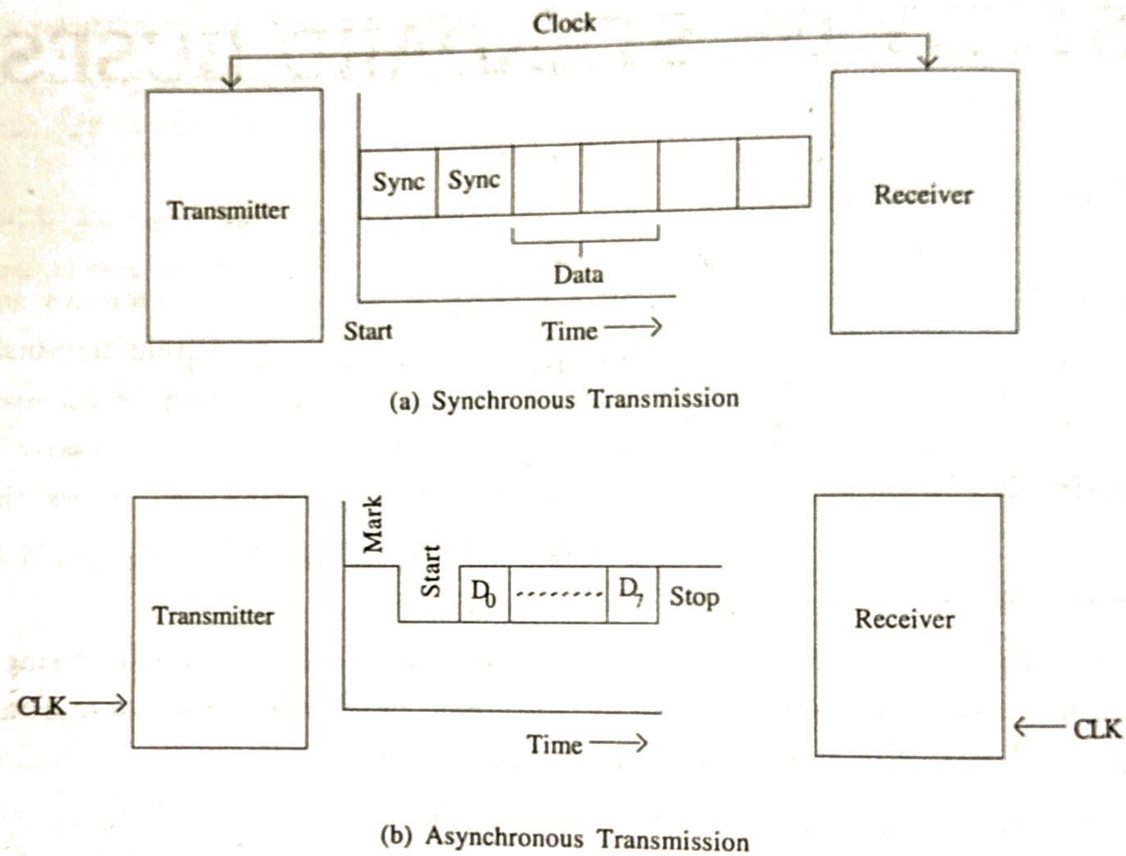


Fig. 7.1 Transmission format

Serial communication is further classified according to the direction of data flow.

(a) Simplex transmission

(b) Duplex transmission

(a) Simplex transmission : In simplex transmission data is transmitted in only one direction. e.g. Transfer of data from micro computer to a printer.

(b) Duplex transmission : In this type of transmission data flows in both the directions. If the transmission takes place only in one direction at a time it is called as half duplex. If the transmission takes place simultaneously in both the directions it is called as full duplex.

Baud : The rate at which bits are transmitted (bits/second) is called as baud. Technically it may be defined as the number of signal changes per second.

7.2 PARITY

Testing whether the transmission is being done correctly or not can be done through the parity bit. The transmitter adds a parity bit depending on the contents of data bits. The receiver checks whether the relation between the parity bit and data bits is correct. If it is not then the receiver sends a error to the transmitter.

Even parity : The total number of ones including the parity bit is even. e.g. If the data to be transmitted is 01000010 so the total number of ones in the data stream is even (2) so the parity bit is set to 0 for even parity.

Odd parity : The total number of ones including the parity bit is odd. e.g. If the data to be transmitted is 01000010 so the total number of ones in the data stream is even (2) so the parity bit is set to 1 for odd parity.

Space or Zero parity : A parity bit is used but it is always set to 0.

Mark parity : Parity bit is always set to 1.

7.3 MODEM

It is a circuit that converts digital data into analog data during transmission and converts analog data into digital data during reception.

Necessity : Two computers can communicate with each other through telephone lines, but telephone lines are designed to handle voice whereas the digital signal has rise time in nanoseconds, so it requires a bandwidth much greater than that of telephone lines. In order to enable the computers use telephone lines there should be a mechanism for converting digital signals into analog signals and vice versa. For this purpose a modern is used.

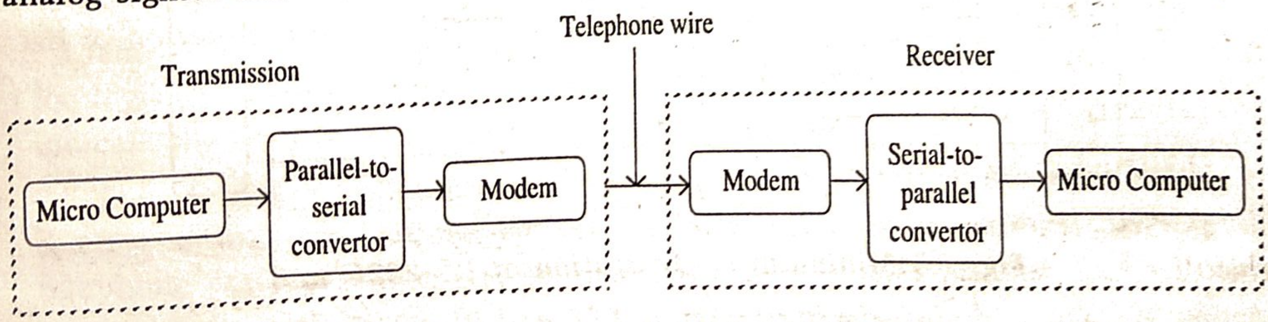


Fig. 7.2 Communication between two computers using modems

A parallel word is converted into serial bits, the modem generates two frequencies for logic 0 and logic 1, these frequencies are transmitted over telephone lines, at the receiving end the audio frequencies are converted into 0 and 1, the serial bits are converted into parallel word using register which can be read by the computer.

7.4 RS 232C

Standards should be developed which define how to interconnect the equipment made by different manufacturers. These standards should define both the physical and functional characteristics of the interface. Standard interface refers to the collection of points at which instruments are connected together. RS–232C the standard developed by Electronics Industry Association has gained wide acceptance.

RS–232C is a data communication standard that defines voltage signals in reference to Data terminal equipment and Data communication equipment. RS–232C specifies 25 signal pins and it specifies that DTE (Data Terminal Equipment) connector should be a male and DCE (Data Communication Equipment) connector should be a female. The voltage levels for all RS–232C signals are as follows. A logic high or mark is a voltage between –3V and –15V. A logic low or space is a voltage between +3V and +15V. Voltages such as ±12V are commonly used. As the voltage levels are not compatible with TTL levels, MC 1488 is used for TTL to RS 232C interface and MC 1489 is used for RS 232C to TTL interface.

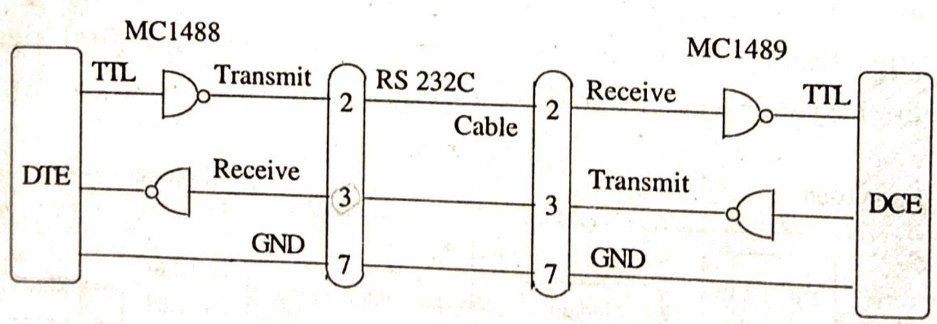


Fig. 7.3 Minimum configuration of RS–232C and interfacing between TTL and RS–232C

MC 1488 converts logic 1 into –9V and logic 0 into +9V. The minimum interface between a computer and peripheral requires three lines. i.e. pin 2,3 and 7 as shown in Fig. 7.3. The DTE terminal transmits on pin 2 and receives on pin 3. On the other DCE terminal transmits on pin 3 and receiver on pin 2. Fig. 7.4 shows signal definitions and pin assignments of RS–232C.

Table : Lists the RS 232C interface signals and the pin designations

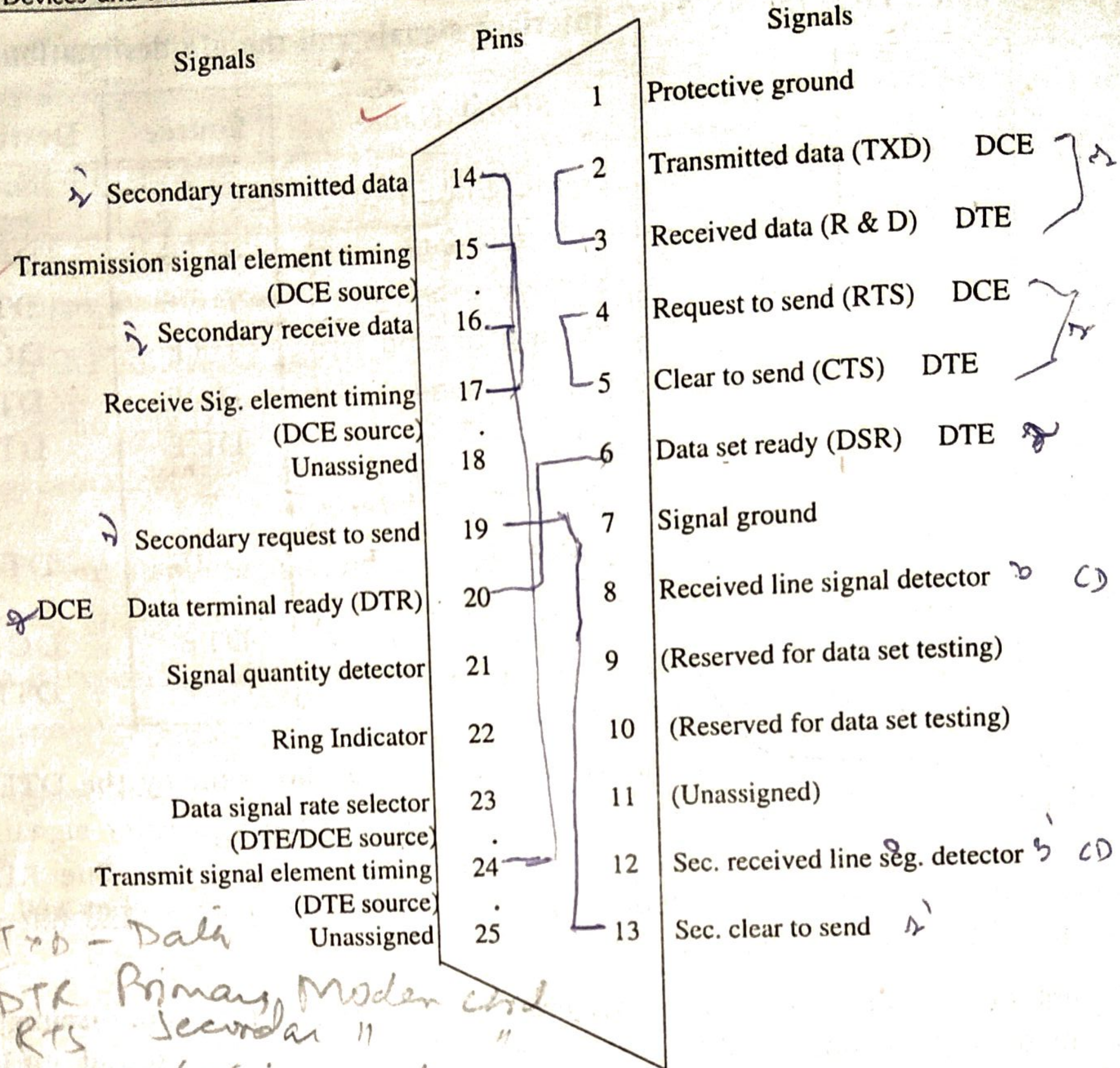
Sr.No.	Pin No.	Signal	Signal Name	Source	Destination
1.	1	–	Frame ground	–	–
2.	2	TXD	Transmit data	DTE	DCE
3.	3	RXD	Receive data	DCE	DTE
4.	4	RTS	Request to send	DTE	DCE
5.	5	CTS	Clear to send	DCE	DTE
6.	6	DSR	Data set ready	DCE	DTE
7.	7	SG	Signal ground	–	–
8.	8	RLSD or CD	Received line signal detect (carrier detect)	DCE	DTE
9.	20	DTR	Data terminal ready	DTE	DCE
10.	22	RI	Ring indicator	DCE	DTE

The TXD is the serial data line carrying the data bits sent by the DTE. The modem receives the TXD signal and uses it for modulating carrier signal. The RXD is the serial data line from DCE (modem) to the DTE. The RDX is generated by the modem by demodulating the signal received on the telephone line from the other end modem.

Before sending data to the other end, the DTE requests for permission from the modem by issuing the RTS signal. The modem has a method to find out if the telephone line is free and if the other end modem is ready. When the modem finds that the communication path (consisting of the telephone line, the other end modem and DTE) is ready for communication, it issues the CTS signal to the DTE as an acknowledgment (sanction for data transmission) for the RTS.

The DTE issues the DTR signal when it is powered-on, error free and ready for logical connection through the modem. The modem issues a DSR signal to indicate that it is powered-on and is error-free.

The RI and RLSD signals are used with the dialled modem. When the telephone line is a shared (switched) line, a dialled modem is used and a telephone set is attached to the modem. When a DTE at one end wants to communicate with a DTE at the other end it initiates a dial sequence. The modem at the sending end sends a dial tone on the telephone line. In response, the called modem issues RI signal to its DTE, and sends an answer tone for 2 sec to the calling modem. Then the calling modem sends an 8 ms duration tone on the telephone line. Now the called modem issues CD (Carrier Detect Signal) to its DTE. The CD is an indication to the DTE that it will soon be receiving the data sent by the other end DTE.



TxD to TxD – Data
DTR to DTR Primary Modem ctrl
RTS to RTS Secondary " "
Gnd – Gnd – Gnd
CTS to CTS Secondary
DCD to CDD – Primary Modem ctrl
RxD from RxD Data

Fig. 7.4 RS 232C signal definitions and pin assignments

7.5 IEEE 488

This bus was developed by Hewlett Packard. It provides an interface between programmable devices like printers, voltmeters, tape recorders etc. It is universally accepted as IEEE 488 standard. It is also known as general purpose interface bus (GPIB) or Hewlett packard interface bus (HPIB).

The important features of this bus are :

(a) Data transfer among the interconnected devices is digital.

(b) A maximum of 15 devices can be connected to one continuous bus.

(c) Transmission path is upto 20 m per device.

(d) Maximum data rate on any signal line is 1mb/sec.

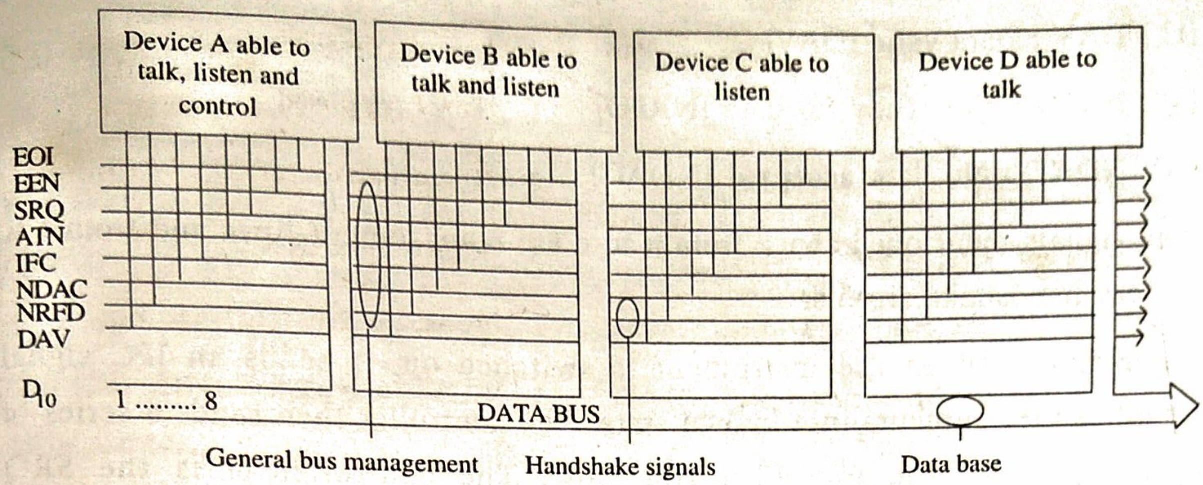


Fig. 7.5 IEEE 488 bus interface

This bus has 24 signals out of which eight are bidirectional data lines, five are bus management lines, three are handshake signals and eight are ground. Fig. 7.5 shows four types of devices connected to the bus. This devices are classified as follows :

(a) Listener : It is a device capable to receive data when addressed. At a time between devices can listen at a time. e.g. Signal generator.

(b) Talker : It is a device capable of transmitting data when addressed. At a given time only one device can act as a talker. e.g. Tape recorder.

(c) Listener/Talker : It is a device capable of transmitting and receiving data over a bus. e.g. Digital voltmeter.

(d) Controller : It is a device which controls the signal over the bus and decides which device can talk and which device should listen.

The function of the various signal lines are as follows :

(a) IFC : The interface clear (IFC) line, it resets all the devices on the bus to a starting state. It is similar to reset.

(b) ATN : When the attention (ATN) line is low it indicates that the controller is putting an universal command or an address command like listen on the data bus. If ATN is high then data line contains data.

(c) SRQ : Service request (SRQ) it is similar to interrupt. A device can transfer data on the data bus by making SRQ low.

(d) REN : The remote enable (REN) allows an instrument to be controlled directly by the controller rather than by front panel switches.

(e) EOI : The end or identify (EOI) signal is raised by taker to indicate that the block of data transfer is complete.

(f) **DAV** : Data valid (DAV)

(g) **NRFD** : Not ready for data (NRFD) line

(h) **NDAC** : No data accepted (NDAC)

The signals mentioned above from a to e are management lines and from f to h they are handshake signals.

Operation : When the instrument is switched on, it sends an IFC signal to set all the instruments in a known state. The controller then sends a series of commands by making the ATN time low. The controller polls the SRQ line for service request. If the SRQ line is low, the controller checks each device until it finds the device which is requesting for service. After the controller finds the device which has raised SRQ, the controller sends listener address command to each listener that is to receive data and talk address command to the talker that requested service. The controller then raises ATN high and the data transfer takes place as follows : When all the listeners have released NRFD line the talker makes the DAV line low to indicate that a valid data byte is placed on the bus. The listeners start accepting the data by making NRFD low, after all the listeners accept the data, NDAC line will be made high and the cycle repeats. After the data transfer is complete the talker raises FOI line.

Bus standards :

Buses	I/O mode	Applications/Description
RS – 232 C	Serial	Interface between the micro computer and serial peripherals such as a terminal and a printer.
RS – 422 and RS – 423	Serial	High speed serial communication for distances longer than 20 metres.
Current loop	Serial	Interface with current operated peripherals such as teletype.
GPIB (IEEE 488)	Parallel	Interface between the micro computer and measurement equipment such as a volt meter.

7.6 CENTRONIC PARALLEL INTERFACE

Centronics type printers have a 36 pin interface connector. Fig. 7.7 shows the pin assignments and descriptions for this connector as it is used in IBM PC printer and EPSON printer. The large number of lines is caused by the fact that each data and signal line has its own individual ground return line. e.g. pin 2 is the LSB of the data character sent to the printer and pin 20 is the ground return for this signal. The purpose for using individual ground returns is to reduce the chance of picking electric noise in the lines, pin 16 is logic ground and pin 17 is chassis ground. In order to prevent large noise currents from flowing in the logic ground wire, these wires should be connected together in micro computer.

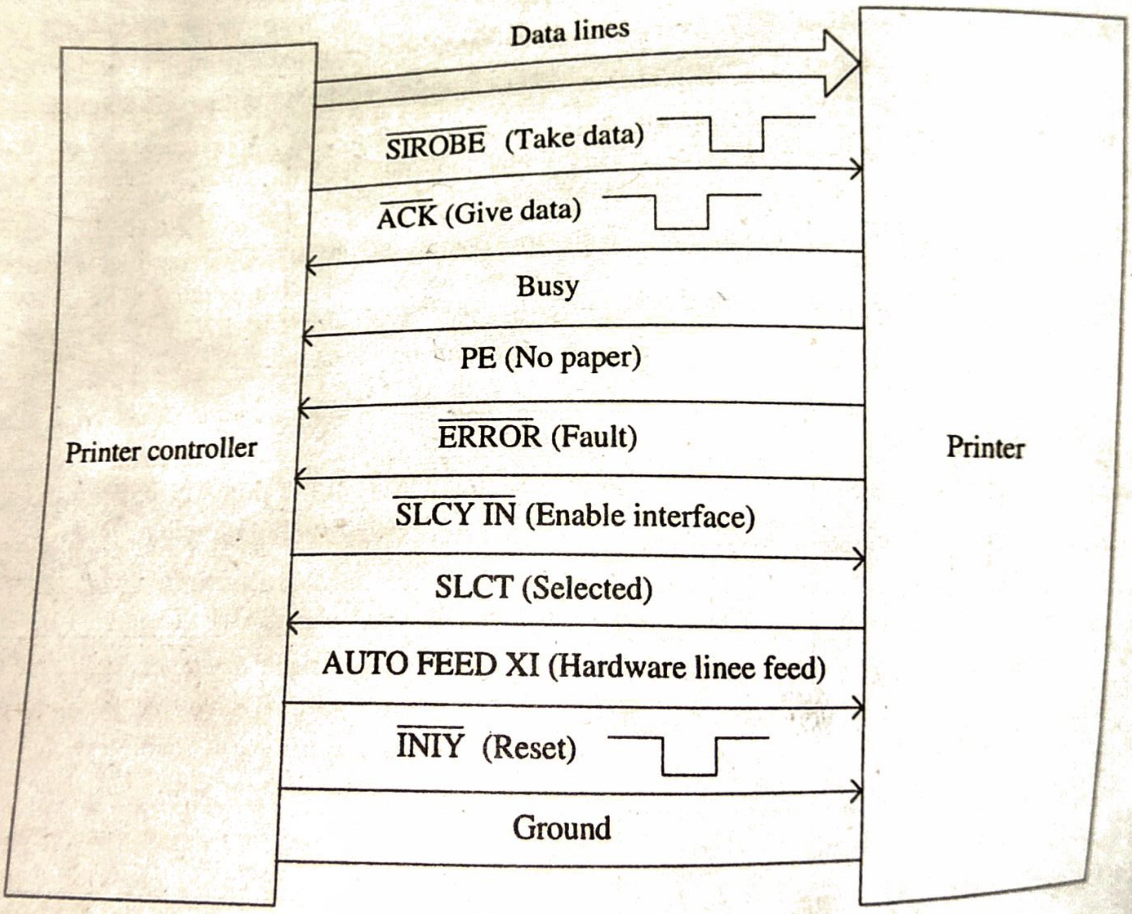


Fig. 7.6 Signals in centronics interface

The rest of the pins on the 36 pin connector fall into two categories :

(a) Signals sent to printer to tell it what operation to do.

(b) Signals from printer to indicate its status.

Signal Pin No.	Return Pin No.	Signal	Direction	Description
1.	19	$\overline{\text{STROBE}}$	IN	STROBE pulse to read data in pulse width must be more than 0.5 µs at receiving terminal the signal level is normally "high"; read-in of data is performed at the low of this signal.
2.	20	DATA 1	IN	These signals represents information of the 1st to 8th bits of parallel data respectively. E signal is at "high" level when data is logical "1" and "low" when logical "0".
3.	21	DATA 2	IN	
4.	22	DATA 3	IN	
5.	23	DATA 4	IN	
6.	24	DATA 5	IN	
7.	25	DATA 6	IN	
8.	26	DATA 7	IN	
9.	27	DATA 8	IN	
10.	28	$\overline{\text{ACKNLG}}$	OUT	Approximately 5 µs pulse; "low" indicates that has been received and the printer is ready to accept other data.
11.	29	BUSY	OUT	A "high" signal indicates that the printer cannot receive data. The signal becomes "high" in the following cases : 1. During data entry. 2. During printing operation. 3. In "office" state. 4. During printer error status.
12.	30	$\overline{\text{PE}}$	OUT	A "high" signal indicates that the printer is out of paper.
13.	-	SLCT	OUT	This signal indicates that the printer is in the selected state.
14.	-	$\overline{\text{AUTO FEED XT}}$	IN	With this signal being at "low" level, the paper is automatically fed one line after printing. (The signal level can be fixed to "low" with DIP SW pin 2-3 provided on then control circuit basic).
15.	-	NC	-	Not used.
16.	-	OV	-	Logic GND level.
17.	-	CHASSIS-GND	-	Printer chassis GND. In the printer, the chassis GND and the logic GND isolated from earth other.
18.	-	NC	-	Not used.
19.-30.	-	GND	-	"Twisted-Pair Return" signal; GND level.
31.	-	$\overline{\text{INIT}}$	IN	When the level of this signal becomes "low" the printer controller is rest to its initial state and the print buffer is cleared. This signal is normally at "high" level, and its pulse width must be more than 50 µs at the receiving terminal.
32.	-	$\overline{\text{ERROR}}$	OUT	The level of this signal becomes "low" when thee printer is in "Paper End" state, "Offline" state and "error" state.
33.	-	GND	-	Same as with pin number 19 to 30.
34.	-	NC	-	Not used.
35.	-	-	-	Pulled up to +5 V dc through 4.7 ohms resistance.
36.	-	$\overline{\text{SLCT IN}}$	IN	Data entry to the printer is possible only when. the level of this signal is "low" (Internal fixing can be carried out with DIP SW 1-8. The condition at the time of shipment is set "low" for this signa).

Fig. 7.7 Pin connection and descriptions for centronics type parallel interface