Autograder Results

Results | Code

Files Submitted Properly: File Check (0.5/0.5)

Microcode: fetchPC (0.25/0.25)

Microcode: fetchClockCycles (0.25/0.25)

Microcode: fetchUnchangedRegisters (0.25/0.25)

Microcode: addPC (0.25/0.25)

Microcode: addClockCycles (0.49/0.49)

Microcode: addChangedRegisters (1.23/1.23)

Microcode: addUnchangedRegisters (0.49/0.49)

Microcode: addCC (0.49/0.49)

Microcode: andPC (0.25/0.25)

Microcode: andClockCycles (0.49/0.49)

Microcode: andChangedRegisters (1.23/1.23)

Microcode: andUnchangedRegisters (0.49/0.49)

Microcode: andCC (0.49/0.49)

Microcode: notPC (0.25/0.25)

Microcode: notClockCycles (0.49/0.49)

Microcode: notChangedRegisters (1.23/1.23)

Microcode: notUnchangedRegisters (0.49/0.49)

Microcode: notCC (0.49/0.49)

Microcode: leaPC (0.25/0.25)

Microcode: leaClockCycles (0.49/0.49)

Microcode: leaChangedRegisters (1.23/1.23)

Microcode: leaUnchangedRegisters (0.49/0.49)

Microcode: leaCC (0.49/0.49)

Microcode: jmpPC (0.25/0.25)

Microcode: jmpClockCycles (0.49/0.49)

Microcode: jmpChangedRegisters (1.23/1.23)

Microcode: jmpUnchangedRegisters (0.49/0.49)

Microcode: jmpCC (0.49/0.49)

Microcode: ldPC (0.25/0.25)

Microcode: ldClockCycles (0.49/0.49)

Microcode: ldChangedRegisters (1.23/1.23)

Microcode: ldUnchangedRegisters (0.49/0.49)

Microcode: ldCC (0.49/0.49)

Microcode: ldrPC (0.25/0.25)

Microcode: ldrClockCycles (0.49/0.49)

Microcode: ldrChangedRegisters (1.23/1.23)

Microcode: ldrUnchangedRegisters (0.49/0.49)

Microcode: ldrCC (0.49/0.49)

Microcode: ldiPC (0.25/0.25)

Microcode: ldiClockCycles (0.49/0.49)

Microcode: ldiChangedRegisters (1.23/1.23)

Microcode: ldiUnchangedRegisters (0.49/0.49)

Microcode: ldiCC (0.49/0.49)

Microcode: stPC (0.25/0.25)

Microcode: stClockCycles (0.49/0.49)

Microcode: stChangedRegisters (1.23/1.23)

Microcode: stUnchangedRegisters (0.49/0.49)

Microcode: stCC (0.49/0.49)

Microcode: strPC (0.25/0.25)

Microcode: strClockCycles (0.49/0.49)

Microcode: strChangedRegisters (1.23/1.23)

Microcode: strUnchangedRegisters (0.49/0.49)

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Microcode: stiPC (0.25/0.25)

Microcode: stiClockCycles (0.49/0.49)

Microcode: stiChangedRegisters (1.23/1.23)

Microcode: stiUnchangedRegisters (0.49/0.49)

Microcode: stiCC (0.49/0.49)

Microcode: aitwocsimPC (0.25/0.25)

Microcode: aitwocsimClockCycles (0.49/0.49)

Microcode: aitwocsimChangedRegisters (1.23/1.23)

Microcode: aitwocsimUnchangedRegisters (0.49/0.49)

Microcode: aitwocsimCC (0.49/0.49)

Microcode: jlrPC (0.25/0.25)

Microcode: jlrClockCycles (0.49/0.49)

Microcode: jlrChangedRegisters (1.23/1.23)

Microcode: jlrUnchangedRegisters (0.49/0.49)

Microcode: coveragetest0ClockCycles (0.49/0.49)

Microcode: coveragetest0Registers (1.96/1.96)

Microcode: coveragetest0CC (0.49/0.49)

Microcode: coveragetest0PC (0.74/0.74)

Microcode: coveragetest1ClockCycles (0.49/0.49)

Microcode: coveragetest1Registers (1.96/1.96)

Microcode: coveragetest1CC (0.49/0.49)

Microcode: coveragetest1PC (0.74/0.74)

Microcode: coveragetest2ClockCycles (0.49/0.49)

Microcode: coveragetest2Registers (1.96/1.96)

Microcode: coveragetest2CC (0.49/0.49)

Microcode: coveragetest2PC (0.74/0.74)

Homework 4: LC-3 Datapath

● Graded

Student

Vidit Dharmendra Pokharna

Total Points

100 / 100 pts

Autograder Score

50.0 / 50.0

Passed Tests

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Question 2

Demo **50** / 50 pts