Homework 7

● Graded

Student

Vidit Dharmendra Pokharna

Total Points

100 / 100 pts

Question 1

Translation Lookaside Buffer (TLB) **20** / 20 pts

1.1 **Hit / Miss 1** **5** / 5 pts

✔ **– 0 pts** Correct

– 5 pts Incorrect

1.2 **Hit / Miss 2** **5** / 5 pts

✔ **– 0 pts** Correct

– 5 pts Incorrect

1.3 **Hit / Miss 3** **5** / 5 pts

✔ **– 0 pts** Correct

– 5 pts Incorrect

1.4 **Context Switch** **5** / 5 pts

✔ **– 0 pts** Correct

– 5 pts Incorrect

– 2 pts Did not mark Entry 2

– 2 pts Did not mark Entry 3

– 2 pts Did not mark Entry 4

– 2 pts Marked Entry 1

– 5 pts Blank/no answer

Question 2

Cache Addressing **30** / 30 pts

2.1 **Offset size** **10** / 10 pts

- ✔ **– 0 pts** Correct
- **– 10 pts** Incorrect
- **– 6 pts** Incorrect offset bit size (9)
- **– 2 pts** Incorrect cache address offset (010101001; accept follow through from bit size)
- **– 10 pts** Blank/no answer/incorrect

2.2 **Index** **10** / 10 pts

- ✔ **– 0 pts** Correct
- **– 2 pts** Did not use set associativity while collecting bit size (did not divide by 4)
- **– 2 pts** Used words/block instead of bytes/block when calculating bit size (divided by 128 instead of 128 * 4 = 512)
- **– 6 pts** Incorrect index bit size for other/unknown reason (7)
- **– 2 pts** Incorrect cache address index (should be 0110010; accept follow through from bit size and previous parts)
- **– 10 pts** Blank/no answer/incorrect
- **– 10 pts** Incorrect

2.3 **Tag** **10** / 10 pts

- ✔ **– 0 pts** Correct
- **– 0 pts** Incorrect bit size due to follow-through from a previous part
- **– 6 pts** Incorrect tag bit size for other/unknown reason (16)
- **– 2 pts** Incorrect cache address tag (1101101010101111; accept follow through from bit size and previous parts)
- **– 10 pts** Blank/no answer/incorrect
- **– 10 pts** Incorrect

2.4 **Work (Optional)** **0** / 0 pts

- ✔ **+ 0 pts** Correct

Question 3

Effective Memory Access Time **24** / 24 pts

3.1 **Memory 1 EMAT** **10** / 10 pts

✔ **– 0 pts** Correct (5.35)

– 0 pts Correct

– 2 pts Incorrect rounding

– 2 pts Minor math error

– 5 pts Set miss rate equal to hit rate (i.e used m = (1 - .11)) (61.21)

– 6 pts Does not include hit time in the calculation, only the miss rate * hit time, (44.55)

– 10 pts Other incorrect/blank/no answer

– 10 pts Incorrect

3.2 **Memory 2 EMAT** **10** / 10 pts

✔ **– 0 pts** Correct (30.73)

– 0 pts Correct

– 2 pts Incorrect rounding

– 2 pts Minor math error

– 5 pts Set miss rate equal to hit rate (i.e. used m = (1 - .55)) (44.23)

– 6 pts Does not include hit time in the calculation, only the miss rate * hit time, (8.82)

– 10 pts Other incorrect/blank/no answer

– 10 pts Incorrect

3.3 **EMAT Comparison** **4** / 4 pts

✔ **– 0 pts** Correct

– 0 pts Correct (follow through)

– 4 pts Incorrect

3.4 **Work (Optional)** **0** / 0 pts

✔ **+ 0 pts** Correct

Question 4

Cache Trace **26** / 26 pts

4.1 **Cache Trace 1** **8** / 8 pts

✔ **+ 8 pts** Correct

Hit/Miss

+ 4 pts Marks conflict miss

+ 1 pt Marks cold/compulsory miss (previously referenced)

+ 0 pts Marked capacity miss (the cache is not full) or hit

Modified Cache

+ 2 pts Marks C3

+ 2 pts Marks correct cache for incorrect index (see below)

+ 0 pts Marks any other cache or None

Modified Index

+ 2 pts Marks Index 1

+ 0 pts Marks any other index or None

+ 0 pts Incorrect

4.2 **Cache Trace 2** **8** / 8 pts

✔ **+ 8 pts** Correct

Hit/Miss

+ 4 pts Marks cold/compulsory miss

+ 1 pt Marks any other miss

+ 0 pts Marks hit

Modified Cache

+ 2 pts Marks C1

+ 2 pts Marks correct cache for incorrect index (see below)

+ 0 pts Marks any other cache or None

Modified Index

+ 2 pts Marks Index 2

+ 0 pts Marks any other index or None

+ 0 pts Incorrect

4.3 **Cache Trace 3** **8** / 8 pts

✔ **+ 8 pts** Correct

Hit/Miss

+ 4 pts Marks hit

+ 0 pts Mark miss

Modified Cache

+ 2 pts Marks None (no cache is modified on a hit)

+ 1 pt Marks C3 (the correct cache), even though it is not modified

+ 0 pts Marks any other cache

Modified Index

+ 2 pts Marks None

+ 1 pt Marks Index 0 (the correct index), even though it is not modified

+ 0 pts Marks any other index

+ 0 pts Incorrect

4.4 **(no title)** **2** / 2 pts

✔ **+ 2 pts** Correct (5)

+ 0 pts Incorrect

Q1 Translation Lookaside Buffer (TLB)

20 Points

The table below represents the current entries in the translation lookaside buffer (TLB).

No.	User/Kernel	VPN	PFN	Valid/Invalid
1	Kernel	12	17	Valid
2	User	99	80	Invalid
3	User	130	16	Valid
4	User	80	3	Invalid

Q1.1 Hit / Miss 1

5 Points

While executing the current user process, an attempt to access the page at VPN $= 80$ is made. Is this TLB lookup a hit or miss?

- ○ Hit
- ◉ Miss

Q1.2 Hit / Miss 2

5 Points

While executing the current user process, an attempt to access the page at VPN $= 130$ is made. Is this TLB lookup a hit or miss?

- ◉ Hit
- ○ Miss

Q1.3 Hit / Miss 3
5 Points

While executing the current user process, an attempt to access the page at VPN $= 118$ is made. Is this TLB lookup a hit or miss?

- ○ Hit
- ◉ Miss

Q1.4 Context Switch
5 Points

The processor executes a context switch. Which entries in the TLB are purged?

- ☐ Entry 1
- ☑ Entry 2
- ☑ Entry 3
- ☑ Entry 4

Q2 Cache Addressing

30 Points

Listed below are the cache parameters that describe the cache layout for a byte-addressable memory system:

- 4 way set associative
- 32 bit address
- block size of 128 words
- word size of 4 bytes
- total cache size of 64K words (256 KB)

Use these parameters to evaluate how this cache will interpret an address and the sizes of each part of the address. (Also, use 1 KB = 1024 B = 2^10 B)

Q2.1 Offset size

10 Points

What is the size (in bits) of the offset?

9

Given the following cache address, what is the offset (in binary)? Assume the cache address follows the format *tag* | *index* | *offset*.

Cache address = 11011010101011110110010010101001

010101001

Q2.2 Index
10 Points

What is the size (in bits) of the index?

7

Given the following cache address, what is the index (in binary)? Assume the cache address follows the format *tag* | *index* | *offset*.

Cache address = 11011010101011110110010010101001

0110010

Q2.3 Tag
10 Points

What is the size (in bits) of the tag?

16

Given the following cache address, what is the tag (in binary)? Assume the cache address follows the format *tag* | *index* | *offset*.

Cache address = 11011010101011110110010010101001

1101101010101111

Q2.4 Work (Optional)
0 Points

For partial credit, show your work in the field below.

2.1: log_2(128*4) = 9 -> addr[8:0]
2.2: log_2((2^16)/512) = log_2(2^7) = 7 -> addr[15:9]
2.3: 32 - 7 - 9 = 16 -> addr[31:16]

Q3 Effective Memory Access Time

24 Points

Say we have two setups for hierarchical memory with the following miss rates and hit times:

Memory 1

Hardware	Miss Rate	Hit Time
L1 Cache	0.16	3 ns
L2 Cache	0.11	7 ns
Main Memory	0	70 ns

Memory 2

Hardware	Miss Rate	Hit Time
L1 Cache	0.55	4 ns
L2 Cache	0.33	9 ns
Main Memory	0	120 ns

Q3.1 Memory 1 EMAT

10 Points

What is the EMAT (effective memory access time) for Memory 1 in ns? Round your answer to 2 decimal places.

5.35

Q3.2 Memory 2 EMAT
10 Points

What is the EMAT (effective memory access time) for Memory 2 in ns? Round your answer to 2 decimal places.

30.73

Q3.3 EMAT Comparison
4 Points

Which setup has a better EMAT?

- (●) Memory 1
- ( ) Memory 2

Q3.4 Work (Optional)
0 Points

If you would like partial credit in case of an incorrect answer on the previous parts, show your work in the field below.

3.1: ((70*0.11)+7)*0.16+3 = 5.352
3.2: ((120*0.33)+9)*0.55+4 = 30.73

Q4 Cache Trace
26 Points

You are given a 4-way set associative cache. Each cache set has four cache entries, valid bits, and "Least Recently Used (LRU)", which holds a sequence of caches ordered based on how recently were they used. For example, an entry of

$$C1 \rightarrow C2 \rightarrow C3 \rightarrow C0$$

indicates $C0$ as the least recently used cache entry.

In the tables below, an entry denotes the memory address whose data is stored at that location, not the data itself. Additionally, assume the entry in the "Valid" column for an index is the value of the valid bit for each entry at that index. An "O" means each entry in the index is valid, and an "X" means each entry in the index is invalid.

Q4.1 Cache Trace 1
8 Points

Given the current state of the cache below, what will happen if the CPU accesses the memory location of **49**? Assume that location 49 **has** been previously referenced in the cache.

Index	C0	C1	C2	C3	Valid	LRU
0	4	--	36	28	X	--
1	33	5	9	45	O	$C2 \rightarrow C0 \rightarrow C1 \rightarrow C3$
2	14	38	30	18	O	$C0 \rightarrow C2 \rightarrow C3 \rightarrow C1$
3	39	11	7	27	O	$C1 \rightarrow C3 \rightarrow C0 \rightarrow C2$

Hit/Miss & Type:

- ○ Hit
- ○ Miss - Cold/Compulsory
- ○ Miss - Capacity
- ◉ Miss - Conflict

Modified Cache Entry (Choose cache & its index)

Cache

- ○ C0
- ○ C1
- ○ C2
- ◉ C3
- ○ None

Index

- ○ Index 0
- ◉ Index 1
- ○ Index 2
- ○ Index 3
- ○ None

Q4.2 Cache Trace 2
8 Points

Given the current state of the cache below, what will happen if the CPU accesses the memory location of **14**? Assume that location 14 **has NOT** been previously referenced in the cache.

Index	C0	C1	C2	C3	Valid	LRU
0	32	4	16	8	O	$C2 \rightarrow C0 \rightarrow C1 \rightarrow C3$
1	5	13	33	41	O	$C3 \rightarrow C1 \rightarrow C2 \rightarrow C0$
2	18	30	26	22	O	$C0 \rightarrow C3 \rightarrow C2 \rightarrow C1$
3	35	43	15	7	O	$C1 \rightarrow C0 \rightarrow C2 \rightarrow C3$

Hit/Miss & Type:

- ○ Hit
- ◉ Miss - Cold/Compulsory
- ○ Miss - Capacity
- ○ Miss - Conflict

Modified Cache Entry (Choose cache & its index)

Cache

- ○ C0
- ◉ C1
- ○ C2
- ○ C3
- ○ None

Index

- ○ Index 0
- ○ Index 1
- ◉ Index 2
- ○ Index 3
- ○ None

Q4.3 Cache Trace 3
8 Points

Given the current state of the cache below, what will happen if the CPU accesses the memory location of **12**? Assume that location 12 **has** been previously referenced in the cache.

Index	C0	C1	C2	C3	Valid	LRU
0	8	16	0	12	O	$C1 \rightarrow C3 \rightarrow C2 \rightarrow C0$
1	1	13	21	9	O	$C2 \rightarrow C1 \rightarrow C0 \rightarrow C3$
2	-	-	-	-	X	----
3	3	11	7	19	O	$C1 \rightarrow C2 \rightarrow C3 \rightarrow C0$

Hit/Miss & Type:

- (●) Hit
- ( ) Miss - Cold/Compulsory
- ( ) Miss - Capacity
- ( ) Miss - Conflict

Modified Cache Entry (Select the cache & its index)

Cache

- ( ) C0
- ( ) C1
- ( ) C2
- ( ) C3
- (●) None

Index

- ○ Index 0
- ○ Index 1
- ○ Index 2
- ○ Index 3
- ◉ None

Q4.4
2 Points

How many bits are required to keep track of the ordering of 4 way set associative?

- ○ 24
- ○ 10
- ◉ 5
- ○ 4