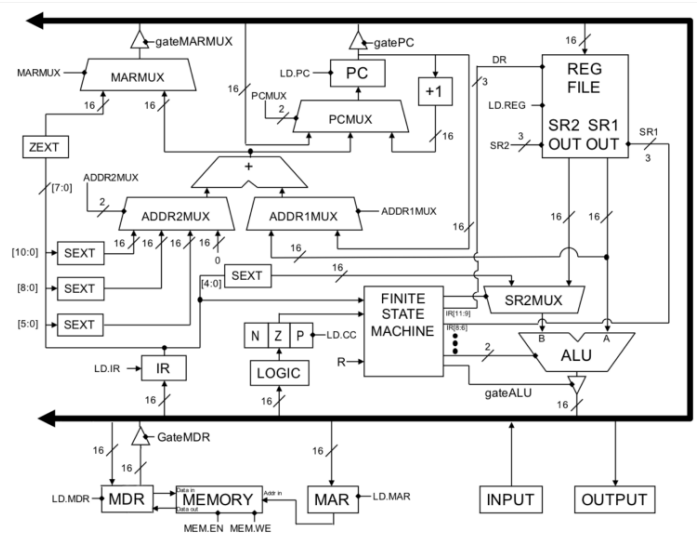
Q1 LC-3 Reference Sheet

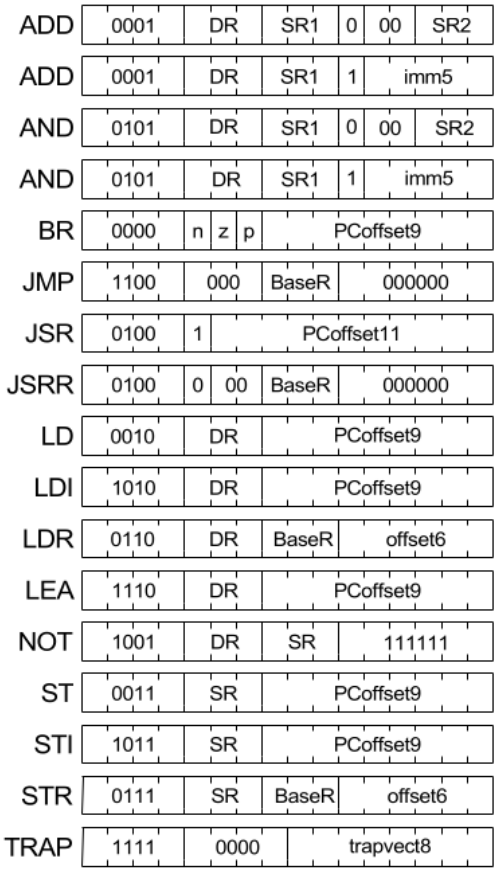
0 Points



Boolean Signals	
LD.MAR	GateMARMUX
LD.MDR	GateMDR
LD.REG	GatePC
LD.CC	GateALU
LD.PC	LD.IR
MEM.EN	MEM.WE

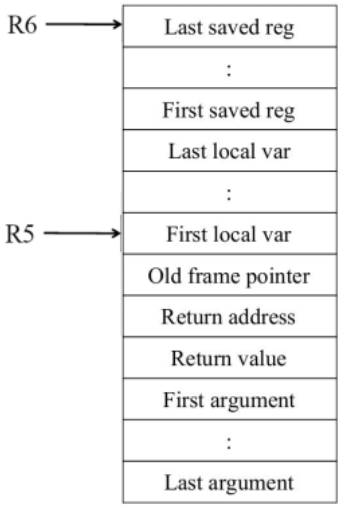
MUX Name	Possible Values
ALUK	ADD, AND, NOT, PASSA
ADDR1MUX	PC, BaseR
ADDR2MUX	ZERO, offset6, PCoffset9, PCoffset11
PCMUX	PC+1, BUS, ADDER
MARMUX	ZEXT, ADDER
SR2MUX	SR2, SEXT

CS2110 REFERENCE SHEET



Trap Vector	Assembler Name
x20	GETC
x21	OUT
x22	PUTS
x23	IN
x25	HALT

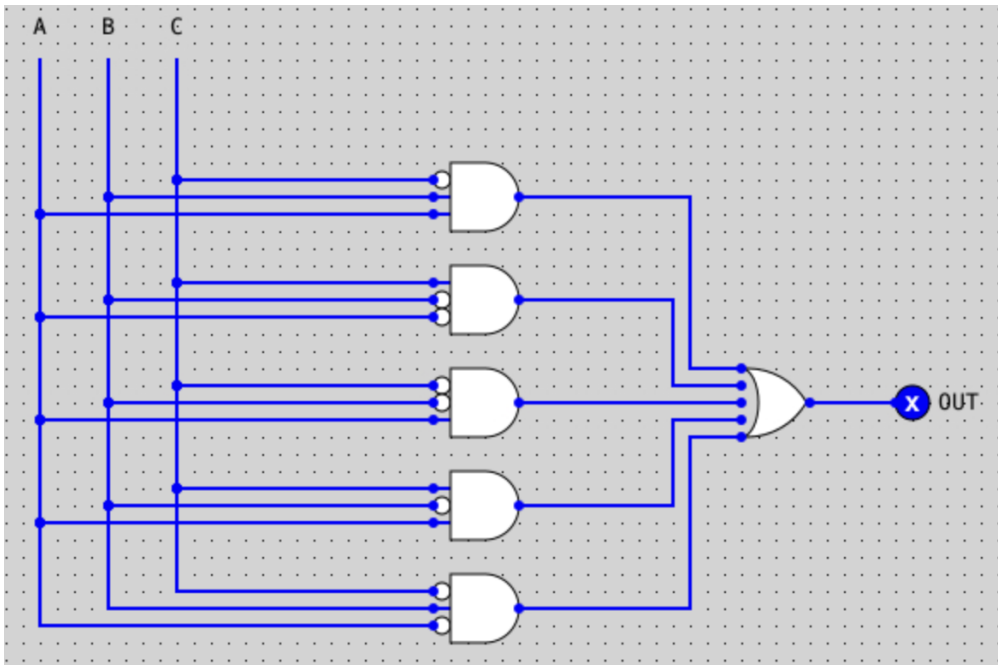
Device Register	Address
Keybd Status Reg	xFE00
Keybd Data Reg	xFE02
Display Status Reg	xFE04
Display Data Reg	xFE06



Q2 Circuit Tracing

4 Points

Based on the circuit below, fill in the **OUT** column of the truth table. For example, if the cell with a (2) should be filled in with a 0, then type 0 in a corresponding box for (2).



A	B	C	OUT
0	0	0	(1)
0	0	1	(2)
0	1	0	(3)
0	1	1	(4)
1	0	0	(5)
1	0	1	(6)
1	1	0	(7)
1	1	1	(8)

(1)

0

(2)

1

(3)

1

(4)

1

(5)

1

(6)

1

(7)

0

(8)

0

Q3 Sum of products

4 Points

Fill the Truth table below based on the provided sum-of-products expression. For example, if the cell with a (2) should be filled in with a 0, then put 0 in a corresponding box for (2).

A'BC + ABC’ + A'BC' + A'B'C':

A	B	C	OUT
0	0	0	(1)
0	0	1	(2)
0	1	0	(3)
0	1	1	(4)
1	0	0	(5)
1	0	1	(6)
1	1	0	(7)
1	1	1	(8)

(1)

1

(2)

0

(3)

1

(4)

1

(5)

0

(6)

0

(7)

1

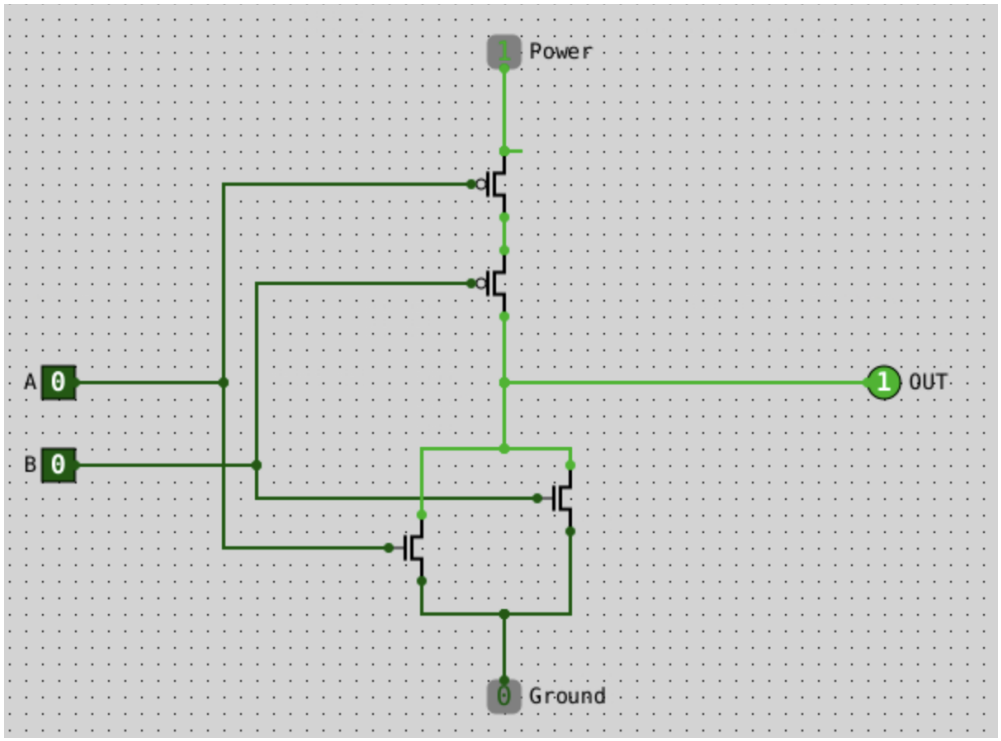
(8)

0

Q4 Gates

6 Points

What type of gate is the circuit below?



OR

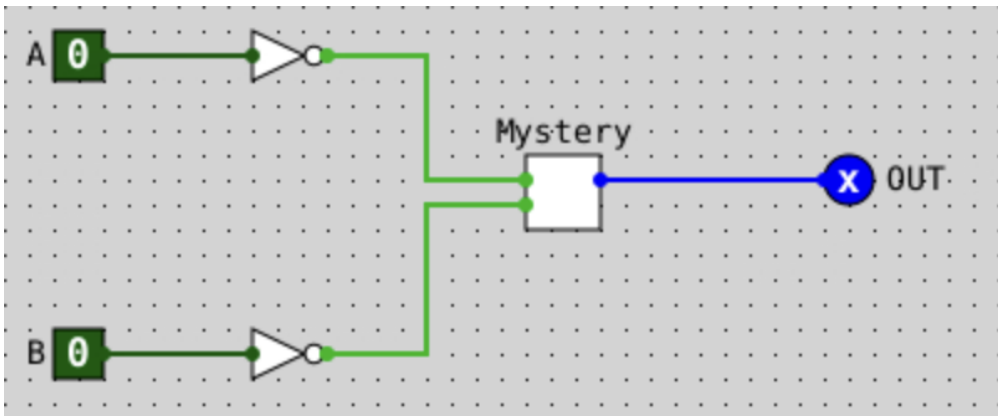
XOR

NOR

AND

NAND

What type of gate can we replace **Mystery** with in the image below to create a **NOR** gate?



NAND

AND

OR

XOR

NOR

Q5 Plexers
6 Points

Fill in the blanks:

If the multiplexer has 8 inputs, then its selector has **Blank A** bits. If the decoder has 32 inputs, then it can set **Blank B** output(s) based on the input value.

Blank A

2

1

3

8

Blank B

1

2

5

32

Q6 Explanation
3 Points

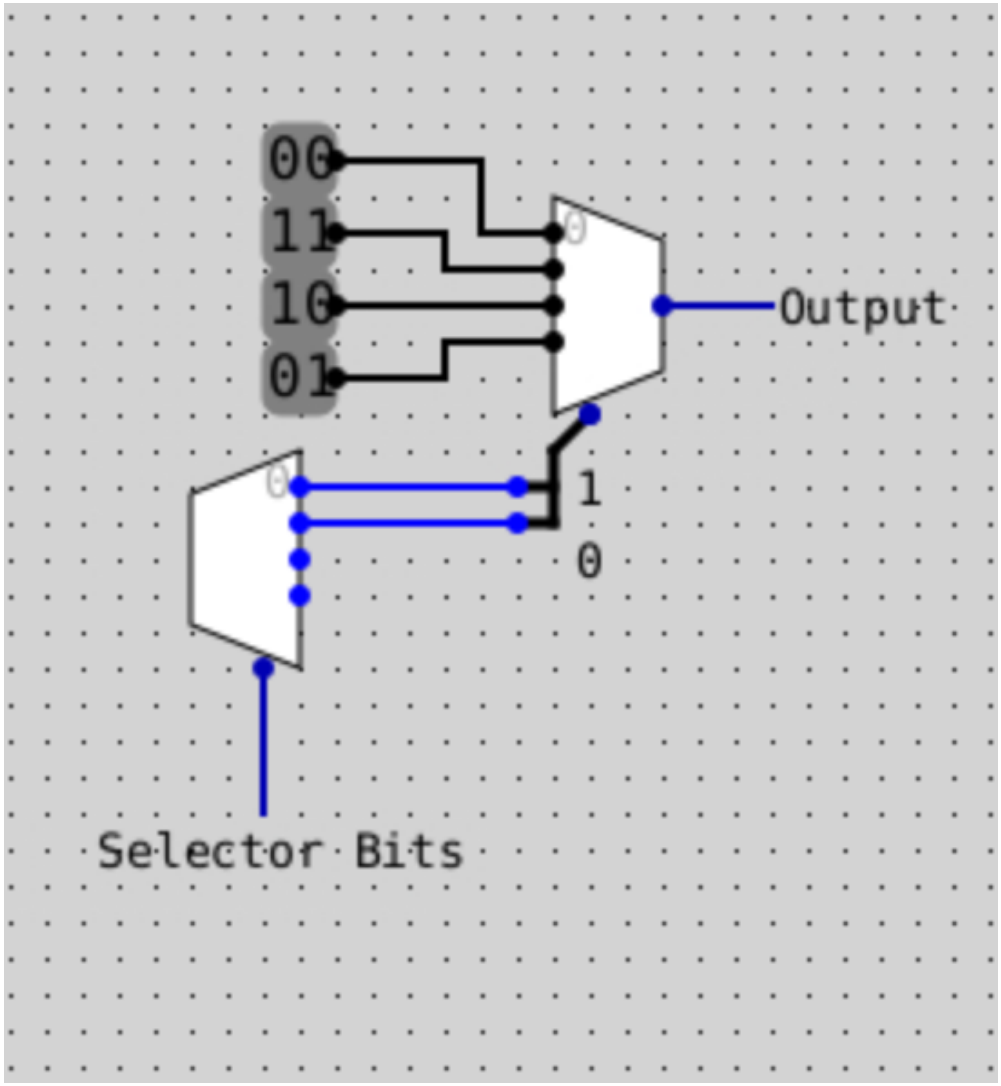
Please explain how you solved the previous problem (Q5 Plexers) in 1-3 sentences or bullet points. Make sure to address both parts

of the previous problem.

A: To select any of the 8 bits for the multiplexer, you must have a binary representation of 0-7, which is possible with a minimum of 3 bits.

B: The decoder always entails 1 output value, regardless of the number of inputs.

Q7 Circuit Analysis
4 Points



Which of the following **cannot** be output by the circuit above?

00

11

10

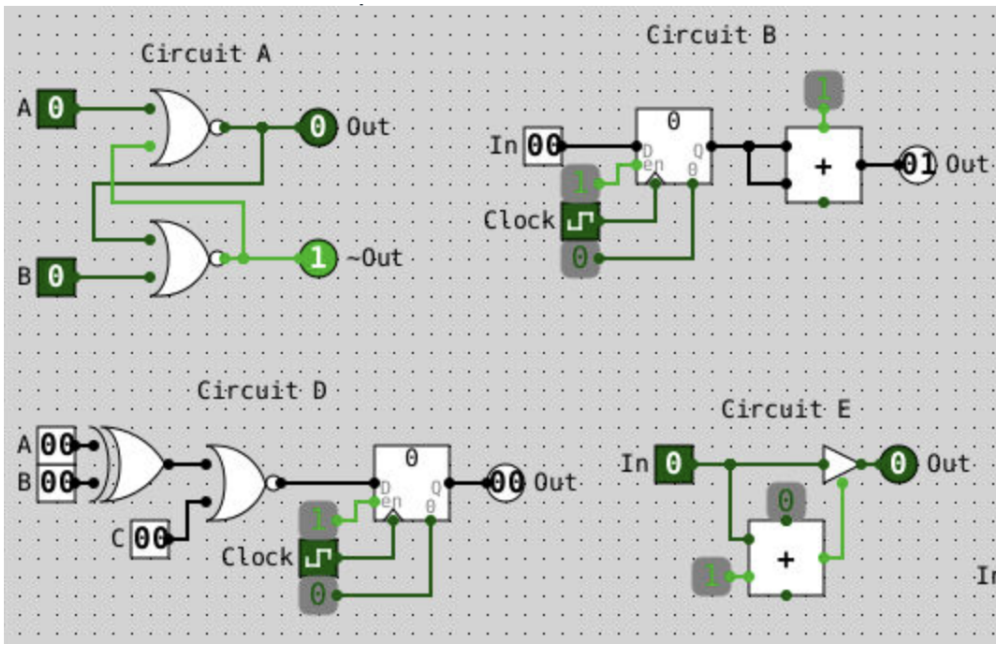
01

Q8 Explanation
4 Points

Explain how you solved the previous problem (Q7 Circuit Analysis) with 1-3 sentences.

I noticed that the selector bits for the demux can only allow three values to reach the selector bits for the mux. These values are 00, 10, and 01, and therefore, only allow those respective inputs to pass through the mux. Thus, the value at 11 (which is 01), cannot be outputted by the mux.

Q9 Categorizing Logic Types
9 Points



Categorize the following circuits. If a circuit's implementation requires only combinational logic, classify it as combinational. If a

circuits implementation requires any sequential logic, classify it as sequential.

Q9.1
3 Points

Which of the of the following circuits only implement **combinational logic**?

- [ ] The Microcontroller (FSM in LC-3)
- [x] Decoder
- [ ] Instruction Register (in LC-3)
- [ ] Circuit B
- [x] NAND Gate
- [ ] Circuit D
- [ ] RS-Latch
- [x] Circuit E
- [ ] Circuit A

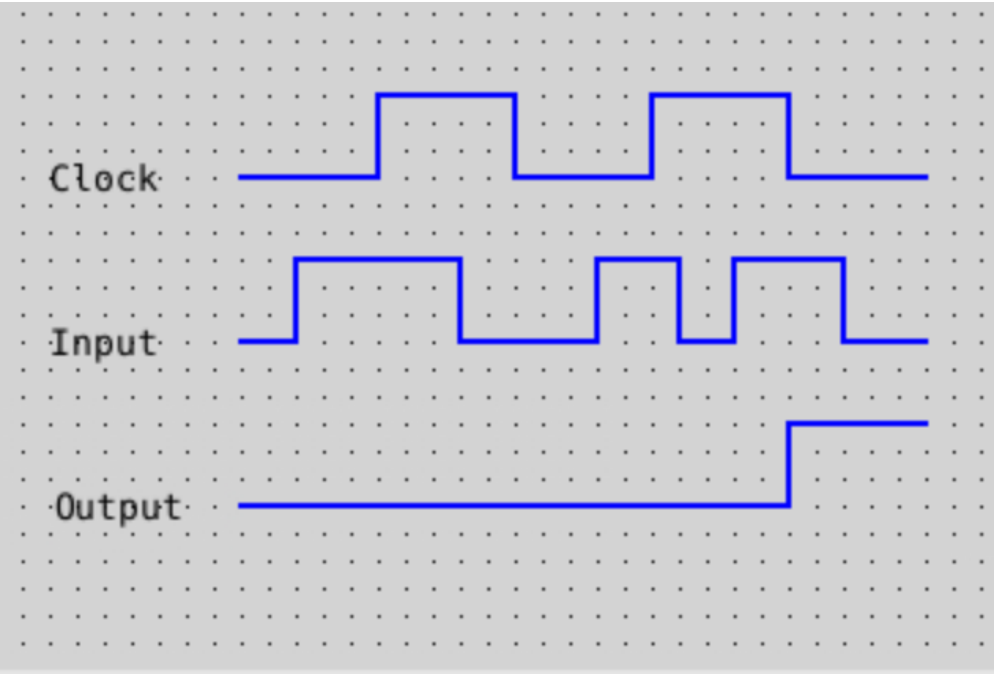
Q9.2
6 Points

Which of the of the following circuits necessarily implement **sequential logic**?

- [x] Circuit D
- [ ] Decoder
- [x] RS-Latch
- [x] Circuit B
- [x] Instruction Register (in LC-3)
- [x] Circuit A
- [ ] NAND Gate
- [ ] Circuit E
- [x] The Microcontroller (FSM in LC-3)

Q10 Level/Edge Triggered-Logic

5 Points



Assume there is a circuit that connects input to output and depends on the clock. The diagram above shows all three of these signals. Based on this diagram, what type of logic is this circuit using?

- Neither
- Level-Triggered
- Edge-Triggered

Q11 Explanation
5 Points

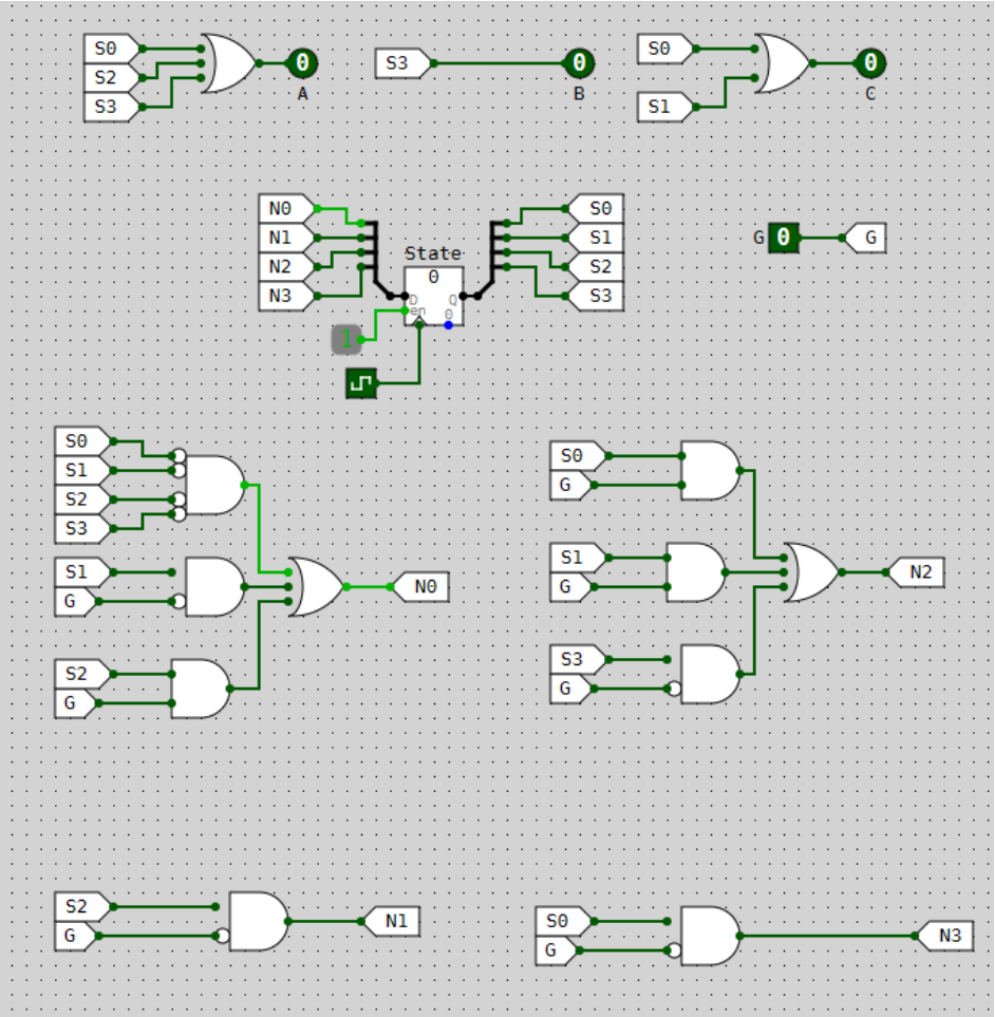
Please explain your reasoning for the previous question (Q10 Level/Edge Triggered-Logic) in 1-3 sentences and/or bullet points. Specifically reference edge and level triggered logic in your explanation, and what differences between them and what properties each has led to your answer.

I noticed that the output only changed when the clock fell on the second cycle. If changes are made on a falling edge clock cycle, then this is a type of edge-triggered logic. Edge-triggered logic constantly changes the values of the output when the clock is rising or falling, while level-triggered only changes the values of the output when the clock is static.

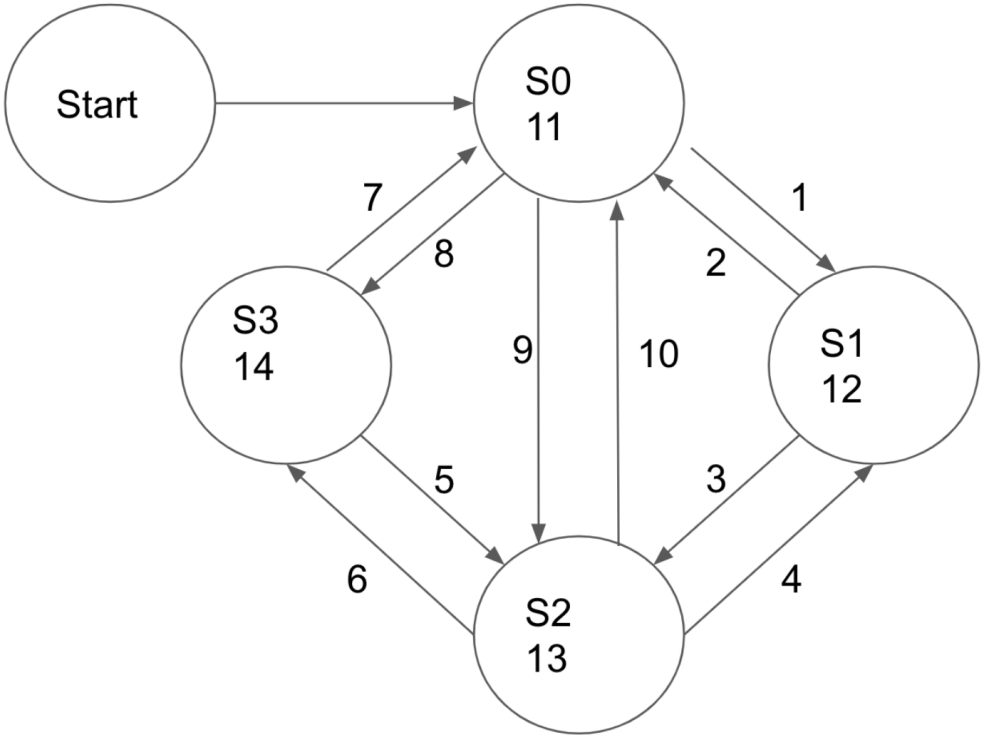
Q12 State machines
7 Points

The circuit below implements a one-hot state machine. Your task is to fill in the blanks to recreate the state diagram of the state machine.

Utilizing the circuit below, fill in the blanks with you think would go in that position in the state diagram (also shown below).



For each node in the state diagram, fill in the values that would be outputted in that state. For each arrow, fill in the input that would cause that state transition, or "None" if the arrow should not be present in the state diagram.



Please only use G, G', A, B, C, AB, AC, BC, or None when inputting your answers.

1 =

None

2 =

G'

3 =

G

4 =

G'

5 =

G'

6 =

None

7 =

None

8 =

G'

9 =

G

10 =

G

11 =

AC

12 =

C

13 =

A

14 =

AB

Q13 K-maps #1

4 Points

Given the truth table below, which of the following K-maps is filled out correctly AND has optimal groupings? Green cells denote the overlap between the yellow-colored grouping and the cyan-colored grouping.

A	B	C	OUT
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	X
1	1	0	0
1	1	1	1

	AB	AB'	A'B'	A'B
C	1	X	1	1
C'	0	1	0	0

	AB	AB'	A'B	A'B'
C	1	X	1	1
C'	0	1	0	0

	AB	AB'	A'B'	A'B
C	1	X	1	1
C'	0	1	0	0

	AB	AB'	A'B'	A'B
C	1	X	1	1
C'	0	1	0	0

Q14 K-maps #2
4 Points

From the K-map below, give the minimally reduced Boolean expression in sum-of-products form. Don't add any spaces in your answer and follow the S1/S0/G order of the headers for each term, e.g. "S1S0G+S1'G'" instead of "GS0S1+G'S1'".

	S1S0	S1S0'	S1'S0'	S1'S0
G	1	1	0	1
G'	X	0	0	1

S1G+S0

Q15 LC-3 #1
4 Points

Please explain the difference between the MAR and MDR. How can we use these registers to access memory? (2-3 sentences)

MAR can store an incoming address while MDR can store incoming data. Once you store these respective items in either the MAR or MDR, you can enable memory through MEM.EN and access the memory from MAR or MDR.

Q16 LC-3 #2
5 Points

Which of the following LC-3 components contain registers? Select all that apply.

- [x] MAR
- [x] MDR
- [ ] Bus
- [x] IR
- [ ] PC

Q17 LC-3 #3
5 Points

In the LC-3, what is stored inside of the IR? What is stored inside of the PC? (1-2 sentences)

PC holds the address of the next instruction, and IR holds the value of the current instruction.

Q18 LC-3 #4
4 Points

Which of the following control signals are needed to load a value into the MAR?

- MARMUX
- GateMARMUX
- LD.MAR
- GateMAR

Q19 LC-3 #5
4 Points

Which of the following operations modify NZP?

- [x] LD
- [x] NOT
- [ ] JMP
- [x] STR

Q20 Address Space and Addressability
6 Points

You are given a system with 10-bit addressability which uses 8 bits to represent its memory addresses.

How much memory is this system able to address, in bits?

2560

Q21 Assumptions
0 Points

If you have to make any unstated assumptions while answering any of the questions on the quiz, let us know the question numbers and assumptions you made here.

None

Quiz 2C

● Graded

Student
Vidit Dharmendra Pokharna

Total Points
86 / 93 pts

Question 1
LC-3 Reference Sheet — **0** / 0 pts

Question 2
Circuit Tracing — R **3** / 4 pts

Question 3
Sum of products — **4** / 4 pts

Question 4
Gates — **3** / 6 pts

Question 5

Plexers **6** / 6 pts

Question 6

Explanation **3** / 3 pts

Question 7

Circuit Analysis **4** / 4 pts

Question 8

Explanation **4** / 4 pts

Question 9

Categorizing Logic Types **9** / 9 pts

9.1 (no title) **3** / 3 pts

9.2 (no title) **6** / 6 pts

Question 10

Level/Edge Triggered-Logic **5** / 5 pts

Question 11

Explanation **5** / 5 pts

Question 12

State machines **7** / 7 pts

Question 13

K-maps #1 **4** / 4 pts

Question 14

K-maps #2 R **4** / 4 pts

Question 15

LC-3 #1 **4** / 4 pts

Question 16

LC-3 #2 R **4** / 5 pts

Question 17

LC-3 #3 **5** / 5 pts

Question 18

LC-3 #4 **4** / 4 pts

Question 19

LC-3 #5 R **2** / 4 pts

Question 20

Address Space and Addressability **6** / 6 pts

Question 21

Assumptions **0** / 0 pts