Vidush Singhal

School of Electrical and Computer Engineering
Purdue University
465 Northwestern Avenue
West Lafayette, IN 47907

singhav@purdue.edu

862-324-1823

OBJECTIVE: To secure an internship in compiler development, compilers for performance, compilers for GPU and/or HPC.

RESEARCH INTERESTS

- High Performance Computing (HPC)
- Compilers
- Programming Languages
- Compilers for GPU
- Automatic Vectorization
- Parallelization
- Data Layout Optimization

EDUCATION

Ph.D. @ Purdue University, West Lafayette, IN — **May 2021 – May 2026**
Electrical and Computer Engineering — (Expected)

B.Sc. @ Purdue University, West Lafayette, IN — **Aug 2017 – May 2021**
Bachelor of Science in Computer Engineering

WORK EXPERIENCE

Research Intern @Microsoft Research, Redmond, WA, USA — **May 2025 - August 2025**

- **C2Pulse**
  - Research Topic: Verifying memory correctness of C code.
  - Developed a functional Clang based transpiler to compile C code to Pulse code.
  - Researched about how to model C instructions in Pulse, for instance, predicates for structs, loops, mutable variables, integer promotion and unions to name a few.
  - Designed Annotations/Macros for the user to specify specs in the C code.
  - Added a test suite with tests to test the correctness of the transpiler.
  - The generated code was verified with FStar to verify properties based on user added specifications.

Computing Scholar Intern @Lawrence Livermore National Labs, Livermore, CA, USA — **May 2024 – August 2024**

- **LLVM Attributor:**
  - Developed a new pass to optimize layout of bytes in an allocation for better spatial locality.
  - For instance, eliminating dead bytes and reordering bytes in an allocation.
- **LLVM GPU Sanitizer:**
  - Optimized the performance of the sanitizer by hoisting pointer checks out of loops when possible.
  - Observed a 6 percent runtime improvement on the XSBench framework.
  - Developing a pass to merge checks for multiple pointers when possible.
- Wrote an LLVM pass to permute the order of basic blocks in LLVM IR to see variations in code and performance.

Machine Learning Compiler Engineering Intern *@NodAI labs*, Santa Clara, CA, USA **May 2022 – August 2022**

- **Torch-MLIR:** A framework to provide compiler support from PyTorch eco-system to the MLIR ecosystem.
    - Implemented Kernels for various Pytorch Operators.
    - Worked on supporting the Facebook DLRM recommendation model.
- **APLA:** A framework to automate inter and intra level parallelism for Distributed Deep Learning.
    - Worked on literature review to improve the ILP solver central to the scheduling of Alpa.

Engineering Intern @*Astrome Technologies Private Limited,* Bangalore, India **March 2019 - August 2019**

- Integrated an EMMC IP with an Axilite to Wishbone IP by creating a wrapper around the IPs in System Verilog.
- Performed behavioral simulations of the IPs on Vivado software to ensure that it worked as expected.
- Developed XSLT files for data stored in XML files for custom data representation.
- Developed code in Python to output the XML data as HTML on a private webpage used by the company.
- Implemented a fast Convolution Encoding and Viterbi Decoding algorithm in C for error correction and detection.
- The resulting binary was significantly faster than the python implementation.

RESEARCH EXPERIENCE

Graduate Research Assistant *@Purdue University* **Aug 2021 - Present**

PLCL Group

- **Gibbon:** A compiler that transforms high level functional programs to operate on serialized data.
    - Developed **Marmoset**: A compiler for optimizing the layout of fields in an Algebraic Data Type.
    - Developing a compiler to support a structure of arrays representation for an Algebraic Data Type.
    - Developing a compiler pass to automatically vectorize traversals over packed ADTs.
- **Grafter:** A framework to fuse general tree traversals over heterogenous trees.
    - Developed **Orchard**: A compiler framework to automatically extract parallelism from tree traversal applications. Observed speedup ranging from 1-5x over baseline tree traversals.
- **Copse:** A framework to evaluate FHE decision trees in a vectorized fashion.
    - Developed a baseline for comparison against Copse using Intel's TBB library.

PurS3 Lab

- **Cornucopia:** A framework for generating a corpus of binaries for a source file by utilizing compiler optimizations.
    - Developed a stable framework that uses fuzzing to generate a database of binaries using llc's compiler flags.
    - Modified the LLVM compiler to store a hash value as an identifier for the code of the binary.
    - Found various bugs with the LLVM compiler's optimization passes.
    - Found that binary analysis tools like Angr, Ghidra etc. failed to decompile various such binaries.
- Developing a framework that stores ground truth meta-data in the binary and test against BATs.

Senior Design Project, Dr. Mark Johnson, Prof. Samuel Midkiff, SoCET, Purdue University **July 2020 – Spring 2021**

- Developed a compiler tool for proprietary RISCV hardware using the LLVM framework.
- The compiler's objective was to optimize C programs for sparsity.
- Modified the LLVM RISCV backend by writing multiple machine IR passes.
- The passes identified sparse regions and annotated them for the hardware to identify them at runtime and perform runtime checks.

COURSEWORK

Advanced Compilers, Compilers for GPUs, Advanced Algorithms, Computer Architecture, Software Security, Artificial Intelligence, Discreet Math, Object Oriented Programming in C++, Microprocessors and micro-controllers, Data Structures in C, Python for Data Science, Advanced C programming, Random Variables, Digital Design, Graph Theory, Category Theory

SKILLS

Programming skills: C, C++, Haskell, Python, Java, Bash, Assembly (ARM, X86), MATLAB, System Verilog, HTML
Software Toolchains worked with: LLVM, GCC, AFL++, Gem5, OpenCilk, Intel TBB, Pthreads, OpenMp, Intel Cilk Tools

Version control: GIT
Soft skills: A calm minded, inclusive, and humble individual who believes in good communication skills and teamwork.

TEACHING EXPERIENCE

Undergraduate Teaching Assistant, Prof. Cheng Kok Koh, ECE 368, Purdue University **Spring 2020**
Student Grader for Signals and Systems, prof. Chih-Chun Wang, Purdue University **Fall 2019**

AWARDS/AFFILIATIONS/HONORS

- Dean's List & Semester Honors **Fall 2017 - Spring 2018**
- Semester Honors **Fall 2019 - Spring 2020**
- Member of Eta Kappa Nu, Purdue Electrical and Computer Engineering Honors Society **Fall 2018 - Present**

PUBLICATIONS

- Raghav Malik, **Vidush Singhal**, Benjamin Gottfried, and Milind Kulkarni. 2021. Vectorized secure evaluation of decision forests. In Proceedings of the 42nd ACM SIGPLAN International Conference on Programming Language Design and Implementation (PLDI 2021). Association for Computing Machinery, New York, NY, USA, 1049–1063. [DOI]
- **Vidush Singhal**, Akul Abhilash Pillai, Charitha Saumya, Milind Kulkarni, and Aravind Machiry. 2023. Cornucopia: A Framework for Feedback Guided Generation of Binaries. In Proceedings of the 37th IEEE/ACM International Conference on Automated Software Engineering (ASE '22). Association for Computing Machinery, New York, NY, USA, Article 27, 1–13. [DOI]
- **Vidush Singhal**, Laith Sakka, Kirshanthan Sundararajah, Ryan Newton, and Milind Kulkarni. 2024. Orchard: Heterogeneous Parallelism and Fine-grained Fusion for Complex Tree Traversals. ACM Trans. Archit. Code Optim. 21, 2, Article 41 (June 2024), 25 pages. [DOI]
- Chaitanya S. Koparkar, **Vidush Singhal**, Aditya Gupta, Mike Rainey, Michael Vollmer, Artem Pelenitsyn, Sam Tobin-Hochstadt, Milind Kulkarni, and Ryan R. Newton. 2024. Garbage Collection for Mostly Serialized Heaps. In Proceedings of the 2024 ACM SIGPLAN International Symposium on Memory Management (ISMM 2024). Association for Computing Machinery, New York, NY, USA, 1–14. [DOI]
- **Vidush Singhal**, Chaitanya Koparkar, Joseph Zullo, Artem Pelenitsyn, Michael Vollmer, Mike Rainey, Ryan Newton, and Milind Kulkarni. Optimizing Layout of Recursive Datatypes with Marmoset: Or, Algorithms {+} Data Layouts {=} Efficient Programs. In 38th European Conference on Object-Oriented Programming (ECOOP 2024). Leibniz International Proceedings in Informatics (LIPIcs), Volume 313, pp. 38:1-38:28, Schloss Dagstuhl – Leibniz-Zentrum für Informatik (2024) [DOI]

SERVICE/GRANTS

- Student Volunteer for SPLASH 2021.
- Student Volunteer for ECOOP/ISSTA 2024.
- Member of the Artifact Evaluation Committee (AEC) for PPoPP 2023.
- Member of the Artifact Evaluation Committee (AEC) for PPoPP 2024.
- Member of the Artifact Evaluation Committee (AEC) for CGO 2025.
- Member of the Artifact Evaluation Committee (AEC) for ICFP 2025.
- Received a travel grant to attend the 2024 LLVM developers meeting.
- Moderated a session at the 2024 LLVM developers meeting.

MENTORING

- Qingyuan (Peter) Li (Undergrad @Purdue)
    - SURF summer research Mentor