Vidushi Bhadana

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SUMMARY

Computer Engineering graduate student seeking a full time position.

EDUCATION

Masters in Computer Engineering — Jan 15 - Sep 16 (expected)
Santa Clara University, California, USA — GPA: 3.8 / 4.0

Masters in Computer Applications — Aug 09 - July 12
DKES-School of Computer Science, GGSIP University, New Delhi, India — GPA: 3.97 / 4.0

B.Sc. (H) Computer Science — July 06 - June 09
Indraprastha College for Women, University of Delhi, New Delhi, India — GPA: 3.67 / 4.0

WORK EXPERIENCE

ARSD College, University of Delhi, New Delhi, India — Jan 13 - Jan 15
Assistant Professor (Ad hoc)

- Taught Computer Networks, Operating systems and Databases.
- Designed examination papers and graded exams.

TECHNICAL SKILLS

Languages: Java, C, C++, Python, Visual Basic, Verilog, PHP
Web Technologies: HTML, HTML5, CSS, JavaScript, XML, AJAX, Bootstrap, JQuery, AngularJS
Technologies and Tools: GitHub, Eclipse IDE, Visual Studio IDE, Xilinx ISE Design Suite
Databases: SQL Server, Oracle 11g, MySQL, Elasticsearch, Solr, MongoDB
Testing frameworks: Selenium, JUnit
Networking tools: NS3 Simulator

PROJECTS

Event management software

- Designed and implemented an event management software that allowed the organizer to send invites with surveys. Organizer could then monitor the survey responses.
- Designed web front end with Django, used MongoDB as backend.
- Wrote integration tests for web UI using Selenium Webdriver.

Search engine on Yelp dataset

- Created a search engine on Yelp dataset challenge academic dataset.
- Used Apache Solr and Lucene for indexing and searching data. Support for text search, faceted search and filtering.

Caching system technique to distribute files across RAM of multiple nearby machines

- Implemented a peer to peer caching algorithm to store data on multiple systems.
- Cache eviction strategy designed to reduce disk access time with low network overhead.
- Reduced total disk access time by caching files in peers.

MIPS Single Cycle CPU

- Designed and implemented a hardware description for a single cycle CPU using Verilog.
- Support for Load/Store, Arithmetic and Logic operations and Branch on equal instructions.

Simulation of a recycling system

- Wrote a simulation of recycling system with multiple machines and monitoring stations.
- A flexible implementation in an object oriented fashion that allowed dynamically adding and removing recycling machines. Each recycling machine implemented with Model-View-Controller pattern.
- GUI implementation in Java Swing.

OTHER ACHIEVEMENTS

- Cleared UGC NET/JRF [National Eligibility Test/ Junior Research Fellowship] Computer Science, June 2012.
- Among top 5% of candidates in GATE 2011 [Graduate Aptitude Test in Engineering].
- Event organizer of various cultural and technical events at University of Delhi.