ANALOG AND DIGITAL ELECTRONICS
67 IMPORTANT MCQ

Q.1 For the circuit shown in Fig.1, the input resistance R_{id} will be

(A) $2R_1$. **(B)** $2R_1 + R_2$.

(C) $2(R_1 + R_2)$. **(D)** Infinity.

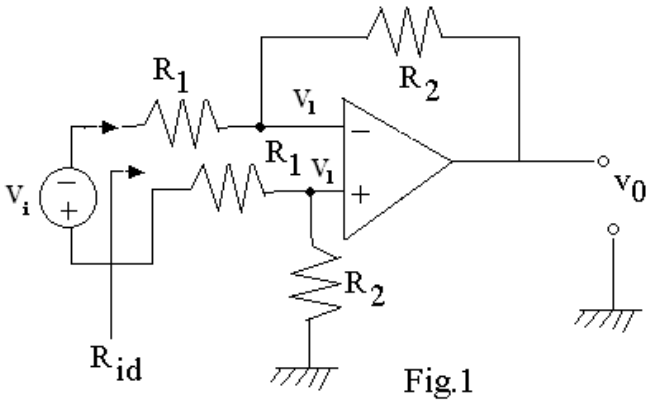


Fig.1

Ans: A

$R_{id} = \frac{v_i}{i_i}$ where i_i is the current drawn from the source. Since the two input terminals of OPAMP track each other in potential therefore writing loop equation- $v_i = R_1 i_i + 0 + R_i i_i$ thus

Rid = $R_{id} = \frac{v_i}{i_i} = 2R_1$

Q.2 A second order filter has its poles at $s = -1/2 \pm j\sqrt{3}/2$. The transmission is zero at $m = 2$ rad/s and is unity at $m = 0$. The transfer function of the filter is

(A) $\frac{1}{4}\frac{(s^2 + s)}{(s^2 - s + 1)}$. **(B)** $\frac{1}{4}\frac{(s^2 + s)}{(s^2 + s + 1)}$.

(C) $\frac{1}{4}\frac{(s^2)}{(s^2 + s + 0.25)}$. **(D)** $\frac{1}{4}\frac{(s^2 - s)}{(s^2 - s - 1)}$.

Ans: Answer should be $\frac{S - 2}{2\,(S^2 + S - \frac{1}{2})}$

As from given data the transfer function should be $\frac{S-2}{2\left(S+\frac{1}{2}+j\frac{\sqrt{3}}{2}\right)\left(S^2+\frac{1}{2}-j\frac{\sqrt{3}}{2}\right)}$

Q.3 Transfer function of a filter is given by $T(s)=\frac{a_1 s}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$. It represents a _____filter.

(A) Low pass. **(B)** High pass.
(C) Band pass. **(D)** Band stop.

Ans: C

Q.4 In applications where measurement of a physical quantity is involved, the OPAMP circuit recommended is

(A) Basic non-inverting amplifier. **(B)** A comparator.
(C) An active filter. **(D)** An instrumentation amplifier.

Ans: D

Q.5 The circuit shown in Fig.3 represents_____gate

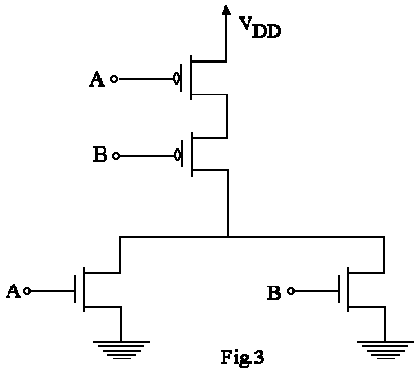


Fig.3

(A) AND.
(B) NAND.
(C) OR.
(D) NOR.

Ans: D

Q.6 Active loaded MOS differential circuit has a

(A) high CMRR. **(B)** low CMRR.
(C) high delay. **(D)** high differential gain.

Ans: D

Q.7 NPN transistor is not suitable for good analog switch because

(A) $I_C - V_{CE}$ characteristic curve pass directly through origin.
(B) the device has very high input impedance.
(C) the device is asymmetrical with an offset voltage V_{CE} off.
(D) it has well defined transition frequency f_T .

Ans: C

Q.8 CMOS logic has the property of

(A) increased capacitance and delay. **(B)** decreased area.
(C) high noise margin. **(D)** low static power dissipation.

Ans: D

Q.9 The order of input resistance in 741 OPAMP is

(A) 1 to $10^4\ \Omega$. **(B)** $10^3\ \Omega$.

(C) $10^5\ \Omega$. **(D)** $10^6\ \Omega$.

Ans: D

Q.10 The ratio of change in input offset voltage when variation in supply voltage is made is called

(A) PSRR. **(B)** CMRR .

(C) transient response. **(D)** input offset voltage stability.

Ans: A

Q.11 The equiripple response filter is called_____, while maximally flat time delay response is given by_____filter.

(A) Chebyshev, Bessel. **(B)** Butter worth, Bessel.

(C) Bessel, Chebyshev. **(D)** Chebyshev, Butter Worth.

Ans: D

Q.12 A notch filter is a

(A) Wide band pass filter. **(B)** Narrow band pass filter.

(C) Wide band reject filter. **(D)** Narrow band reject filter.

Ans: D

Q.13 The problem faced by switched capacitor filters is

(A) aliasing **(B)** amplitude distortion

(C) slower roll off rate **(D)** longer time and phase delay

Ans: Only draw back with switched capacitor filters is that they generate more noise than active filter circuits.

Q.14 For a 3-bit flash ADC, the number of comparators required are

(A) 5 **(B)** 9

(C) 7 **(D)** 3

Ans: C

Q.15 The typical quiescent power dissipation of low-power CMOS units is

(A) 1mW. **(B)** 0.5 mW.

(C) 2 nW. **(D)** 50 nW.

Ans: C

Q.16 The access times of MOSRAMS is approximately

(A) 35 ns. **(B)** 80 ns.

(C) 400 ns. **(D)** 20 ns.

Ans: Question seems to be invalid as it is not mentioned weather static or dynamic RAM and access time varies by large magnitude from chip to chip.

Q.17 For which of the following flip-flops, the output is clearly defined for all combinations of two inputs.

(A) D type flip-flop. **(B)** R-S flip-flop.
(C) J-K flip-flop. **(D)** none of these.

Ans:C

Q.18 Active load is used in the collector of the difference amplifier of an Op-amp:

(A) To increase the output resistance.
(B) To increase the differential gain.
(C) To handle large signals.
(D) To provide symmetry.

Ans: B

Q.19 A second order filter has a transfer function

$T(S) = \dfrac{s^2 + 4}{s^2 + s + 1}$ the poles and zeros of this filter are at

(A) $\omega = 2, s = 0.5 \pm j\sqrt{3}/2$. **(B)** $\omega = 1, s = -1 \pm j\sqrt{3}$.
(C) $\omega = 2, s = -1 \pm j\sqrt{3}$. **(D)** $\omega = 1, s = -0.5 \pm j\sqrt{3}/2$.

Ans: A

For given transfer function poles are $0.5 \pm j\dfrac{\sqrt{3}}{2}$ and zeroes are $\pm$ 2j

Q.20 The circuit shown in Fig.1 represent a

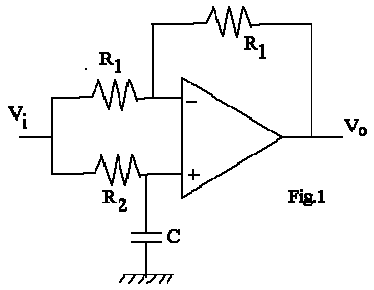


Fig.1

(A) Low pass filter.
(B) High pass filter.
(C) Band pass filter.
(D) None of the above.

Ans: A

Q.21 The circuit in Fig.2 is used to realize the logic function of

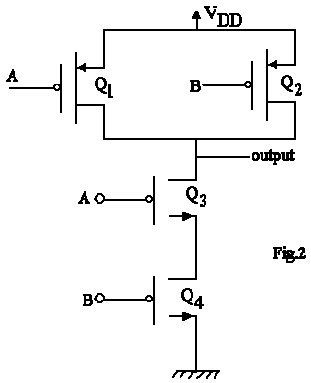


Fig.2

(A) Inverter.
(B) NOR gate.
(C) NAND gate.
(D) XOR gate.

Ans: C

Q.22 Consider an inverting op amp circuit at Fig.3 with feedback resistor equal to 100 K Ω and the input resistor equal to 1K Ω with a gain of 100 if the op amp has infinite open loop gain. If the op amp has a finite open loop gain at 10^4 ; the gain of the op amp circuit is

(A) 100. **(B)** 101.
(C) 98. **(D)** 99.

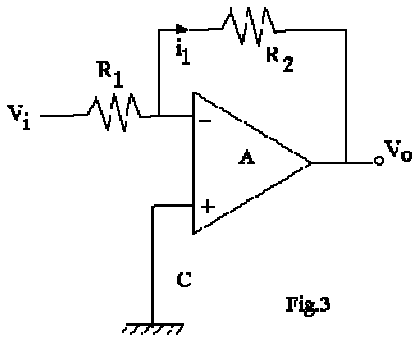


Fig.3

Ans: D

As. Gain = $\dfrac{-A_{OL} \times R_F}{R_F + R_1(1 + A_{OL})} = 99$ Putting the values we get gain as 99

Q.23 For standard TTL logic circuits, the values of V_{OL} and V_{OH} are

(A) 0.8 V and 2.0 V. **(B)** 0 V and 5 V.
(C) 0.4 V and 2 V. **(D)** 0.4 V and 2.4 V.

Ans: D

V_{OL} = 0.4 V & V_{OL}= 0.4 & V_{OH} = 2.4 V

Q.24 An op amp with input offset voltage V_{io} = 0 is used in the circuit shown in Fig.4. If the input bias currents $I_{B1} = I_{B2}$ = 100 nA then the value of Resistance R_3, such that the output voltage is zero for zero input voltage, is

(A) 100kΩ
(B) 1MΩ
(C) 110kΩ
(D) 90.9kΩ

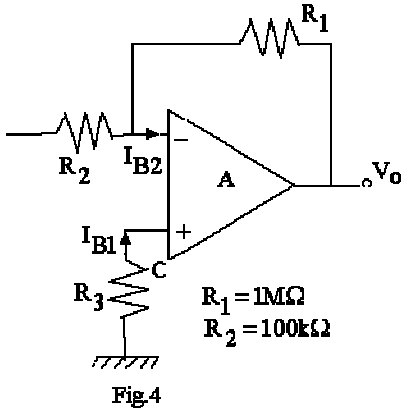


Fig.4

Ans: D

R_3 = 90.91 k ($R_1$11 R_2)

Q.25 In a sample and hold circuit the following statement is false

(A) Sample time is much smaller than hold time.
(B) Aperture time is the delay between the time that the pulse is applied to the switch and the actual time the switch closes.
(C) Acquisition time is the time it takes for the capacitor to charge from one voltage to another voltage.
(D) The voltage across the hold capacitor changes by 50% during hold time.

Ans: A

Q.26 The voltage between the emitter and collector of a silicon transistor when the transistor is biased to be at the edge of saturation is:

(A) 5 volts. **(B)** 10 volts.
(C) 0.1 volts. **(D)** 0.3 volts.

Ans: D
V_{EOS} = 0.3V

Q.27 The fastest switching logic family is

(A) CMOS. **(B)** TTL.
(C) DTL. **(D)** ECL.

Ans: D

Q.28 A 32 to 1 multiplexer has the following features.

(A) 32 outputs, one input and 5 control signals
(B) 32 inputs, one output and 5 control signals
(C) 5 inputs, one control signal and 32 outputs
(D) 5 inputs 32 control signals and one output

Ans: B

Q.29 The unity gain bandwidth of 741 OPAMP is typically

(A) 4 MHz. **(B)** 2 MHz.
(D) 6 MHz. **(D)** 1 MHz.

Ans: D

Q.30 The conversion time of a dual-slope ADC is typically in the range of

(A) 5 to 10 ns. **(B)** 10 to 100 ns.
(C) 100 to 200 ns. **(D)** 2 to 3 ns.

Ans: C
In dual slope low conversion time is not the primary concern.

Q.31 In a transistor switch, the voltage change from base-to-emitter which is adequate to accomplish the switching is only about

(A) 0.2 V. **(B)** 0.4 V.
(C) 0.1 V. **(D)** 0.5 V.

Ans: D
0.5 V assuming silicon transistors.

Q.32 Worst case ECL noise margins are approximately

(A) 100 mV. **(B)** 50 mV.
(C) 250 mV. **(D)** 400 mV.

Ans: C
Noise margin = 250 mv.

Q.33 A certain multiplexer can switch one of 32 data inputs to its output. How many different inputs does this MUX have?

(A) 30 data inputs & 5 select inputs.
(B) 32 data inputs and 4 select inputs.
(C) 32 data inputs and 5 select inputs.
(D) None of the above.

Ans: C
32 data inputs and 5 select input as (2^5=32).

Q.34 What J-K input condition will always set 'Q' upon the occurrence of the active clock transition?

(A) J = 0, K = 0 **(B)** J = 1, K = 1
(C) J = 1, K = 0 **(D)** J = 0, K = 1

Ans: C

Q.35 Given a MOD-14 ripple counter using J-K flip-flops. If the clock frequency to the counter is 30 KHz, then the output frequency of the counter will be

(A) 2.2 KHz. **(B)** 30 KHz.
(C) 2.14 KHz. **(D)** 3.2 KHz.

Ans: C
2.14 KHz as clock frequency gets divided by n (n = no of mod).

Q.36 The open-loop voltage gain of 741 OPAMP is typically

(A) 40 dB. **(B)** 200 dB.
(C) 100 dB. **(D)** 70 dB.

Ans: C
Open loop gain = 10^5 (20 log 10^5 = 100 dB)

Q.37 How many comparators would a 12-bit flash ADC require?

(A) 4000 **(B)** 3095
(C) 4095 **(D)** 2512

Ans: C
Numbers of comparators for 12 bit flash ADC
$= 2^n-1$
$=2^{12}-1$
$=4095$

Q.38 Schottky TTL gates have propagation delay time of the order of

(A) 6 ns. **(B)** 5 ns.
(C) 2 ns. **(D)** 8 ns.

Ans: C
Schottky TTL gates have propagation delay of order of 2ns as the storage time delay is removed in schottky transistor.

Q.39 The number of flip-flops required to construct a MOD-10 counter that counts from zero through decimal '9' is

(A) 8. **(B)** 16.
(C) 32. **(D)** 4.

Ans: D

To construct Mod-10 counter it requires to count from 0000 to 1001(9). Thus for 4 bits, 4 flip-flops are required.

Q.40 MOSRAMS are available with around
(A) 1024 memory cells. **(B)** 4096 memory cells.
(C) zero memory cells. **(D)** 800 memory cells.

Ans: B

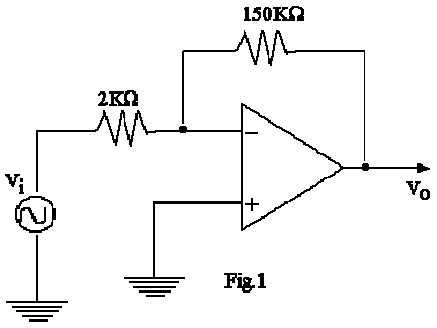
Very popular SRAM. MOS memory chip is 2114 having 4096 bits.

Q.41 A typical value of the output resistance at room temperature for the 741 OPAMP is
(A) 2MΩ. **(B)** 20KΩ.
(C) 75Ω. **(D)** 300Ω.

Ans: C

Q.42 If the OPAMP specifications lists the input offset voltage as 1.2 mV, then for the circuit shown in Fig.1, the output offset voltage is

(A)81.2 mV.
(B) 72.2 mV.
(C) 91.2 mV.
(D) 90 mV.



Ans: D

Q.43 In a first-order high-pass active filter, if the values of the resistance and the capacitance used are 2.1 KΩ and 0.05μF respectively, then the cut-off frequency of the filter is equal to
(A) 15 KHz. **(B)** 1.5 KHz.
(C) 3.5 KHz. **(D)** 0.95 KHz

Ans: B

f_c = 1.5KHz as $f_c = 1/2nRC$

Q.44 For a counter-type ADC, if the conversion time is around 4.1 ms then the minimum number of conversions that could be carried out each second would be approximately
(A) 150 per second. **(B)** 244 per second.
(C) 90 per second. **(D)** 209 per second.

Ans: B

as conversion time = $\frac{1}{f}*(2^n - 1)$

Q.45 Typical propagation delay of a CMOS gate ranges from
(A) 2 to 15 ns. **(B)** 25 to 150 ns.

(C) 100 to 200 ns. **(D)** 80 to 120 ns.

Ans: A

Q.46 The number of address bits needed to operate a 2K × 8-bit RAM are:
(A) 9 **(B)** 25
(C) 15 **(D)** 11

Ans: D

Q.47 A one-to-sixteen demultiplexer requires
(A) 2 select input lines. **(B)** 3 select input lines.
(C) 8 select input lines. **(D)** 4 select input lines.

Ans: D
As 1*16 Demux requires 4 (2^4 = 16) select lines to select one among the 16 outputs.

Q.48 The charge coupled devices are implemented using
(A) CMOS Technology **(B)** PMOS Technology
(C) MOS Technology **(D)** NMOS Technology

Ans: C

Q.49 Schottky diodes exhibit a storage time of approximately
(A) Zero sec. **(B)** 20 sec.
(C) 30 ns. **(D)** 32 ms.

Ans: C
30ns storage time is reduced due to metal-semiconductor junction.

Q.50 In an analog multiplier, if both the inputs are positive or negative then the multiplier is said to be
(A) a two quadrant multiplier. **(B)** a one quadrant multiplier.
(C) a four quadrant multiplier. **(D)** a three quadrant multiplier.

Ans: C

Q.51 The large signal differential voltage amplification of the 741 OPAMP is typically about
(A) 100 V/mv. **(B)** 500 V/mv.
(C) 1000 V/mv. **(D)** 200 V/mv.

Ans: C
as Gain-Bandwidth product= 1 MHz

Q.52 If the input offset current and the average input bias current for an OPAMP are respectively 5nA and 30 nA, then the input bias currents at each input of the OPAMP are respectively
(A) 32.5 nA & 27.5 nA. **(B)** 22.5 nA & 30.2 nA.
(C) 10 nA & 16 nA. **(D)** 2.5 nA & 3.02 nA.

Ans: A

$I_B^+ - I_B^- = I_{0s}$ | *offset current* = 5*nA*

$I_B^+ + I_B^- = I_{Bavg}$ *Bias current* = 30*nA*

Thus input bias current at each input solving above two equations gives Ans (A)

Q.53 In a first-order low-pass active filter, if the values of the resistance and the capacitor used are 1.2 KΩ and 0.02μF respectively, then the cut-off frequency of the filter is

(A) 3.6 KHz. **(B)** 8.7 KHz.
(C) 8.2 Hz. **(D)** 6.63 KHz.

Ans: D

As $f_c = \frac{1}{2\pi RC}$

Q.54 A clock rate of one megahertz operating a 12-stage counter of a counter-type ADC would need a maximum conversion time of approximately

(A) 3.2 ms. **(B)** 4.1 ms.
(C) 8 ms. **(D)** 7.1 ms.

Ans: A

Conversion time = $\frac{1}{f} \times (2^n - 1)$

N = 12 , f = 1MHz

Q.55 Typical propagation delay of an ECL circuit is

(A) 10 ns. **(B)** 5 ns.
(C) 1 ns. **(D)** 3.2 ns.

Ans: B

5 ns – fastest logic family.

Q.56 The number of states in its counting sequence that a ring counter consisting of 'n' flip-flops can have is

(A) $2^n - 1$ **(B)** 2^{n-1}
(C) n **(D)** 2^{n+1}

Ans: C

n bit shift register connected as ring counter can count total N-states.

Q.57 The number of select input lines required by a 1-to-8 demultiplexer are

(A) Two. **(B)** One.
(C) Four. **(D)** Three.

Ans: D

1 to 8 Demux require 3 ($8=2^3$) select lines to select one output among 8.

Q.58 The Maximum binary number counted by a ripple counter that uses four FlipFlop's is

(A) $(0000)_2$ **(B)** $(1011)_2$
(C) $(1111)_2$ **(D)** $(0101)_2$

Ans: C
as ripple counter with four FF's will count 16 states from zero to fifteen.

Q.59 The cut-in voltage of the aluminium n-type Schottky diode is about
(A) 0.5 V. **(B)** 0.5 μV.
(C) 0.35 V. **(D)** 0.35 mV.

Ans: C
as the cut in voltage becomes half due to metal – sc function.

State True or False

Q.60 The amplifiers in the sample and hold circuit are used to provide voltage amplification.
(A) True **(B)** False

Ans: B
Sample and hold circuit does not have amplifiers.

Q.61 In a Chebyshev filter of odd order, the oscillatory curve of the magnitude response does not start from unity
(A) True **(B)** False

Ans: B
As the magnitude response starts from unity in chebyshev odd order filters.

Q.62 Due to its simple circuit structure, MOS circuitry is not so well suited for LSI
(A) True **(B)** False

Ans: B

Q.63 The bit storage cells in a RAM, when high speed is required make use of a BJT

(A) True **(B)** False

Ans: A
True as switching speed of BJT is high.

Q.64 An instrumentation amplifier should not have a high CMRR
(A) True **(B)** False

Ans: B
Instrumentation Amplifier amplifies the difference of the I/P signal.

Q.65 In a Chebyshev filter of even order, the oscillatory curve of the magnitude response starts from unity
(A) True **(B)** False

Ans: B
Magnitude response of even order Chebyshev filter does not start from unity.

Q.66 As the gate voltage switches from a LOW voltage to a HIGH voltage, the N-MOSFET will switch from a very LOW resistance to a HIGH resistance

(A) True **(B)** False

Ans: B

As the gate voltage switches from low voltage to high voltage. NMOS starts conducting and it will switch from very high resistance to low resistance.

Q.67 The circuit for a DEMUX is basically the same as for a decoder, provided the decoder has an enable input

(A) True **(B)** False

Ans: A

DEMUX & Decoder are same circuits with decoder has an enable input.