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Continuous Internal Evaluation – I
UCSH 603: Introduction to High Performance Computing

Time: 40 min
Marks: 10

Consider a processor operating at 1GHz connected to a DRAM with a latency of 100ns. This processor has two multiply-add units and each is capable of executing a FMA in one cycle. The block size (bus width) is 32 bytes. Enough number of 8-byte registers are available in each processor.

1) What is the peak processor rating in FLOPS?

[1M]

2) Consider the following dot product computation:

```
//Each double is 8 bytes, assume that variable sum is already in a register.
double sum= 0.0, A[100]= {}, B[100]= {};
for(i= 0; i < 100; i++)
  sum= sum + A[i] * B[i];
```

How many FLOPS does this computation achieve in the above system (no cache)?

[3M]

3) Assume a Cache with line size of 64 bytes, 1 ns latency and ideal cache replacement strategy. With a large enough cache size to fit in both A and B, how many FLOPS does this computation achieve?

[3M]

4) What is the Cache Hit Ratio?

[1M]

5) For the same cache setting as above, assume that all elements of A and B are first brought into cache and then the actual computation begins. How many FLOPS would this type of computation achieve?

[2M]