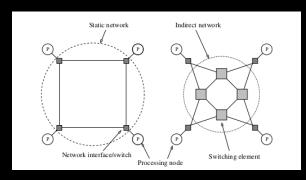
Physical Organization of Parallel platforms PRAM: Ideal Model, p processors, unswanded global Memory All p avers Same memory Simultaneons Memory Acess EREN CREN ERCH FOR p processors & m memory Common Arbitrary Sum =) Q (pm) interconnections - Not practical =) Study of Interconnection Networks Berneen processons & Memory modules Between Processing Nodes

Link, Switch, Network Interface => Network

Capacitive Coupling, Signal Attenuation Device with Set of input ports & Output ports Capable of mapping input to Output ports Total No. of Ports = Degree of a Switch Can internally buffer, perform honting & Capability to multicast. Cost of Switch dependent on mapping hardrare, peripheral hardrane & parkaging.
(« degree²) (« degree²) Interface: Has input & Dutput ponts that pipe data into and Out of the network Packetizing data Buffer incoming and outgoing data for marching speeds of nemonk and processing elements Error cheeting Position of parement can determine performance (Ilo Bus, Memory hus)

Link: Physical media connection (wines)

Network Dynamic Static (Direct) (Indinect)



Memore Topologies

- Bus-based Networks

- Shared Medium

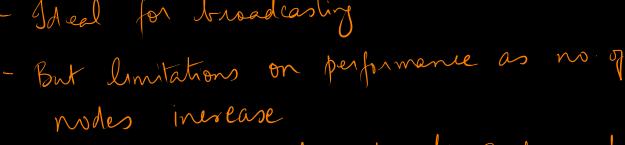
- Cost of Nemonk Scales

linearly with P

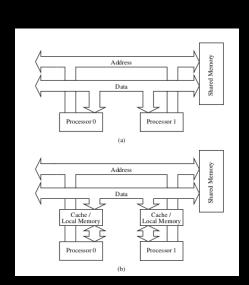
- Distance between any

two nodes is constant

- Ideal for broadcasting



- Add cache at each node to reduce demands on his bandwidth



p processors, each accessing k data items, each data access takes time t, then Minimum time needed to complete the application

Dut of the R accesses, if 50% accesses are local, and if cached, then,

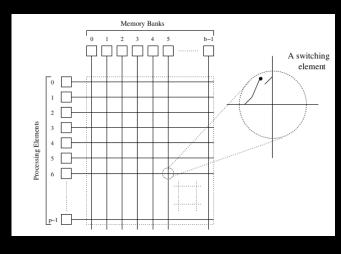
Minimum time needed to Complete the application z 0.5 ktp + 0.5 kt

(assuming same Cache access time)
as p becomes large,

≈ 0.5tkp => 50% improvement in the lower bound

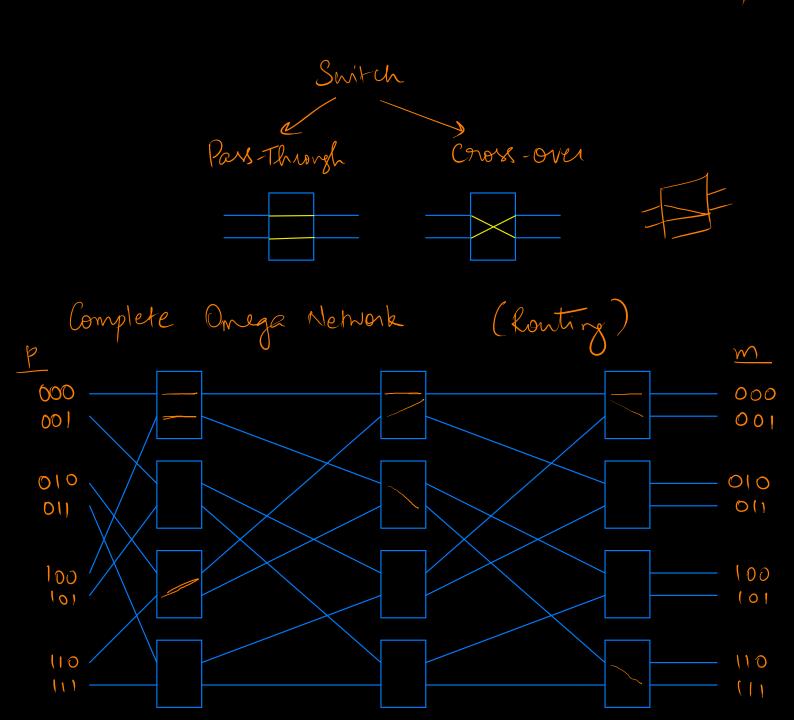
II. Crosslar Nemorles

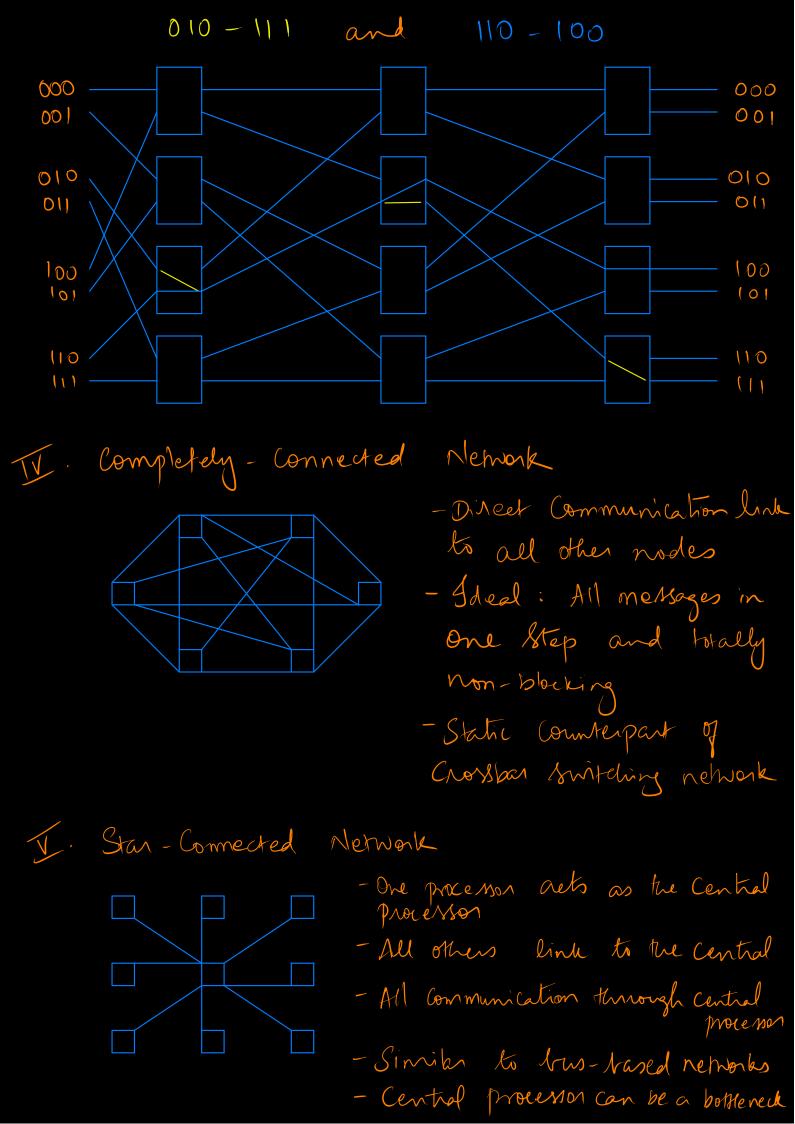
to memory banks processors to

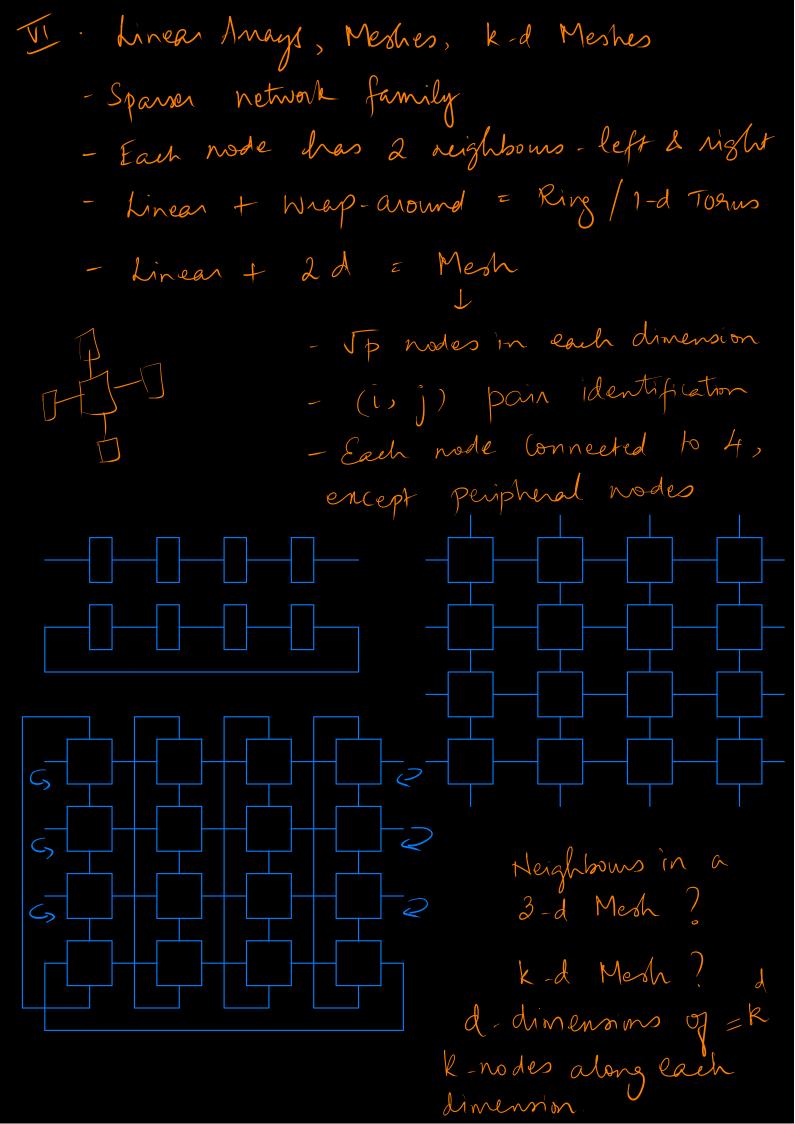


| - Non-Blocking network | | |
|------------------------------------|---------------|--|
| - But total no. of | huitching no | des = O(pb) |
| - Reasonable to assi | ume b ≥ | þ |
| =) No. y Switching | nodes = N | -(p²) |
| - Not Scalable in | terms of Cost | |
| TT. Multistage Network | <i>L</i> 3 | |
| Crosslar - Not & | calable in | terms of Cost |
| Bus - n | | r performance |
| =) Intermediate & | vention | |
| General Schematic: | [| connection network Memory banks O Stage n b-1 |
| Omega Mehwork i - Commonly used | 2 | Shuffle (Left Rotate) |
| - p z b | 000 0 | 1 001 |
| - log p trages | 010 2 | 2 010 |
| - P/2 Switches at | 011 3 | 3 011 |
| each stage | 100 4 | 4 100 |
| - O (plug p) Switches (not o (p | 1015 | 5 101 |
| (7001 0 (7 | 10 7 | 7 111 |
| | | |

In integer authoritie $j = \int_{2i}^{2i} 0 \le i \le p/2-1$ $\int_{2i+1-p}^{2i} p/2 \le i \le p-1$







T). Hypercute Nework 110 0 00 10 20 40 Numbering Isheme for hypercube: k+1 - dimensional k-dimensional hypercute -> hypercute k-dimensionel hypercute - prodes =) a) p/2 nodes + b) P/2 modes Prefix a) with O =) Mrimum distance between Prefix b) with 1 two nodes = No. of bits that are different in the two latels

Thee based Networks Processing Elements - Only one path between any pain of nodes - Star & Linear aways are special cases - Same node bends message up the tree until it Leaches Lost of the Smallest Subtree Containing both some à destration nodes. Then message is nonted down to destination - Bottleneck in the modes higher up the tree - Alleviated in dynamic tree by increasing no- of Communication links and Switching nodes closer to the host - Fat Tree