SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA

School of Electrical Engineering

B. Tech. (EE) Minor-I Examination (Odd) 2023-24

Entry No: | | | | | | | | | |

Date: 27th Sept. 2023

Total Number of Pages: [01]

Total Number of Questions: [04]

Course Title: Advanced Embedded Systems

Course Code: ECE 4082

Time Allowed: 1.0 Hours

Max Marks: [20]

Instructions / NOTE (Faculty may insert/delete other relevant instructions if required)

i. Attempt All Questions.
ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
iii. Assume an appropriate data / information, wherever necessary / missing.

	Section - A		
Q1.	(a) An embedded system uses UART to send data at a baud rate 115,200 bits/s with 7 data bits. How many total symbols transmitted for a 240 KB of data. (A) 1,520,320 bits, (B) 1,620,320 bits, (C) 1,720,320 bits, (D) 1,820,320 bits	[01]	CO2
	(b) SPI protocol is (A) Simplex, (B) Half duplex, (C) Full duplex	[01]	CO2
	(c) MOSI in SPI protocol means (A) Line for master to send data to slave, (B) Line for the slave to send data to the master (C) Line for the clock signal, (D) Line for the master to select which slave to send data to	[01]	CO2
	(d) Digital Signal Processors are especially suited for (A) Control dominated circuits (B) Data dominated circuits (C) general purpose circuits (D) None of the above	[01]	CO1
	(e) Pipelining generally provides (A) High performance (B) High throughput (C) Both A and B	[01]	CO1
	Section - B		
Q2.	Describe Embedded Co-design Process with neat flow diagram.	[05]	CO1
Q3.	Write step-by-step, the partitioning algorithm in Embedded Co-design process.	[05]	CO1
Q4.	Sketch with a neat and detailed flow diagram the Finite State Machine (FSM) Model for the Elevator Controller design with following specifications: 1) Move the elevator either up or down to reach the requested floor. 2) Once at the requested floor, open the door for at least 10 seconds, and keep it open until the requested floor changes. 3) Ensure the door is never open while moving. 4) Don't change directions unless there are no higher requests when moving up or no lower requests when moving down *No need to write any description. The FSM diagram should be complete.*	[05]	CO2

Course Outcomes

CO1. Acquire a basic knowledge about fundamentals of embedded systems with application examples
CO2. Acquire knowledge co-design, hardware software synthesis, system architecture
CO3. Various Scheduling algorithms and embedded architectural aspects
CO4. Hardware Synthesis and software using C for various applications

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1	1(d), 1(e), 2, 3	12	100
CO2	1(a), 1(b), 1(c), 4	8	100
CO3			
CO4			

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	(b) SPI protocol is (A) Simplex, (B) Half duplex, (C) Full duplex	[01]	CO2
	(c) MOSI in SPI protocol means (A) Line for master to send data to slave, (B) Line for the slave to send data to the master (C) Line for the clock signal, (D) Line for the master to select which slave to send data to	[01]	CO2
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SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA

School of Electrical Engineering

B. Tech. (ECE & EE) Minor-II Examination (Odd) 2023-24

Entry No: | | | | | | | | | |

Date: 8th Nov. 2023

Total Number of Pages: [01]

Total Number of Questions: [04]

Course Title: Advanced Embedded Systems

Course Code: ECE 4082

Time Allowed: 1.0 Hours **Max Marks: [20]**

Instructions / NOTE

i. Attempt All Questions.
ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
iii. Assume an appropriate data / information, wherever necessary / missing.

	Section - A		
Q1.	(a) Define the process and thread. (b) Define the scheduling policy (c) Mention the various scheduling states of a process (d) Define Rate monolithic scheduling (e) Define Earliest Deadline First Scheduling (f) Define Priority Inversion (g) Mention two different styles for Inter Process Communication (h) Define time quantum.	[01*8]	CO2 CO3
	Section - B		
Q2.	Explain various scheduling policies in detail.	[04]	CO3
Q3.	Explain preemptive operating systems in detail.	[04]	CO4
Q4.	Explain various inter process communication mechanism in detail.	[04]	CO4

Course Outcomes

CO1. Acquire a basic knowledge about fundamentals of embedded systems with application examples
CO2. Acquire knowledge co-design, hardware software synthesis, system architecture
CO3. Various Scheduling algorithms and embedded architectural aspects
CO4. Hardware Synthesis and software using C for various applications

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1			
CO2	1	2	102
CO3	1, 2	10	102
CO4	3, 4	8	102

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CO2	1	10	102
CO3	1, 2	8	102
CO4	3, 4		