SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics and Communication Engineering
B. Tech. ECE and Elect. Engineering 2nd Year- Midterm Examination (Odd)
2021-22 (October-2021)

Entry No: 2 0 b e c 0 8 5 | **Total Number of Pages:[02]**
Date: | **Total Number of Questions: [14]**

Course Title: Digital Electronics
Course Code: ECL 2070

Time Allowed1: 1:30Hours **Max Marks: [30]**

All questions are compulsory

Q1.	How many entries will be in the truth table of a 4-input NAND gate?	[01]
Q2.	How many bits are needed to store one BCD digit?	[01]
Q3.	Convert $(312)_8$ into decimal	[01]
Q4.	Which of these sets of logic gates are known as universal gates? a. XOR, NAND, OR b. OR, NOT, XOR c. NOR, NAND, XNOR d. NOR, NAND	[01]
Q5.	What is the addition of the binary number 101001 + 010011=?	[01]
Q6.	1's complement of 101101 is -------	[01]
Q7.	In Digital electronics (Boolean algebra), the OR operation is performed by which of the given properties a. Distributive properties b. Commutative properties c. Associative properties d. All of these	[01]
Q8.	DeMorgan's Law states that a. $(A+B)' = A'*B$ b. $(AB)' = A' + B'$	[01]

	d. (AB)' = A + B	
Q9.	The logical sum of two or more than two logical products is termed as a. OR operation b. POS c. SOP d. NAND operation	[01]
Q10.	The Minterms for four variable (a) 4 (b) 8 (3) 12 (4) 16	[01]
Q11.	Show how to connect NAND gates to get an AND gate and OR gate?	[05]
Q12.	Using K map, minimize the expression $F(A,B,C,D) = \sum m(1,2,3,8,14,15)$	[05]
Q13.	Realize the Boolean expression Z=ABC + AD + CD' using NAND gates only.	[05]
Q14.	What is two's - complement method of representing integer numbers. Is it better than one's complement method of representation?	[05]

Course Outcomes

1. To provide the skills to efficiently acquire knowledge on digital electronic circuit analysis and design.
2. To acquire Knowledge of various number systems and codes from historic point of View and to understand the logic families in digital circuits.
3. To obtain the ability to analyze various aspects of combinational circuit design.
4. To obtain the ability to analyze various aspects of sequential circuit design.
5. To learn the design procedure for Sequential Circuits and data converters.

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA

School of Electronics and Communication Engineering

B. Tech. (E&CE and EE and Backlog) Major Examination (Odd Sem) 2023-24

Entry No: 2 2 b e c 0 8 8

Total Number of Pages: [02]

Date:

Total Number of Questions: [07]

Course Title: Digital Electronics

Course Code: ECL 2070

Time Allowed: 3 Hours

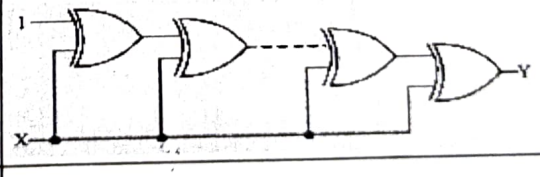
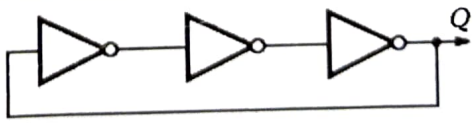
Max Marks: [50]

Instructions / NOTE

i. Attempt All Questions.

ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.

iii. Assume any missing data to suit the case/derivation/answer.

Q. No.1.	i.	Consider the number D is given by the decimal expression: $D = 16^3 \times 9 + 16^2 \times 7 + 16 \times 5 + 3$. Determine the number of 1's in the unsigned binary representation of D.	[2]	CO1
	ii.	In canonical SOP form, the no. of min terms representing the logical expression $A + \overline{B}C$ is	[2]	CO1
	iii.	How many corrections are required in the BCD addition of $(45)_{10} + (23)_{10}$?	[2]	CO1
	iv.	By which factor the output of last flip-flop of a ripple counter divides the i/p clock frequency?	[2]	CO2
	v.	A 5-bit DAC converter produces $V_{OUT} = 0.2$ V for a digital input of 0001. Find the value of V_{OUT} for an input of 11111.	[2]	CO4
	vi.	For a 3-bit ripple counter using D flip flops, the propagation delay of each flip flop is 50 nsec. Determine the maximum clock frequency that can be used in the counter.	[2]	CO3
	vii.	Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?	[2]	CO2
Q. No.2.	i.	What is the output of the digital circuit consisting of a cascade of 20 EX-OR gates as shown here? 	[4]	CO2
	ii.	Consider the propagation delay of each NOT Gate equal to t_{pd}. Draw the output of the circuit in the form of a timing diagram. 	[4]	CO2
Q. No.3	i.	What are the different types of hazards and their sources in the design of digital circuits?	[4]	CO3
	ii.	Show the design of a static hazard-free 1-bit full adder using NOR gates only.	[4]	CO3
Q. No.4		Assume input to a 7-segment common cathode LED is a four-bit BCD numeral from 0 to 9. Show the design of a Decoder for the segment 'b' of the LED.	[5]	CO3
Q. No.5		Implement the logical expression $f(A,B,C) = \sum_m(1,2,3,5,6,7)$ using a 4:1 multiplexer.	[5]	CO3
Q. No.6.		Design a synchronous counter to count the sequence 0-1-2-3-4-5-0. The counter should return to reset state (0) if any unwanted state is encountered.	[5]	CO3
Q. No.7.		Show the design process and the logic diagram to convert a D to J-K flip flop.	[5]	CO3

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics and Communication Engineering
B. Tech. (EE/ECE)-2nd Year- Minor-2 Examination (ODD) 2022-23 (November-22)

Entry No: | | | | | | | | | |

Date:

Total Number of Pages:[01]
Total Number of Questions: [5]

Course Title: Digital Electronic
Course Code: ECL 2070

Time Allowed1: 1:30Hours **Max Marks: [20]**

Instructions / NOTE

i. Attempt All Questions.
ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
iii. ***No marks will be awarded for just attempting a question/writing the formula/drawing merely the figure without proper explanation.***
iv. ***Step marking is not proposed.***
v. Assume any missing data to suit the case / derivation / answer. Symbols have their usual meaning

Q1.	Implement 16:1 mux using 8:1 multiplexers.	[04]
Q2.	Implement the expression using a multiplexer. $f(A, B, C, D) = \Sigma m(0, 2, 3, 6, 8, 9, 12, 14)$	[04]
Q3.	Design 3 to 8 binary decoder.	[04]
Q4.	Write truth table for a basic half adder and implement its designing using basic gates.	[04]
Q5.	Four messages are encoded in the following code words: *Message* — *Code* M_1 — 01101 M_2 — 10011 M_3 — 00110 M_4 — 11000 Determine the minimum distance of this code.	[04]

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA

School of Electronics and Communication Engineering

B. Tech. (EE/ECE)-2nd Year- Minor-1 Examination (ODD) 2022-23 (September-22)

Entry No: 2 1 B E C 1 2 7

Date: 28/09/22

Total Number of Pages:[01]

Total Number of Questions: [5]

Course Title: Digital Electronics

Course Code: ECL 2070

Time Allowed1: 1:30Hours **Max Marks: [20]**

Instructions / NOTE

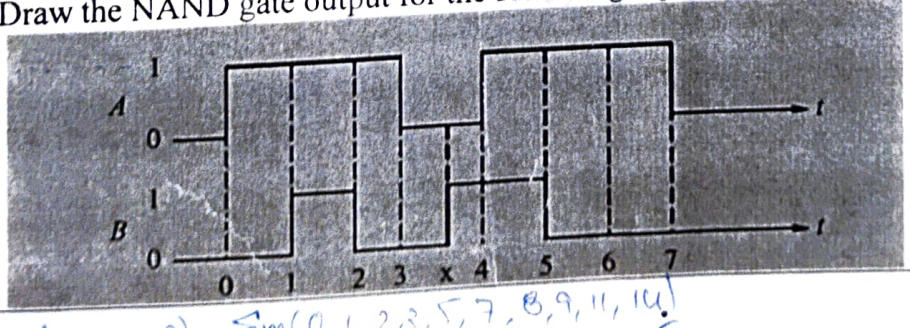
i. Attempt All Questions.

ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.

iii. ***No marks will be awarded for just attempting a question/writing the formula/drawing merely the figure without proper explanation.***

iv. ***Step marking is not proposed.***

v. Assume any missing data to suit the case / derivation / answer. Symbols have their usual meaning.

Q1.	What is canonical form of representation of logic functions? Explain with suitable examples	[04]
Q2.	Minimise the four-variable logic function using K-map: $f(A, B, C, D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$	[04]
Q3.	Minimise the following function and implement the same with basic gates. $f(A, B, C, D) = \Pi M(4, 5, 6, 7, 8, 12).\ d(1, 2, 3, 9, 11, 14)$	[04]
Q4.	Minimise the four variable logic function $f(A,B,C,D) = (A+B+\bar{C}+\bar{D})\cdot(\bar{A}+C+\bar{D})\cdot(\bar{A}+B+\bar{C}+\bar{D})\cdot(\bar{B}+C)\cdot(\bar{B}+\bar{C})\cdot(A+\bar{B})\cdot(\bar{B}+\bar{D})$	[04]
Q5.	Draw the NAND gate output for the following input signal. 	[04]

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics and Communication Engineering
B. Tech. (Electrical/Electronic Engineering)-2nd Year- Major Examination (Odd)
2022-23 (December-2022)

Entry No: 2 1 B E C 1 | | | |
Date:

Total Number of Pages:[01]
Total Number of Questions: [8]

Course Title: Digital Electronic
Course Code: ECL 2070

Time Allowed1: 3 Hours **Max Marks: [50]**

Instructions / NOTE

i. Attempt All Questions.
ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
iii. ***No marks will be awarded for just attempting a question/writing the formula/drawing merely the figure without proper explanation.***
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Q1.	Draw general block diagram of a sequential circuit and differentiate it with a combinational circuit.	[06]
Q2.	Design D-FF from a general JK FF. Write its characteristic table. Explain two applications of DFF.	[06]
Q3.	Draw parallel – comparator ADC and explain its working principle.	[06]
Q4.	Using SR FF as Toggle FF find the output of the sequence "1001101"	[06]
Q5.	Draw block diagram of a successive approximation ADC. Explain its operating principle.	[06]
Q6.	Write short notes on any two : (1) Register (2) Dual slope ADC (3) Ring counter	[08]
Q7.	Design basic memory cell element using NAND gates and explain its operation	[06]
Q8.	Differentiate between DRAM and SRAM and draw their conceptual circuits.	[06]