Shri Mata Vaishno Devi University, Katra

School of Electronics & Communication Engineering

B. Tech. (CS&E) /B.Tech.(ECE)/B.Tech.(EE)-4th Semester

Minor-I (Even Semester) 2022-23

Entry No._____ Date: 20/02/2023

Course Title: Microprocessor & Interfacing

Course Code: ECL 2060

Time Allowed: 1 ½ Hours **Max Marks: [20]**

i. Attempt All Questions. ii. Make Assumptions as needed

Q1.	Assuming that a crystal of 4MHz is connected to the 8085 micro-processor, calculate the number of T-states and the time required for execution of the following programs: **(2 Marks x 2=4 Marks)** a) LDA 2000H LXI H, 2002H MOV, M, A b) LXI H, 2020H MVI M, 7FH MVI A, 0FH ADD M	CO3
Q2.	What is the importance of the following signals of 8085 microprocessor: **(1 Marks x 3=3 Marks)** a) IO/$\overline{M}$ b) ALE c) READY	CO2
Q3.	Draw the Timing diagram showing the fetch and execution of 8085 instruction *LXI*. **(3 Marks)**	CO2
Q4.	Interface one 8K ROM IC & two 2K RAM ICs with 8085 with starting address of ROM from 0000H and all subsequent addresses of the memory ICs in sequence. Show complete process for arriving at the design of the address decoding logic and draw the diagram showing the circuit for the same. **(3 Marks)**	CO2
Q5.	Write a program in 8085 assembly language to perform the addition of two 16-bit numbers. First number is stored at 6100H (Lower byte) & 6101H (Upper byte) while the second number is stored at 6102H (Lower byte) & 6103H (Upper byte). The 16-bit sum is to be stored at memory location 6104H (Lower byte) & 6105H (Upper byte). **(3 Marks)**	CO1

Q6.	Indicate the status of all the flags & contents of Accumulator after completion of execution of these instructions: **(4 x 1 Marks = 4 Marks)**
	a) MVI A,0AH
	SUI 00H
	ADI FFH
	b) MVI A, 0AH
	LXI H, FFFFH
	MOV M,A
	ADD M
	c) MVI A, 29H
	MVI B, F9H
	SUB B
	d) LXI H, 2020H
	MVI C, 5AH
	SUI 01H
	MOV M, C
		CO1

Shri Mata Vaishno Devi University, Katra

School of Electronics & Communication Engineering

B. Tech. (CS&E) /B.Tech.(ECE)/B.Tech.(EE)-4th Semester

Minor-II (Even Semester) 2022-23

Entry No._____ **Date: 29/03/2023**

Course Title: Microprocessor & Interfacing

Course Code: ECL 2060

Time Allowed: 1 ½ Hours **Max Marks: [20]**

i. Attempt All Questions. ii. Make Assumptions as needed

Q1.	Assuming that a crystal of 6MHz is connected to the 8085 micro-processor, indicate the status of Register A, HL, SP and BC and the flags after the execution of the following programs. Also calculate the time for execution of each program: **(2 Marks x 2=4 Marks)** a) MVI A, ACH LXI H, 2002H Again: DCR A INX H JNZ Again XRA A b) LXI SP, 27FFH MVI A, 7FH DCR A PUSH PSW DCR A POP BC	CO3
Q2.	a) What is the difference between a sub-routine and an Interrupt Service Routine for a hardware interrupt? **(1 Marks)** b) What are the steps taken by the microprocessor in response to PUSH Instruction. **(1 Marks)** c) What are the steps taken by the microprocessor when proper triggering signal is received on TRAP interrupt pin of the microprocessor? **(1 Marks)**	CO2
Q3.	Draw the Timing diagram showing the fetch and execution of 8085 instruction **RET. (3 Marks)**	CO2
Q4.	A circuit has been designed to count the number of steps taken by the user. The circuit generates a pulse for every step taken by the user which is connected to the RST 7.5 interrupt of the microprocessor. Write the main program and the Interrupt Service Routine for RST 7.5 such that the count at memory location 2000H always shows the actual number of steps taken by the user at any time. **(3 Marks)**	CO2
Q5.	Write a program in 8085 assembly language which checks the number stored at all memory locations between 2000H and 2021H and replaces them with another number as follows. For each of these memory locations if the number at the memory location is 31H, then the number is replaced by 00H, if number is greater than 31H then it is replaced by 99H and if the number is less than 31H then it is replaced by 11H. **(3 Marks)**	CO
Q6.	Write a sub-routine called UNPACK which accepts a packed BCD number in Accumulator and returns the two unpacked BCD digits in Register B & C. e.g. if Register A contains 78H then the subroutine will separate the two digits and return 07H in Register B & 08H in Register C. Now write a program which reads the packed BCD number from memory location 2000H and stores the unpacked BCD digits at 2001H and 2002H by calling the subroutine UNPACK. **(4 Marks = 3 Marks)**	CO

CO	Course Outcome

Shri Mata Vaishno Devi University, Katra

School of Electronics & Communication Engineering

B. Tech. (E&CE/CS&E/EE)-4th Semester Major (Even Semester) 2022-23

Entry No. 21BEC127 Date: 08/05/2023

Course Title: Microprocessor & Interface ECL 2060

Time Allowed: 3 Hours **Max Marks: [50]**

i. Attempt All Questions. ii. Make Assumptions as needed. iii. Assume a crystal of 6MHz

.	**Answer the following in brief: (2 + +2+ 4 x 1 = 8 Marks)**	
	(a) Calculate the delay generated because of the following code snippet: **(2 Marks)**	CO3
	LXI B, 2002H Again: DCR C INR B JNZ Again	
	(b) What is DMA? How is it useful with a microprocessor? **(2 Marks)**	CO2
	(c) Write the structure of the RIM instruction of 8085 µ-processor.	CO1
	(d) What is the INT 0 interrupt in 8086 µ-processor used for?	CO3
	(e) MUL instruction in 8086 µ-processor can be used to multiply two ____-bit numbers to get a ____-bit product.	CO2
	(f) Calculate the 20-bit address if the content of DS=2100H and SI=1345H. Show how it is calculated.	CO2
Q2.	a) Explain the architecture of the 32-bit ColdFire™ V2 Core with a diagram to show why this architecture supports faster fetch and execution of a program. **(4 Marks)**	CO2
	b) Write a program in 8086 assembly language to divide a 16-bit number by an 8-bit number and find the quotient and remainder. **(4 Marks)**	CO1
Q3.	a) Write a Delay subroutine in 8085 assembly language which generates a delay of 220 µs if the data at memory location 4100H is DCH or generates a delay of 110 µs if the data at memory location 4100H is 6AH. Assume that the crystal frequency is 6MHz. **(4 Marks)**	CO1/ CO3
	b) Draw a properly labeled Timing diagram for the fetch & execute cycle for the instruction **LDAX B**. Assume that this instruction is stored starting from memory location 3000H. **(4 Marks)**	CO1/ CO3
Q4.	a) Design and draw a circuit diagram showing the interface of two 8KB ROMs, & two 2 KB RAM ICs with 8085 µ-processor with starting address of ROM at 0000H while the address of RAMs should start from 5000H. **(4 Marks)**	CO2
	b) Write about the addressing modes of instructions in 8086 µ-processor with an example. Identify the addressing modes for following instructions a) MOV AX, [BX+DI] b) MOV AX, [1592H]. **(3+1=4 Marks)**	CO1
Q5.	a) What is the advantage of memory segmentation as implemented in 8086 µ-processor? **(2 Marks)**	CO4
	b) Why does the execution of the instruction MOV AX, [DS:1200] require only one memory read cycle while the execution of the instruction MOV AX, [DS:1201] requires 02 memory read cycles? **(2 Marks)**	CO4
	c) Draw the internal block diagram of 8255PPI and write briefly about Mode 0 and Mode 1. Show the structure of the Control Register of 8255PPI and show what number should be stored in the Control register so that all ports work as output ports and both groups function in Mode 0. **(3+1=4 Marks)**	CO2
Q6.	a) Explain the difference in response between the 8085 µ-processor & the 8086 µ-processor when they receive an external interrupt signal on the INTR pin. **(5 Marks)**	CO4
	b) Write a subroutine **PROD** for 8085 µ-processor which accepts two 8-bit numbers in H & L and returns their 16-bit product in registers B & C. Write another program to perform the multiplication of two bytes stored at memory location 4000H and 4001H and store the 16-bit product at 4002H (LSB) and 4003H (MSB) by calling the **PROD** subroutine. **(5 Marks)**	CO1

Course Outcomes

Shri Mata Vaishno Devi University, Katra

School of Electronics & Communication Engineering

B. Tech. (E&CE & EE -Backlog)-4th Semester Major (Even Semester) 2024-25

Entry No._____ Date: 24/07/2025

Course Title: Microprocessor & Interface ECL 2060/ECL DC206

Time Allowed: 3 Hours Max Marks: [40]

i. Make Assumptions as needed. ii. Assume a crystal of 4MHz

Q1.	**Answer the following in brief: (9 Marks)**	
	(a) If the value in the DS Register of 8086 microprocessor is 0010H and SI register is 3200H then what is the physical 20-bit address? Show how this is calculated? **(2 Marks)**	CO4
	(b) What is MAX mode of 8086 microprocessor? Name any two signals which are used in MAX mode? **(2 Marks)**	CO2
	(c) Draw the structure of Control register of 8255 and explain its bits? **(2 Marks)**	CO2
	(d) Can interrupts be implemented in 8085 microprocessor without stack? **(1 Mark)**	CO3
	(e) If the address of Port C of 8255 is 92H then what's the address of Port A and Control Register? **(2 Marks)**	CO2
Q2.	a) Write a program in 8085 assembly language to add two 16-bit numbers stored at memory locations 2000H & 2001H and 2002H & 2003H and store the 16-bit sum at 2004H and 2005H (Assume answer will be of 16 bit only). Calculate Total T-states for the execution of the program **(3 Marks)**	CO3
	OR	
	Write a program in 8086 assembly language to add two 8-bit numbers stored at memory locations 5000H & 5001H and store the 16-bit sum at 5002H and 5003H. Assume the value of DS=2100H. **(3 Marks)**	CO3
	b) Write program in 8085 assembly language to copy even numbers stored between memory location 2000H to 2010H to memory locations starting from 2020H onwards. **(3 Marks)**	CO1
	OR	
	What will be the contents in the Accumulator such that on execution of SIM instruction RST 5.5 and RST 6.5 are masked while RST 7.5 is not masked.? Show properly with reference to SIM instruction **(3 Marks)**	CO1
	c) With neat sketch, explain the interrupt architecture of 8085 microprocessor. **(3 Marks)**	CO2
Q3.	a) With the help of a diagram show how an instruction queue is implemented in the 8086 microprocessor? What is its advantage? Does 8085 have an equivalent mechanism? **(2+2=4 Marks)**	CO4
	OR	
	What is the use of a) BHE signal and b) MN/MX signal in the 8086 microprocessor? Are there equivalent signals in 8085 microprocessor? **(4 Marks)**	CO4
	b) Why is there a need for memory segmentation in the 8086 µ-processor? **(2 Marks)**	CO2
	c) With help of a diagram show how Even & Odd memory addresses are accesses from the Even and Odd memory banks of the 8086microprocessor? How many memory read cycles will be required for accessing 2 bytes of data if the start address is from the Even bank e.g. MOV AX, [DS:1200] **(4 Marks)**	CO2
Q4.	a) Show the interface of two 8K ROM and two RAM of 2K each, with the address of first ROM starting from 0000H and all other addresses in continuation. Show complete design process. **(4 Marks)**	CO1
	b) Draw a properly labeled Timing diagram for the fetch & execute cycle for the instruction **MOV A, M OR ADD M**. Assume that this instruction itself is stored starting from memory location 0000H. **(4 Marks)**	CO2
	c) Draw a circuit diagram showing the interface of one common anode 7 segment LED display with Port A of the 8255. **(1 Marks)**	CO2

	For the above circuit write code in assembly language to display the number 9 on the display. Assume that the address of Port A is 90H, Port B is 91H, Port C is 92H and Control Register is 93H. **(3 Marks)**	CO1

Course Outcomes

CO	Course Outcome
CO1	The student will be able to analyze, specify, design, write and test assembly language programs for 8085 microprocessor and basic programs to run on 8086 microprocessor-based systems.
CO2	The student will be able to understand the various aspects of the internal architecture of the 8085 microprocessor and will be able to design hardware circuits to interface the 8085 microprocessor to various ICs like RAM, ROM, 8255 etc.
CO3	The student will be able to calculate the worst-case execution time of programs or parts of programs, and to design and build, or to modify, software to maximize its run-time memory or execution-time behavior.
CO4	The student will be able to compare the architecture design for 8085, 8086 & Coldfire 32-bit microprocessor