SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. ECE (5th Sem) Minor-II Examination (Odd) 2023-24

Entry No: | | | | | | | | | |
Date:

Total Number of Pages: [02]
Total Number of Questions: [04]

Course Title: Digital System Design Using Verilog
Course Code: ECL 2071

Time Allowed: 1.0 Hours **Max Marks: [20]**

Instructions / NOTE (Faculty may include any other relevant instruction, if required)

i. Attempt All Questions.
ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
iii. Assume an appropriate data / information, wherever necessary / missing.
iv. Use of IS Code (Mention Number) is permissible in examination.

	Section – A		
Q1.	**(a)** Which out of these is not a positive edge (i) 0 to 1 (ii) X to Z (iii) Z to 1 (iv) 0 to Z	**[01]**	**CO1**
	(b) casex treats ____x____ and ____2____ as ____don't care____.	**[02]**	**CO1**
Q2.	**(a)** Design the state diagram (only) of a sequence detector to detect "0001" (from left to right), and gives a HIGH output for one clock cycle when detected successfully ?	**[03]**	**CO2**
	(b) Explain the difference between **forever –loop and repeat loop**	**[04]**	**CO2**
	Section – B		
Q3.	Write behavioral modeling code for 8:1 Mux using **case-statement.** **Or** Write behavioral modeling code for +ve level triggered 4-bit D-Latch with active low asynchronous RESET using **if-statement.**	**[05]**	**CO3**
Q4.	Write behavioral modeling code for -ve edge triggered 8-bit Up-Down counter, as UP counter if MODE = HIGH and as DOWN counter if MODE = LOW active low asynchronous RESET.	**[05]**	**CO3**

Course Outcomes

CO1. Describe the language constructs and programming fundamentals of Verilog HDL.
CO2. Choose the suitable abstraction level for a particular digital design
CO3. Construct Combinational and sequential circuits in different modeling styles

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1	Q1	05	84
CO2	Q2	05	84
CO3	Q3, Q4	10	84

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. ECE (5th Sem) Minor-1 Examination (Odd) 2023-24

Entry No: 2 0 2 e c 0 0 3
Date:

Total Number of Pages: [02]
Total Number of Questions: [05]

Course Title: Digital System Design Using Verilog
Course Code: ECL 2071

Time Allowed: 1.0 Hours **Max Marks: [20]**

Instructions / NOTE (Faculty may include any other relevant instruction, if required)

i. Attempt All Questions.
ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
iii. Assume an appropriate data / information, wherever necessary / missing.
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	Section – A		
Q1.	**(a)** Verilog identifier can be two types: _____ and _____.	**[01]**	**CO1**
	(b) In behavioral modeling **begin-end** is a _____ while **fork-join** is a _____.	**[01]**	**CO1**
	(c) If A=1 'b1, B=4 'h B, C=3 'O 3, then, y={4{A},2{B},C} equals i) 14 'b1111_1011_1011_11 ii) 15 'b1111_1011_1011_011 iii) 15 'b1000_0000_0110_011 iv) 15 'b0100_1011_1011_011	**[01]**	**CO1**
Q2.	**(a)** The two inputs applied to a 4-bit full adder verilog module while simulating the design are: **in1 = 4 'b 101x** and **in2 = 4 'b 1101**. What would be the SUM and CARRY outputs for this combination of inputs ?	**[02]**	**CO3**
	(b) What values are assigned to left hand side object on its execution if RUN = 'b 0101_1101_1011 and FAST = 'h ABCD ? **(i)** GOAL = ~& (RUN) ; **(ii)** GOAL = & (~RUN) ; **(iii)** GOAL =RUN & (~FAST) ;	**[03]**	**CO1**
	Section – B		
Q3.	**(a)** Draw the state diagram of a toggle flip flop.	**[02]**	**CO2**
	(b) Design state machine diagram of JK flip flop using toggle flip flop.	**[03]**	**CO2**
Q4.	Design a Verilog module for **2:1 mux** using behavioral modeling. Then use this **2:1 multiplexer** Verilog module to design another Verilog module for **4:1 multiplexer**. **(Must be supported with Block/circuit diagrams; Note: name of ports must objective of the question)**	[04]	**CO3**

Q5.	Draw the test pattern generated from the following Verilog code:	[03]	CO4

```
module test_bench ();
-----
   initial
      clk = 1 'b0;
   always
      # 15 clk = ~ clk;
   initial
     begin
        #12  run <= 1;
        #5   bun <= 0;
        begin
           tun = 1;
           #5  gun = 0;
           #5  run  = 0;
        end
     end
-----
endmodule
```

Course Outcomes

CO1. Describe the language constructs and programming fundamentals of Verilog HDL.

CO2. Choose the suitable abstraction level for a particular digital design

CO3. Construct Combinational and sequential circuits in different modeling styles using Verilog

CO4. Analyse and Verify the functionality of digital circuits/systems using test benches

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1	1(a), 1(b), 2(b)	06	84
CO2	3(a), 3(b)	05	84
CO3	2(a), 4	06	84
CO4	5	03	84