

RAK811 Lora Module

Datasheet V1.4

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1. General Description

RAK811 Low-Power Long Range LoRa Technology Transceiver module, provides an easy to use, small size, low-power solution for long range wireless data transmission.

First, The RAK811 module complies with the latest LoRaWAN Class A & C protocol specifications, it is simple to access LWPA IOT platforms, such Actility etc. Second, it also support Lora Point to Point communications, this function can help customers implement their own private long range Lora network fast.

Module integrates semtech SX1276 and stm32L, offer user an serials At commands with UART Interface .It is easy to accomplish their applications, such as simple long range sensor data applications with external host MCU, low-power feature is suitable for battery applications.

This compact module is a total solution which developing of LORA-wan protocol techniques. The module's applications as following:

- 1. Automated Meters Reading
- 2. Home and Building Automation
- 3. Wireless Alarm and Security Systems
- 4. Industrial Monitoring and Control
- 5. Long Range Irrigation Systems

2. Features

- > LoRaWAN protocol supported, support global license-free ISM band, full certification by region.
 - Lora Point to Point communication, Activation by OTAA/ABP
- Easy to use, UART interface, serial port AT command, baud rate and air rate online change supported, simple ASCII command set.
 - Maximum output power 100MW (20dBm), adjustable from 5 to 20dBm.
 - ➤ High sensitivity,-148 dBm, enabling extremely long range connectivity.
 - > Long range greater than 15 km.
 - High capacity of up to 1 million nodes
 - > Low power consumption, 500nA on standby, in-air wake-up supported.
 - Multi-channel, dual data buffer (256byres each).
 - ➤ LoRa/FSK/GFSK/OOK modulation, bidirectional 2 way communications.
 - Long battery life over 10 years.
- > LoRa technology is capable of demodulating 20 dB below noise level, significantly improving immunity to the interference when combined with integrated forward error correction.



3. System Block Diagram

The block diagram of module is depicted in the figure below.

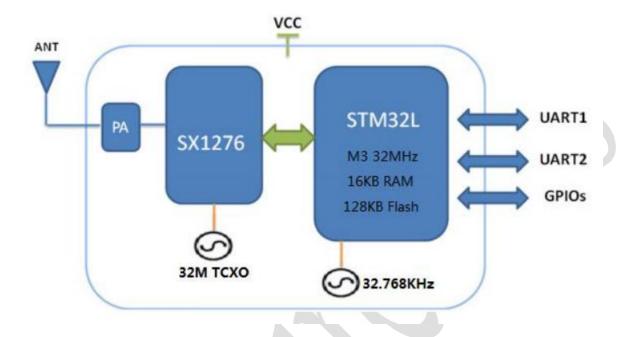


Figure 3-1 System Diagram



4. Hardware Description

4.1 Low RF Hardware

Low radio frequency hardware support the regions of EU433 and CN470.

4.1.1 Low RF Pin Outline

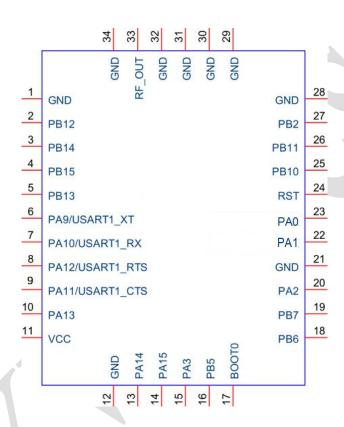


Figure 4-1 Low RF Pin outline

4.1.2 Low RF Pin definition

Table 4-1 Low RF Pin Definition

NO	Name	Type	Description
1	GND	_	Ground connections
2	PB12/ADC	I/O	ADC_IN18
3	PB14/ADC	I/O	ADC_IN20
4	PB15/ADC	I/O	ADC_IN21
5	PB13	I/O	B part for GPIO port
6	PA9/UART1_TX	О	UART1 Interface
7	PA10/UART1_RX	I	UART1 Interface



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8	PA12	О	A part for GPIO port	
9	PA11	I	A part for GPIO port	
10	PA13	I/O	A part for GPIO port	
11	VCC	P	Main power voltage source input	
12	GND	_	Ground connections	
13	PA14	I/O	A part for GPIO port	
14	PA15	I/O	A part for GPIO port	
15	PA3	I/O	A part for GPIO port	
16	PB5	I/O	B part for GPIO port	
17	BOOT0	I	Boot mode GPIO enable pin,high active	
18	PB6/I2C_SCL	I/O	I2C1_SCL	
19	PB7/I2C_SDA	I/O	I2C1_SDA	
20	PA2/ADC	I/O	ADC_IN2	
21	GND	_	Ground connections	
22	PA1/ADC	I	ADC_IN1	
23	PA0/ADC	О	ADC_IN0	
24	RST	I	Reset trigger input, low active	
25	PB10	I/O	B part for GPIO port	
26	PB11	I/O	B part for GPIO port	
27	PB2	I/O	B part for GPIO port	
28	GND	4	Ground connections	
29	GND		Ground connections	
30	GND		Ground connections	
31	GND		Ground connections	
32	GND		Ground connections	
33	RF_OUT	I/O	RF I/O port	
34	GND		Ground connections	

4.2 High RF Hardware

High radio frequency hardware support the regions of EU868, US915, AU915, KR920, AS923, IN865.

4.2.1 High RF Pin Outline

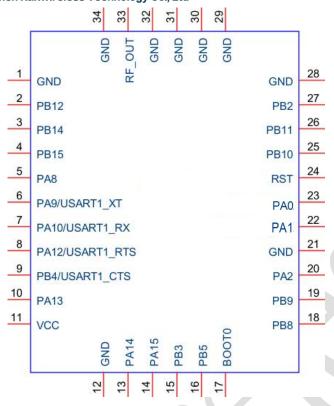


Figure 4-2 High RF Pin outline

4.2.2 High RF Pin definition

Table 4-2 High RF Pin Definition

NO	Name	Type	Description	
1	GND	_	Ground connections	
2	PB12/ADC	I/O	ADC_IN18	
3	PB14/ADC	I/O	ADC_IN20	
4	PB15/ADC	I/O	ADC_IN21	
5	PA8	I/O	A part for GPIO port	
6	PA9/UART1_TX	О	UART1 Interface	
7	PA10/UART1_RX	I	UART1 Interface	
8	PA12	О	A part for GPIO port	
9	PB4	I	B part for GPIO port	
10	PA13	I/O	A part for GPIO port	
11	VCC	P	Main power voltage source input	
12	GND	_	Ground connections	
13	PA14	I/O	A part for GPIO port	
14	PA15	I/O	A part for GPIO port	
15	PB3	I/O	B part for GPIO port	



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16	PB5	I/O	B part for GPIO port	
17	BOOT0	I	Boot mode GPIO enable pin, high active	
18	PB8/I2C_SCL	I/O	I2C1_SCL	
19	PB9/I2C_SDA	I/O	I2C1_SDA	
20	PA2/ADC	I/O	ADC_IN2	
21	GND	_	Ground connections	
22	PA1/ADC	I	ADC_IN1	
23	PA0/ADC	О	ADC_IN0	
24	RST	I	Reset trigger input,low active	
25	PB10	I/O	B part for GPIO port	
26	PB11	I/O	B part for GPIO port	
27	PB2	I/O	B part for GPIO port	
28	GND	_	Ground connections	
29	GND	_	Ground connections	
30	GND		Ground connections	
31	GND		Ground connections	
32	GND	-(Ground connections	
33	RF_OUT	I/O	RF I/O port	
34	GND	_	Ground connections	

4.3 Physical Dimensions

(Unit: mm)

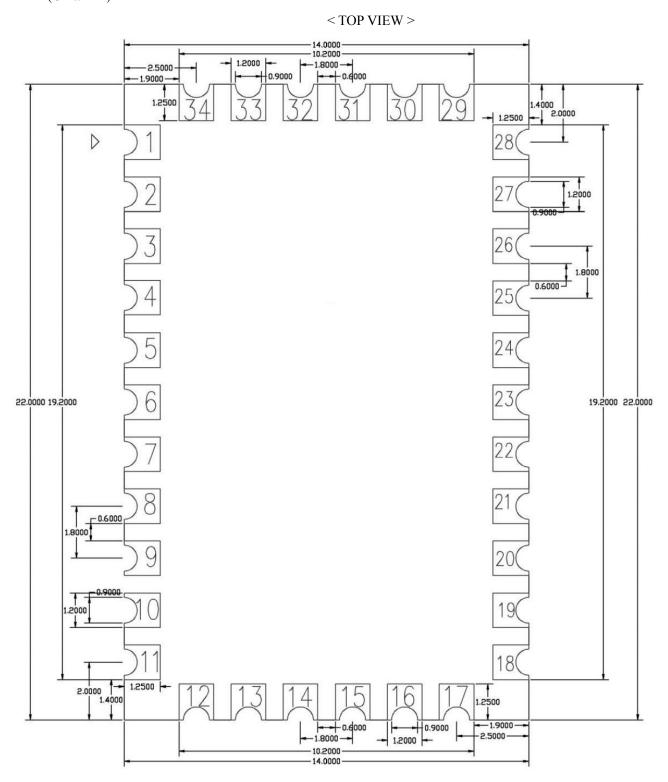
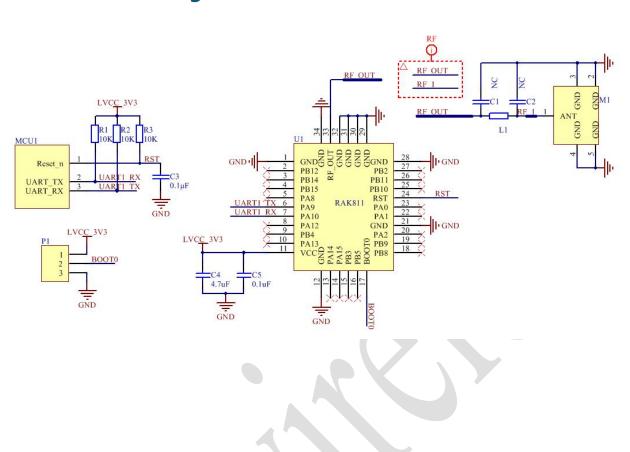


Figure 4-3 Module dimensions



5. Reference design





6. General Specification

6.1 General specification

Model Name	RAK811
Dimension	L x W x H: 22 x 14 x 1.7 mm
Interface	UART1, GPIOs
Operating temperature	-40°C to 85°C
Storage temperature	-40°C to 85°C

6.2 Recommended Operating Rating

	Min.	Тур.	Max.	Unit
Operating Temperature	-40	25	85	deg.C
VCC	3.15	3.3	3.45	V

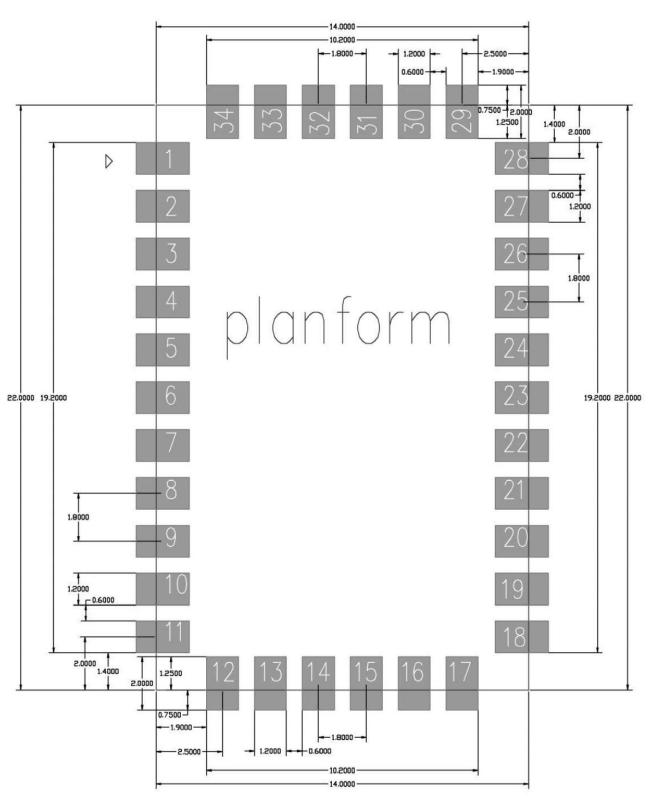
6.3 Specification

Feature	Description						
General Specification							
Frequency Band	RAK811-LF: EU433, CN470						
Trequency Bund	RAK811-HF: EU868, US915, AU	915, KR92	0, AS923	, IN865			
Host Interface	UART						
Characteristics	Condition	Min	TYP	MAX	UNIT		
Transmit	TX Power		14	20	dBm		
DV Congitivity	RSSI	-130	-		dBm		
RX Sensitivity	SNR	-15			dB		
	TX mode	30 (14dBm)			mA		
Current Consumption	RX mode	5.5			mA		
	Sleep mode	7.2			uA		

7. Layout Recommendation

(Unit: mm)

< TOP VIEW >



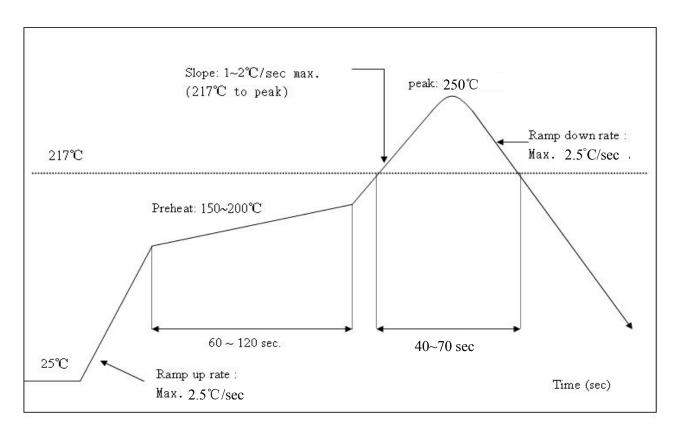


8. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250° C

Number of Times : ≤2 times







9. Contact information

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10. Revision History

Version	Date	Change
V1.0	2016-06-11	Draft
V1.1	2016-11-15	Add LoraP2P mode
V1.2	2017-08-11	Modify the Mode Pin Function , add reference design
V1.3	2017-08-18	Modify the Mode Pin Function
V1.4	2018-11-01	Modify the LF and HF module pins and supported regions