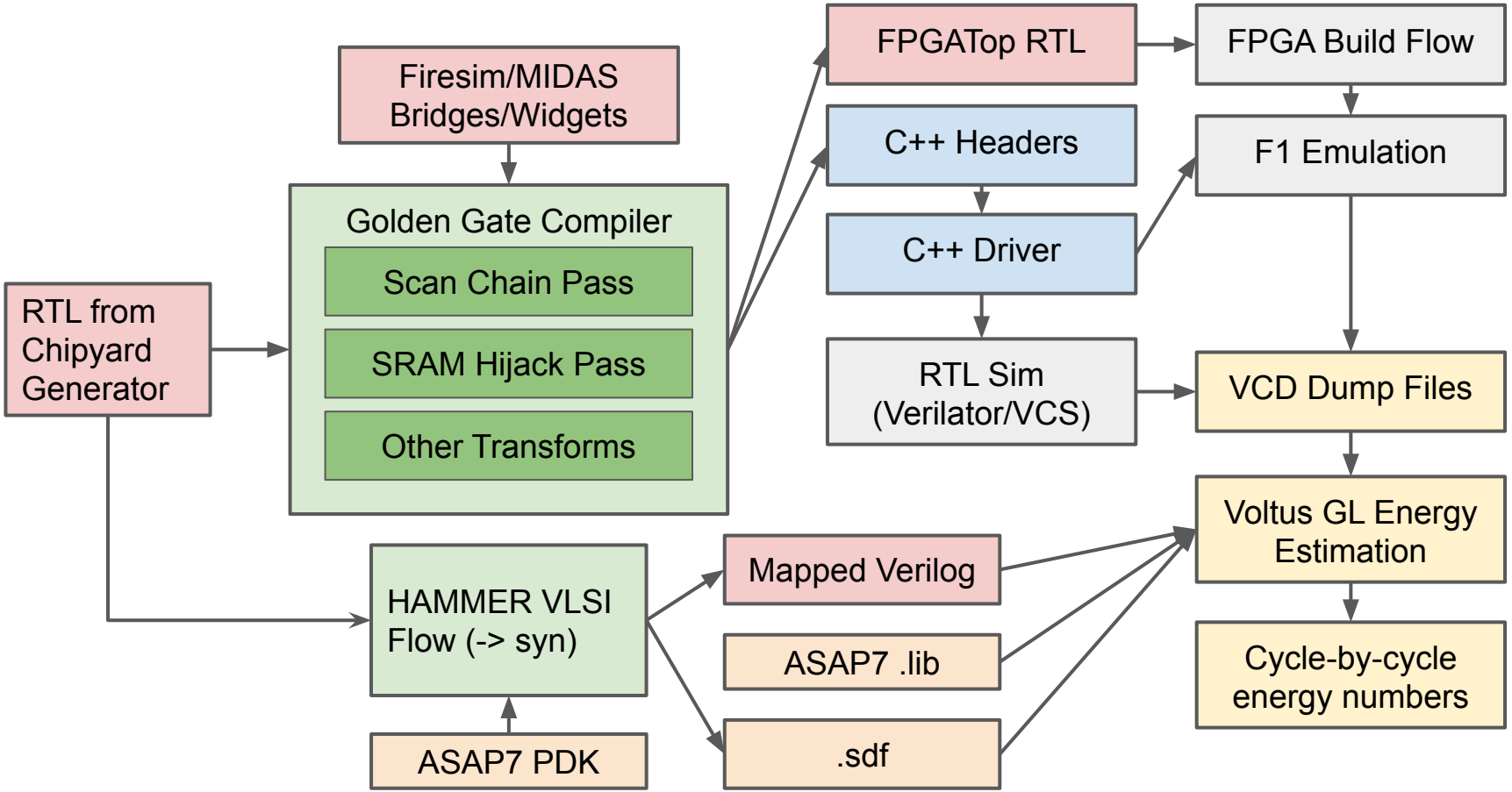
Energy Estimation Flow



Checkpoint 1 (4/10) Goals and Progress

- RTL simulation of a simple circuit (Risc/GCD) after default Firesim transformation
  - Worked through some build issues, and this seems to work fine. The MIDAS-level RTL simulation works with Verilator for the Risc and GCD midasexamples.
- ASAP7 Genus synthesis of the circuit and SRAM macros
  - Worked through EE241B Lab 1 which uses HAMMER to synthesize a GCD circuit (w/out SRAMs). Working through Lab 4 which uses HAMMER in the Chipyard environment. Going to add energy estimation support via Voltus via HAMMER for next checkpoint.
- Formal mapping of RTL VCD to gate-level VCD
  - This doesn't seem to be necessary as we looked through a Cadence RAK (for Voltus) that can estimate energy for GL netlists with RTL VCDs and automatically map them
- Scan-chain stitching and SRAM hijack FIRRTL pass working in RTL simulation
  - Still working on understanding the Golden Gate compiler and what each pass does. Recently multiclock support has made the compiler more complex. Probably going to use shadow scan chain technique instead of stitched for less complexity

Changes to Timeline

- Checkpoint 2 (4/24): Sample circuit simulating on F1 FPGA, uArch state dumping, initial energy estimation evaluation
  - Still need to get the Golden Gate scan chain instrumentation pass working
  - Not planning to go to FPGA just yet, we're going to focus on getting VCD dumping working in RTL sim possibly with Rocket before trying the FPGA build flow
  - We want to run a Rocket MIDAS-level RTL sim with VCD state dumping and state sampling and run the VCD snapshots through Voltus with a synthesized Rocket design
- Final Report (5/8): Rocket with Gemmini simulating on F1 FPGA, DRAM interface and Gemmini-specific performance instrumentation, Gemmini energy estimation for pre-written ResNet50 and Mobilenet implementations, DRAMSim2 energy estimation
  - Not enough experience to know if all of this is possible. We hope at least to get Rocket with Gemmini in MIDAS-level RTL sim with state dumping and Voltus energy estimation when running a simple matmul ubenchmark and maybe a small DNN