HW6 Reference SOL

(a) The mixer input is not 50Ω. What will be the problem if this mixer is used as a connector module like the ones sold by MiniCircuits ?
https://www.minicircuits.com/WebStore/Mixers.html

Usually people assume the input and output impedance of adjacent stages are $50(\Omega)$ and they would design their circuits based on this assumption. If it's not $50(\Omega)$, the mixer could not extract maximum available power from previous stage.

(b) Plot the stability factor (k) of this device versus frequency. Is the device unconditionally stable at 1 GHz? If not, find a (passive) device load impedance such that the real part of the device input impedance is negative at 1 GHz.

(c) Following (b), find the (passive) source impedance at 1 GHz that moves the system pole to the imaginary axis.

As we can see from Figure. 1, at $1(GHz)$, the device is not unconditionally stable because its K is 0.001, much smaller than 1. The impedance I found is $100 + 50j(\Omega)$. With this load, the input impedance is shown in Figure. 2.

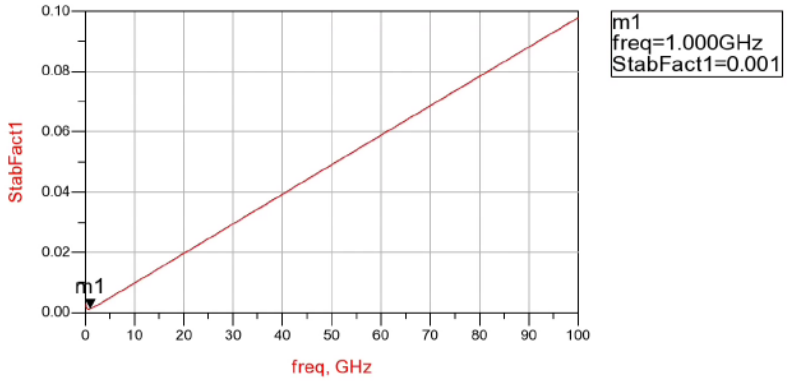


Figure 1: Stability factor.

freq	Zin1
1.000 GHz	-342.145 - j4.750E3

Figure 2: Input impedance has negative real part.

To move the system pole to the imaginary axis, we need to fulfill:

$$(Y_S + y_{11})(Y_L + y_{22}) - y_{12}y_{21} = 0$$

Equivalently,

$$Y_S + Y_{in} = 0$$

From simulation, we can get the value of Y_{in} directly, which is shown in Figure. 3. Thus, $Y_S = -Y_{in}$ and therefore $Z_S = \frac{1}{Y_S} = -\frac{1}{Y_{in}} = 342.36 + 4750.9j(\Omega)$

freq	Yin1
1.000 GHz	-1.509E-5 + j2.094E-4

Figure 3: Value of Y_{in}.

(d) Add a series resistor at the transistor gate to make the device unconditionally stable at 5 GHz with $k = 1.2$. What are the resistor value and the maximum transducer gain of this new device (FET + resistor) at 5 GHz? Plot k versus frequency.

After sweeping the gate resistance, the resistance of $434(\Omega)$ can lead to $k = 1.2$ at $5(GHz)$. The maximum gain is $22.616dB$ and the results are shown in Figure. 4.

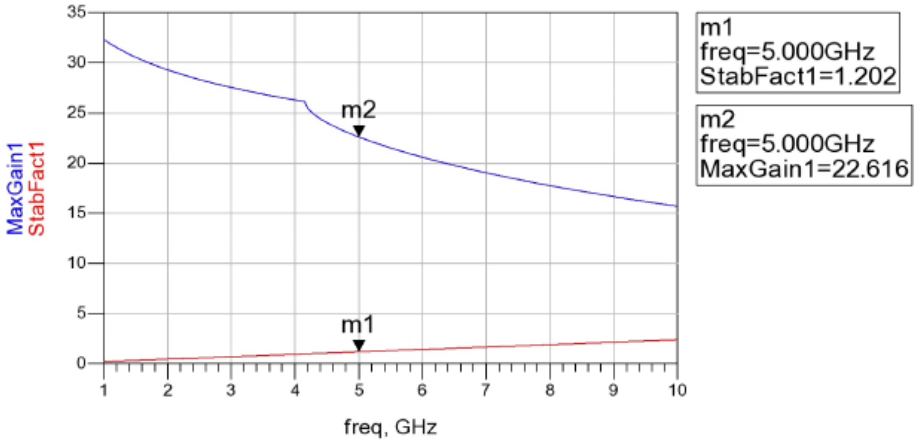
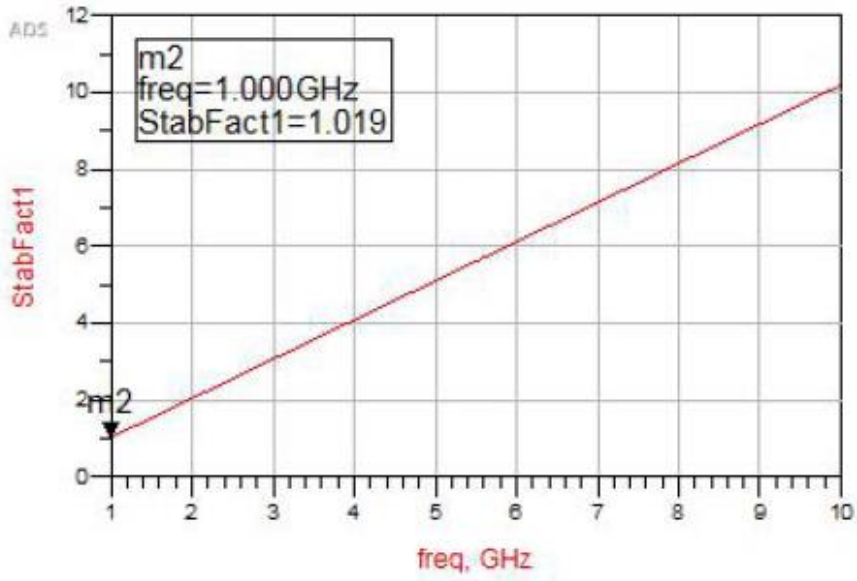


Figure 4: k and maximum gain.

(e) The new device still has $k < 1$ at 1 GHz, which is undesirable because the load and source impedances of a 5-GHz design are usually not controlled at 1 GHz. Therefore, a pair of undesired source and load impedances at 1 GHz can make the system unstable and the 5-GHz amplifier is no longer usable. Further increasing the series resistor can make $k > 1$ at 1 GHz. What is the main drawback of this approach?

(e)

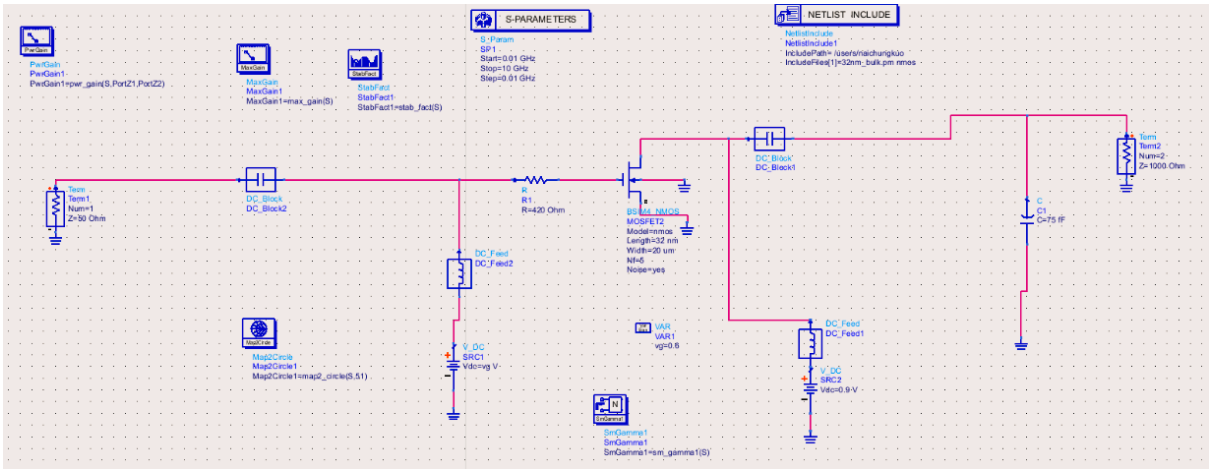
Increase the series resistor to 1.8k,

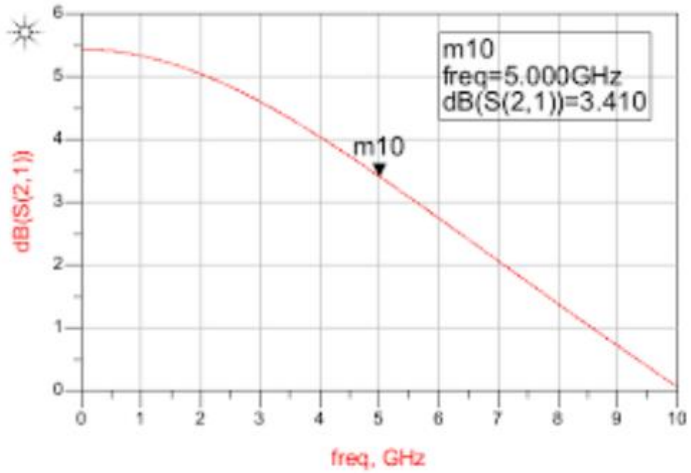


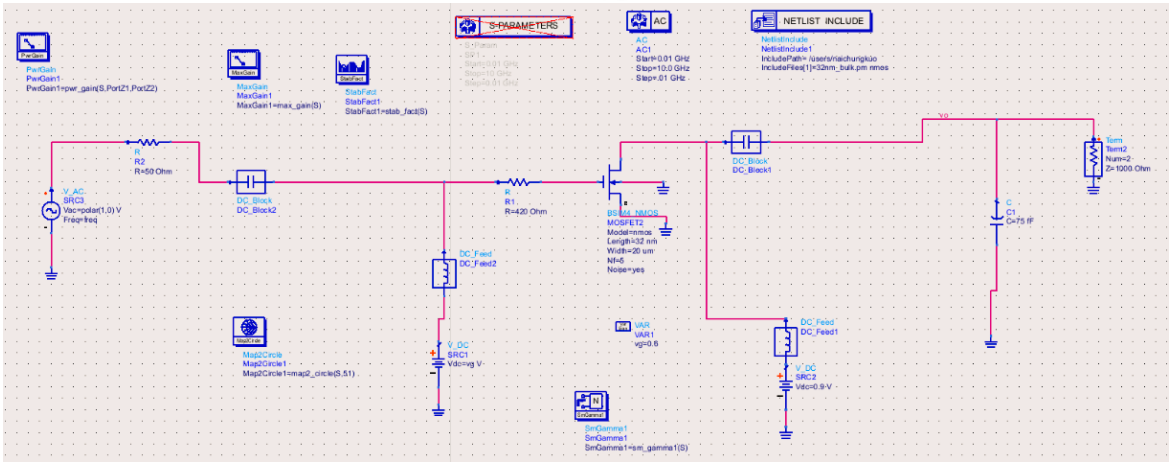
.

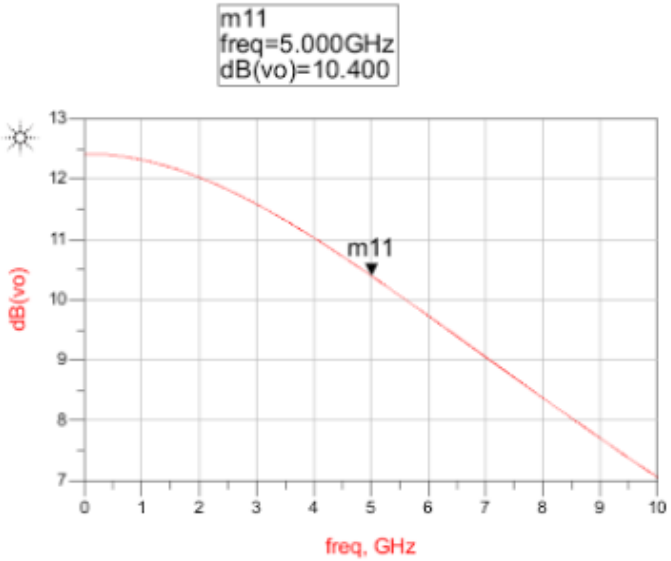
The main drawback of this method is that it will reduce the maximum transducer gain.

(f) We will eventually make $k > 1$ at all frequencies with a better method. Lets focus on the 5-GHz design for now. Assume the source resistor is 50Ω, what is the voltage gain ($V_{in,mixer}/V_s$) and power gain ($P_{in,mixer}/P_{avs}$) without any matching network.




m10
freq=5.000GHz
dB(S(2,1))=3.410
m10
dB(S(2,1))
freq, GHz


S-PARAMETERS
AC
NETLIST_INCLUDE
V_AC
SRC3
R
R2
R=50 Ohm
DC_Block
DC_Block2
R
R1
R=420 Ohm
DC_Feed
DC_Feed2
V_DC
SRC1
MOSFET
DC_Block
DC_Block1
DC_Feed
DC_Feed1
V_DC
SRC2
Vdc=0.9 V
VAR
VAR1
vg=0.6
C
C1
C=75 fF
Term
Term2
Num=2
Z=100 Ohm
Vo
Map2Circle
Map2Circle1
SmGamma
SmGamma1


m11
freq=5.000GHz
dB(vo)=10.400
m11
dB(vo)
freq, GHz

(g) Lecture 9 introduces bi-conjugate matching and the formula to calculate the optimal source and load impedances of a device for the maximum power gain. What are the optimal source and load impedances of your device (FET+gate resistor) at 5 GHz? Verify your calculation by the ADS function *SmGamma*.

```
%Data from ADS
y11 = 1.884e-4 + 1i*6.403e-4;
y12 = -4.031e-5 + 1i*-1.37e-4;
y21 = 0.046 + 1i*-0.014;
y22 = 0.012 + 1i*0.003;

syms Ys
YL = conj(y22 - y12*y21/(Ys + y11));
eqn = y11 - y12*y21/(YL + y22) == conj(Ys);
ys = double(solve(eqn, Ys));
ys = ys(2); %pick positive resistance
yl = conj(y22 - y12*y21/(ys + y11));
zs = 1./ys
zl = 1./yl
```

```
zs =

  2.3903e+02 + 1.0845e+03i

zl =

  25.4728 +37.6104i
```

From Nguyen

1.g

To get maximum gain, we need

$Y_S^* = Y_{in}$

$Y_L^* = Y_{out}$

The simulation result is shown in Figure. 7. From the Gamma values, we can get source impedance and load impedance values, which are $26.457+j36.465(\Omega)$ and $262.953+j1083(\Omega)$respectively.

(h) Design both the input and output matching networks (using lossless inductors and capacitors) to maximize the power/voltage gain. What are the maximum voltage gain and the maximum power gain. What is the 3-dB bandwidth?

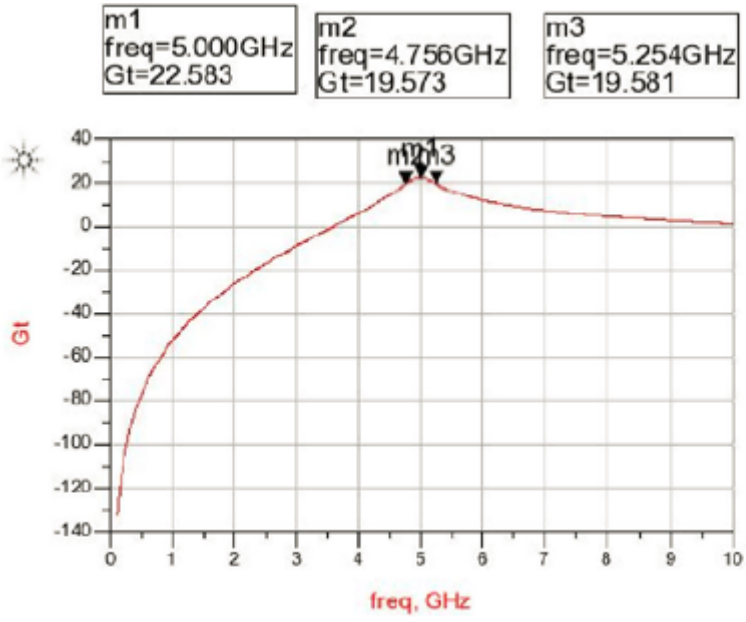
h) Designing matching network for load at 5 GHz:

Z_L consists of 1000 Ω and –j 424.413 Ω in parallel. There will be a parallel component with the load, followed by a series component. Now, $Q_L = \sqrt{\frac{1000}{24.548} - 1} = 6.304$, so $X_{p,L} = \frac{R_L}{Q_L} = 158.629\Omega$, and $X_{s,L} = -\frac{X_{p,L}}{1+Q_L^{-2}} = -154.735\Omega$. Thus $X'_{p,L} = X_{p,L}||(424.413) = 115.471\Omega$, which is a **3.68 nH inductor in parallel**. Also $X'_{s,L} = X_{s,L} + (37.742) = -116.993\Omega$, which is a **0.27 pF capacitor in series**.

Designing matching network for source at 5 GHz:

$Z_s = 50\Omega$. There will be a series component with the load, followed by a parallel component. Now, $Q_s = \sqrt{\frac{5211.047}{50} - 1} = 10.160$, so $X_{s,s} = R_s Q_s = -508\Omega$, which is a **62.66 fF capacitor in series**; and $X_{p,s} = -X_{s,s}(1 + Q_s^{-2}) = 512.921\Omega$. Thus $X'_{p,s} = X_{p,s}||(1133.915) = 353.167\Omega$, which is a **11.242 nH inductor in parallel**.

Using this matching network, at 5 GHz, the voltage gain is $60.174\angle{-54.761^o}$. $P_{in,mixer} = 453.164mW$, so power gain $\frac{P_{in,mixer}}{P_{avs}} = 22.583dB$, which is the maximum transducer gain of this device (FET+resistor). The 3dB bandwidth of the transducer gain is ~0.5 GHz, as seen below:



from
AYAN BISWAS

Notice: The power gain you achieve here after matching should be the same to the maximum gain you obtain in (d), and it is simply dB(S21) of the new circuit

(i) (*242A only*) If you are allowed to use two-section matching networks, what the maximum bandwidth that can be achieved?

i) Designing 2 section matching network for load at 5 GHz:

$Q_L = \sqrt{\sqrt{\frac{1000}{24.548}} - 1} = 2.32$, so $X_{p1,L} = \frac{R_L}{Q_L} = 431.034\Omega$, and $X_{s1,L} = -\frac{X_{p1,L}}{1+Q_L^{-2}} = -363.499\Omega$.

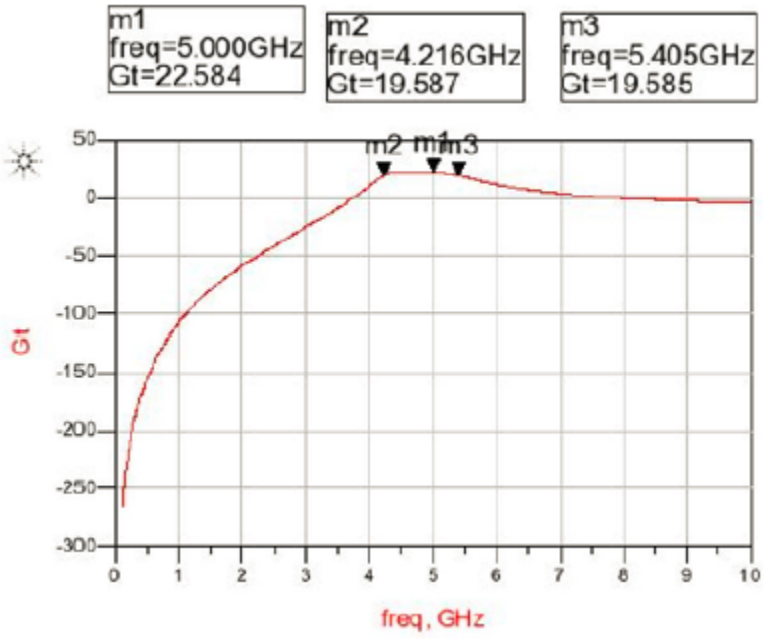
Now, $R_{i,L} = \sqrt{1000 \times 24.548}\Omega = 156.678\Omega$, so $X_{p2,L} = \frac{R_{i,L}}{Q_L} = 67.534\Omega$, and $X_{s2,L} = -\frac{X_{p2,L}}{1+Q_L^{-2}} = -56.953\Omega$. Thus $X'_{p1,L} = X_{p1,L}||(424.413) = 213.849\Omega$, which is a **6.81 nH inductor in parallel**.

$X_{s1,L} = -363.499\Omega$ implies a **87.57 fF capacitor in series**. $X_{p2,L} = 67.534\Omega$ implies a **2.15 nH in parallel**. Also $X'_{s2,L} = X_{s2,L} + (37.742) = -19.211\Omega$, which is a **1.66 pF capacitor in series**.

Designing 2 section matching network for source at 5 GHz:

$Q_s = \sqrt{\sqrt{\frac{5211.047}{50}} - 1} = 3.03$, so $X_{s1,s} = R_s Q_s = -151.5\Omega$, which is a **0.21 pF capacitor in series**; $X_{p1,s} = -X_{s1,s}(1 + Q_s^{-2}) = 168.002\Omega$, which is a **5.35 nH inductor in parallel**; $R_{i,s} = \sqrt{50 \times 5211.047}\Omega = 510.443\Omega$; so $X_{s2,s} = R_{i,s}Q_s = -1546.642\Omega$, which is a **20.58 fF capacitor in series**; $X_{p2,s} = -X_{s2,s}(1 + Q_s^{-2}) = 1715.105\Omega$. Thus $X'_{p,s} = X_{p2,s}||(1133.915) = 682.615\Omega$, which is a **21.728 nH inductor in parallel**.

As expected, the power gain at 5 GHz is 22.584 dB. The power gain increases slightly to reach a maximum around ~4.5 GHz, probably due to precision error while calculating the lumped component values. The 3 dB bandwidth is ~1.18 GHz, as shown below:

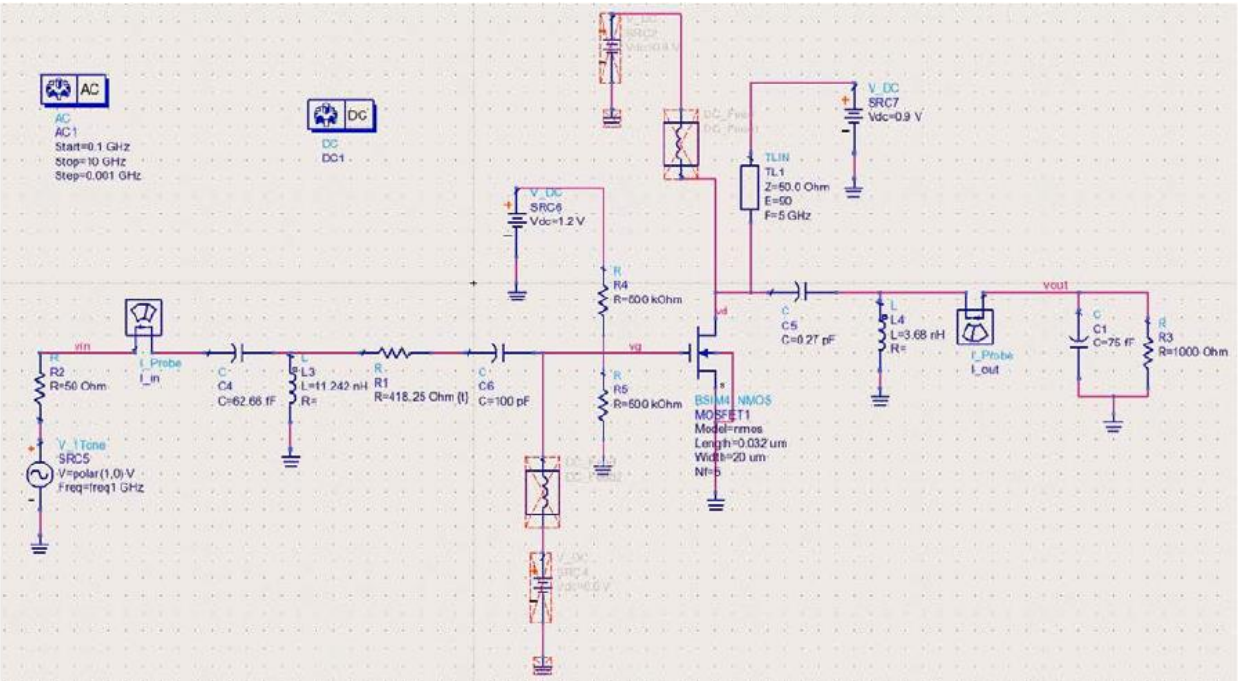


From Ayan

(j) Following (h), simulate the stability factor for the circuit composed the FET, gate resistor and the two matching networks. Compare the result to that obtained in (d).

The same !!!

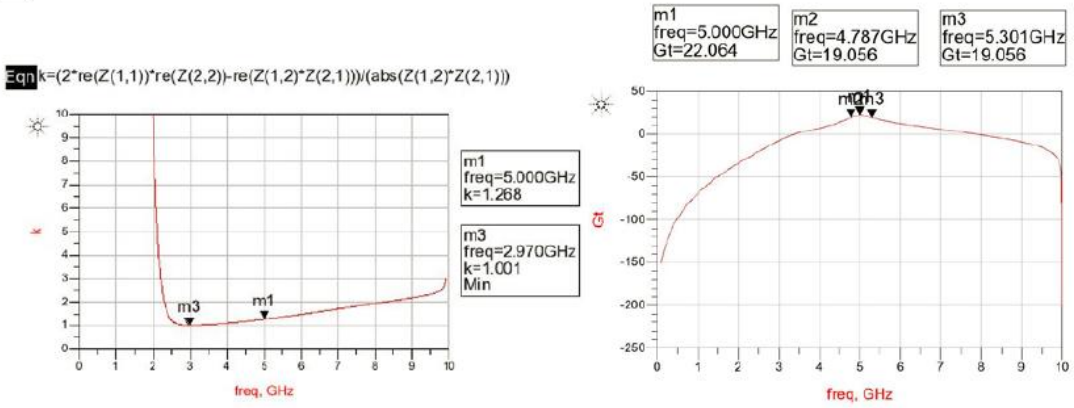
(k) If you have not already done so, provide a reasonable bias network to your circuit without using any ideal dc block and dc feed in the schematic.



From Ayan

(l) Stabilize the circuit such that $k > 1$ at all frequencies. If $k < 1$ at a lower frequency (e.g. 100 MHz), bypass circuit can be used to introduce loss and increase k at that frequency. (For example, the ac ground in your matching networks can be replaced by a 30 pF capacitor in parallel with a 10Ω resistor.) Try to achieve $k > 1$ at all frequencies with the power gain at 5 GHz degrading less than 2 dB from the maximum gain.

l) To stabilize the circuit at all frequencies, the AC ground in the matching network is replaced by a parallel combination of 11.76 pF capacitor and 10 Ω resistor. The gain at 5 GHz reduces to **22.064 dB**, and the minimum $k = 1.001$ is at 2.97 GHz.



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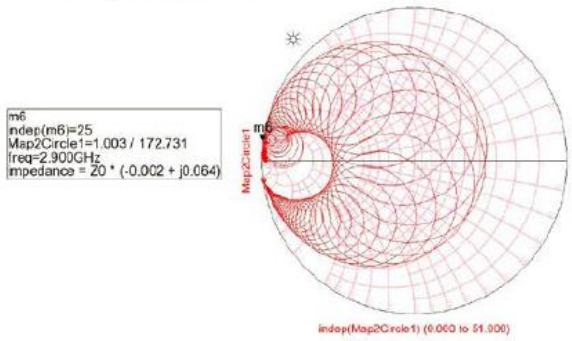
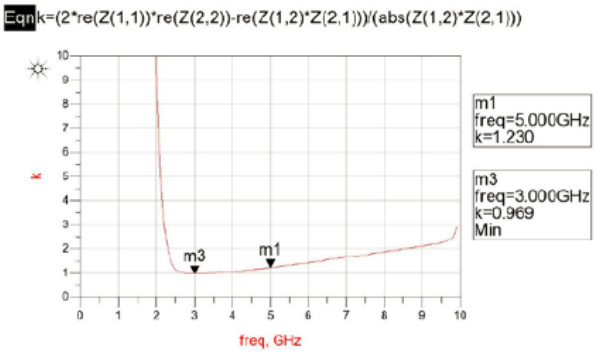
m) Now the design constraint is "*the amplifier output conductance is larger than -0.0005 S under an arbitrary source impedance*". When the gate resistor is decreased to **405 Ω**, the worst case output impedance seen by the load is depicted below:



Here, $Re(Y_{out}) = -4.88 \times 10^{-4} S$. The stability factor vs frequency for the modified circuit is shown below:



As can be seen, minimum value of k is less than 1. The power gain increases to **22.30 dB** at 5 GHz.

From Ayan