EE142 Problem Set 6

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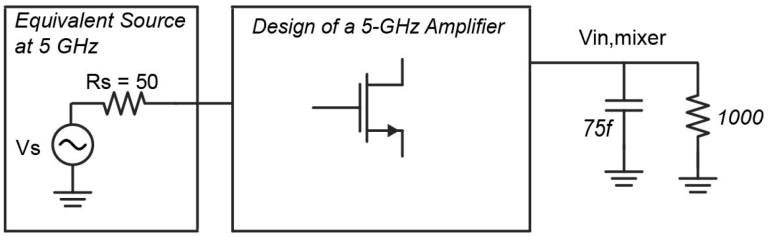
October 15, 2017

1 Design of a 5-Ghz Linear Microwave Amplifier

Use the 32nm PTM HP NMOS model with:

V_D	0.9 V
V_G	0.6 V
L	32 nm
W_{tot}	20 μm
$N_{fingers}$	5



1.a Mixer Input Impedance

The mixer input is not 50Ω. What will be the problem if this mixer is used as a connector module like the ones sold by MiniCircuits?

The connector modules assume operation in a 50Ω environment. Since the mixer input is 1000Ω, any modules driving it will not be able to achieve the maximum possible power transfer to the mixer. Also, the reflections produced will distort the input waveform to the mixer.

1.b Stability Factor

Plot the stability factor (k), of this device versus frequency. Is the device unconditionally stable at 1 Ghz? If not, find a (passive) device load impedance such that the real part of the device input impedance is negative at 1 Ghz.

The stability factor (k) provides a necessary condition for unconditional stability of a 2-port network. It enforces that the input admittance/impedance of the two-port doesn't have a negative real part.

$$Y_{in} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}$$
$$Y_{out} = y_{22} - \frac{y_{12}y_{21}}{y_{11} + Y_S}$$
$$\text{For instability: } \Re(Y_{in}) < 0 \text{ and } \Re(Y_{out}) < 0$$

We set up a S-parameter simulation in ADS to calculate the stability factor versus frequency, using the provided transistor sizing and biasing.

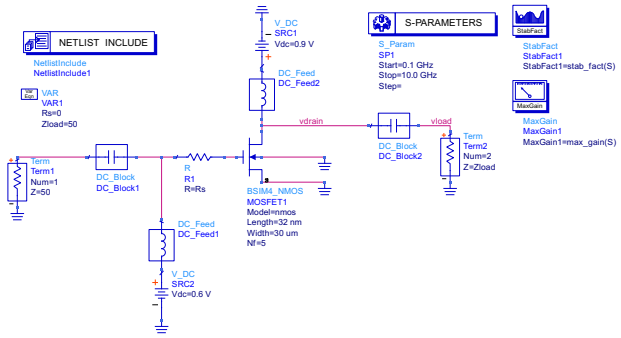


Figure 1: Stability Factor Testbench

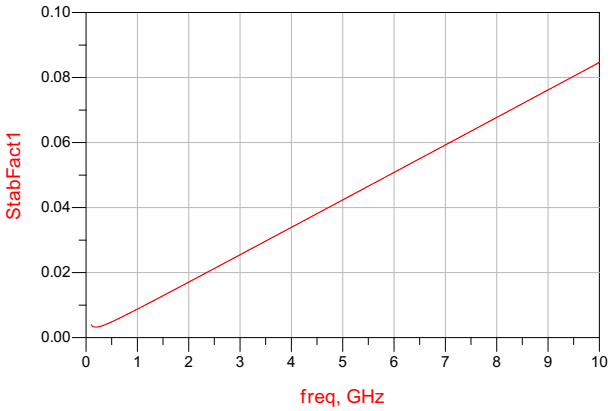


Figure 2: Stability Factor vs. Frequency

The transistor is not unconditionally stable at 1 Ghz. To find a passive load impedance that gives a negative real impedance, we can use the stability analysis (circle) feature of ADS.

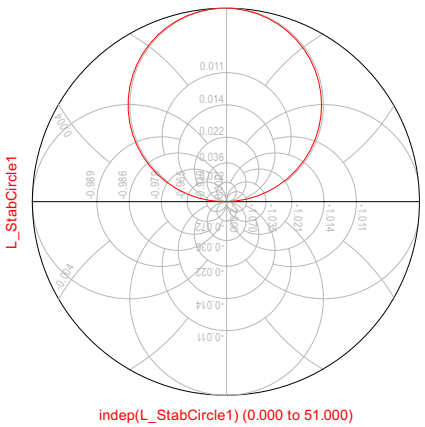


Figure 3: Load Stability Circle (not scaled to unit impedance circle)

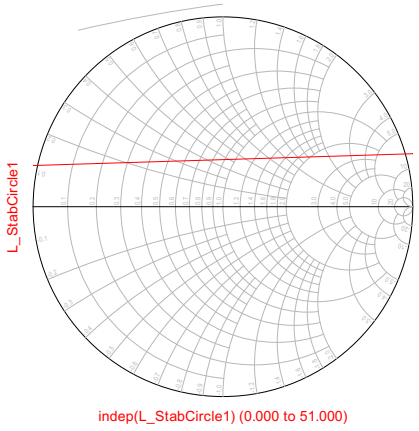


Figure 4: Load Stability Circle (in unit impedance circle)

It can be seen that for sufficiently inductive loads, the transistor isn't stable. For instance a load of $Z_L = 50 + 1.2j$ will lead to a negative input impedance.

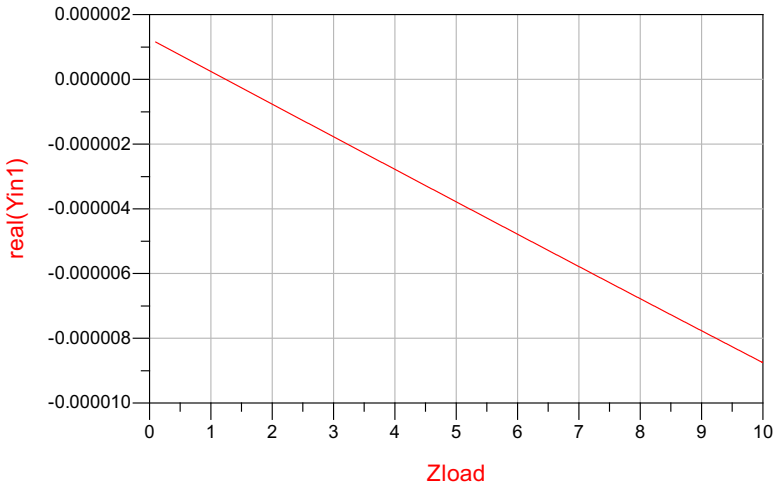


Figure 5: $Z_L = 50 + jZ_{load}$

1.c Move Pole to Im Axis

Following (b), find the passive source impedance at 1 Ghz that moves the system pole to the imaginary axis.

If the system pole is moved to the imaginary axis, it indicates that the system is marginally stable. This would correspond to when the system poles for this circuit move from possible instability to certain stability by changing the source impedance. We can plot the source stability circle and take a point right on the circle.

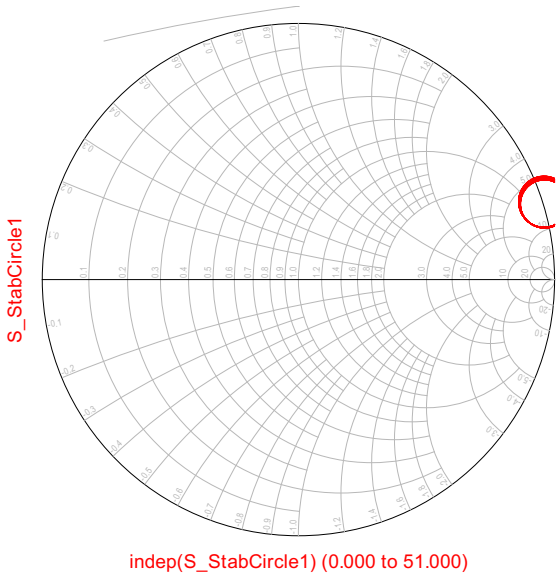


Figure 6: Source Stability Circle

We can immediately read off a value of $Z_s = 1.0 + 5j$ (normalized to 50 Ω).

1.d Stabilize with Series Resistor

Add a series resistor at the transistor gate to make the device unconditionally stable at 5 Ghz with $k = 1.2$. What is the resistor value and the maximum transducer gain of this new device (FET+resistor) at 5 Ghz? Plot k versus frequency

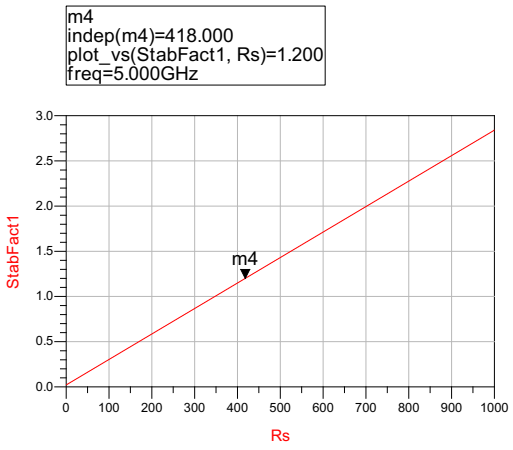


Figure 7: Series resistance sweep vs. K

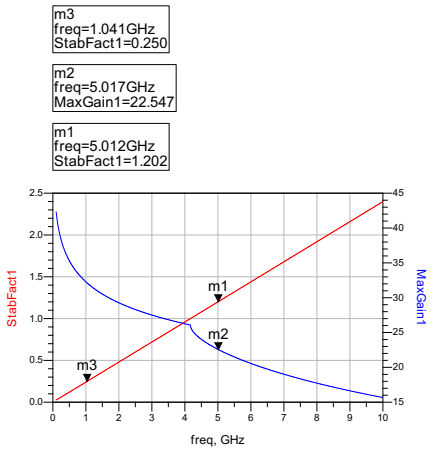


Figure 8: Stability and Gain of Device at 5 Ghz

We see an ideal series resistance of 418Ω and a max gain of 22.5 dB.

1.e Drawbacks of Series Resistance

The new device still has $k < 1$ as 1 Ghz, which is undesireable because the load and source impedances of a 5 Ghz design are usually not controlled at 1 Ghz. Therefore, a pair of undesired source and load impedances at 1 Ghz can make the system unstable and the 5 Ghz amplifier is no longer useable. Further increasing the series resistor can make $k > 1$ at 1 Ghz. What is the main drawback of this approach?

The main drawback is losing maximum transducer gain. As the source resistance increases, the effective transconductance of the entire device (FET + resistor) goes down and the overall power gain of the circuit is reduced.

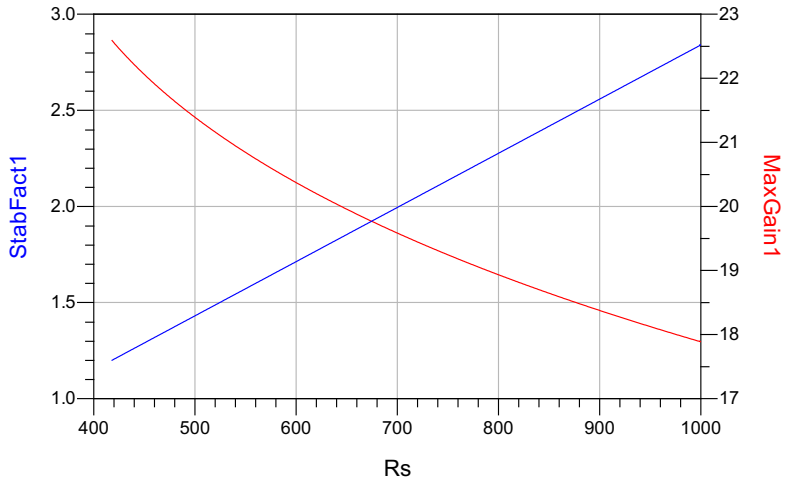


Figure 9: K and Max Gain versus R_s at 5 Ghz

1.f Max Voltage Gain and Power Gain

We will eventually make $k > 1$ at all frequencies with a better method. Let's focus on the 5 Ghz design for now. Assuming the source resistor is 50Ω, what is the voltage gain ($V_{in,mixer}/V_s$) and power gain ($P_{in,mixer}/P_{avs}$) without any matching network?

We use a 50Ω source resistance and the gate resistance from part (d) to stabilize the amplifier at 5 Ghz. The load is replaced with the mixer input impedance model.

To use a standard S-parameter termination instead of (1000 Ω || 75 fF), we use a parallel to series conversion at 5 Ghz with $R_p = 1000\Omega$ and $X_p(\omega) = \frac{-1}{\omega C}$.

$$
\begin{aligned}
X_p(\omega)|_{\omega=5e9\cdot 2\pi} &= -424.413 \\
Q_p(\omega) = \frac{R_p}{X_p} &= \frac{1000}{-1/(\omega(75\text{ fF}))} \\
Q_p(\omega)|_{5e9\cdot 2\pi} &= -2.356 \\
R_s = \frac{R_p}{1+Q_p^2} &= 152.633 \\
X_s = \frac{X_p}{1+\frac{1}{Q_p^2}} &= -359.633
\end{aligned}
$$

We find power gain of -2.711 dB and voltage gain of 4.729 dB. This is the schematic used:

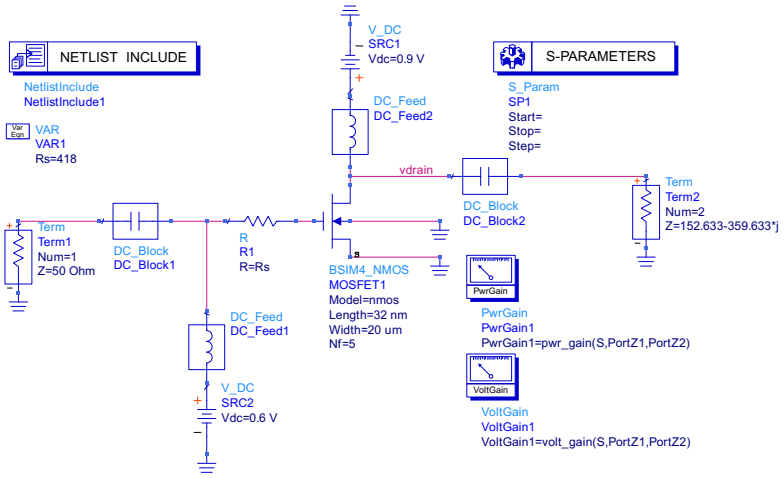


Figure 10: Schematic used to find power and voltage gain

However, when using a 75 fF cap in parallel with a 1000 Ohm termination, I get different power and voltage gain results.

1.g Find Ideal Source/Load Impedance

Lecture 9 introduced bi-conjugate matching and the formula to calculate the optimal source and load impedances of a device for the maximum power gain. What are the optimal source and load impedances of your device (FET + gate resistor) at 5 Ghz? Verify your calculation by the ADS function *SmGamma*.

From lecture, we found:

$$Y_{in} = Y_{11} - \frac{Y_{12}Y_{21}}{Y_L + Y_{22}} = Y_S^*$$
$$Y_{out} = Y_{22} - \frac{Y_{12}Y_{21}}{Y_S + Y_{11}} = Y_L^*$$
$$Y_S = \frac{1}{50} = 0.02$$
$$Y_L = \frac{1}{152.633 - 359.633j} = 0.001 + 0.0023561939267246505j$$

We find the Y parameters of the 2-port from ADS. Then we calculate the optimal $Y_{in,opt}$ and $Y_{out,opt}$, and the hand-calculated SmGamma values.

Here is the technique:

$$Y_{in,opt} = conj(Y_{11} - ((Y_{12}Y_{21})/(Y_L + Y_{22})))$$
$$Y_{out,opt} = conj(Y_{22} - ((Y_{12}Y_{21})/(Y_S + Y_{11})))$$
$$Z_{in,opt} = \frac{1}{Y_{in,opt}}$$
$$SmGamma1 = (Z_{in,opt} - 50)/(Z_{in,opt} + 50)$$
$$SmGamma2 = (Z_{out,opt} - 1000)/(Z_{out,opt} + 1000.0)$$

Here are the values:

$$Z_{in,opt} = (571.205191257 + 791.739522743j)$$
$$Z_{out,opt} = (66.3703128933 + 32.7697815535j)$$
$$SmGamma1 = (0.938661386357 + 0.0781773967356j)$$
$$SmGamma2 = (-0.873751609891 + 0.0575807767707j)$$

We find SmGamma from ADS:

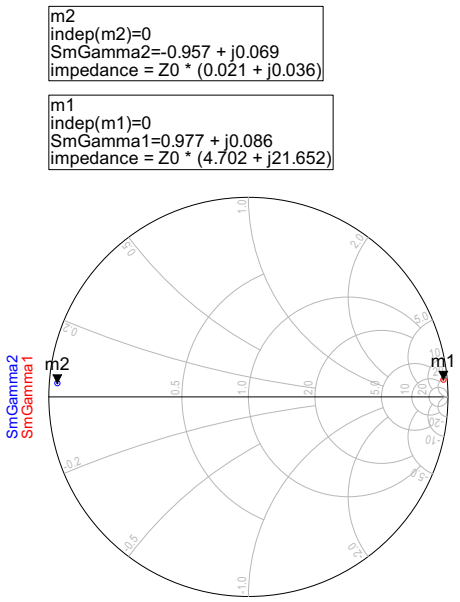


Figure 11: SmGamma of FET+resistor with 1000 Ohm termination and 75 fF in shunt

We can see that the SmGamma values hand-calculated match up well enough with the values found by ADS.

We can also use the equations given later in the lecture to find the optimal power match impedances:

$$Y_{s,opt} = -1j\Im Y_{11}\frac{Y_{12}Y_{21} - 2\Re Y_{11}\Re Y_{22} + |Y_{12}Y_{21}|(K + \sqrt{K^2 - 1})}{2\Re Y_{22}}$$

We get $Z_{in} = (4.709253134778841 + 21.648285783477746j)$ and $Z_{out} = (0.02063245553111879 + 0.035740205135909385j)$ which closely matches the ADS impedance values.

1.h Matching Networks

Design both the input and output matching networks (using L/C) to maximize the power/voltage gain. What are the maximum voltage gain and the maximum power gain? What is the 3-dB bandwidth?

We find the impedances for optimal matching from ADS, so we can now compute regular L networks as in the previous homework assuming we can resonante out the complex part of each load.

1.h.1 Input Match

We want to match from $Z_S = 50\Omega$ to $Z_L = 235.463 - 1082.4143j\Omega$.

We begin by resonating out the the load reactance with a 34.36 nH inductor in series, then design a regular L matching network with $C_p = 0.26$ pF, and $L_s = 3.06$ nH.

1.h.2 Output Match

We want to match from $Z_S = 20.632 + 35.740$ to $Z_L = 1000\Omega||75$ fF.

We begin by resonating out the load reactance with a 13.51 nH inductor in shunt, then follow up with a $L_p = 4.66$ nH, and $C_s = 0.222$ pF. We make the source impedance purely real with a series 1.145 nH inductor.

We can see after adding the matching networks, that SmGammas move to the origin of the circle, and the power/voltage gains are improved and positive.

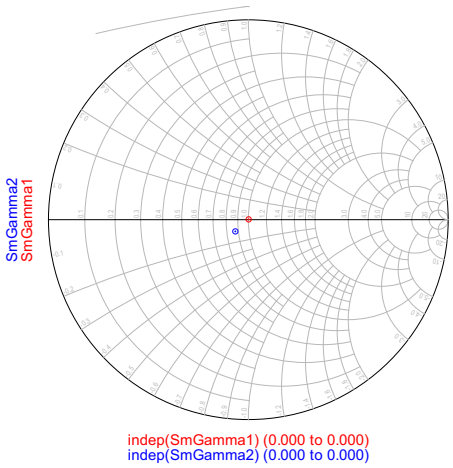


Figure 12: SmGamma 1 and 2

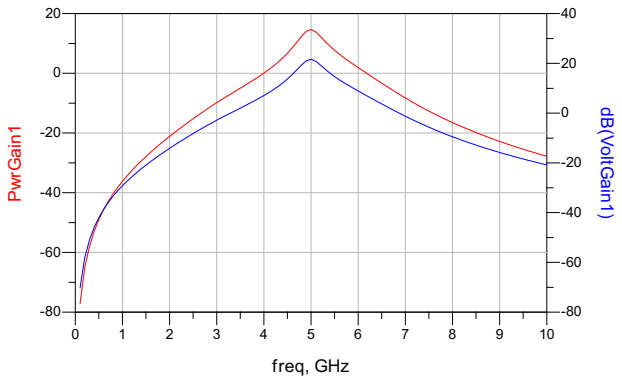


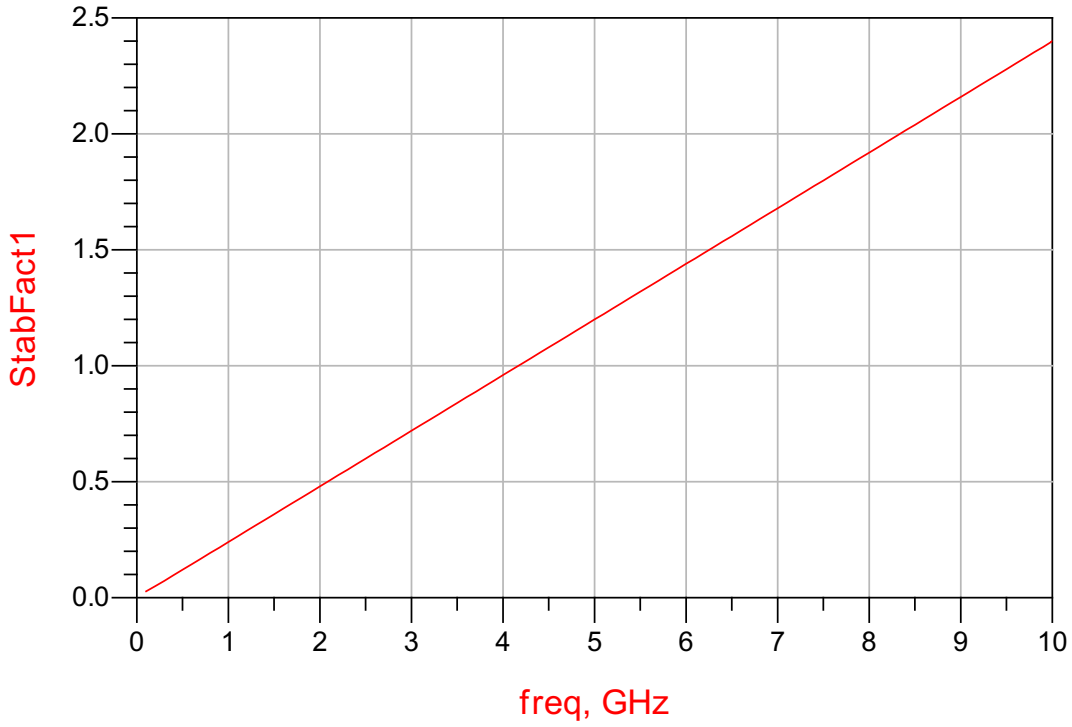
Figure 13: Power and Voltage Gain vs Frequency

The -3dB bandwidth is roughly 500 Mhz and the max power gain is 14 dB and the max voltage gain is 20 dB.

1.i 242A only

1.j Stability Analysis After Matching

Following (h), simulate the stability factor for the circuit composed of the FET, gate resistor and the two matching networks. Compare the result to that obtained in (d).:

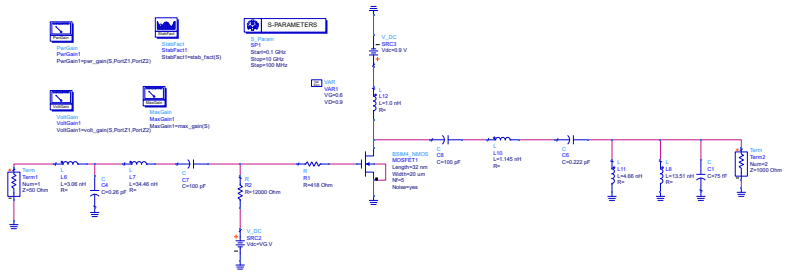


As expected, the stability factor doesn't change from part (d) since K only depends on the two-port transistor model and any **lossy** elements placed around it.

1.k Bias Network

If you have not already dont so, provide a reasonable bias network to your circuit without using any ideal dc block and dc feeds in the schematic.

We replace DC feeds with resistors or inductors and replace DC blocks with 100 pF capacitors. Here is the new schematic:



1.1 Full Stability

Stabilize the circuit at all frequencies. Introduce loss if needed, but keep the power gain at 5 Ghz from degrading more than 2dB from the max gain.

Calculating the stability factor, I find that it is already above 1 for all frequencies due to the resistor at the amplifier input to sustain the gate bias voltage. By boosting the inductor from the V_D supply from 1 nH to 100 nH, I was able to regain the lost gain at 5 Ghz and achieve stability for all frequencies.