Integrated Circuits for Communication
Berkeley

Two-Port Noise Analysis

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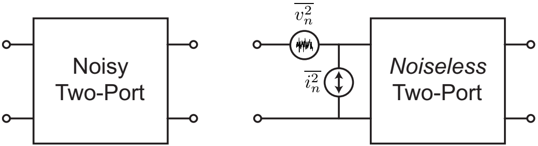
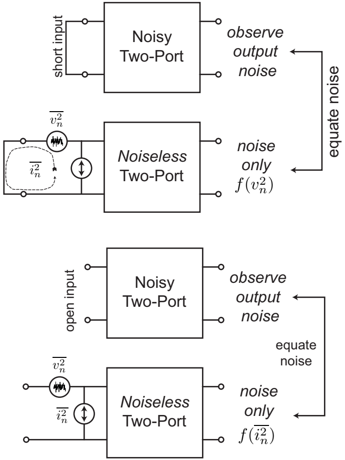
Equivalent Noise Generators



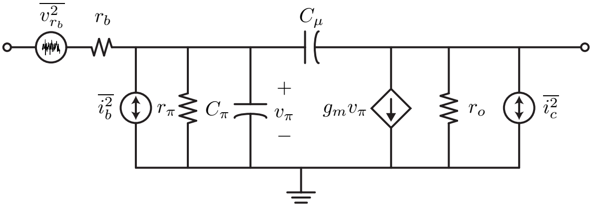
- Any noisy two port can be replaced with a *noiseless* two-port and equivalent input noise sources
- In general, these noise sources are correlated. For now let's neglect the correlation.

Equivalent Noise Generators (cont)

- The equivalent sources are found by opening and shorting the input.



Example: BJT Noise Sources



- If we leave the base of a BJT open, then the total output noise is given by

$$\overline{i_o^2} = \overline{i_c^2} + \beta^2 \overline{i_b^2} = \overline{i_n^2}\beta^2$$

or

$$\overline{i_n^2} = \frac{\overline{i_c^2}}{\beta^2} + \overline{i_b^2} \approx \overline{i_b^2}$$

- If we short the input of the BJT, we have

$$\overline{i_o^2} \approx g_m^2 \overline{v_n^2} \left(\frac{Z_\pi}{Z_\pi + r_b} \right)^2 = \beta^2 \frac{\overline{v_n^2}}{(Z_\pi + r_b)^2}$$

$$= \beta^2 \frac{\overline{v_{r_b}^2}}{(Z_\pi + r_b)^2} + \overline{i_c^2}$$

- Solving for the equivalent BJT noise voltage

$$\overline{v_n^2} = \overline{v_{r_b}^2} + \frac{\overline{i_c^2}(Z_\pi + r_b)^2}{\beta^2}$$

$$\overline{v_n^2} \approx \overline{v_{r_b}^2} + \frac{\overline{i_c^2} Z_\pi^2}{\beta^2}$$

BJT Generators at Low Freq

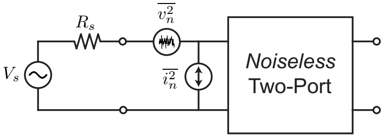
at low frequencies...

$$\overline{v_n^2} \approx \overline{v_{r_b}^2} + \frac{\overline{i_c^2}}{g_m^2}$$

$$\overline{v_n^2} = 4kTBr_b + \frac{2qI_C B}{g_m^2}$$

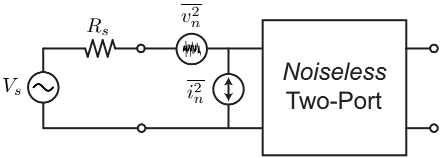
$$\overline{i_n^2} = \frac{2qI_c}{\beta}$$

Role of Source Resistance



- If $R_s = 0$, only the voltage noise $\overline{v_n^2}$ is important. Likewise, if $R_s = \infty$, only the current noise $\overline{i_n^2}$ is important.
- Amplifier Selection: If R_s is large, then select an amp with low $\overline{i_i^2}$ (MOS). If R_s is low, pick an amp with low $\overline{v_n^2}$ (BJT)
- For a given R_s, there is an optimal $\overline{v_n^2}/\overline{i_n^2}$ ratio. Alternatively, for a given amp, there is an optimal R_s

Equivalent Input Noise Voltage

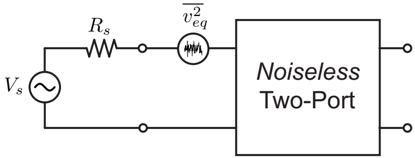


- Let's find the total output noise voltage

$$\overline{v_o^2} = (\overline{v_n^2}A_v^2 + \overline{v_{R_s}^2}A_v^2)\left(\frac{R_{in}}{R_{in}+R_s}\right)^2 + \left(\frac{R_{in}}{R_{in}+R_s}\right)^2 R_s^2\overline{i_n^2}A_v^2$$

$$= (\overline{v_n^2} + \overline{i_n^2}R_s^2 + \overline{v_{R_s}^2})\left(\frac{R_{in}}{R_{in}+R_s}\right)^2 A_v^2$$

Noise Figure



- We see that all the noise can be represented by a single equivalent source
$$\overline{v_{eq}^2} = \overline{v_n^2} + \overline{i_n^2} R_s^2$$
- Applying the definition of noise figure
$$F = 1 + \frac{N_{amp,i}}{N_s} = 1 + \frac{\overline{v_{eq}^2}}{\overline{v_s^2}}$$

Optimal Source Impedance

- Let $\overline{v_n^2} = 4kTR_nB$ and $\overline{i_n^2} = 4kTG_nB$. Then

$$F = 1 + \frac{R_n + G_nR_s^2}{R_s} = 1 + G_nR_s + \frac{R_n}{R_s}$$

- Let's find the optimum R_s

$$\frac{dF}{dR_s} = G_n - \frac{R_n}{R_s^2} = 0$$

- We see that the noise figure is minimized for

$$R_{opt} = \sqrt{\frac{R_n}{G_n}} = \sqrt{\frac{\overline{v_n^2}}{\overline{i_n^2}}}$$

Optimal Source Impedance (cont)

- The major assumption we made was that $\overline{v_n^2}$ and $\overline{i_n^2}$ are not correlated. The resulting minimum noise figure is thus

$$F_{min} = 1 + G_n R_s + \frac{R_n}{R_s}$$

$$= 1 + G_n \sqrt{\frac{R_n}{G_n}} + \sqrt{\frac{G_n}{R_n}} R_n$$

$$= 1 + 2\sqrt{R_n G_n}$$

- Consider the difference between F and F_{min}

$$F - F_{min} = G_n R_s + \frac{R_n}{R_s} - 2\sqrt{R_n G_n}$$

$$= \frac{R_n}{R_s}(1 + \frac{G_n R_s^2}{R_n} - 2\frac{R_s}{R_n}\sqrt{R_n G_n})$$

$$= \frac{R_n}{R_s}\left(1 + \left(\frac{R_s}{R_{opt}}\right)^2 - \frac{2R_s}{R_{opt}}\right)$$

$$= \frac{R_n}{R_s}\left|\frac{R_s}{R_{opt}} - 1\right|^2$$

$$= R_n R_s \left|G_{opt} - G_s\right|^2$$

Noise Sensitivity Parameter

- Sometimes R_n is called the noise sensitivity parameter since

$$F = F_{min} + R_n R_s \left| G_{opt} - G_s \right|^2$$

- This is clear since the rate of deviation from optimal noise figure is determined by R_n. If a two-port has a small value of R_n, then we can be sloppy and sacrifice the noise match for gain. If R_n is large, though, we have to pay careful attention to the noise match.
- Most software packages (Spectre, ADS) will plot Y_{opt} and F_{min} as a function of frequency, allowing the designer to choose the right match for a given bias point.

BJT Noise Figure

- We found the equivalent noise generators for a BJT

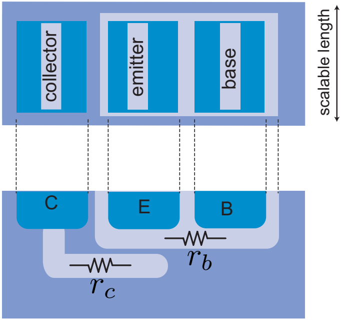
$$\overline{v_n^2} = \overline{v_{r_b}^2} + \frac{\overline{i_c^2}}{g_m^2} = 4kTBr_b + \frac{2qI_C B}{g_m^2} \qquad \overline{i_n^2} = \overline{i_b^2}$$

- The noise figure is

$$F = 1 + \frac{4kTr_b + \frac{2qI_C}{g_m^2}}{4kTR_s} + \frac{2qI_C R_s^2}{\beta 4kTR_s} = 1 + \frac{r_b}{R_s} + \frac{1}{2g_m R_s} + \frac{g_m R_s}{2\beta}$$

- According to the above expression, we can choose an optimal value of $g_m R_s$ to minimize the noise. But the second term r_b/R_s is fixed for a given transistor dimension

BJT Cross Section



- The device can be scaled to lower the net current density in order to delay the onset of the Kirk Effect
- The base resistance also drops when the device is made larger

BJT Device Sizing

- We can thus see that BJT transistor sizing involves a compromise:
  - The transconductance depends only on I_C and not the size (first order)
  - The charge storage effects and f_T only depend on the base transit time, a fixed vertical dimension.
  - A smaller device has smaller junction area but can only handle a given current density before Kirk effect reduces performance
  - A larger device has smaller base resistance r_b but larger junction capacitance

Correlated Noise Sources

- Let's partition the input noise current into two components, a component correlated ("parallel") to the noise voltage and a component uncorrelated ("perpendicular") of the noise voltage

$$i_n = i_c + i_u$$

- where we assume that $< i_u, v_n >= 0$ and

$$i_c = Y_C v_n$$

- We can therefore write

$$v_{eq} = v_n(1 + Y_C Z_S) + Z_S i_u$$

Noise Figure of Two-Port

- Which is a sum of uncorrelated random variables. The variance is thus the sum of the variances

$$\overline{v_{eq}^2} = \overline{v_n^2}|1 + Y_C Z_S|^2 + |Z_s|^2 \overline{i_u^2}$$

- This allows us to immediately write the noise figure as

$$F = 1 + \frac{\overline{v_n^2}|1 + Y_C Z_S|^2 + |Z_s|^2 \overline{i_u^2}}{\overline{v_s^2}}$$

- Let $\overline{v_n^2} = 4kTBR_n$, $\overline{i_u^2} = 4kTBG_u$, and $\overline{v_s^2} = 4kTBR_s$. Then

$$F = 1 + \frac{R_n|1 + Y_C Z_S|^2 + |Z_s|^2 G_u}{R_s}$$

Optimum Source Impedance

- If we let $Y_c = G_c + jB_c$, $Y_s = Z_s^{-1} = G_s + jB_s$, it's not to difficult to show that the optimum source impedance to minize F is given by

$$B_{opt} = B_s = -B_c$$

$$G_{opt} = G_s = \sqrt{\frac{G_u}{R_n} + G_c^2}$$

- The minimum acheivable noise figure is

$$F_{min} = 1 + 2G_c R_n + 2\sqrt{R_n G_u + G_c^2 R_n^2}$$

- For $G_c = 0$, this reduces to our previously derived expression.

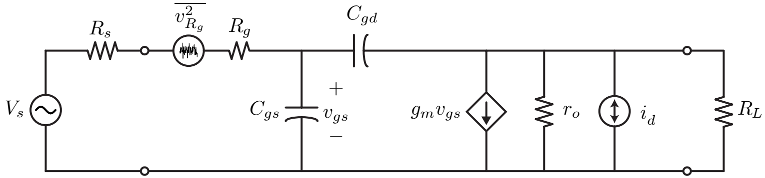
Minimum Noise F_{min}

- Very similar to the uncorrelated case, we have

$$F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2$$

- This equation stats that if the source impedance $Y_s \neq Y_{opt}$, the noise figure will be larger by a factor of the "distance" squared times the factor R_n/G_s.
- A good device should have a low R_n so that the noise match is not too sensitive.

FET Common Source Amplifier



- Consider the following noise sources:

R_s	$\overline{v_s^2} = 4kTBR_s$
R_g	$\overline{v_g^2} = 4kTBR_g$
R_{ch}	$\overline{i_d^2} = 4kTBg_{d0}\gamma B$
R_L	$\overline{i_L^2} = 4kTBG_L$

Total FET Drain Noise

- Summing all the noise at the output (assume low frequency)

$$\overline{i_o^2} = \overline{i_d^2} + \overline{i_L^2} + (\overline{v_g^2} + \overline{v_s^2})g_m^2$$

- Which results in the noise figure

$$F = 1 + \frac{\overline{v_g^2}}{\overline{v_s^2}} + \frac{\overline{i_d^2} + \overline{i_L^2}}{g_m^2 \overline{v_s^2}}$$

$$= 1 + \frac{R_g}{R_s} + \frac{g_{d0}\gamma + G_L}{R_s g_m^2}$$

FET Noise Figure (low freq)

- Assume $g_m = g_{d0}$ (long channel)

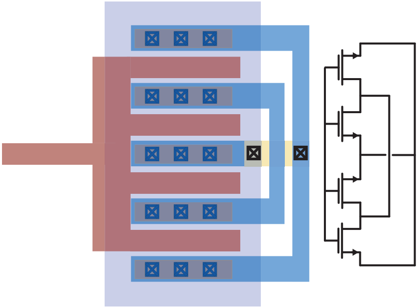
$$= 1 + \frac{R_g}{R_s} + \frac{\gamma}{g_m R_s} + \frac{G_L G_S}{g_m^2}$$

- If we make g_m sufficiently large, the gate resistance will dominate the noise.
- The gate resistance has two components, the physical gate resistance and the induced channel resistance

$$R_G = R_{poly} + \delta R_{ch} = \frac{1}{3}\frac{W}{L}R_{\square} + \frac{1}{5}\frac{1}{g_m}$$

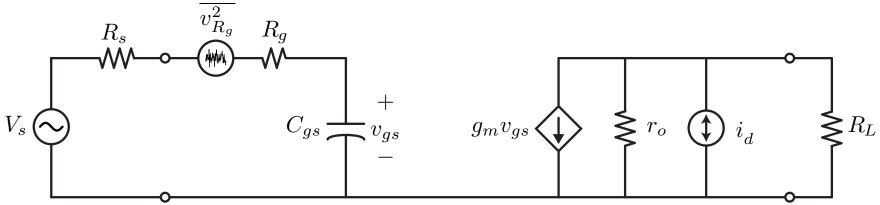
- The factors 1/3 and 1/5 come from a distributed analysis (EECS 117). They are valid for single-sided gate contacts.

FET Layout



- To reduce the gate resistance, a multi-finger layout approach is commonly adopted. As a bonus, the junction capacitance is reduced due to the junction sharing.

CS Noise at Medium Frequencies



- If we repeat the calculation at medium frequencies, ignoring C_{gd}, we simply need to input refer the drain noise taking into account the frequency dependence of G_m

$$G_m = g_m \frac{1/(j\omega C_{gs})}{1/(j\omega C_{gs}) + R_s + R_g}$$

$$= \frac{g_m}{1 + j\omega C_{gs}(R_s + R_g)}$$

CS Noise (cont)

- The drain noise is input referred by the magnitude squared

$$|G_m|^{-2} = g_m^{-2}(1 + \omega^2 C_{gs}^2 (R_s + R_g)^2)$$

- So the noise figure is simply given by (neglect the noise of R_L)

$$F = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\left(1 + \omega^2 C_{gs}^2 (R_S + R_g)^2\right)$$

- Assume that $R_s \gg R_g$ (good layout). The "high" frequency noise is given by

$$F_\infty = 1 + \frac{\gamma}{\alpha}\frac{\omega^2 C_{gs}^2 R_s^2}{g_m R_S} = 1 + \frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right)^2 g_m R_s$$