Integrated Circuits for Communication

Berkeley

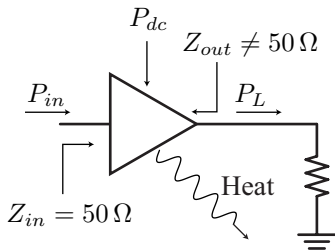## Power Amplifiers

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- Power Amplifiers (PA) deliver power to a given load with maximum efficiency while faithfully transferring the modulation from the input to the output.
- Like small-signal amplifiers, PAs are typically matched at the input. However, the output of the PA is usually unmatched in order to maximize power and efficiency (which results in lower power gain).

Audio PA Example
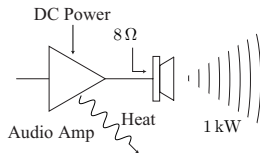
- Consider a PA that delivers $1\,\text{kW}$ of power into 8Ω speakers.
- Assuming a sinusoidal input, the peak voltage and current are

$$V = \sqrt{2RP} = \sqrt{2 \cdot 8 \cdot 1000} = 126\,\text{V}$$

$$I = \frac{2P}{V} = 15.8\,\text{A}$$

- Such large currents and voltages require special techniques and/or technology.

Efficiency

- The *Power Added Efficiency*, or *PAE*, is a measure of how much power is added to a signal normalized by the DC power consumption
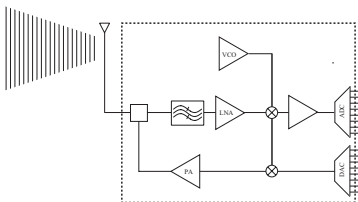
$$PAE = \eta = \frac{P_L - P_{in}}{P_{dc}}$$

- If the power gain is large

$$PAE = \frac{P_L(1 - G_p^{-1})}{P_{dc}} \approx \frac{P_L}{P_{dc}}$$

- The drain or collector efficiency is defined as
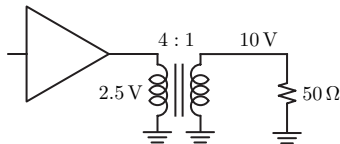
$$\eta_{c|d} = \frac{P_L}{P_{dc}}$$

Mobile Phone Example

- Consider a typical mobile phone that delivers $1\,\mathrm{W}$ in to a 50Ω antenna. Here we find that

$$V_0 = \sqrt{2PR} = \sqrt{2 \cdot 50} = 10\,\mathrm{V}$$

$$I_0 = 2/10 = 0.2\,\mathrm{A}$$

- Most high-frequency Si transistors cannot handle $10\,\mathrm{V}$ due to breakdown. Thus we need to transform the voltage down to a safe value.

- Note that in the process of transforming the voltage down, the current transforms up, $I = 0.8\,\text{A}$. This requires careful layout to minimize "series" parasitic loss. For a $1\,\Omega$ parasitic loss, we throw away nearly $1/3$ of the power to the load

$$P_{L,s} = \tfrac{1}{2}I^2 R = 320\,\text{mW}$$

- If the core amplifier efficiency is say 50%, then this external loss cuts the efficiency to

$$P_{loss} = 320\,\mathrm{mW} + \frac{P_L}{\eta} = 2.32\,\mathrm{W}$$

$$\eta = \frac{1\,\mathrm{W}}{2.32\,\mathrm{W}} = 43\%$$

- If the transformer has $2\,\mathrm{dB}$ of insertion loss, then the efficiency (and output power) drops by a factor 0f .63, or $\eta = 27\%$.

Power Amplifier Considerations

- PAs drive large voltages/currents into small load impedances. Thus matching networks are critical. Any loss in the matching network has a severe impact on the efficiency of the amplifier.
- Heat generation is high. We need to carefully provide heat sinks to keep the junction temperatures as low as possible.
- Due to the interface with the external "off-chip" world, packaging and board parasitics are very important.
- The spectral "leakage" and harmonic generation in a PA must be kept to the a minimum in order to minimize interference to other users.

- The emitter follower is a popular output stage. It does not have any voltage gain but it has power gain. What's the efficiency of such an amplifier?
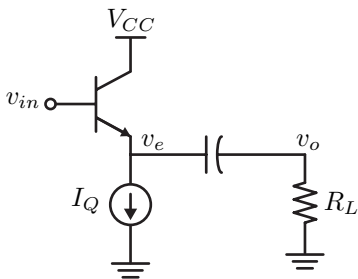
$$P_L = \frac{v_o^2}{2R_L}$$

$$P_{dc} = V_{CC} I_Q$$

$$\eta_c = \frac{P_L}{P_{dc}} = \frac{1}{2} \frac{v_o}{R_L} \frac{v_o}{V_{CC} I_Q}$$

$$\eta_c = \frac{1}{2} \left(\frac{i_o}{I_Q} \right) \left(\frac{v_o}{V_{CC}} \right) = \frac{1}{2} \bar{i} \bar{v}$$

Normalized Current/Voltage Swing

- Apparently in order to maximize the efficiency of the follower stage, we must maximize the normalized current swing $\bar{i}$ and the voltage swing $\bar{v}$.

- Of course the current and voltage swing are related by the load impedance, so if it is fixed, we cannot independently change both.

$$R_L = \frac{v_o}{i_o}$$

- An impedance matching network, therefore, adds one more degree of freedom to the optimization problem, allowing us to maximize $\bar{i}$ and $\bar{v}$ independently.
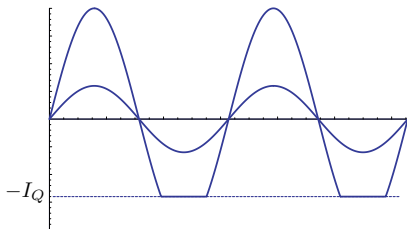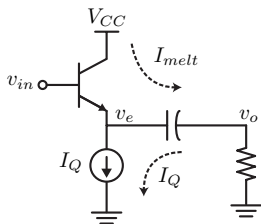
- Consider the output current i_o. The BJT can supply an unlimited current to the load during positive excursions of the input drive but the negative excursion is limited by the current source I_Q.
- In order to avoid clipping the waveform, therefore, $i_o \leq I_Q$ and therefore $\bar{i} \leq 1$.

Voltage Swing

- The maximum positive output voltage certainly cannot exceed the power supply voltage V_{CC}. Also, if the follower transistor remains active during the entire cycle, then the maximum voltage is set by the input bias level minus V_{BE}.

- If the input voltage exceeds the supply, the transistor base-collector junction forward biases. Under "saturation", the maximum voltage is therefore given by $vo_{max} = V_{CC} - V_{CE,sat}$. In reality, we would never push our transistor this hard because it would generate a lot of distortion.

- Likewise, the minimum voltage occurs when we saturate our current source, at a value of $vo_{min} = V_{CE,sat}$
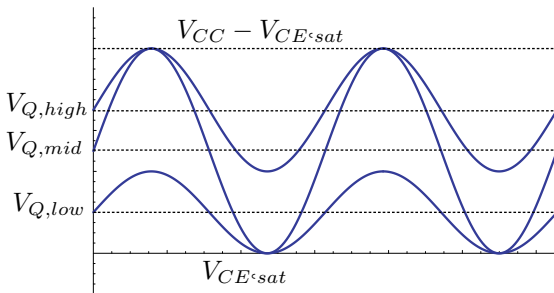
- To maximize the swing, we would bias the output at the midpoint

$$V_Q = \frac{V_{CC} - 2V_{CE,sat}}{2}$$

Follower Efficiency

- For a follower we see that $\bar{i} \leq 1$ and $\bar{v}$ depends heavily on the supply voltage. Let's take $V_{CC} = 3\,\text{V}$. Then

$$\bar{v} = \frac{V_{CC} - 2V_{CE,sat}}{2V_{CC}} = \frac{1}{2} - \frac{V_{CE,sat}}{V_{CC}}$$

- Typically $V_{CE,sat} \approx 300\,\text{mV}$, and say $V_{CC} = 3\,\text{V}$. Then

$$\bar{v} = \frac{1}{2} - \frac{1}{10} = 0.4$$

$$\eta \leq 20\%$$

- For CMOS followers, similar considerations apply where the limits are imposed by keepign the devices in the saturation region (V_{dsat}).

## Output Power when Matching for Gain

- Suppose we match the output of a PA to get the best power gain. Assuming a simple unilateral device with output capacitance C_o and output resistance r_o, the optimum load is a parallel L and R network with $R = r_o$.

- The maximum power that we can deliver to this load is given by

$$P_L = \frac{V_{SUP}}{2r_o}$$

which may be too low unless V_{SUP} is impractically large. Note that V_{SUP} cannot be larger than limits imposed by breakdown.

- Also note that the efficiency of such a PA is bounded by 50% times the efficiency of the core PA if we negelect r_o. That's because half the power is lost in the matching network.

- So in PA design, we sacrifice gain for output power.
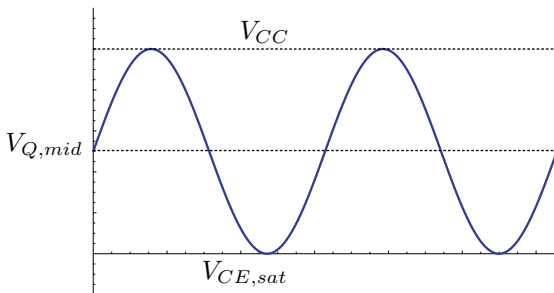
CE/CS Power Amplifier
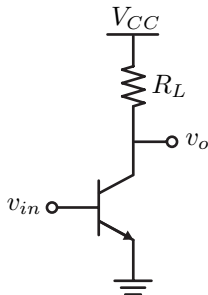
- The CE amplifier has the advantage of higher power gain (there is voltage gain and current gain). The collector efficiency is given by

$$\eta_c = \frac{P_L}{P_{dc}} = \frac{\frac{1}{2} v_o i_o}{V_{CC} I_Q} = \frac{1}{2} \overline{v} \times \overline{i}$$

- As before, the efficiency is maximized if we can set the voltage swing and current swing independently.
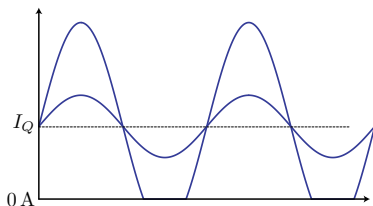
Voltage Swing Waveforms

- We see that to avoid clipping, we should bias the transistor at the midpoint between V_{CC} and $V_{CE,sat}$. Thus

$$v_o \leq \frac{V_{CC}}{2}$$

- The current in the transistor cannot go negative. Therefore, the maximum current is set by the bias current.

$$i_o \leq I_Q$$

- The efficiency is therefore still limited to 25%

$$\eta \leq \frac{1}{2} \times \frac{1}{2} = \frac{1}{4}$$

- It's important to note that to achieve these optimum efficiencies, the value of the load resistance is constrained by the current and voltage swing

$$R_{opt} = \frac{v_o}{i_o} = \left(\frac{\overline{v}}{\overline{i}}\right)\left(\frac{V_{CC}}{I_Q}\right)$$

- Since the load resistance is usually fixed (e.g. transmission line, antenna impedance or filter interface), a matching network is required to present the optimum load to the amplifier.
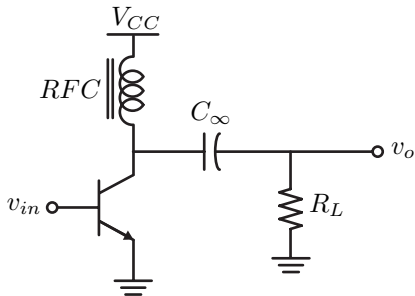
- If we AC couple a load R_L to the amplifier, then the Q point of the amplifier collector voltage is set at V_{CC} through the choke inductor.
- The maximum swing is now nearly twice as large. Notice that the collector voltage can swing *above* the supply rail.
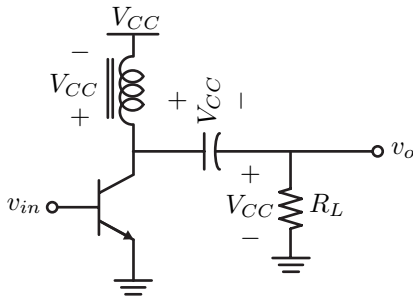
- Does this bother you? Recall that the voltage polarity across the inductor is given by dI/dt, which can go negative. Thus the collector voltage is equal to the supply minus or *plus* the absolute voltage across the inductor.

- Since the swing is almost double, the efficiency now approaches 50%

$$v_o \leq V_{CC}$$

$$\eta = \frac{1}{2} \frac{i_o v_o}{I_Q V_{CC}} \leq \frac{1}{2}$$

- In practice, due to losses in the components and back-off from maximum swing to minimize distortion, the actual efficiency can be much lower.

- Package parasitics (see later slides) also limit the voltage swing.
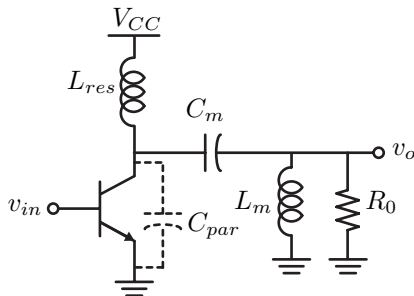
- In practice the collector inductor can double as a resonant element to tune out the collector parasitics. The coupling capacitor C_c can be replaced by a matching capacitor C_m.

Package Parasitics
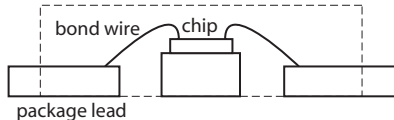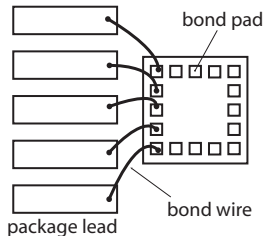
- In a normal inexpensive package, the pads of the chip are wire-bonded to the chip leads. Since the aspect ratio of the leads is much larger than the pad pitch, long bond wires are required to make the connections, leading to large inductance.
- The model of the package/chip should include the pads, the bond wires, as well as the package leads.

Emitter Degeneration
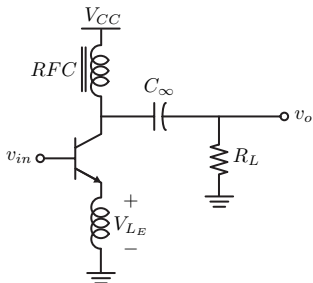
- Emitter inductance has a detrimental effect on PA efficiency since it reduces the swing. The voltage across the emitter is given by

$$V_E = j\omega L_E i_o$$

- For a current swing of 1 A at 1 GHz, a typical parasitic inductance of 1 nH will "eat" up 6.28 V of swing (but not in phase, so its impact is somewhat reduced)! We need to reduce L_E or to use a much higher V_{CC}.

- In practice both approaches are taken. We choose a technology with the highest breakdown voltage and the package with the lowest L_E.

Advanced Packaging

bump, chip, via, pads, down bond, chip, bond wire, package lead, exposed "paddle"
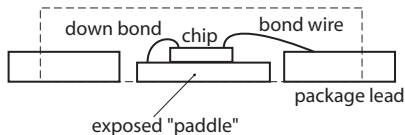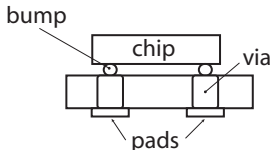
- In flip-chip technology, the chip is flipped and "bumped" onto a carrier substrate (on onto the board directly). This results in small inductance connections.
- In an exposed "paddle" package, there is a ground plane inside the package. We use conductive glue to mount the chip onto the package. Short down-bonds then create low inductance ground connections.
- In the extreme case, we can use several down-bonds in parallel surrounding the chip in addition to thinning the die.

High Frequency Design Challenges

- High frequency transistors (high f_T) have lower breakdown voltages, so the supply voltage cannot be too large, and this limits the output power.

  - PA's are hard to design at any frequency, but even harder at high frequencies
  - One cannot simply increase the width of the transistor to increase the output current (and hence power) because of two limits. First the added capacitance may be too large to tune out. Second, the required matching ratio in to drive such a load may be impractically large (and require high Q matching components)