Problem Set 6

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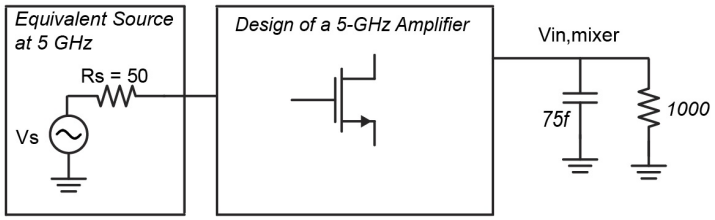
1. Design of a 5-GHz Linear Microwave Amplifier

   Use the 32nm PTM HP NMOS model with VD = 0.9 V, VG = 0.6 V, gate length of 32 nm, total width of 20 um, and NF (number of finger) of 5. The amplifier targets to drive a mixer, and the mixer input impedance is modeled by a 1000Ω resistor in parallel with a 75 fF capacitor, as illustrated in the below figure. (The device model can be downloaded at `http://ptm.asu.edu/modelcard/HP/32nm_HP.pm`.)



   (a) The mixer input is not 50Ω. What will be the problem if this mixer is used as a connector module like the ones sold by MiniCircuits ?
   `https://www.minicircuits.com/WebStore/Mixers.html`

   (b) Plot the stability factor (k) of this device versus frequency. Is the device unconditionally stable at 1 GHz? If not, find a (passive) device load impedance such that the real part of the device input impedance is negative at 1 GHz.

   (c) Following (b), find the (passive) source impedance at 1 GHz that moves the system pole to the imaginary axis.

   (d) Add a series resistor at the transistor gate to make the device unconditionally stable at 5 GHz with $k = 1.2$. What is the resistor value and the maximum transducer gain of this new device (FET + resistor) at 5 GHz? Plot k versus frequency.

   (e) The new device still has $k < 1$ at 1 GHz, which is undesirable because the load and source impedances of a 5-GHz design are usually not controlled at 1 GHz. Therefore, a pair of undesired source and load impedances at 1 GHz can make the system unstable and the 5-GHz amplifier is no longer usable. Further increasing the series resistor can make $k > 1$ at 1 GHz. What is the main drawback of this approach?

   (f) We will eventually make $k > 1$ at all frequencies with a better method. Lets focus on the 5-GHz design for now. Assuming the source resistor is 50Ω, what is the voltage gain ($V_{in,mixer}/V_s$) and power gain ($P_{in,mixer}/P_{avs}$) without any matching network.

(g) Lecture 9 introduced bi-conjugate matching and the formula to calculate the optimal source and load impedances of a device for the maximum power gain. What are the optimal source and load impedances of your device (FET+gate resistor) at 5 GHz? Verify your calculation by the ADS function *SmGamma*.

(h) Design both the input and output matching networks (using lossless inductors and capacitors) to maximize the power/voltage gain. What are the maximum voltage gain and the maximum power gain. What is the 3-dB bandwidth?

(i) (*242A only*) If you are allowed to use two-section matching networks, what the maximum bandwidth that can be achieved?

(j) Following (h), simulate the stability factor for the circuit composed the FET, gate resistor and the two matching networks. Compare the result to that obtained in (d).

(k) If you have not already done so, provide a reasonable bias network to your circuit without using any ideal dc block and dc feeds in the schematic.

(l) Stabilize the circuit such that $k > 1$ at all frequencies. If $k < 1$ at a lower frequency (e.g. 100 MHz), bypass circuit can be used to introduce loss and increase k at that frequency. (For example, the ac ground in your matching networks can be replaced by a 30 pF capacitor in parallel with a 10Ω resistor.) Try to achieve $k > 1$ at all frequencies with the power gain at 5 GHz degrading less than 2 dB from the maximum gain.

(m) (*242A only*) Now your amplifier has $k > 1$ at all frequencies. Note that unconditionally stability is a very strong condition that allows arbitrary source and load impedances. In this particular design, the load impedance is actually controlled; therefore, the power gain can be improved by decreasing the gate resistor to some extent such that the amplifier output resistance is still positive under an arbitrary source impedance, and the amplifier input resistance is positive under the given load impedance. What is the power-gain improvement that can be achieved? Plot k versus frequency for the modified circuit.