Today's Agenda (Nov. 29)
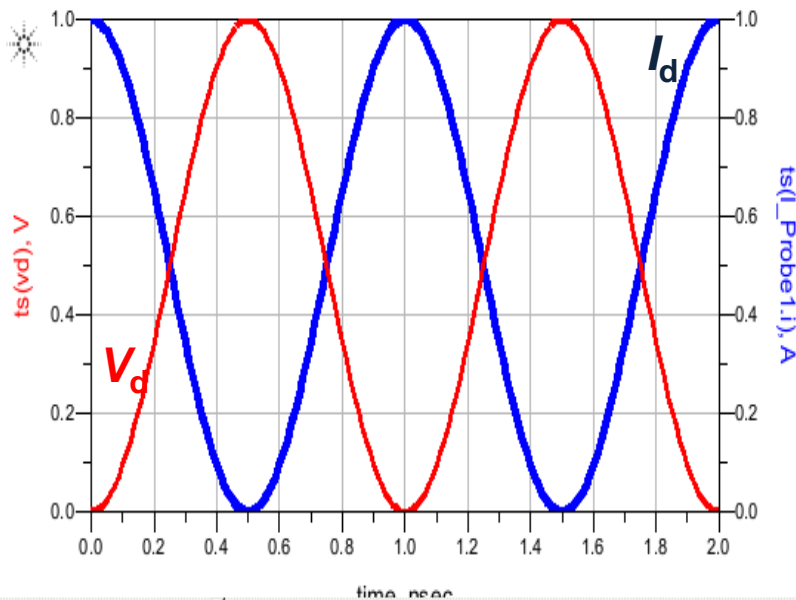
o PA Waveform and Efficiency: Class A & B

o Maximum Gain and Maximum Power Designs

o PA Load Pull
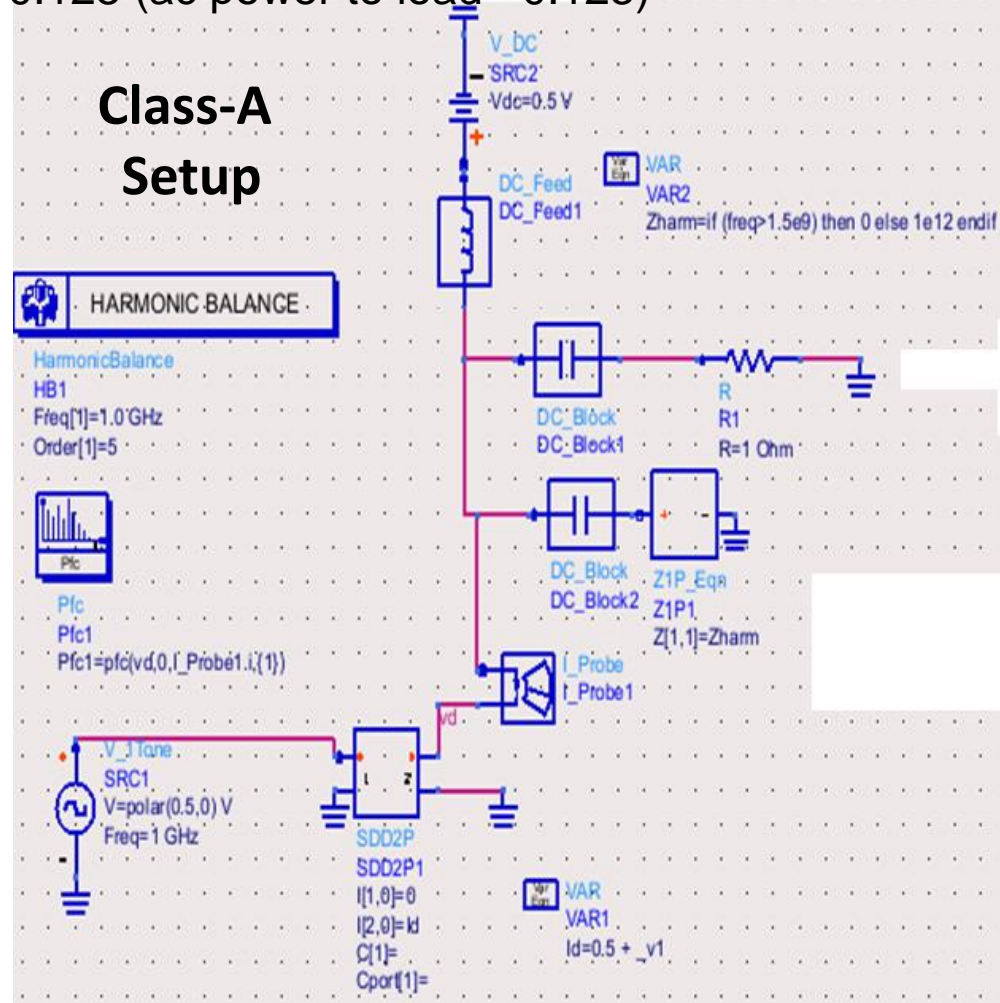
o PA Design Example

PA Waveform and Efficiency: Class A

- ❑ Assume the maximum current is 1 A and the supply voltage is 0.5 V
- ❑ Current is $0.5+0.5\cos(\omega t)$; Voltage is $0.5-0.5\cos(\omega t)$
- ❑ Power from supply: $0.5\times0.5 = 0.25$
- ❑ FET power dissipation: $\langle Current\times Voltage\rangle = \langle 0.25-0.25\cos^2(\omega t)\rangle = \langle 0.25 - 0.125\rangle = 0.125$
- ❑ FET fund. pow. dissipation : $0.5\times-0.5/2 = -0.125$ (ac power to load $=0.125$)

Class-A Waveform @ Drain

| freq	mag(Pfc1/0.5/I_Probe1.i[0])	Pfc1
1.000 GHz	0.500	-0.125

Class-A Setup

PA Waveform and Efficiency: Class A

I. Class-A PA peak power = $(V_{max} - V_{min}) \times I_{max} /8$
II. Class-A PA peak drain efficiency = 50%
III. @ 6-dB power back-off:

a. FET current is $0.5 + 0.25\cos(\omega t)$; FET drain voltage is $0.5 - 0.25\cos(\omega t)$
b. Power from supply = $0.5 \times 0.5 = 0.25$
c. FET power dissipation: $<0.25 - 0.0625\cos^2(\omega t)> = 0.125 - 0.03125$
d. FET fund. pow. dissipation : $0.25 \times -0.25/2 = -0.03125$ (ac power to load =0.03125)
e. Drain Efficiency (DE) = 12.5%

dc power consumption

Efficiency

fundamental power at ω
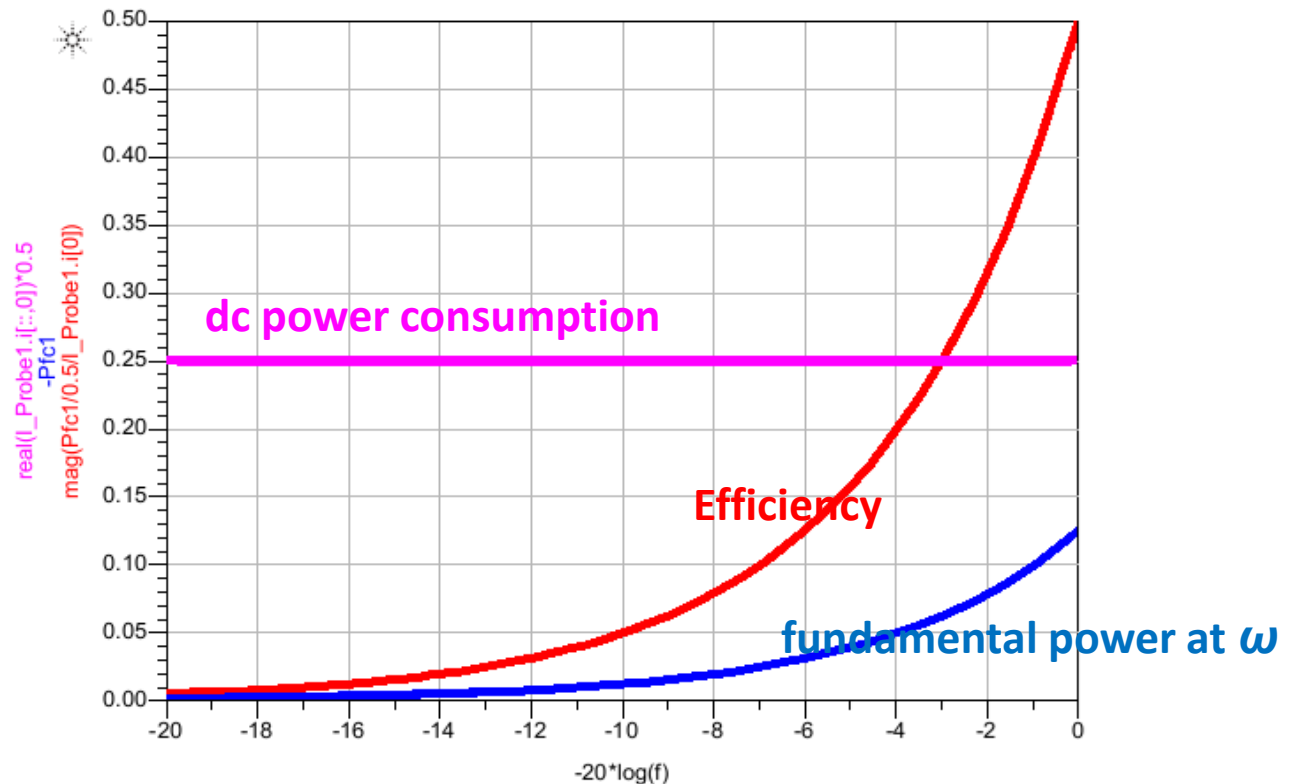
PA Waveform and Efficiency: Class B

- ❑ Assume the maximum current is 1 A and the supply voltage is 0.5 V
- ❑ Current is $(1/\pi)$ +0.5cos(ωt)+harmonics; Voltage is 0.5-0.5cos(ωt)
- ❑ Power from supply: $0.5 \times 1/\pi$
- ❑ FET power dissipation: dc(Current×Voltage)= $(0.5 \times 1/\pi - 0.125)$
- ❑ FET fund. pow. dissipation at ω: $0.5 \times -0.5/2 = -0.125$ (ac power to load =0.125)

Class-B Waveform
@ Drain
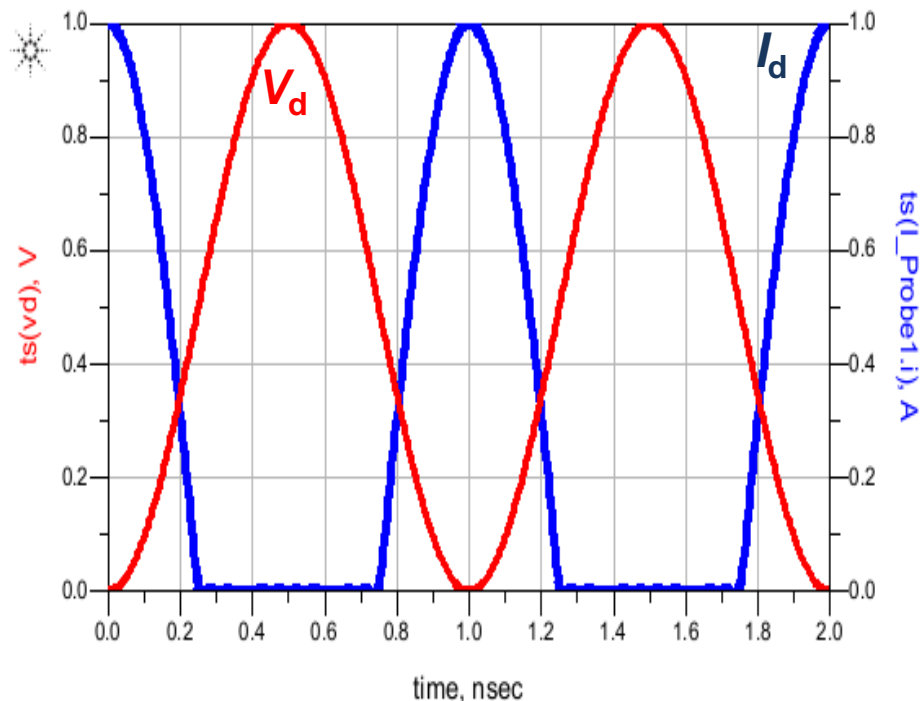
Class-B
Setup
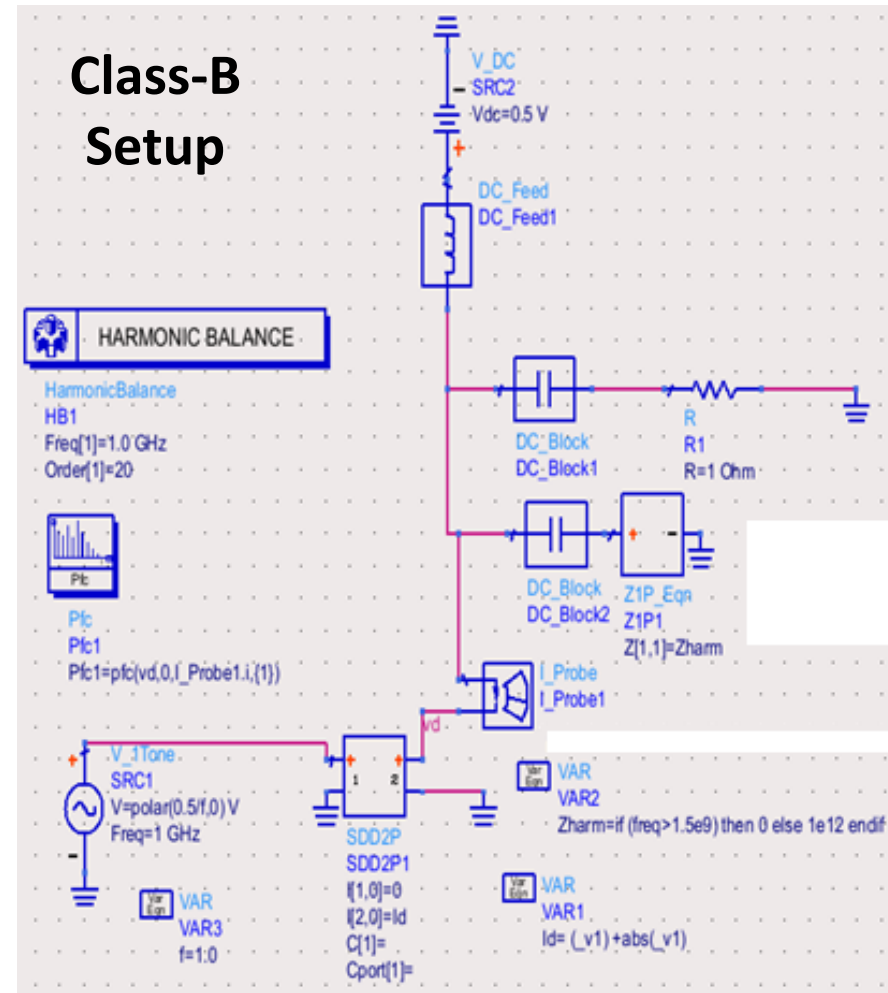
PA Waveform and Efficiency: Class B

I. Class-B PA peak power $=(V_{max}-V_{min}) \times I_{max}/8$
II. Class-B PA peak DE = 78.5%
III. @ 6-dB power back-off:

a. FET Current is $(0.5/\pi) +0.25\cos(\omega t)+$harmonics

b. FET Drain Voltage is $0.5-0.25\cos(\omega t)$

c. power from supply = $0.5 \times 0.5/\pi$

d. FET power dissipation:
$<0.25/\pi-0.0625\cos^2(\omega t)> = 0.25/\pi \ - 0.03125$

e. FET fund. pow. dissipation at ω:
$0.25\times-0.25/2 = -0.03125$
(ac power to load $=0.03125$)

f. DE = 39.3%
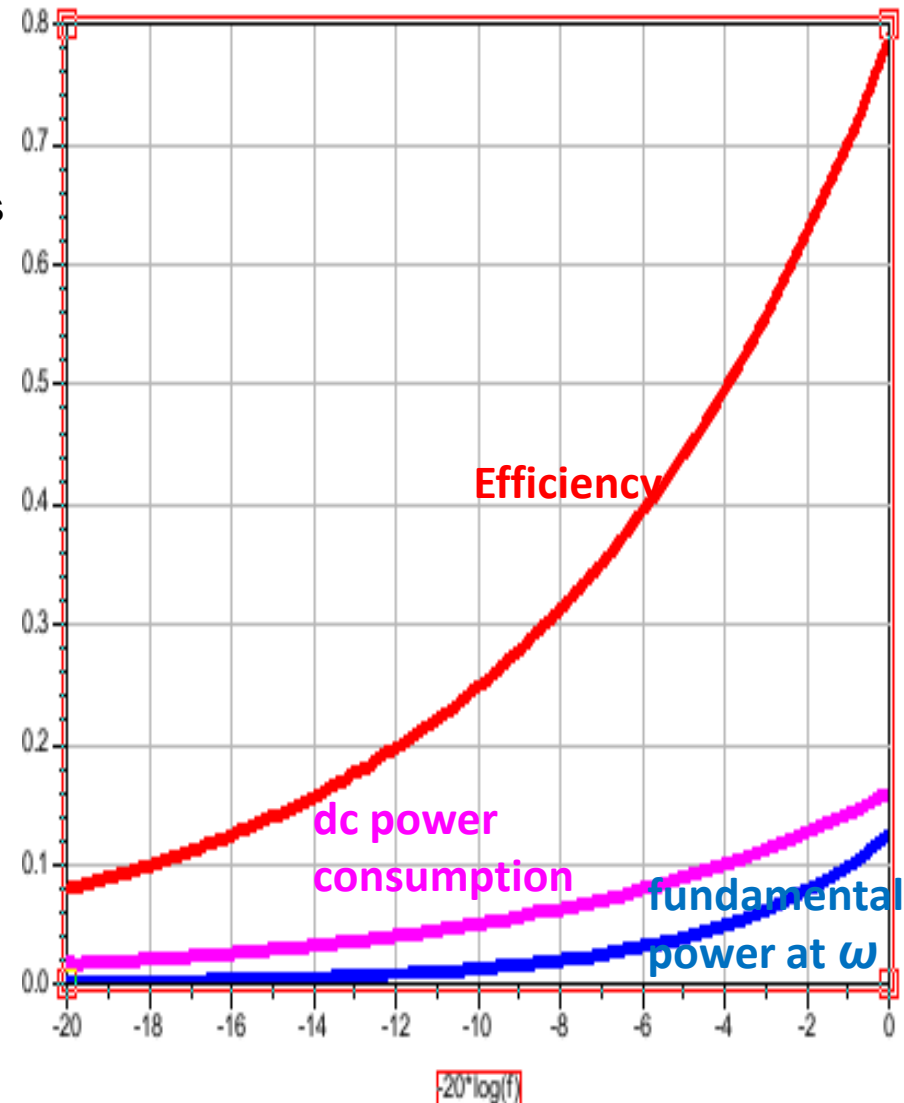
Design for Max. Gain or Max. Power

❑ Load impedance for the max. power does not depend on the small-signal parameters
❑ Load impedance for the max. gain depends on the small-signal parameters
❑ Consider an illustrative FET device with $I_d = (V_g - 0.5)(1 + V_d/1000)$ for $V_g > 0.5$ and $V_d > 0$
  assume input = 1000Ω, V_{max} = 10V, V_{min} = 0V, and I_{max} = 1A

Maximum Power Design, R_L = 10
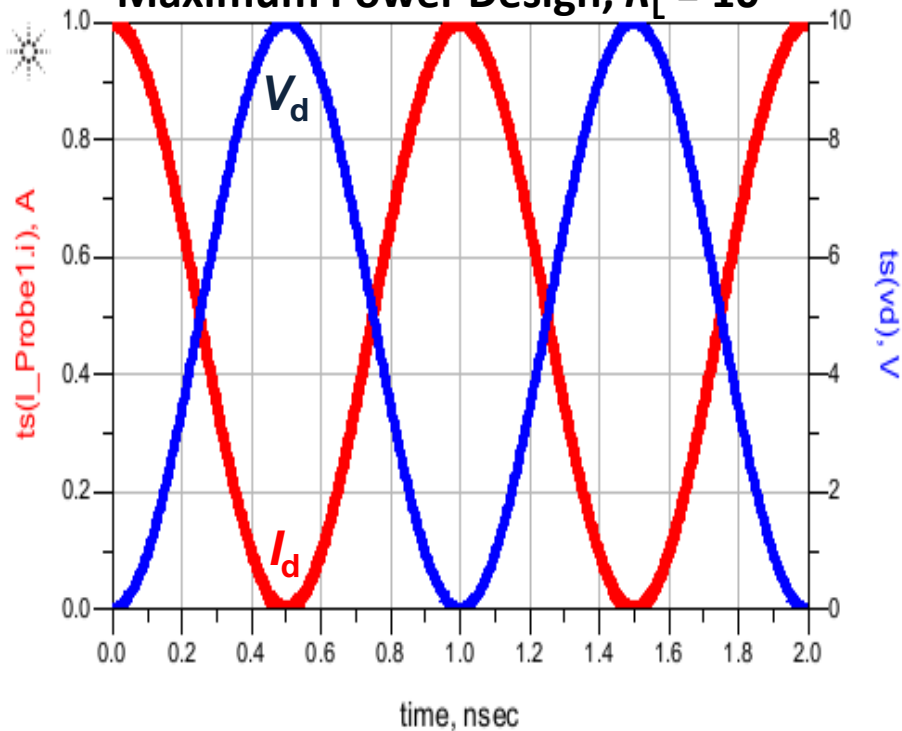
Power = 5*0.5/2 = 1.25 W
Eff = 50%
Gain = 5 W / 0.125 mW = 40 dB

Maximum Gain Design, R_L = 1000
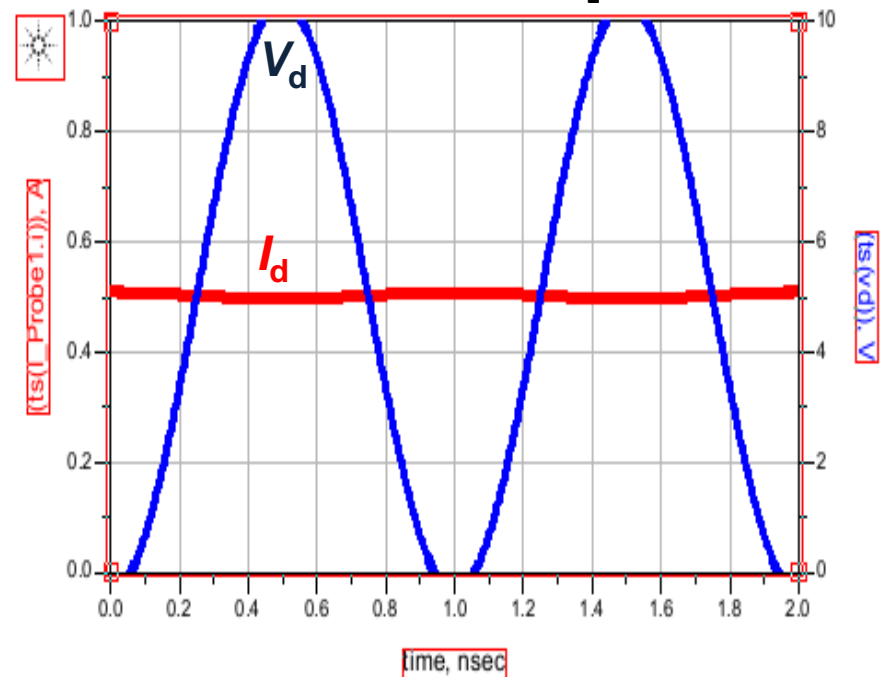
Power = 5*0.005/2 = 12.5 mW
Eff = 5%
Gain = 12.5 mW / 0.6 uW = 56 dB
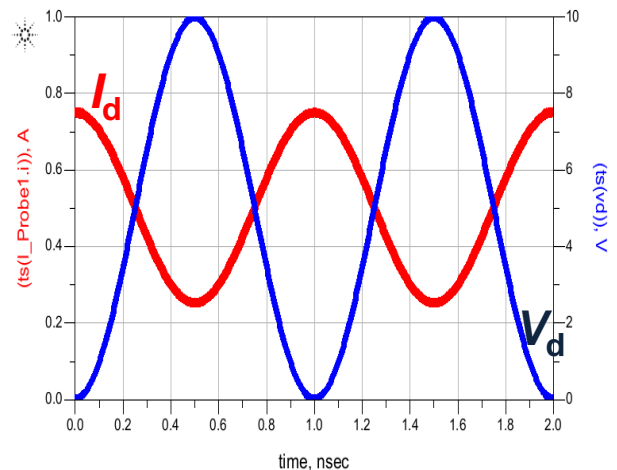
PA Load-Pull Contours (1/2)

❑ **The previous example** shows the maximum power is achieved with a unique Z_L

❑ Ideally, PA power saturates when the drain voltage or current reaches the maximum

$R_L = 10$ Ω
$P_{max} = 1.25$ W
$P_{supply} = 2.5$ W

$R_L = 1$ kΩ
$P_{max} = 12.5$ mW
$P_{supply} = 2.5$ W

$R_L = 5$ Ω
$P_{max} = 0.63$ W
$P_{supply} = 2.5$ W
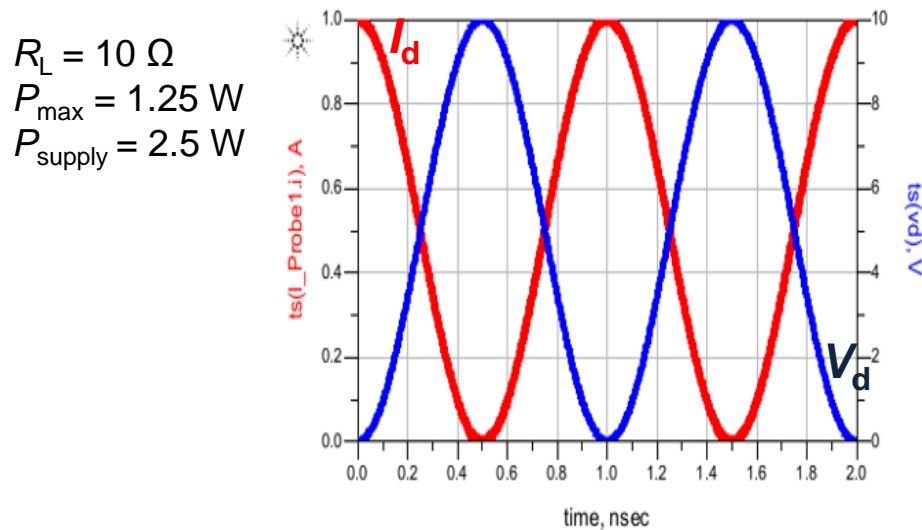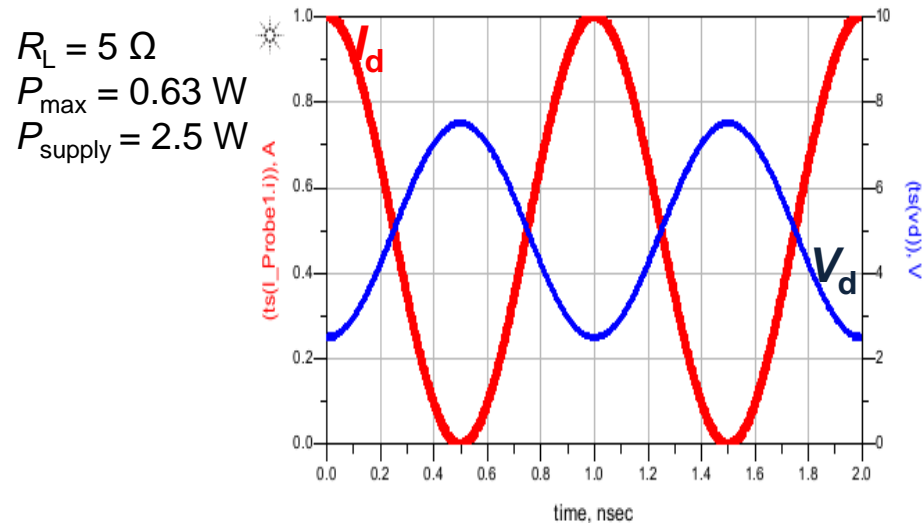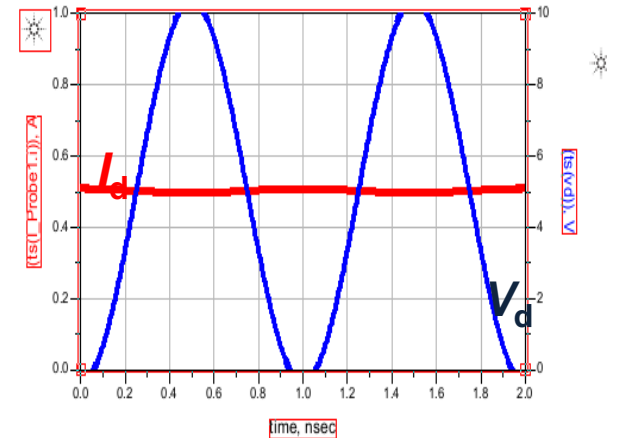
$R_L = 20$ Ω
$P_{max} = 0.63$ W
$P_{supply} = 2.5$ W

PA Load-Pull Contours (2/2)

❑ Only a unique load impedance (e.g. 10Ω) achieves P_{max} = 1.25W

❑ The other (lower) P_{max} can be achieved by multiple load impedances

❑ Constant-P_{max} contours can be drawn on Smith Chart to help PA designs

P_{max} = 1.25W

P_{max} = 0.625W
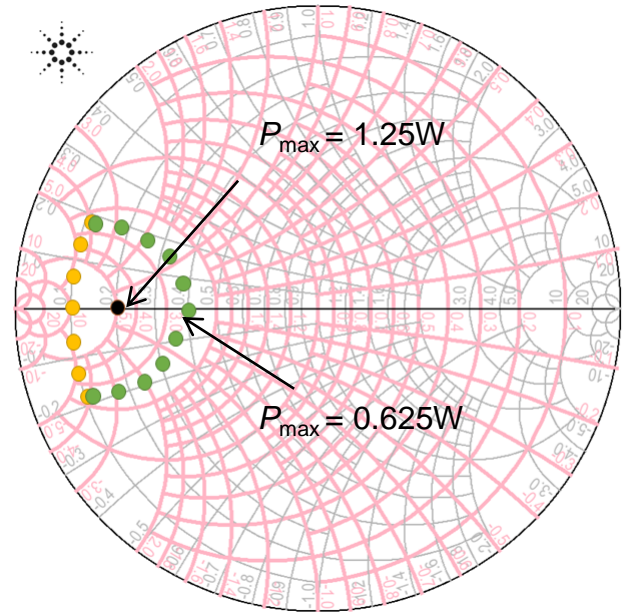
Ex. Load Impedances for maximum power 3-dB lower than 1.25W (P_{max} = 0.625W)

| If current-limited:	If voltage-limited:
0.5*Real{0.5A × 0.5A ×(R+jX)} = 0.5 × 1.25 W	0.5*Real [5V × 5V /(R+jX)] = 0.5 × 1.25 W
$\Rightarrow$ **R = 5**	$\Rightarrow$ Real [1/(R+jX)] ≡ **G =** 0.05
0.5A× |Z| < 5 V => **|Z| < 10**	0.5A × |Z| > 5 V or **|Y| < 0.1**

The two branches form a closed loop!!!

PA Design Example (1/2)

Design a pseudo-differential PA with ideal differential-to-single-ended transformer at 2.4 GHz under 0.9 V supply using 32 nm PTM model. Satisfy the following specifications: (1) Power Gain > 15 dB, (2) Output P1dB = +20 dBm. (3) Drain Efficiency at Output P3dB > 30%.

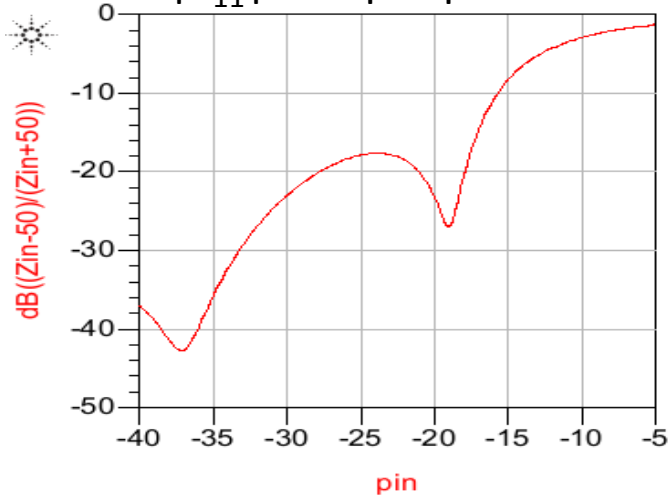**First Step: Estimate the required device size, bias, and load resistance**
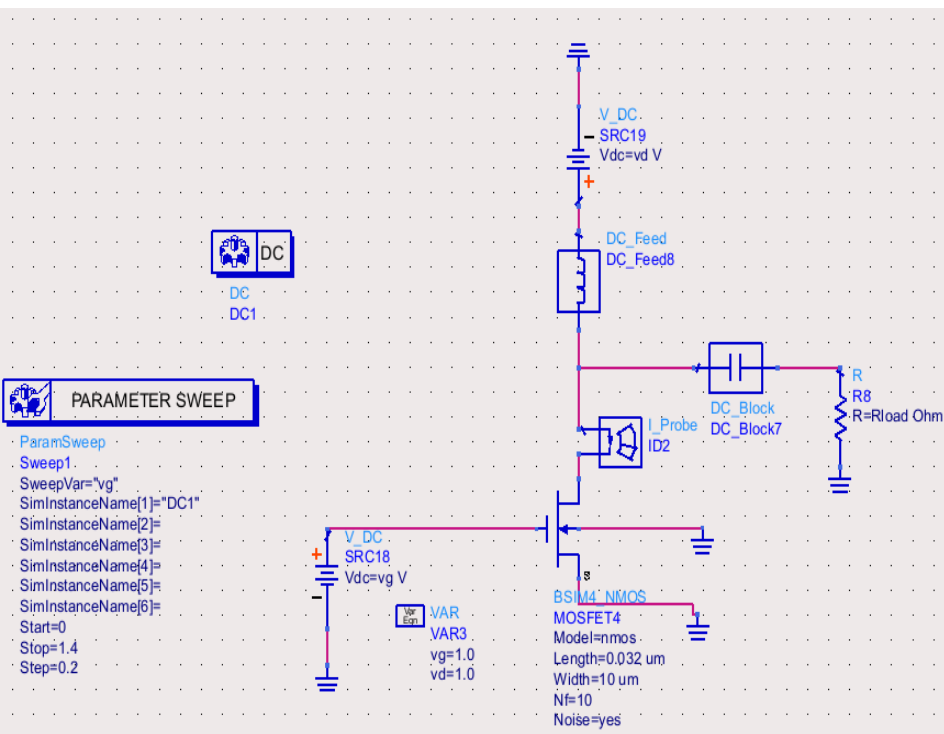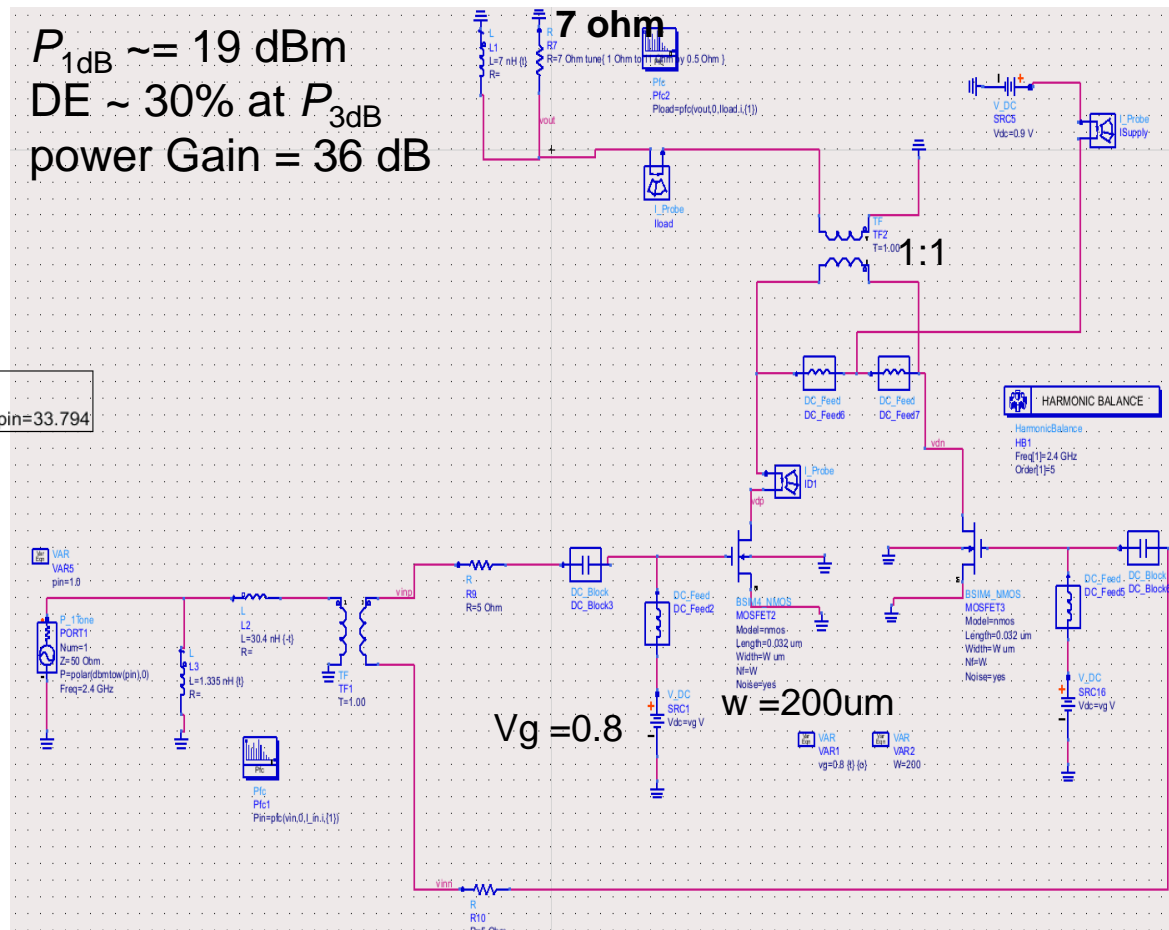

Test Device Size = 10 um
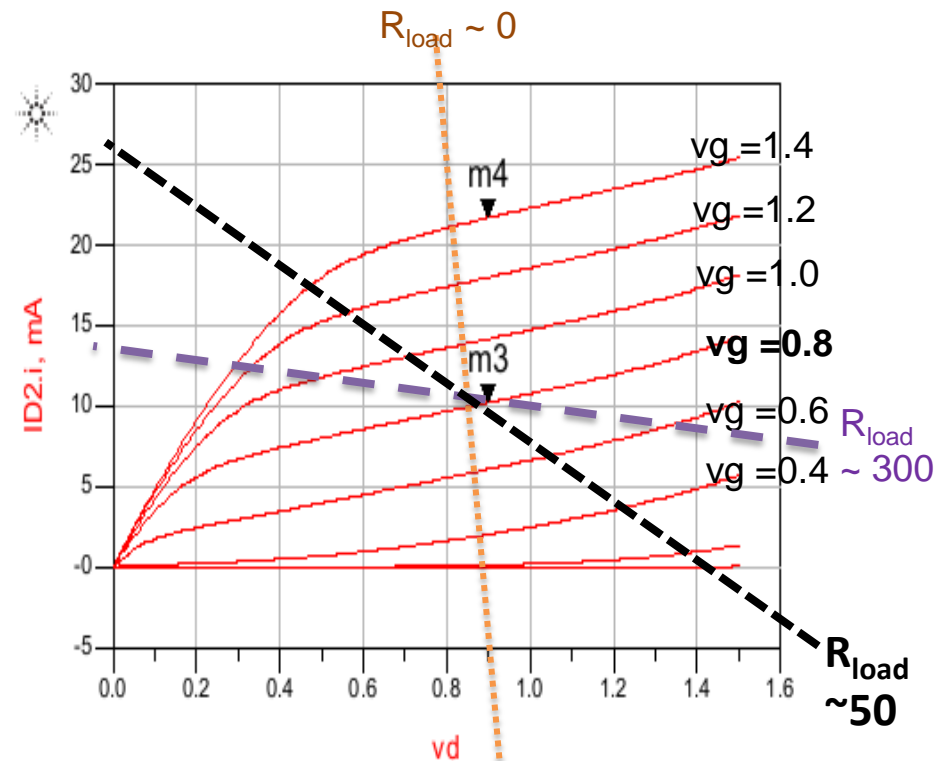
PA Design Example (2/2)
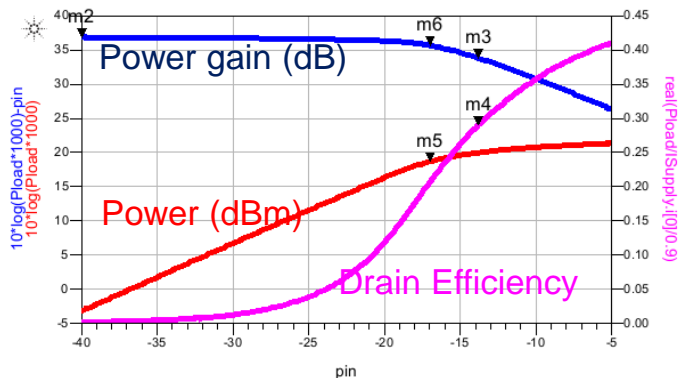
DE and PAE

❑ Drain Efficiency = Output Power/ Supply Power

❑ Power Added Efficiency (PAE)

= (Output Power – Input Power)/ (Supply Power)

= DE× (1- Power Gain^{-1})

❑ PAE is more important than DE
in most cases

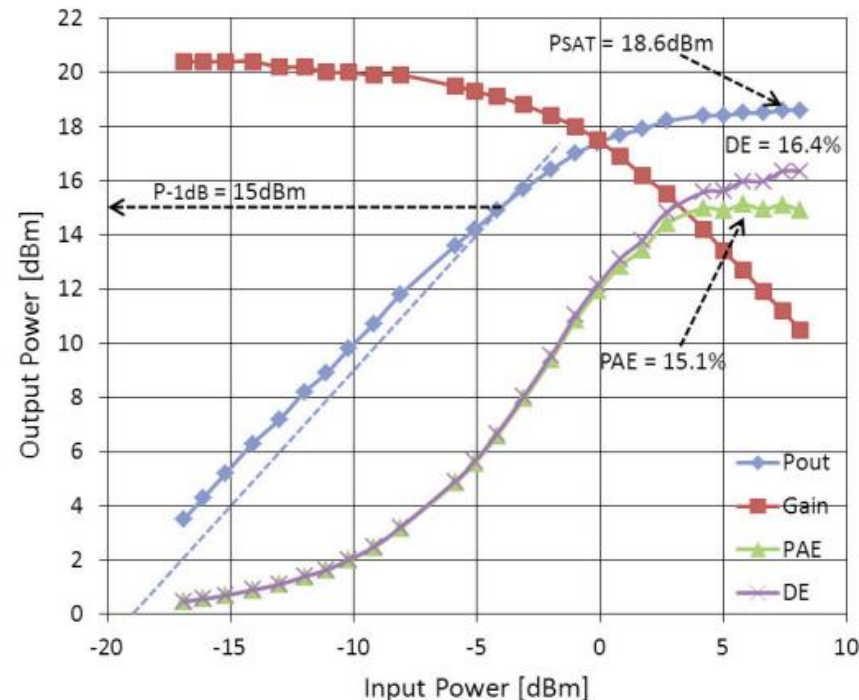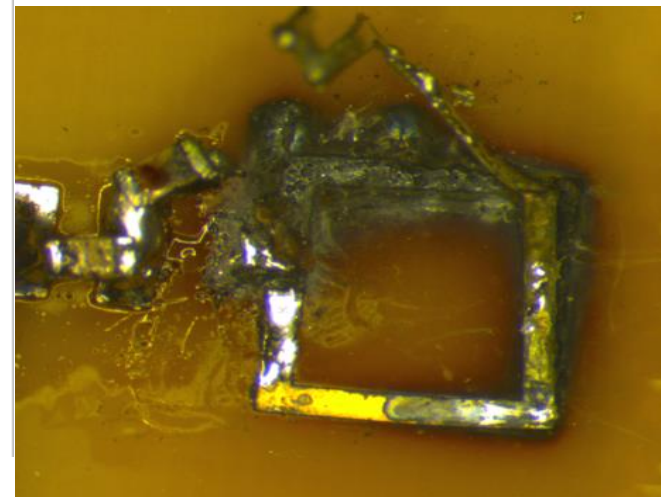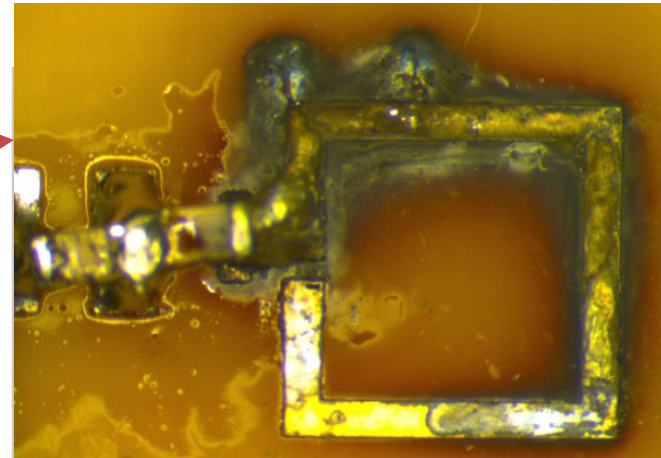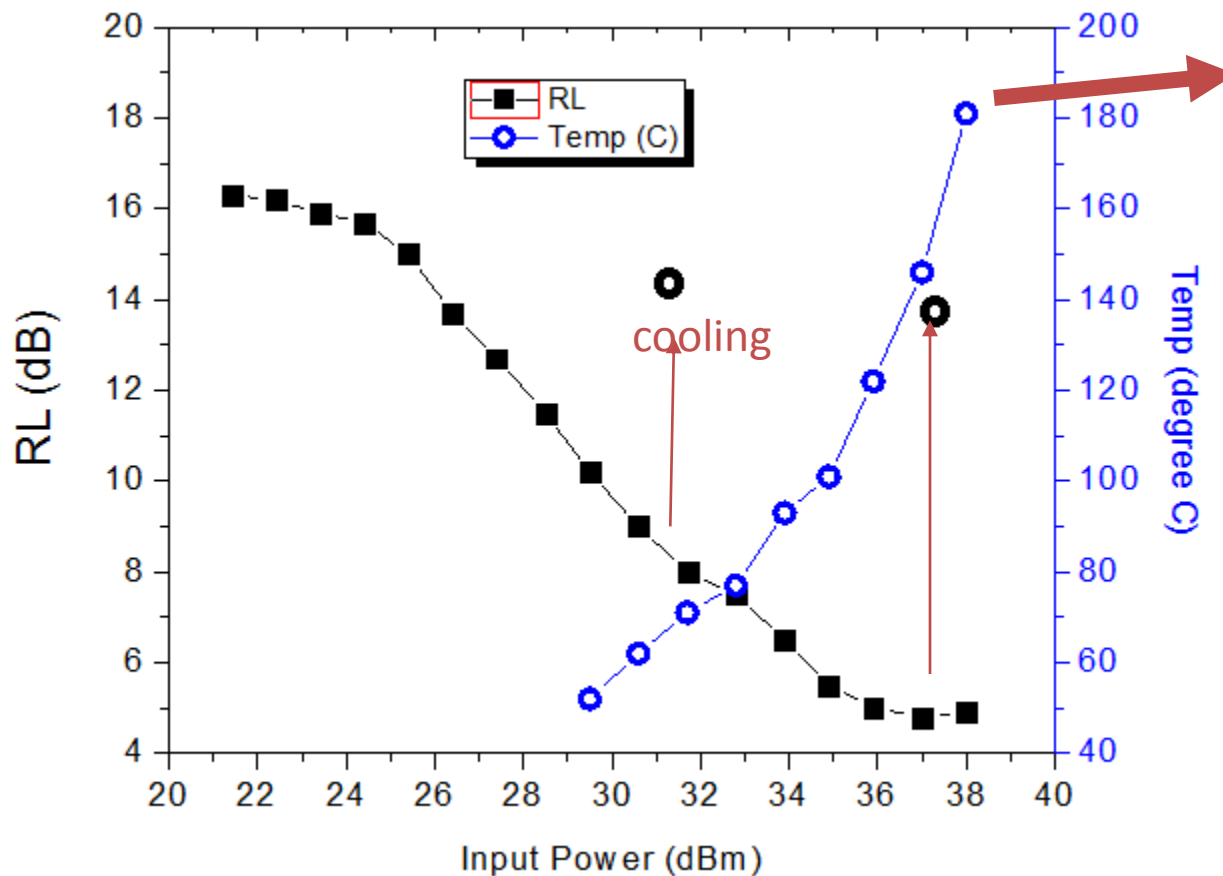The most important figure in a PA work

Figure 24.5.4: Measured PA output power, gain, drain efficiency and PAE.

Thermal Issue in Designs

1.8 GHz magnetic loop
Power dissipation increases temperature
Many high-temperature issues follow

cooling

5 W (37 dBm) is the maximum input power into the PCB