

EECS 142 Laboratory #3

High Frequency Amplifiers

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1 Introduction

Amplifiers are key building blocks in any communication system. In a receiver the weak incoming signal needs to be amplified to a sufficiently large value so that it can be detected or digitized. On the transmit side, the signal amplitude needs to be large enough for long-range transmission through free space or cables. In this laboratory you will design, simulate, and build a high-frequency narrowband amplifier. You will characterize your fabricated amplifier using a *Network Analyzer* by measuring the two-port parameters such as input impedance, output impedance, and power gain. The fabricated amplifier will be compared against your simulations.

1.1 Amplifier Design Techniques

The design of amplifiers begins with the specifications for the performance. For this lab, we will focus on the following specifications:

- Amplifier power gain. Most RF amplifiers are specified in terms of power gain and the load/source impedance are known (e.g. $Z_0 = 50\ \Omega$). In an integrated amplifier, the internal impedance may be higher and unmatched, in which case voltage gain might be more appropriate.
- Amplifier bandwidth. We usually desire operation over a specified bandwidth, where we expect the gain and group delay to be relatively flat (to avoid distortion) over a certain range. Two common amplifiers are baseband amplifiers, which must operate from DC or low frequency up to a given bandwidth (say DC - 100 MHz), and narrowband amplifiers which operate at RF (say 1 GHz). Narrowband amplifiers operate at a given center frequency and realize selectivity through the use of resonant circuitry.
- Input and output match are usually specified as the maximum tolerable reflection coefficient at the input and output (e.g. $S_{11} < -10\text{ dB}$). Matching is important in order to extract the maximum power from a source (antenna), to properly terminate a transmission line (otherwise the power gain will depend on the length of the line which changes with frequency), or to provide the proper termination for a filter for proper filter response.
- Amplifier stability. A robust amplifier should be stable over all frequency ranges and over process and temperature. Process and temperature variations cause the operating point to shift and thus stability should be checked under these conditions. Absolute stability ($K > 1$) implies that the amplifier is stable for any source or load impedance. A conditionally stable amplifier ($K < 1$) will become unstable if the load/source take on particular values. The stability circle plot on the Smith Chart shows the regions of instability. If the load and source are fixed (say at Z_0), then a conditionally stable amplifier may be acceptable. The designer should ensure that the unstable region is far from the origin of the Smith Chart and does not come too close under all conditions (frequency/temperature/process/bias voltage variations). Stability versus load variations is often specified through *SWR*, or the standing wave ratio. If an amplifier

is stable over an $N : 1$ SWR , that means the magnitude of the load can vary by a factor of N above or below the nominal value.

In reality, other important specifications include:

- Amplifier noise figure for receiver applications. Noise figure is a measure of how much noise the amplifier adds to the signal, which degrades the signal-to-noise ratio (SNR) of the signal, resulting in lower receiver sensitivity. Noise is most important when dealing with weak or small signals, when the noise signal amplitude is a substantial fraction of the input signal. We will cover this topic in depth in a later lab.
- Amplifier distortion generated by active device non-linearity. Distortion specifications include harmonic distortion (HD), which occur at harmonics of the input frequency, and intermodulation (IM) distortion, which also occur in-band, or near the operating frequency. In RF applications, IM distortion is much more important since harmonic distortion can be filtered out. These distortion products must be kept sufficiently small so that the amplified signal is not severely distorted. The strength of the distortion signals increases rapidly with the signal amplitude (faster than linear), which means that we mostly care about distortion when the signal is strong.
- Amplifier performance under process and temperature variations. In practice every amplifier will perform slightly differently due to inevitable variations in component parameters, especially active devices. Active devices are especially sensitive to temperature variations, and much effort is typically dedicated in designing a biasing network to cope and compensate for such variations.
- Amplifier efficiency. The efficiency is determined by comparing how much power is delivered to the load divided by the DC power consumption of the amplifier. This metric is most important for power amplifiers which consume significant power and it's desirable to use as much of this power as possible (power transmitted through the antenna versus wasted power converted to heat). If the gain is low, the input power should also be counted in the *power added efficiency*

$$\eta = \frac{P_L - P_{in}}{P_{DC}}$$

The next step in the design is the selection of the active devices (technology) and the bias point for the transistors. The bias point must be chosen carefully to meet power dissipation constraints, imposed either by physical limitations, such as thermal and DC voltage headroom, or to minimize the power consumption. Once a device has been selected, the designer should plot the maximum achievable gain (G_{max}/G_{MSG}) for the device over the frequency range of interest. If the device is unconditionally stable, then in practice we can come close to this maximum gain, but keep in mind that there is some loss in the matching networks at the input and output of the amplifier. If the device is conditionally stable, the designer may intentionally introduce loss or feedback in the device to stabilize the device. Other techniques such as neutralization through feedback or the use of a compound device

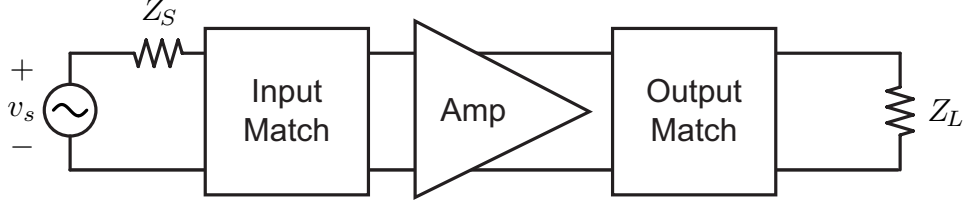


Figure 1: The design of an RF amplifier can be factored into the design of the input matching network, the bias of the amplifier, and the output match network.

(such as a cascode) are other options. If the required gain cannot be realized with a single device, then two or more stages are required. But keep in mind that the bandwidth may be limited by the matching networks. If the device optimal source/load impedances are vastly different than Z_0 , then the Q of the required matching networks will be very large, which will limit the bandwidth.

An important consideration in the design of amplifiers is the use of feedback. If the loop gain is sufficiently high, then negative feedback amplifier performance is determined by the passive feedback network rather than by the active component parameters, leading to less variation with process and temperature. Feedback amplifiers may introduce instability at high frequency due to the phase shift through the device, which converts negative feedback into positive feedback, de-stabilizing the circuit. At high frequencies it's common to avoid this effect by only using “local” feedback, or feedback around a single device (shunt or series feedback). In addition, in narrowband applications it's advantageous to use reactive components (for instance series feedback using an inductor) so as to introduce less noise into the circuit. Most importantly, even if the designer does not wish to employ feedback, at high frequency it's hard to avoid parasitic feedback, which occurs due to small feedback capacitors (such as the Miller capacitor) in active devices and due to board and package parasitics. The package introduces inductive parasitics in the form of lead inductance around the transistor and mutual inductive coupling between the leads of the transistor. If the amplifier is fully integrated and employs sufficient bypass capacitors, then package parasitics are only important when making connections to the external world, or at the input and output of the amplifier.

Once the amplifier transistors have been biased and stabilized, one selects the source/load impedance to achieve the desired performance. Typically driving the amplifier directly from a source and load of Z_0 impedance will result in a gain which is too low. For instance, the voltage gain of a simple resistively loaded amplifier contains a term $g_m Z_L$. If the load impedance $Z_L = Z_0$, then the voltage gain will be low since typically $Z_0 \sim 50 \Omega$. On the other hand, if a matching network is used to raise the load impedance to r_o (matched) or a large value (voltage amplifier), then much higher gain can be realized. The source and load are therefore transformed into the desired impedances through matching networks. Matching networks play a crucial role in the design of RF amplifiers, since once the device bias is chosen, the only other degree of freedom is the matching network. In Fig. 1 we show an input matching network cascaded with a two-port amplifier followed by an output matching

network. The overall gain of the two-port can be written as

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{in}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}$$

which can be viewed as a product of the action of the input match “gain”, the intrinsic two-port gain $|S_{21}|^2$, and the output match “gain”. Since the general two-port is not unilateral, the input match is a function of the load. Likewise, by symmetry we can also factor the expression to obtain

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{out}\Gamma_L|^2}$$

In the case of a unilateral amplifier, the above equations simplify to the product of three independent terms ($\Gamma_{in} = S_{11}$)

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} \times |S_{21}|^2 \times \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} = M_1 \times |S_{21}|^2 \times M_2$$

The above equation clearly shows the role of the input and output matching network. For a conjugate match, $\Gamma_S = S_{11}^*$, which means the maximum gain for the input matching network is given by

$$M_{1,\max} = \frac{1}{1 - |S_{11}|^2}$$

If the amplifier has $S_{11} \lesssim 1$, we can improve the transducer gain considerably by matching the input. A similar consideration applies to the output of the amplifier. The design of non-unilateral amplifiers is more complicated but often we can ignore the reverse feedback if $S_{12} \simeq 0$. The Unilateral Figure of Merit UFM is a good metric to test determine the error that would result if you make this assumption

$$UFM = \frac{|S_{11}||S_{22}||S_{12}||S_{21}|}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}$$

which sets an upper and lower bound for the error in gain under the unilateral assumption

$$\frac{1}{1 + UFM^2} < \frac{G_T}{G_{TU}} < \frac{1}{1 - UFM^2}$$

where G_{TU} is the calculated value of gain by neglecting S_{12} .

2 Prelab

Design an amplifier meeting following specifications: Power Gain $G_p > 15$ dB, S_{11} and $S_{22} < -10$ dB, operate at a center frequency of 600 MHz with a bandwidth of at least 100 MHz. The current consumption of the amplifier should not exceed 5 mA.

You may elect to use a single stage or a two-stage amplifier. You can also optionally employ feedback for DC biasing, stability, and matching. Make sure your amplifier will fit into the board provided. There is enough room for an input/output matching network,

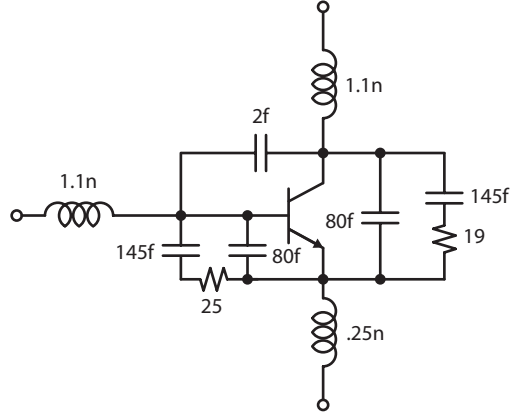


Figure 2: Equivalent circuit for packaged bipolar transistor.

shunt or series local feedback, and a tuned load. If you wish to use global feedback (two-stage design), you can solder wires to the board but be sure to include inductive parasitics in your calculations.

The SPICE model for the transistor should be used. This data is provided by the manufacturer and is available on the website (<http://www.nxp.com/models/spicespar/data/BFG403W.html>). Notice that the transistor model is embedded in a package model which includes the parasitic effects of the package and bond wires, including lead inductance and capacitance, and mutual inductance and capacitance. The component values for the BFG40Wp transistor are given below and an equivalent circuit is shown in Fig. 2. You may elect to use any transistor in the library.

```
subckt BFG403Wp base collector emitter inh_bulk_n
  Q1 (net17 net029 net034 inh_bulk_n) BFG403W region=fwd
  I10 (net4 net034) res r=19
  I9 (net6 net034) res r=25
  I8 (net17 net4) cap c=1.45e-13
  I7 (net029 net6) cap c=1.45e-13
  I6 (net17 net034) cap c=80e-15
  I5 (net029 net034) cap c=80e-15
  I4 (net029 net17) cap c=2e-15
  I3 (net034 emitter) ind l=0.25e-9
  I2 (collector net17) ind l=1.1e-9
  I1 (base net029) ind l=1.1e-9
ends BFG403Wp

.MODEL BFG403W NPN
+ IS = 5.554E-18
+ BF = 145
+ NF = 0.9934
+ VAF = 31.12
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+ IKF = 35.75E-03
+ ISE = 3.535E-14
+ NE = 3
+ BR = 11.37
+ NR = 0.985
+ VAR = 1.874
+ IKR = 14.3E-03
+ ISC = 5.708E-17
+ NC = 1.546
+ RB = 122.38
+ IRB = 0
+ RBM = 52.45
+ RE = 1.511
+ RC = 15.119
+ CJE = 3.661E-14
+ VJE = 0.9
+ MJE = 0.3456
+ CJC = 1.621E-14
+ VJC = 0.5569
+ MJC = 0.2079
+ CJS = 7.859E-14
+ VJS = 0.4183
+ MJS = 0.2391
+ XCJC = 0.5
+ TR = 0.0
+ TF = 4.122E-12
+ XTF = 68.2
+ VTF = 2.004
+ ITF = 0.1796
+ PTF = 0
+ FC = 0.5501
+ EG = 1.11
+ XTI = 3
+ XTB = 1.5

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It is very important to take these parasitics into account at high frequency in order to properly predict the performance of the practical amplifier. In addition to the package parasitics, be sure to include an estimate of the component parasitics (see lab #1), such as finite inductor Q . This will impact the matching network, gain, and stability of your amplifier. Finally, be sure to estimate the board level parasitics in the design. For instance, if you short the emitter of the amplifier, it actually must travel through the package and then through the board. A 0603 footprint is added for optional series feedback, which introduces inductance even if it is shorted with a zero ohm resistor. The via also contributes inductance. These parasitics were measured in lab #1.

1. Simulate the f_T of the transistor versus collector current. Find the current where f_T

is maximized and simulate the f_{max} at this bias point. What is the highest frequency one can use this transistor and realize a power gain of 12 dB?

2. Plot the BJT transistor's maximum stable gain (MSG) and stability factor at the design bias point. Be sure to include the package parasitics. At what frequency is the transistor unconditionally stable?
3. Describe the design approach of your amplifier. Include calculations and simulations results used to arrive at the design. Do not use "SPICE monkey" techniques in your design! Make sure the required component values are realizable in 0603 footprint (see lab #1).
4. Design a bias network for your amplifier. Make sure that the bias network can be realized with the prototype board. Common approaches include base resistor dividers with emitter series feedback or self-biasing through a shunt feedback resistor R_f . Size your biasing resistors so that they do not interfere with the amplifier at high frequencies. Use bypass capacitors where appropriate. Check the stability of the biasing scheme by varying the BJT transistor parameters (β_0 and I_S) and verify that the amplifier bias remains relatively constant.
5. Simulate your amplifier (ADS or SpectreRF) and verify the performance. Include plots of the power gain, stability factor, input match, and output match. Identify the bandwidth of the amplifier. Be sure that your simulation includes the bandwidth of the input/output match (simulate port-to-port rather than S_{21}).
6. Compare the gain of the amplifier to $|S_{21}|^2$. How much "gain" do you realize with the input and output match?
7. How does the amplifier's overall gain compare to the MSG of the device? How much gain is lost in the input/output match (due to finite Q components)?
8. Simulate your amplifier using Monte-Carlo analysis by varying the components by 20%. Plot the amplifier stability under variations. Comment.

3 Experimental Work

3.1 Procedure

When soldering active devices such as the BJT transistor, be sure to strap yourself to ground to avoid electrostatic discharge from damaging the device. The board layout for the single-stage amplifier is shown in Fig. 3. The two-stage board is simply the cascade of two single-stage amplifiers. Notice that the board has room for a lot more components than you may actually need to give you the maximum flexibility for your design.

1. Solder the components onto board and make sure the amplifier biases correctly. Solder the transistor chip last to minimize risk of damage to the integrated circuit. Check the device V_{BE} and V_{CE} to ensure proper biasing conditions. If you are having difficulty biasing the transistor, seek help.

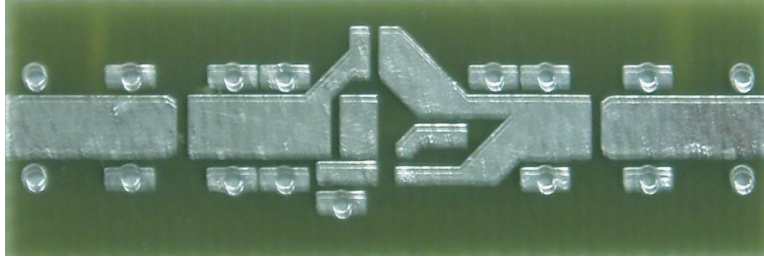


Figure 3: PCB for the amplifier includes footprints for input/output matching, feedback, and biasing.

2. Be sure to include bypass capacitors from DC points to ground. Solder the capacitors on the back-side of the board at points to minimize the inductance of the DC point. Since large capacitors self-resonate at lower frequencies, below the desired operating frequency, use several parallel capacitors (1pF - 1 μ F) to realize a broadband low impedance at the supply.
3. Bias up the amplifier and ensure that the DC operating point matches expectations. Check the DC point at each node and calculate the voltage V_{BE} and V_{CE} to verify the amplifier is in the correct operating region. Do not proceed until the amplifier is operating correctly.
4. If needed, vary the DC bias to match your simulation results for current.
5. Measure and record the amplifier frequency response (S_{11} , S_{22} , S_{21} and S_{12}) on the VNA over the desired frequency range.
6. Measure and record the amplifier frequency response over a broad frequency range (DC to the maximum available frequency of the VNA). Plot the amplifier stability factor over this range.
7. Plot the input/output impedance (magnitude/phase) of the amplifier over the desired frequency range.
8. From measured data, what's the G_{max} of the amplifier at the center frequency?
9. Use matching feature of VNA to improve gain of the amplifier. Find the optimal source/load impedance and virtually "embed" (through simulation on the VNA) these impedances into your amplifier and plot the results.
10. Partner up with another group and measure the cascaded performance of your amplifiers. Measure the small-signal gain and bandwidth. Verify that the measured performance matches with the calculated cascade performance, particularly the overall gain and S_{21} . If the amplifiers are not well matched, be sure to include the effect of mismatch in your gain calculation.

11. (*Optional*) Using the spectrum analyzer observe the output spectrum. Insert a weak tone at 600 MHz (-60 dBm) at the input and observe the output spectrum. Vary the input power and measure the power at the fundamental and a few harmonics. Comment.

Save your amplifier board for future experiments! Take a digital photo of the finished amplifier.

4 Post Laboratory

1. Explain the importance of bypass capacitors in the design. Why does the supply V_{CC} need to be bypassed to ground? Where is the best location to place bypass capacitors?
2. Compare measurement and simulation results by overlapping the measured S_{11} , S_{22} and S_{21} of your amplifier with the simulations. Explain differences.
3. Explain the significance of S_{12} in the design. Compare the measured and simulated S_{12} , especially at higher frequencies. Explain the mismatch between the simulation and measurements.
4. Which board level or component level parasitics were the most detrimental? Explain.
5. Modify schematic to match measurements. You should use your knowledge of the board level parasitics and component parasitics. If you did not measure the components and the board, the GSI can provide you the appropriate data. Make sure you understand the various measurements of the board level parasitics. The component models can also be obtained from the manufacturer.
6. Based on your experience in the lab, comment on any changes in the design of the amplifier which may improve performance or make the amplifier more realizable. If time permits, feel free to redesign and rebuild the amplifier.
7. How much time did you spend on this lab? Any feedback is appreciated.

5 References

References

- [1] A. M. Niknejad, *Electromagnetics for High-Speed Communication Circuits*, 2007, Cambridge University Press.