## Problem Set 9 Submit through becourses

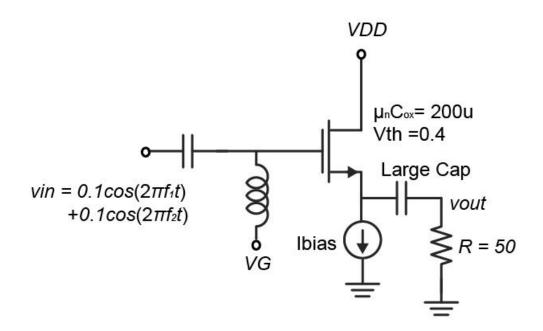
## 1. Review of Important Concepts

Assume a memory-less distortion circuit is modeled by  $I_{out} = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3$  and the input dc bias voltage is  $V_{in,0}$ .

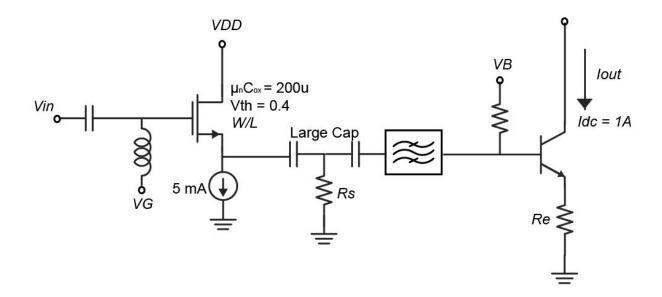
- (a) Derive IIP3, OIP3,  $IP_{1dB}$ , and  $IP_{3dB}$ .
- (b) If *IIP*3 is 10 V, what is the input-blocker level that degrades the small-signal gain of the desired signal by 2 dB?
- (c) Following part (b), what will be the tolerable blocker levels for a two-tone blocker?
- (d) If IIP3 is 10 V, what are the  $IP_{1dB}$  for two-tone and three-tone input signals?
- (e) If the modeled circuit is a BJT with  $I_{out} = I_s[exp(V_{be}/V_T)]$ , use Math tool to find the actual output third-harmonic current as a function of the input magnitude. Compare the actual values to the estimated values via the power series.

## 2. Distortion of a Source Follower

(a) For the source follower shown below. Calculate the required bias current  $(I_{bias})$  and W/L for the long-channel transistor to drive the load with a swing of 100 mV (at both  $f_1$  and  $f_2$ ), with IM3 equal to -50 dBc.



## 3. Pre-distortion and Source-degeneration Linearizer



- (a) For the above schematic, what are the OIP3 of the BJT stage for  $R_e=0\Omega$  and  $R_e=0.02\Omega$ ?
- (b) What are the two possible  $R_e$  for the BJT stage to have an OIP3 of 10A?
- (c) (242 Only) Following part(b), a source follower is placed before the BJT stage in order to achieve a cascade OIP3 better than the BJT-stage OIP3 (10A). Is this linearization approach feasible for both the  $R_e$  you found in part(b)? (There is an ideal BPF that only passes the fundamental and the IM3 components, so the cascade IIP3 formula is exact.)
- (d) (242 Only) Using one of the two  $R_e$  you found in part(b) for the BJT-stage OIP3 of 10A, continue to design the source follower with a fixed bias current of 5mA to achieve (i) cascade OIP3 of 20A and (ii) the highest voltage gain for the source follower. The design variables are the FET size W/L and the feedback resistor  $R_s$ .
- (e) (242 Only) Verify you design in part(d) via ADS Harmonic-balance simulation.