SMALL SIGNAL EQUIVALENT CIRCUIT EXTRACTION FROM A GALLIUM ARSENIDE MESFET DEVICE

by

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Extraction of a Small Signal Equivalent Circuit Model from a Gallium Arsenide MESFET Device

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(ABSTRACT)

The development of microwave Gallium Arsenide Metal Semiconductor Field Effect Transistor (MESFET) devices has enabled the miniaturization of pagers, cellular phones, and other electronic devices. With these MESFET devices comes the need to model them. This thesis extracts a small signal equivalent circuit model from a Gallium Arsenide MESFET device. The approach taken in this thesis is to use measured S-parameters to extract a small signal equivalent circuit model by optimization. Small signal models and S-parameters are explained. The Simplex Method is used to optimize the small signal equivalent circuit model. A thorough analysis of the strengths and weaknesses of the Simplex Method is performed.

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CHAPTER I. INTRODUCTION

1.1 Discussion Of Nature Of Research Work

The work done in this thesis involves measuring scattering parameters (S-parameters) from a three terminal semiconductor device called a Metal Semiconductor Field Effect Transistor (MESFET) and using these S-parameter measurements to extract an equivalent circuit model for the MESFET device. This equivalent circuit represents the device under evaluation in terms of resistors, capacitors, inductors, and current sources. The equivalent circuit form of the MESFET device will show the semiconductor designer the impact of how changing a device characteristic affects a property such as gain or isolation. However, the designer will typically have eight equations representing the real and imaginary parts of the four S-parameters and sixteen unknowns representing the equivalent circuit model. A cost function representing the difference between the modeled S-parameters and the measured S-parameters is set up. Therefore, the solution becomes one of optimization where the sixteen unknowns are varied until the differences between the measured S-parameters and the modeled S-parameters are minimized. This thesis uses the measured S-parameters from a MESFET power device to extract the equivalent circuit values of the device. A FORTRAN extraction code which fits a model to the measured S-parameters of this device is written for this thesis. Transformations from Y-parameters to S-parameters are made, and a Simplex Method optimizer is used to fit the modeled S-parameters to the measured S-parameters.

1.2 Problem To Be Solved

Based on the physical characteristics of a MESFET device, an equivalent circuit model of a MESFET device can be developed. In order to determine these equivalent circuit parameters, the designer measures the Scattering parameters or S-parameters of the device. The device is first DC biased, and then the magnitudes and phase of the scattered and reflected waves are measured with a network analyzer. There are four S-parameters total: S_{11}, the input reflection coefficient; S_{12}, the reverse isolation coefficient; S_{21}, the forward transmission coefficient or voltage gain; and S_{22} , the reverse reflection coefficient. Each S-parameter has a real part and an imaginary part. The S-parameters can be expressed in terms of the equivalent circuit parameters of the device. In the equivalent circuit model used for this thesis, there are eight equations and sixteen unknowns. This situation arises because there are more circuit elements than S-parameters. This problem is termed ill-conditioned, and it is solved with a Simplex optimizer. A cost function which represents the differences between the modeled S-parameters and the measured S-parameters is defined. The optimizer varies the equivalent circuit parameters until the cost function reaches a minimum. Because there are 8 equations and 16 unknowns, an infinite number of solutions exists.

Figure 1.1 represents a similar power MESFET to the one used in this thesis. The MESFET device is DC biased on the Gate and the Drain while the Source is grounded. The AC input signal is fed via the Gate, and the amplified signal is taken from the Drain. Running from the gate are eight fingers which are shown in dark on the drawing. The Source fingers are connected on the left, while the drain fingers are connected on the right. A dielectric isolates the Gate from the Source on the left side and allows an overlap. The dielectric layer is not shown in order to simplify the illustration. The actual device used has 56 Gate fingers, each with a width of 300 μm and a total gate periphery of 16.8 mm. The Gate pitch, or distance between the Gate fingers, is 15 μm. Gate, Source, and Drain, and the physical operation of the MESFET device will be explained in Chapter II.

1.3 Technical Approach

First, on-wafer S-parameter measurements of a MESFET device were made, and they basically probe the particular device(s) in bare form (die) surrounded by other circuitry. On-wafer measurements avoid the inclusion of packaging parasitics. Parasitics are unwanted resistances, capacitances, and inductances. Since the objective is the evaluation of the device operation, it is beneficial to obtain (or to have) the device in a die form rather than a packaged form.

The next step involves extracting an equivalent circuit model from the S-parameters data. A typical equivalent circuit model may have 16 or more elements. Each S-parameter may be expressed in terms of real and imaginary parts, so if one equates real and imaginary parts, there are basically 8 equations and effectively 16 unknowns. In choosing an equivalent circuit model, the designer tries to find physical realism for each component. However, as more components are added, the problem becomes more difficult to solve since there are still only 8 equations, and the designer will question the physical reality of the values of the components. For this thesis, a standard, well-understood small-signal equivalent circuit model was selected. Several matrix transformations are made in order to convert the equivalent circuit model to S-parameters. The Simplex Method minimizes the value of a cost function. After the cost function has been minimized, modeled S-parameters are then generated as a function of frequency. The data is then analyzed.

1.4 Technical Contributions

MFET, A FORTRAN code used for the extraction of an equivalent circuit model, was developed for this thesis. It contains 12 different FORTRAN modules. With this code, the Simplex Method was extensively analyzed. The Simplex Method requires n+1 points, where n is the dimension of the problem to be solved. First, the output equivalent circuit element values were allowed to be any number in sixteen dimensional space. This resulted in some of the output equivalent circuit values being negative which is not physical. Next, bounds were placed on the output equivalent circuit values in order for them to be physically reasonable. The Simplex was spread out over the space in order to

try to improve the fit of the modeled S-parameter values to the measured S-parameter values. Finally, to try to give the best curve fit, a narrowband model was used. The narrowband model picks a frequency range close to the operating frequency of the device. The narrowband model avoids high frequency resonances present in the measurements of S-parameters.

It was noticed that the Simplex was very sensitive to the value of the initial conditions. If one of the values of the Simplex were changed by 1%, the output values would change by more than 1%. This sensitivity issue is investigated in this thesis. The sensitivity to three different parameters is investigated; namely, C_{gs}, the internal Gate-Source capacitance; g_m, the gain parameter for the voltage controlled current source; and R_o, the output resistance. For each of these cases, the Simplex converges to similar cost function values, but gives different equivalent circuit values.

1.5 Thesis Organization

This document is organized into six chapters with this chapter, Chapter I, being the Introduction. Chapter II will provide the basic material to understand the physics of the operation of MESFET devices. Chapter III will describe biasing MESFET devices and introduce the reader to the small signal modeling process. Five different small signal models and their different attributes will be discussed. The reader will also be introduced to a large signal model in this chapter. Chapter IV will describe the methodology used to extract a small signal model for the MESFET device. Finally, Chapter V will describe the measurements taken and analyze the Simplex Method. Chapter VI, the Conclusion, will look at ways to improve the Simplex Method and the optimization process in general, for future efforts.

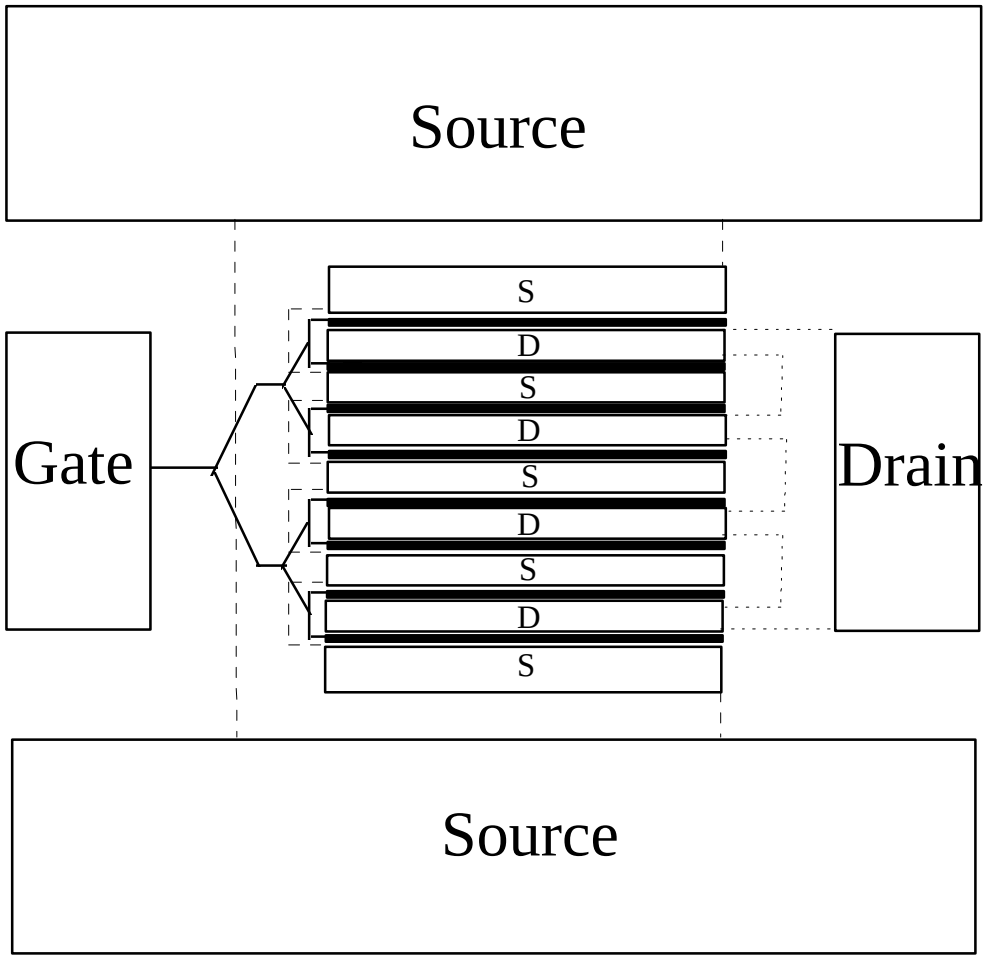

Figure 1.1: Power MESFET Device (Not To Scale) [1].

CHAPTER II. TECHNICAL BACKGROUND

2.1 Introduction

The purpose of this chapter is to give a brief explanation of the physics which describe Metal Semiconductor Field Effect Transistor (MESFET) operation. A Field Effect Transistor or FET is a three terminal electronic device consisting of a Source, Drain, and Gate. Charge carriers (electrons, which carry negative charge, or holes which carry positive charge) flow from the Source to the Drain via the channel. The channel is a doped region in the semiconductor and basically offers good conduction. The flow of carriers in the channel is controlled by the Gate which is either a reverse biased pn junction or a reverse biased Schottky diode. A MESFET device uses a Schottky diode as the Gate. In this Chapter, semiconductor physics will be summarized. Next, the Schottky diode concept will be described; finally, Poisson's equation will be solved to determine the width of the space charge region under the Gate region. An expression will be derived for current flowing in the channel of the MESFET device. Finally, a comparison between GaAs and Silicon materials available for MESFET realization for high frequency device operation will be made. Figure 2.1 shows the cross section of a MESFET device.

2.2 Semiconductor Physics

Electronically, three types of solid materials exist: insulators, metals, and semiconductors. Each type can be differentiated from the other by its bandgap value and the atomic number associated with the specific material. The bandgap is the energy difference between the valence band edge and the conduction band edge. Electrons in the valence band participate in bonding; electrons in the conduction band participate in conduction. The conduction band is at a higher energy level than the valence band. No electrons or holes are allowed to exist in the forbidden bandgap unless an energy level is created through the doping process of the material. An insulator will have its valence band filled, have no electrons in the conduction band, and have a large bandgap hard to surmount by carriers. In the metal case, the conduction band and valence band may overlap; or the conduction band may be partially filled with electrons. A semiconductor will have relatively few electrons in the conduction band, or relatively few holes (the absence of electrons) in the valence band. Also, the bandgap will be moderate compared to the insulator case, but certainly wider than the metal case. The bandgap is a function of temperature [4]:

$$E_g(T) = E_0 - \frac{\alpha T^2}{(T+\beta)} \tag{2.1}$$

Where

E_0 is the absolute value fo the energy bandgap ($= 1.519 eV$ for GaAs),

β is a curve fitting factor ($= 204 K$ for GaAs), and

α is also a curve fitting factor ($= 5.405 \times 10^{-4} eV / K$)

It is the ability to change the doping in semiconductors which radically alters the electronic properties of semiconductors. Figure 2.2 illustrates insulator, semiconductor and metal band diagrams. It is also important to mention that the semiconductors' properties can be altered by subjecting the material to optical excitation.

2.3 Doping Semiconductor Materials [2, 3, 8]

The doping process, the addition of impurities, alters the electronic characteristics of a semiconductor. Two types of doping may be achieved: negative, or n-type; and positive, or p-type. In an intrinsic or undoped semiconductor, all electrons are formed into bonds between neighboring atoms. In pentavalent material doping, an atom is introduced into the semiconductor so that when it bonds with the other atoms of the material, it will result in an extra electron. Silicon has a valence of four, indicating four electrons in the outermost shell. In a lattice, each Silicon atom will form covalent bonds with the four other Silicon atoms surrounding it. For Silicon, boron is a p-type donor because it has three valence electrons; arsenic is an n-type donor because it has five valence electrons. Gallium Arsenide is slightly different; the Gallium ions will be negative and surrounded by positive arsenic or vice versa. In p-type doping, an atom is introduced such that when it bonds with the other atoms in the material it does not have enough electrons to complete all the bonds. In order to adequately describe bonding in GaAs, Miller indices (hkl) numbers must be used to describe the different planes. In either case, the atom remains electrically neutral. An isotope of Silicon, Si^{29}, is an n-type donor for GaAs.

When donor atoms are added to the semiconductor, they create new energy levels near the conduction band. It does not take much energy for the donor atom to ionize and have its electron promoted to the conduction band. When the donor atom is ionized, it is positively charged. Acceptor atoms grab electrons from the valence band, creating holes. When the acceptor is ionized, it becomes negatively charged.

2.4 Mobility

Mobility describes how fast an electron moves under an applied electric field:

$$v = \mu E \tag{2.2}$$

Here,
v indicates the drift velocity,
μ is the carrier mobility,
and E is the applied electric field.
Equation (2.2) holds for Electric fields < 2000 V/cm in GaAs. Above this value, the velocity of electrons decreases. This occurs due to the scattering mechanism. Electrons in the conduction band are transferred from low energy regions of high mobility to high energy regions of low mobility instead of increasing their velocity. [3] Mobility for electrons in the conduction band is greater than for holes in the valence band since in the

conduction band the electrons are farther away from the lattice and are affected less by it. Figure 2.4 compares the carrier drift velocity of electrons in GaAs and Silicon.

2.5 Fermi Level

The Fermi level represents the energy at which the probability of finding an electron is 0.5. The probability of an electron occupying an allowed energy level is provided by the Fermi-Dirac distribution function, $F(E)$, given by,

$$F(E) = \frac{1}{1 + exp\left(\frac{E - E_F}{kT}\right)} \tag{2.3}$$

Where,

E_F is the Fermi level,
E is the energy in question,
k is Boltzmann's constant, and
T is the absolute temperature.

If donor atoms are introduced, the Fermi level rises above the middle of the bandgap because there are more electrons present in the conduction band. If acceptor atoms are introduced, the Fermi level decreases because there are more holes in the valence band which decreases the energy level.

2.6 Schottky Diode Concept [3]

A metal in contact with a semiconductor, each possessing the proper work functions, forms a rectifying contact called a Schottky Diode. This section will define all the energy levels in the Schottky Diode. The difference between the vacuum level and the Fermi energy is the work function; both the metal and the semiconductor have certain work functions. The vacuum level is the energy at which the electrons are no longer bound to the atom. Furthermore, the electron affinity is the difference between the conduction band edge of the semiconductor and the vacuum level. The barrier height is the difference between the metal work function and the electron affinity of the semiconductor. Figure 2.5 shows the energy levels in a Schottky Barrier before each side has been contacted. The metal is on the left side and the semiconductor is on the right side. The formula for the barrier height, expressed as ϕ_{Bn}, is given by

$$q\phi_{Bn} = q(\phi_m - \chi) \tag{2.4}$$

where

q is the electron charge,
ϕ_{Bn} is the barrier height,
ϕ_m is the metal work function, and
χ is the electron affinity of the semiconductor.

In an n-type material, the Fermi level of the semiconductor is greater than that of the metal; while in a p-type material the Fermi level of the semiconductor material is less than that of the metal. In the n-type material case, consider the metal and the semiconductor as not contacting each other. If a hypothetical wire is connected from the semiconductor to the metal, electrons will flow from the semiconductor to the metal; and the Fermi level will decrease in the semiconductor. Metal and semiconductor Fermi levels should now be the same. When the metal is placed in direct contact with the semiconductor, the Fermi levels are required to be the same at equilibrium, the vacuum level, the conduction band, and the valence band must be continuous. This will cause the conduction bands and the valence bands to bend upward or downward depending on whether the semiconductor is p-type or n-type, respectively. Note that the semiconductor is doped. Figure 2.6 illustrates a Schottky Barrier reaching the equilibrium condition.

Under no bias, the electron current from the metal balances the electron current from the semiconductor. When a forward bias is applied, the conduction band is raised closer to the vacuum level. Consequently, more electrons have enough energy to move across the barrier and into the metal. When a reverse bias is applied, the energy of the conduction band is lowered so that fewer electrons are able to cross the barrier. Tunneling currents will dominate in cases of high doping or low temperature. Figure 2.7 shows a Schottky Barrier under forward bias with the bands bent upward. Figure 2.8 shows a Schottky Barrier under reverse bias with the bands bent downward.

The current density for the Schottky barrier can be derived using thermionic emission theory. Thermionic emission calculates the number of electrons with enough energy to cross over the barrier. The total current J_T has the form,

$$J_T = \left[A^* T^2 \, exp\left(-\frac{q\phi_{Bn}}{kT} \right) \right] \left[exp\left(\frac{qV}{kT} \right) - 1 \right] \tag{2.5}$$

$$A^* = \frac{4\pi q m^* k^2}{h^3} \tag{2.6}$$

Where,

A^* is the effective Richardson's constant,
T is the absolute temperature,
k is Boltzmann's constant,
ϕ_{Bn} is the barrier height,
V is the applied voltage,
m^* is the effective mass of the electron, and
h is Planck's constant.

Note that the effective Richardson's constant, A^*, incorporates the effective mass of the electron, m^*.

2.7 Poisson's equation [5]

As a result of contacting the metal and semiconductor, a region of charge now exists in the semiconductor. The potential in this region, ψ, is derived using Poisson's equation, of the form,

$$\frac{d^2\psi}{dy^2} = -\frac{\rho}{\varepsilon} \tag{2.7}$$

The potential distribution is solved by integrating Poisson's equation twice and applying the appropriate boundary conditions:

$$\frac{d\psi}{dy} = -\frac{\rho}{\varepsilon} + C_1 \tag{2.8}$$

Note that equation (2.8) assumes that the charge density, ρ, is constant. This is a reasonable assumption if there is a uniform doping profile.

$$\psi(y) = -\frac{\rho}{2\varepsilon} + C_1 y + C_2 \tag{2.9}$$

The boundary condtions for the electric field must be reexpressed as boundary conditions for the potential ψ.

$$-\left.\frac{d\psi}{dy}\right|_{y=W} = 0 \tag{2.10}$$

Next:

$$\psi(0) - \psi(W) = -V_{bi} = \psi(0) - 0 \tag{2.11}$$

And so:

$$\psi(x) = \frac{-qN_D y^2}{2\varepsilon_s} + \frac{qN_D W y}{\varepsilon_s} - V_{bi} \tag{2.12}$$

Here,

q is the electric charge

N_D is the uniform background doping and has replaced ρ in equation (2.8)

$$V_{bi} = \frac{qN_D W^2}{2\varepsilon_s} \tag{2.13}$$

This equation can be modified to give a depletion width as the function of any applied voltage:

$$W = \sqrt{\frac{2\varepsilon_s (V_{bi} - V_a)}{qN_D}} \tag{2.14}$$

Where,

V_a is the applied voltage,

$V_a = V_f$ positive for forward bias applied, and

$V_a = -V_r$ negative for reverse bias applied.

Note that the built-in potential V_{bi} can be expressed in terms of the barrier height ϕ_{Bn} and the difference between the conduction band and the Fermi level location,

$$V_{bi} = \phi_{Bn} - V_n \tag{2.15}$$

Where,

$V_n = q(E_C - E_F)$,

E_C is the energy at the bottom of the conduction band, and

E_F is the Fermi energy.

2.8 Derivation Of Current -Voltage Characteristics

This section will present the derivation of two different models which describe the current-voltage characteristics of a MESFET device. First, the Schockley [3] derivation is discussed. This uses the gradual channel approximation to simplify the two dimensional Poisson's equation. The Liechti [9] model is also discussed. This model predicts the formation of a dipole in the channel when the current saturates.

2.8.1 Analysis For Schockley Derivation [3]

Recall that the MESFET is a three terminal device. Two terminals will be used to apply voltages: the Gate and the Drain. The Gate is under reverse bias, and a depletion region exists under it. Starting with the two-dimensional Poisson's equation,

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{\rho}{\varepsilon}, \tag{2.16}$$

We assume that the potential along the length of the channel varies only slightly. Thus, the following approximation can be made:

$$\frac{\partial^2 \psi}{\partial x^2} \approx 0 \tag{2.17}$$

Now, the problem is simplified to that of one dimension so that:

$$-\frac{d^2 \psi}{dy^2} = \frac{dE_y}{dy} = \frac{\rho}{\varepsilon} \tag{2.18}$$

This gradual channel approximation is valid for long channel devices. For long channel devices the length is typically 1 μm or greater.

Consider a MESFET device structure such as that in Figure 2.10. The depletion width can be determined at the Drain, x_2, and at the Source, x_1. The depletion width at each end is of the form

$$w(x_2) = \sqrt{\frac{2\varepsilon_s (V_D + |V_G| + V_{bi})}{qN_D}}, \qquad \text{at the Drain Site} \tag{2.19}$$

$$w(x_1) = \sqrt{\frac{2\varepsilon_s (|V_G| + V_{bi})}{qN_D}}, \qquad \text{at the Source Site} \tag{2.20}$$

Here,

ε_s is the permittivity of the semiconductor,
V_D is the applied Drain voltage,
$|V_G|$ is the applied Gate voltage,
V_{bi} is the built in voltage,
q is the electron charge, and
N_D is the doping of the semiconductor.

For a MESFET which has a total channel depth of d, the channel is described as being pinched off when the depletion width equals the channel depth,

$$w(x_2) = d \tag{2.21}$$

When this occurs, the total voltage is called the pinch-off voltage, V_P. V_P is determined by substituting d in equation (2.19) and representing $V_D + |V_G| + V_{bi}$ as V_P. V_P the takes the form,

$$V_p = \frac{qN_D d^2}{2\varepsilon_s} \tag{2.22}$$

Now consider a cross section along the width of the MESFET device. The current flowing through the cross section will be calculated using Ohm's law,

$$J = \sigma(x)\mathrm{E}_x \tag{2.23}$$

The channel conductance, $\sigma(x)$, is expressed as,

$$\sigma(x) = qN_D\mu \tag{2.24}$$

where,
N_D is the doping in the channel,
q is the electron charge,
d is the total channel depth, and
μ_n is the electron mobility.

The cross sectional area of the channel available for conduction is:

$$A = (d - w)Z \tag{2.25}$$

where,
d is the total channel depth,
w is the width of the depletion region, and
Z is the gate width.

The current density in (2.22) can be changed into a current by multiplying by the cross sectional area:

$$I_D = qN_D\mu_n\left(\frac{dV}{dx}\right)(d - w)Z \tag{2.26}$$

The depletion width can be written as a function of x in which the voltage from the Drain to the Source is dependent on x,

$$w(x) = \sqrt{\frac{2\varepsilon_s\left(V(x) + |V_G| + V_{bi}\right)}{qN_D}} \tag{2.27}$$

From this relation the following differential relation may be obtained,

$$dV = \frac{qN_D}{\varepsilon_s} w\,dw \tag{2.28}$$

Finally, an expression for I_D can be determined by subtituting into equation (2.26) and integrating, specifically,

$$I_D = \frac{1}{L}\int_{w_1}^{w_2} 2q\mu_n N_D Z(d-w)\frac{qN_D}{\varepsilon_s} w\,dw \tag{2.29}$$

where

L is the length of the gate. It should be noted that in MESFET devices the length is defined as the direction of current flow.

Integrating equation (2.29) results in the following expression,

$$I_D = \frac{Z\mu q^2 N_D^2 d^3}{6\varepsilon_s L}\left[\frac{3}{d^2}\left(w_2^2 - w_1^2\right) - \frac{2}{d^3}\left(w_2^3 - w_1^3\right)\right] \tag{2.30}$$

I_P is the pinch-off current which occurs when the MESFET device reaches the pinch-off voltage, V_P,

$$I_P \equiv \frac{Z\mu_n q^2 N_D^2 d^3}{6\varepsilon_s L} \tag{2.31}$$

Equation (2.30) is expressed in terms of the applied voltage at the Drain, $V(x)$, the applied voltage on the Gate, $|V_G|$, and the built-in potential, V_{bi}, by defining depleion widths normalized to the channel depth, d. u is the normalized depletion width at any place in the channel; u_1 is the normalize depletion width at the Source end of the channel; u_2 is the normalized depletion width at the Drain end of the channel.

$$u \equiv \frac{w}{d} = \left[\frac{V(x) + |V_G| + V_{bi}}{V_p}\right]^{1/2} \tag{2.32}$$

$$u_1 \equiv \frac{w_1}{d} = \left[\frac{\left(|V_G| + V_{bi}\right)}{V_P}\right]^{1/2} \tag{2.33}$$

$$u_2 \equiv \frac{w_2}{d} = \left[\frac{V_D + |V_G| + V_{bi}}{V_P}\right]^{1/2} \tag{2.34}$$

$$I_D = I_P\left[\frac{V_D}{V_P} - \frac{2}{3}\left(\frac{V_D + |V_G| + V_{bi}}{V_P}\right)^{3/2} + \frac{2}{3}\left(\frac{|V_G| + V_{bi}}{V_P}\right)^{3/2}\right] \tag{2.35}$$

and

V_p as defined before.

Equation (2.35) now expresses the Drain current in terms of the applied Drain voltage, the applied Gate voltage, the built-in potential, and the pinch-off voltage. The linear region of the MESFET device current-voltage characteristic is where the Drain current varies approximately linearly with the Drain voltage. The binomial approximation can be used to

derive an expression for the current in the linear region, provided that: $V_D << |V_G| + V_{bi}$. So,

$$I_D \cong \frac{I_P}{V_P}\left[1 - \sqrt{\frac{|V_G| + V_{bi}}{V_P}}\right]V_D \tag{2.36}$$

In this equation, V_G , I_p , V_P , V_{bi} are constant; I_D is a linear function of V_D.

The saturation region of the MESFET device occurs when the depletion region pinches off. After reaching pinch-off, increasing the Drain bias does not result in an increase in the Drain current for a constant Gate bias. The current in the saturation region is found by evaluating the current at

$$V_P = V_D + |V_G| + V_{bi} \tag{2.37}$$

This results in a current I_{Dsat} of the form

$$I_{Dsat} = I_P\left[\frac{1}{3} - \left(\frac{|V_G| + V_{bi}}{V_P}\right) + \frac{2}{3}\left(\frac{|V_G| + V_{bi}}{V_P}\right)^{3/2}\right] \tag{2.38}$$

Figure 2.11 illustrates the linear and saturation regions of the MESFET device.

After the Drain current reaches saturation, it remains constant as the Drain voltage increases until a phenomenon called Avalanche Breakdown occurs. The increasing Drain voltage increases the energy of the electrons. These electrons collide with the semicondutor lattice. The semiconductor lattice consists of the atoms of the semiconductor and its dopant joined by electron bonds. The energetic electrons collide with the electron bonds which frees electron-hole pairs. These electron-hole pairs collide with the lattice and create more electron-hole pairs. The Drain current then increases very rapidly with the Drain voltage.

Section 2.8.1.1 Transconductance [3]

The ratio of the change in the output current to the change in the Gate voltage is called the transconductance and is an important figure of merit to evaluate the MESFET device performance. The transconductance of the MESFET device, g_m, is a measure of its gain and is expressed as:

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D = constant} \tag{2.39}$$

Where,

g_m is the transconductance,

I_D is the drain current,

V_D is the drain voltage (held constant), and

V_G is the Gate voltage

2.8.1.2 Capacitance [2]

The depletion region under the Gate stores charge and acts as a capacitor. The capacitance of this region is important for MESFET device modeling. The capacitance under the Gate is primarily associated with the Gate-Source contacts. In deriving an expression for this, the space charge per unit area is considered:

$$Q_{SC} = qN_D W = \sqrt{2q\varepsilon_s N_D \left(V_{bi} + |V_G| + V_D\right)} \tag{2.31}$$

Here,

q is the electron charge,
ε_s is the permittivity of the semiconductor,
N_D is the channel doping,
V_{bi} is the built-in voltage,
$|V_G|$ is the applied Gate bias, and
V_D is the applied Drain bias.

Now, the capacitance, C, is defined as

$$C = \left|\frac{\partial Q_{SC}}{\partial V}\right| = \sqrt{\frac{q\varepsilon_s N_D}{2\left(V_{bi} + |V_G| + V_D\right)}} = \frac{\varepsilon_s}{w}, \tag{2.32}$$

where all the parameters have been defined above except for w which is the depletion width.

2.8.2 Liechti Model [9]

The Liechti Model explains the Drain current saturation phenomenon occuring in MESFET devices. The derivation of this model begins with an expression for the current, I_D, in the channel. I_D is of the form

$$I_D = Zqn(x)\mathrm{v}(x)y(x) \tag{2.39}$$

where,

Z is the Gate width,
q is the electron charge,
$n(x)$ is the doping in the channel,
$\mathrm{v}(x)$ is the velocity of the carriers (electrons), and
$y(x)$ is the undepleted channel width.

The Gate is biased and the Drain voltage is gradually increased. The depletion width is now widest near the Drain since this is where the potential is greatest. As E increases, $\mathrm{v}(x)$ increases, and consequently, I_D increases. When the electric field reaches the critical field, the velocity saturates and no longer increases. Note that this will happen toward the Drain end of the device. The velocity is saturated, and the undepleted channel width is very narrow. According to the model, a constant current is maintained by introducing

more negative charge in this channel region. In order to compensate this negative charge, positive charge forms closest to the gate. These negative and positive charges form a dipole layer. Figure 2.12 shows a cross section of a MESFET device illusrating the Liechti Model with a dipole layer of positive and negative charges.

2.9 GaAs Versus Silicon [8]

GaAs MESFET devices have replaced vacuum tubes devices at microwave frequencies and higher. GaAs MESFET devices have succeeded where Silicon has failed. This section addresses the performance of the binary compound GaAs as compared to the elemental semiconductor material Silicon, and constrasts the differences between them. First, GaAs has a higher electron mobility than Silicon. This means that under an applied electric field, more amplification will be obtained from the GaAs device. Also, because of its higher mobility, GaAs electrons will have a shorter transit time in structures made of GaAs. This affects high frequency operation, because after the current is modulated it should exit the device before the next modulation occurs. GaAs has a higher resistivity than Silicon. This means that in monolithic microwave integrated circuits (MMIC), devices can be effectively isolated from each other. GaAs has a lower dielectric constant and consequently has lower device capacitance than Silicon. In addition, GaAs is more radiation hardened. On the other hand, GaAs does have some drawbacks. Because no native oxide exists for GaAs, metal oxide semiconductor FETs cannot be made. This limits the voltages that can be applied to the Gate. Also, GaAs has lower thermal conductance which means it absorbs heat which has deleterious effects on device performance. Table 2.1 gives a comparison between GaAs and Silicon.

2.10 Conclusion

Chapter II provided the technical background necessary to understand MESFET device operation. The MESFET device consists of a Schottky diode placed on a doped semiconductor material. The MESFET device has three contacts: the Gate, the Drain, and the Source. Voltages are typically applied on the Gate and the Source. The Shockley Model and the Liechti Model were introduced to describe semiconductor current voltage characteristics. The Shockly Model uses a gradual channel approximation to simplify Poisson's equation while a dipole layer is predicted in channel with the Liechti Model. An expression for the transconductance, g_m, of the MESFET device is introduced. Furthermore, the Gate-Source capacitance was determined. Chapter III, Small-Signal Equivalent Circuit Models, will describe the physical characteristics of the MESFET device which have been elaborated on in Chapter II in terms of equivalent circuit parameters such as resistances, capacitances, inductances, and voltage controlled current sources.

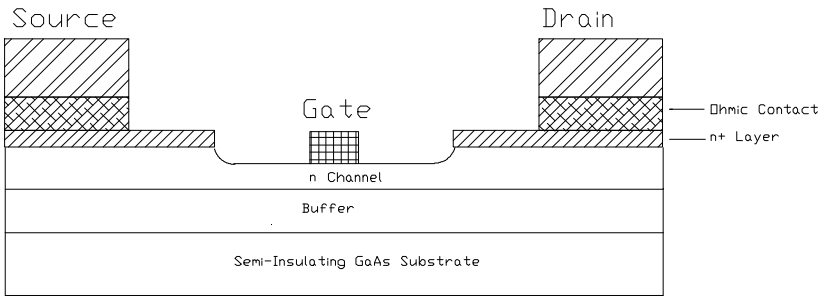

Figure 2.1: MESFET Device Cross Section [8].

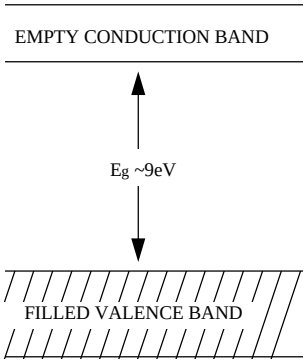

Figure 2.2a: Insulator Band Diagram [2].

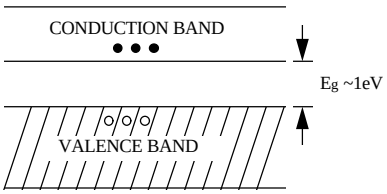

Figure 2.2b: Semiconductor Band Diagram [2].

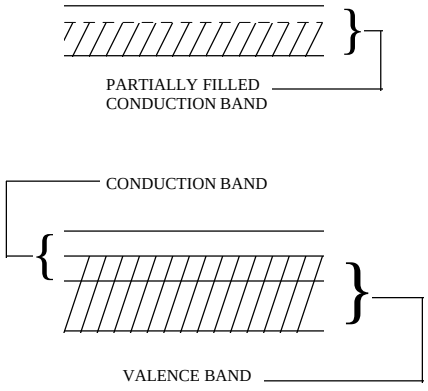

Figure 2.2c: Metal Band Diagram [2].

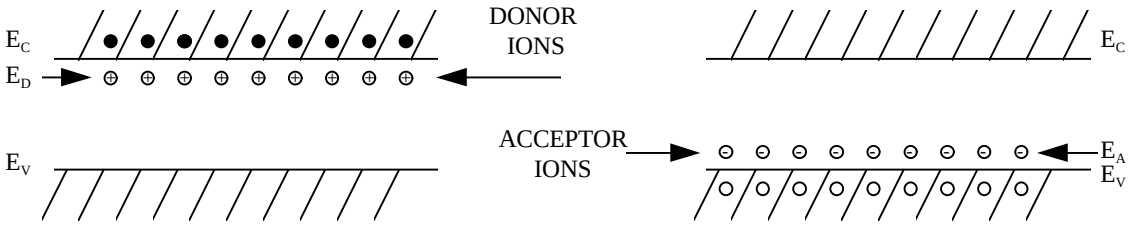

Figure 2.3: Doped Semiconductors, (a) Case Of n-type, (b) Case Of p-type [2].

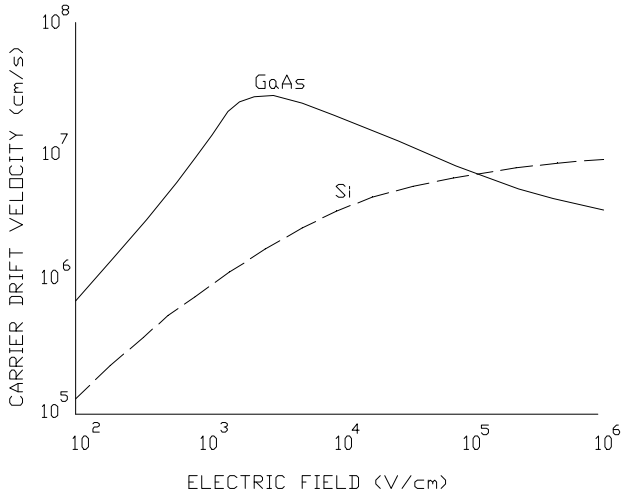

Figure 2.4: Carrier Drift Velocity Of Electrons In GaAs And Silicon [3].

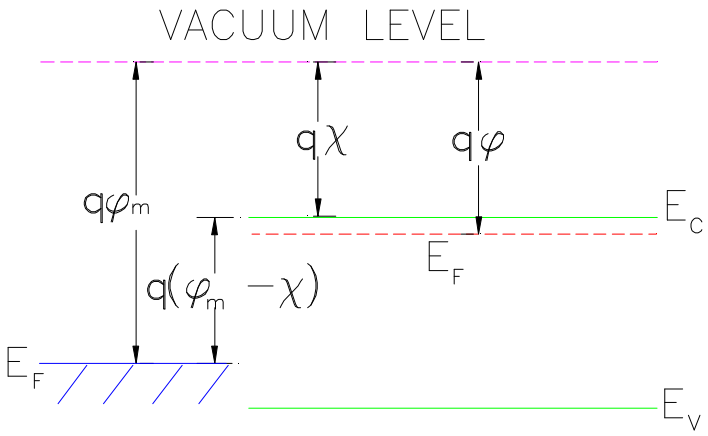

Figure 2.5: Schottky Barrier Energy Levels [3].

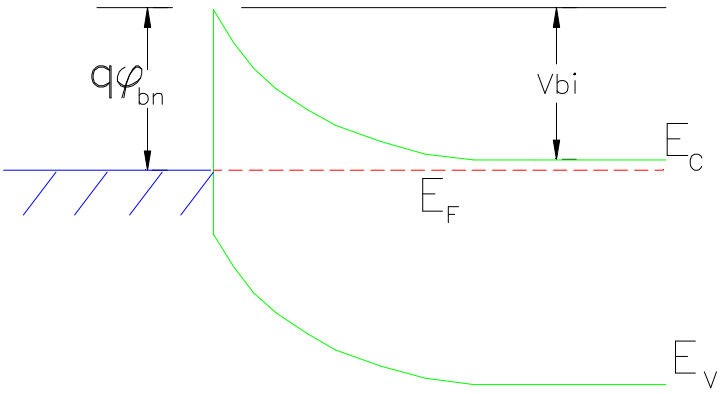

Figure 2.6: Schottky Barrier In Equilibrium [3].

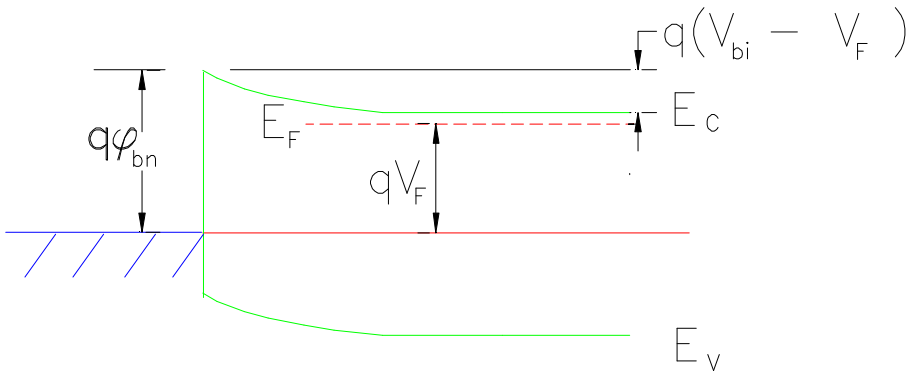

Figure 2.7: Schottky Diode Under Forward Bias [3].

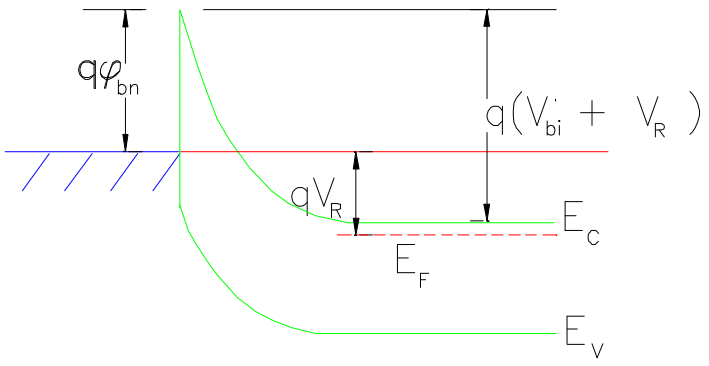

Figure 2.8: Schottky Diode Under Reverse Bias [3]

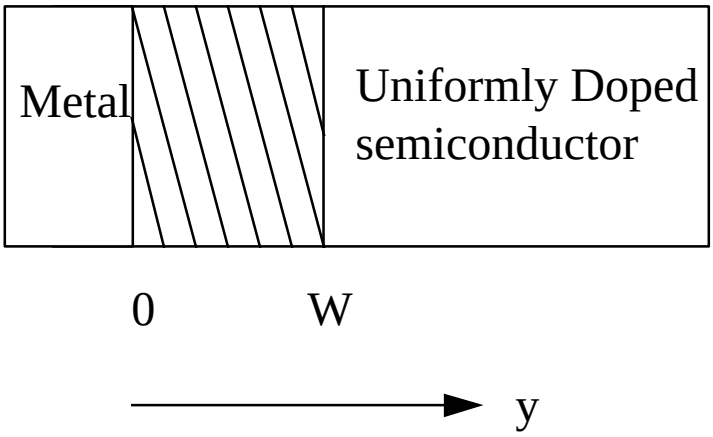

Figure 2.9: Geometry For Poisson's Equation [5].

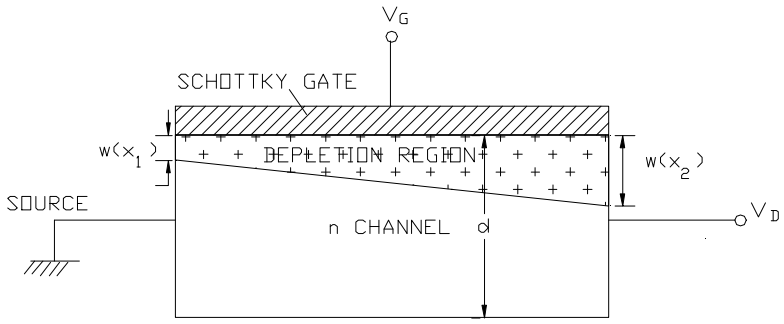

Figure 2.10: MESFET Device Structure With Depletion Region [3].

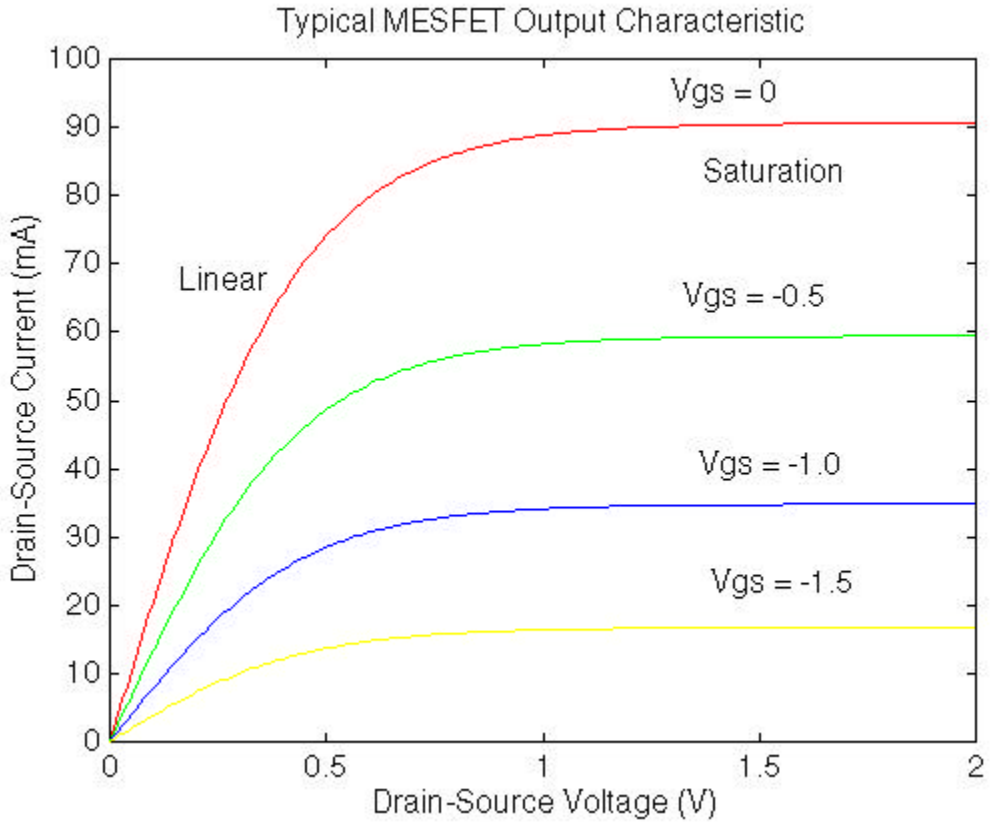

Figure 2.11: MESFET Device Output Characteristic [7].

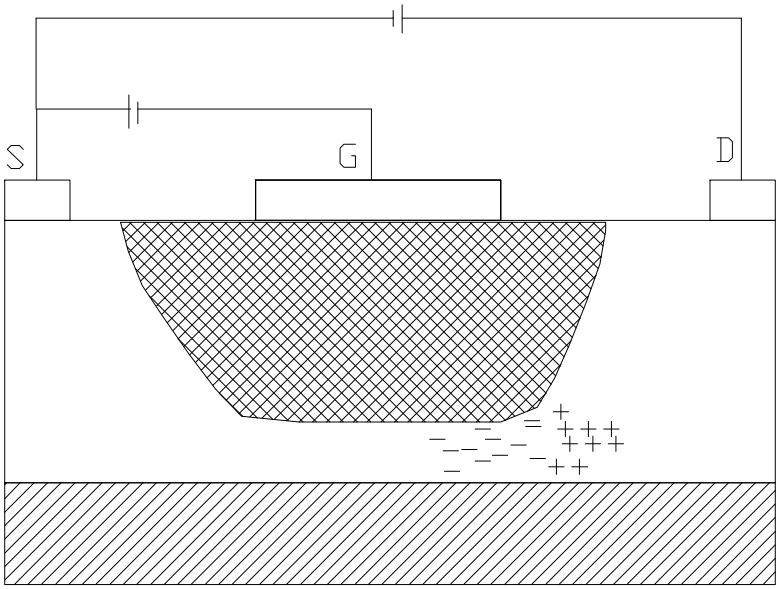

Figure 2.12: MESFET Device Cross Section For Liechti Model [9].

Table 2.1: Comparison of GaAs Versus Silicon [8].

Property	**GaAs**	**Silicon**
Semi-insulating	Yes	No
Resistivity (Ω-cm)	10^7 - 10^9	10^3 - 10^5
Dielectric constant	12.9	11.7
Electronic Mobility ($cm^2/(Vs)$)	4300	700
Saturation Velocity (cm/s)	1.3 x 10^7	9 x 10^6
Radiation Hardness	Very Good	Poor
Density (g/cm^3)	5.3	3.9
Thermal Conductivity (W/(cm °C))	0.46	1.45
Operating Temperature (°C)	350	250
Ease of Handling	Good	Very Good

CHAPTER III. SMALL SIGNAL MODELS

3.1 Introduction And Background [6]

This chapter discusses the physical significance of equivalent circuit models of MESFETs. Equivalent circuit models apply a circuit element to a physical attribute of the device such as a capacitor representing the capacitance of the depletion region under the Gate, a resistor representing the output resistance of the channel, or an inductor representing the parasitic lead inductance of the metallization running to the device. Equivalent circuit modeling requires no information about the doping of the device. Equivalent circuit models are classified into two types: large signal and small signal models.

Small signal models describe the transistor operation in the saturation region. In this region, a small Gate-Source voltage will produce a linear change in the Drain-Source current. At a certain point, if the Gate-Source voltage is allowed to increase, the Drain-Source current change is no longer linear and the small signal model no longer applies. Small signal models set the bias of the transistor and assume that none of the circuit elements vary with the voltage nor with the frequency. Thus, it is a task of biasing the transistor, measuring the S-parameters over a certain frequency range, and extracting the electrical equivalent circuit model to represent the device.

Large signal models require information at multiple bias points, therefore determining the bias dependency of the circuit elements. The designer may need to incorporate frequency dependence. Data from multiple bias points are extracted; empirical or physical expressions as functions of voltage are developed for the capacitances, the resistances, and the inductances. Also, an expression for the Drain-Source current is derived; this may be a two-piece linear approximation, or similarly, a hyperbolic tangent function. The scope of this thesis will be limited to small signal models.

A distinction needs to be made between lumped circuit models and distributed circuit models. In a lumped circuit model, the element is very much smaller than the wavelength of interest; while in a distributed circuit model, the element is on the order of the wavelength. Distributed elements will cause changes in the phase of the voltage waveform. This thesis will consider only lumped circuit models. When the element is large enough to be distributed, a lumped circuit equivalent representation is used, that is if the circuit element is distributed, its value is represented as a lumped circuit element.

In this chapter, the biasing of the device will be discussed first. Next, the most general small signal model is discussed followed by a simplification of it. The General model includes the intrinsic device along with parasitic inductances capacitances and resistances. Next, the Liechti model, which is useful for short channel devices since it includes a channel capacitor to model current saturation, is discussed. A slightly different model describing parasitic effects will be briefly examined. A ten element model which tries to eliminate uncertainty in the equivalent circuit values of the device will also be introduced.

3.2 Biasing The MESFET Device

There are three different biasing configurations for the MESFET device: Common-Source, Common-Drain, and Common-Gate configurations. Figure 3.1 shows these different configurations. This thesis will examine Common-Source equivalent circuit models. Common-Source configurations are most often used in amplifier design. In the Common-Source configuration, the MESFET is first DC biased so that the device is in saturation and the quiescent point (or Q-point) is well away from the pinch-off region. The Drain-Source DC bias will set the current flowing from the Drain to the Source, while the Gate-Source DC bias will set the Gate depletion width and determine the resistance of the undepleted channel. The total DC bias will set all the other circuit parameters to be discussed later in this chapter. A sinusoidal signal is applied so that the transistor will not move out of saturation as the sinusoidal signal changes from positive to negative. The AC operation of the device is then considered. Figure 3.2a illustrates the circuit diagram for the Common-Source biasing of the MESFET Device; it shows the DC bias on the Gate and Drain and an AC signal being input at the Gate. Figure 3.2b illustrates the corresponding Current-Voltage characteristics of the MESFET Device under Common-Source bias and shows a sinusoidal voltage being applied at the Q-point which is in the saturation region. The next five sections will discuss models for the Common-Source configuration of the MESFET device.

3.3 General Model

The General model, represented in Figure 3.3, is the most widely used model [10, 12, 17]. The parasitic inductance elements of the Source, Gate, and Drain metallizations were added in the mid-70's [11]. Figure 3.3 illustrates the physical meaning of each parameter incorporated in this General model. In this equivalent circuit, C_{gs} is the capacitance due to the space charge region between the Gate and the Source, C_{ds} is the capacitance of the substrate between the Drain and the Source. Sometimes, models place this capacitance as being between the Drain and Ground. C_{dg} is the capacitance between the Drain and the Gate. C_{ds} and C_{dg} are primarily due to the fringing fields of the electrodes and are considered to be parasitic. R_o is the output resistance of the channel and R_i is the charging resistance. When the depletion width under the Gate changes as a sinusoidal voltage is applied, the voltage on the Gate swings from positive to negative. When the reverse bias is increased as a result of this sinusoidal voltage, atoms in the undepleted part of the channel must be depleted of their donor electrons. When the the reverse bias decreases, electrons recombine with the depleted atoms. The charging resistance, R_i, models these effects. The channel is charged and discharged by the changing Gate bias. It is important to note that since the Drain to Source bias is set and no sinusoidal voltage is applied there, there is no charging resistance associated with the Drain. $g_m \exp(-j\omega\tau)$ is the voltage controlled current source and is dependent on the voltage on C_{gs}. When one considers the high frequency operation of the device, as C_{gs}

shorts the voltage across it becomes zero, and consequently the output of the current-controlled current source decreases to zero. g_m is the gain parameter of the MESFET device. Also, this component models a delay time, τ, which represents the time it takes the depletion width to respond to a change in voltage on the Gate. This was added by Walter Curtice [6]. R_g, R_d, R_s represent parasitic resistances which are associated with the contacts on the device. These resistive elements do not very with frequency. L_g, L_d, L_s represent parasitic inductances associated with the contacts. Finally, C_{gsext}, C_{dsezxt}, C_{gdext} represent external parasitic capacitances between the contacts. Figure 3.4 shows this widely used model in circuit form.

For analysis purposes, the device is divided into two sections: the intrinsic device and the extrinsic device. The intrinsic device consists of the Schottky Diode, and the doped semiconductor which makes up the channel. The extrinsic device adds the parasitic elements which are associated with the leads and contacts to the device. As a simplification of the General model, the external parasitic capacitances may be neglected.

In the device, there are several feedback paths. One path is via the Drain-Gate capacitor. Another path is via the parasitic Source impedance. Each path returns a portion of the output to the input. Feedback negatively interferes with the Gate-Source signal which is the signal being amplified. Vendelin [11] indicates a negative interference and a reduction in gain due to the feedback, and he has reported that the feedback inductance increases the stability of the MESFET device below 8 GHz, but decreases it above 8 GHz. The external parasitic capacitances provide bypass routes as their impedance decreases. This has the unwanted effect of taking part of the Gate-Source signal away from the device. These are typically the smallest capacitances in the device, being on the order of hundredths of pF.

Results have been reported by Arnold, Golio, Miller, and Beckwith [17] for a Triquint 0.5 μm by 300 μm (length by width, length is defined as the direction of current flow) MMIC device. Since the equivalent circuit values will vary with frequency and bias, a frequency range over which an equivalent circuit is valid and a bias point for the MESFET device are reported. A frequency range from 1 GHz to 18 GHz was used at a bias point of V_{ds}=3V and V_{gs}=-0.8V. The General Model was used without the parasitic capacitances. Extracting an equivalent circuit involves applying a technique to determine the circuit values. Some researchers rely on measurements and approximations, while other use optimization to find the best circuit. Arnold, Golio, Miller, and Beckwith have measured the parasitic resistances under forward bias of the MESFET device. Under forward bias of the MESFET device the Schottky diode becomes a short circuit and the bypasses C_{gs}. In the MESFET device, there is also a diode between the Drain and the Gate. Forward bias of this diode bypasses C_{ds}. Bypassing these diodes allows the parasitic resistances to be measured. Arnold, Golio, Beckwith, and Miller also make a low frequency approximation to determine the intrinsic device parameters from Scattering parameters (or S-parameters). The parasitic inductances are used to fit the errors between the measured and modeled S-parameters. Extraction techniques will be thoroughly elaborated on in Chapter IV.

The smallest capacitance in these results is the Gate-Drain capacitance, C_{gd} followed by the Drain-Source capacitance, C_{ds}, with the largest capacitance being the depletion region under the gate, C_{gs}. These capacitances are on the order of hundredths of pF, tenths of pF, and several tenths of pF, respectively. These results are expected because C_{ds} and C_{gd} are considered to be parasitic.

The parasitic resistances are the smallest resistances, nominally being on the order of a few ohms. In this case the charging resistance, R_i, was omitted since it was found to be very noisy because its value varied greatly with frequency. The largest resistance is the output resistance being on the order of several hundred ohms.

Special attention should be given to the parasitic inductances. In Table 3.1, L_d has been set to zero. This is a result of the extraction proceedure.

3.4 Simplification of General Model [13]

The second model discussed in this chapter represents a simplification of the model discussed in the previous section. The model has two simplifications: (1) the impedance between the Drain and the Gate is assumed to be infinite; and (2) the parasitic resistances and inductances are neglected. The assumption that the impedance between the Gate and the Drain is infinite is due to the fact that C_{gd} is very much smaller than than C_{gs}, and at low frequencies this impedance can be considered to be infinite. Also, the parasitic inductances may be neglected at low frequencies. The parasitic resistances are considered to be the smallest resistances in the circuit, thus they are removed for simplicity. This model is used to provide an analysis of MESFETs since it lacks a lot of circuit elements. Other versions of this model include the addition of a capacitor from the Gate to the voltage controlled current source.

3.5 Liechti Model [9]

Recall from Section 2.8.2 that in short channel MESFETs, the current saturates and a dipole layer is formed in the channel of the MESFET device. The Liechti model includes this dipole layer as a capacitor in small signal model. This model is shown in circuit form in Figure 3.6. Note the presence of the dipole layer capacitor, C_{dc}, from C_{dg} to the negative end of C_{gs}. The output resistance of Liechti's model is labeled R_{ds} instead of R_o as in the general model. Although lacking the external parasitic capacitances and the parasitic inductances, the Liechti model is very similar to the General Model of Section 3.3. Table 3.2 presents values from a 1 μm x 500 μm device; V_{DS}=5V, V_{GS}=0V. Equivalent circuit models are typically extracted over a certain frequency range. Liechti does not indicate over which frequency range this model is valid, nor does he report an extraction method. The inductances reported in Table 3.2 are the contacting inductances of a test fixture used to make the measurements and not the inductances of the metallization running to the device as in the General Model. Note that the value of the channel dipole capacitance, C_{dc}, is smaller than the Drain-Source capacitance, C_{ds}, but

bigger than the Gate-Drain capacitance, C_{dg} . As with the General model results reported by Arnold *et al*, the Gate-Source capacitance, C_{gs}, is the largest capacitance. The value of the output resistance is very similar to the General Model results. Similarly, the parasitic resistances are on the order of a few ohms, and the delay time is on the order of a few picoseconds. The value of the voltage controlled current source is also nearly the same in both cases, being close to 50mS.

3.6 Dambrine Parasitics Model [15]

This model is very similar to the ones discussed previously; however, it arranges the parasitics differently. The parasitic elements in this device are L_g , L_d , L_s, R_g , R_s, R_d , C_{pg} , and C_{pd} . This model differs in that the parasitic capacitances are placed between the parasitic Gate resistor and parasitic Gate inductor, and between the parasitic Drain inductor and the parasitic Drain resistor. Also, the parasitic Gate-Drain capacitor has been omitted. In the MESFET the Gate is close to the Drain; therefore, it seems logical that a Gate-Drain parasitic capacitance should be included. This model does include a delay time on the voltage-controlled current source which affects how rapidly the depletion width under the Gate responds to changes in bias.

3.7 Gate-Source Resistor [18]

Figure 3-8 shows a circuit diagram of this model. Although this model is very similar to the General Model, it tries to better match the impedance under the gate with a resistor, R_{gs}, in parallel with the capacitor, C_{gs} . This model does include the delay time, but does not have the parasitic Drain inductance of the General Model, or the parasitic resistances of the General Model. The charging resistance, R_i, can be considered to include two parasitic resistances, R_s and R_g. Also the transconductance of this circuit, g_m, is the actually the following,

$$g_m = \frac{g_m^*}{1 + g_m^* R_s} \tag{3.1}$$

Where,

g_m^* is the transconductance of the General model, and

R_s is the parasitic resistance of the General model

The Drain parasitic resistor, R_D, may have been small enough to have been neglected in this model or it may have been omitted to keep the number of circuit elements at a minimum. The output resistance of the channel, labeled R_{ds} in this model, may include some of the parasitic Drain resistance in this model.

The data presented in Table 3-3 is for a low noise MESFET with 0.5 μm gate length; the bias is at V_{DS}=3V, I_D=10mA; the frequency range is from 2-18 GHz. Notice that R_{gs} is on the order of 1kΩ. Since it is the largest value of resistance, it could have

been neglected, and an open circuit substituted. The other values are very similar to those reported for the General Model and the Liechti Model. Note that the parasitic inductances are reported in pH instead of nH. This data was optimized, but the exact optimization method is not given. Optimization involves varying the equivalent circuit parameters to fit a set of modeled S-parameters to measured S-parameters. For each of the four S-parameters, there is a real and imaginary part. This gives eight equations for the ten equivalent circuit parameters of this model instead of the sixteen equivalent circuit parameters of the General Model. Each circuit element is an unknown; too many circuit elements create much uncertainty in their final values. The ten equivalent circuit parameter model avoids uncertainty in the final values of the equivalent circuit by keeping the number of equivalent circuit elements close to the number of equations.

3.8 Conclusion

While Chapter II introduced the physics behind MESFET devices, Chapter III represented the physical elements of the device as circuit elements. The emphasis in Chapter III was on small signal models. In the saturation region, a linear change in the Gate-Source voltage will produce a linear change in the Drain current. The advantage of small-signal modeling is that the designer does not need to incorporate a bias dependence on any of the circuit elements.

There are different bias configurations of the MESFET device: Common-Source, Common-Gate, and Common-Drain. This Chapter focuses on five different Common-Source models. Each small signal model can be divided into two parts: an intrinsic part and an extrinsic part. The intrinsic part considers the internal part of the device which consists of the Schottky diode (including the Gate), the channel, the Source, and the Drain; that is, the device without the metallization contacting it. The extrinsic part includes the metallization. Dividing the device into two parts will make the extraction methodology of Chapter IV easier. The models introduced in this Chapter share similar elements; they all include the voltage controlled current source, the Gate-Source capacitor, the Drain-Source Capacitor, the output resistance of the channel, and the charging resistance. The General model is widely used; it has well-understood circuit elements. A simplification of this model was introduced; it offers a basic understanding of a MESFET device. The Liechti model introduces a capacitor to model saturation in short channel MESFETs. According to Liechti's model, when the current saturates a dipole is formed in the channel. The Dambrine model was introduced. This model places the parasitic capacitances in slightly different places than the General model. One drawback of equivalent circuit models is that too many elements causes uncertainty in their values. In order to reduce the uncertaintly some researchers, such as Vaitkus [18], use circuit models with fewer elements. His model does include a resisor in parallel with the Gate-Source capacitor.

This thesis will use the General model. Chapter IV describes an equivalent circuit extraction proceedure for the General model in which matrix transformations from Y-parameters to Z-parameters then back to Y-parameters and finally to S-parameters are

done. Then, a Simplex Method optimizer is used to determine the equivalent circuit for the MESFET device.

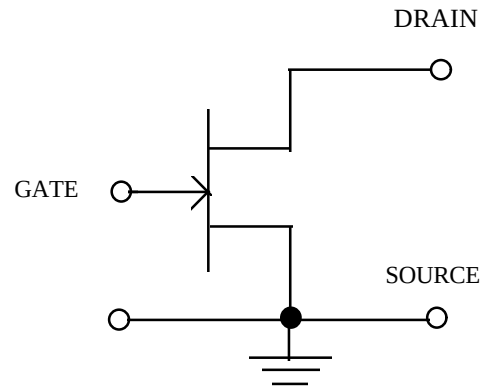

Figure 3.1a: Common-Source Configuration [14].

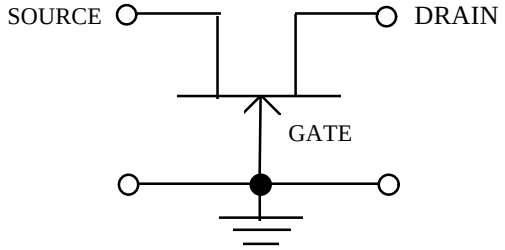

Figure 3.1b: Common-Gate Configuration [14].

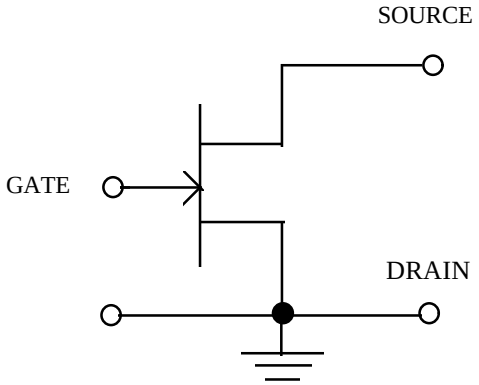

Figure 3.1c: Common-Drain Configuration [14].

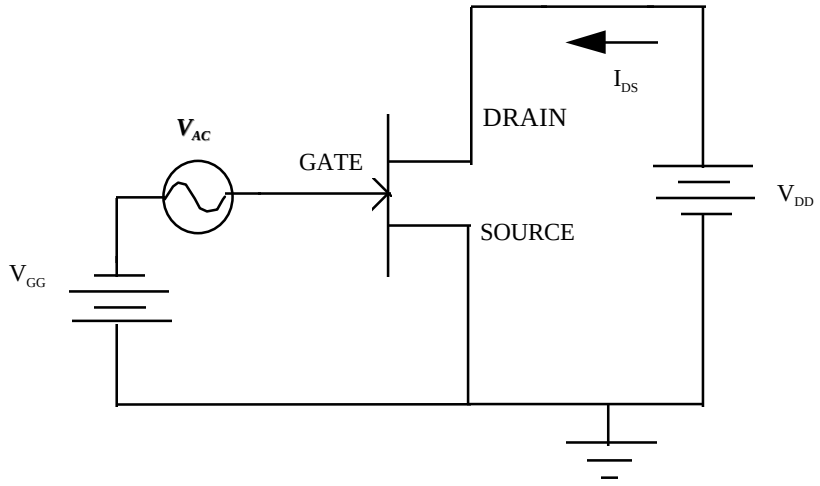

Figure 3.2a: Common-Source Bias.

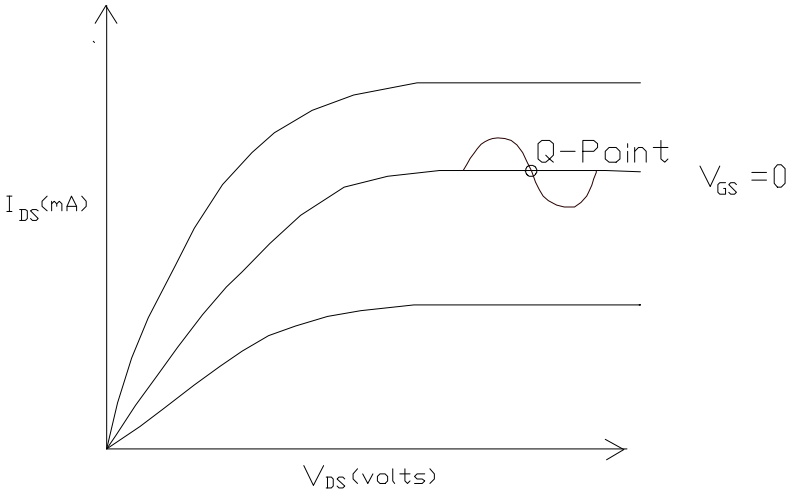

Figure 3.2b: Small-Signal Voltage Applied to FET in Saturation.

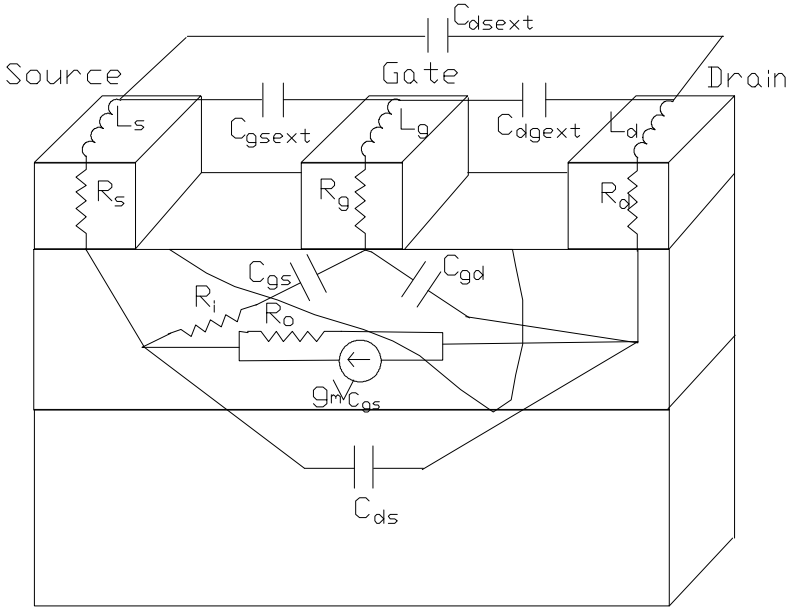

Figure 3.3: Physical Representation of Equivalent Circuit Elements [10].

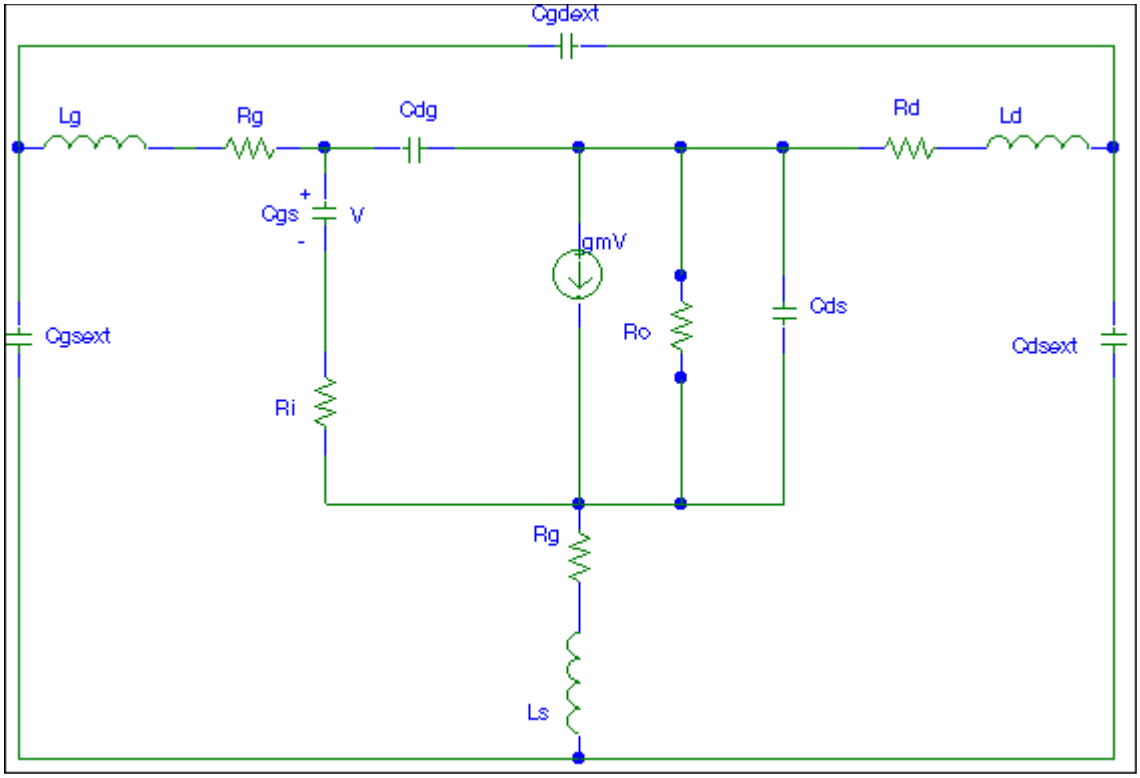

Figure 3.4: General Model in Circuit Form.

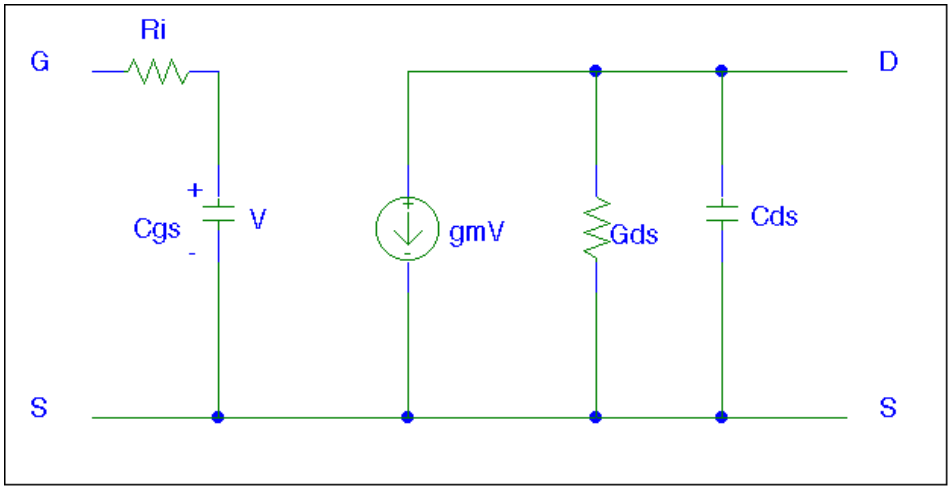

Figure 3.5: Simplified Small Signal Model [13].

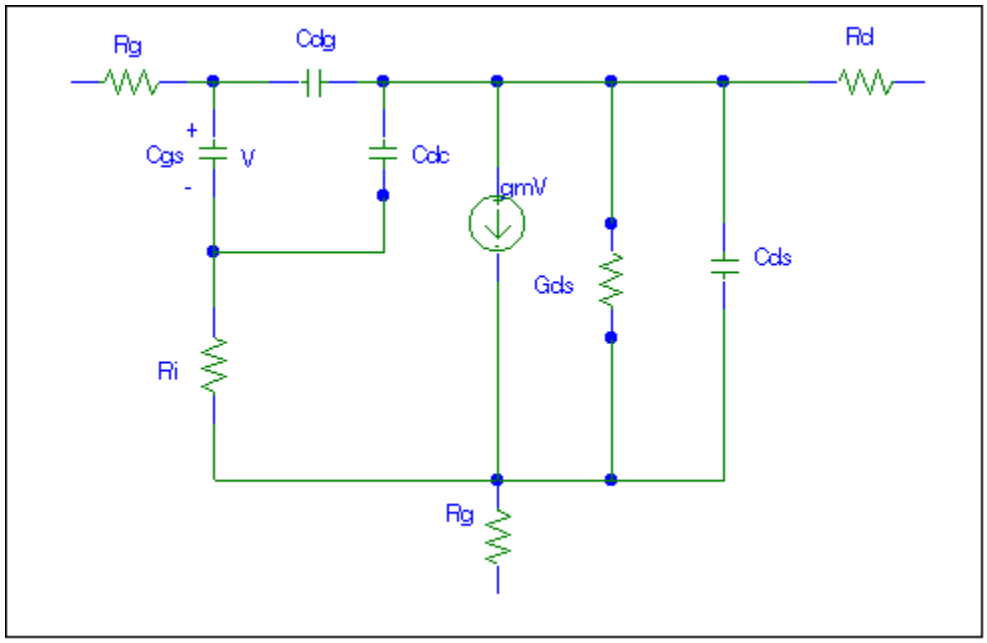

Figure 3.6: Liechti Model In Circuit Form [9].

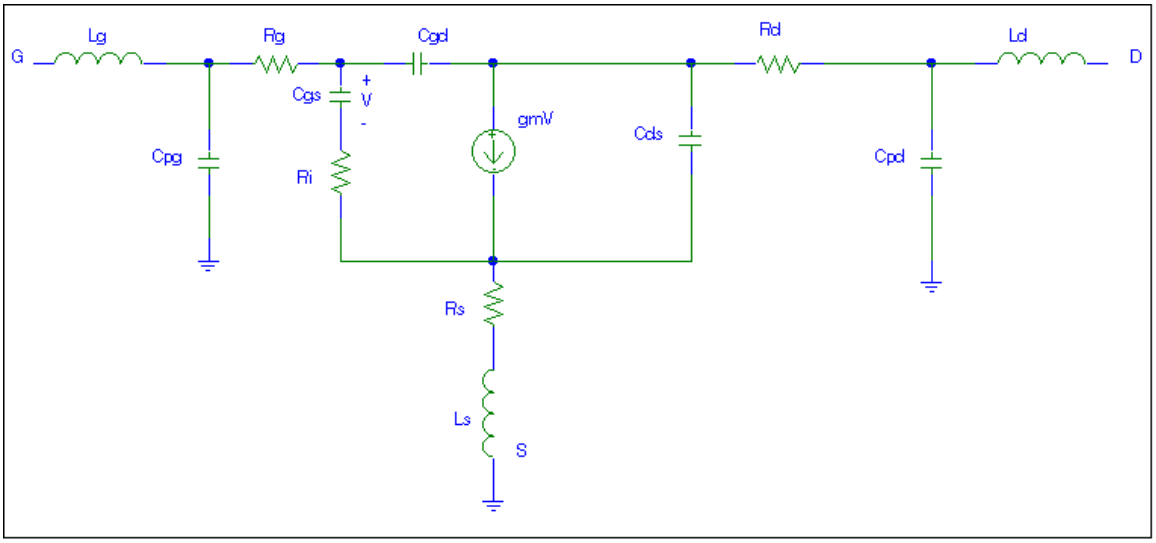

Figure 3.7: Dambrine Parasitics Model [15].

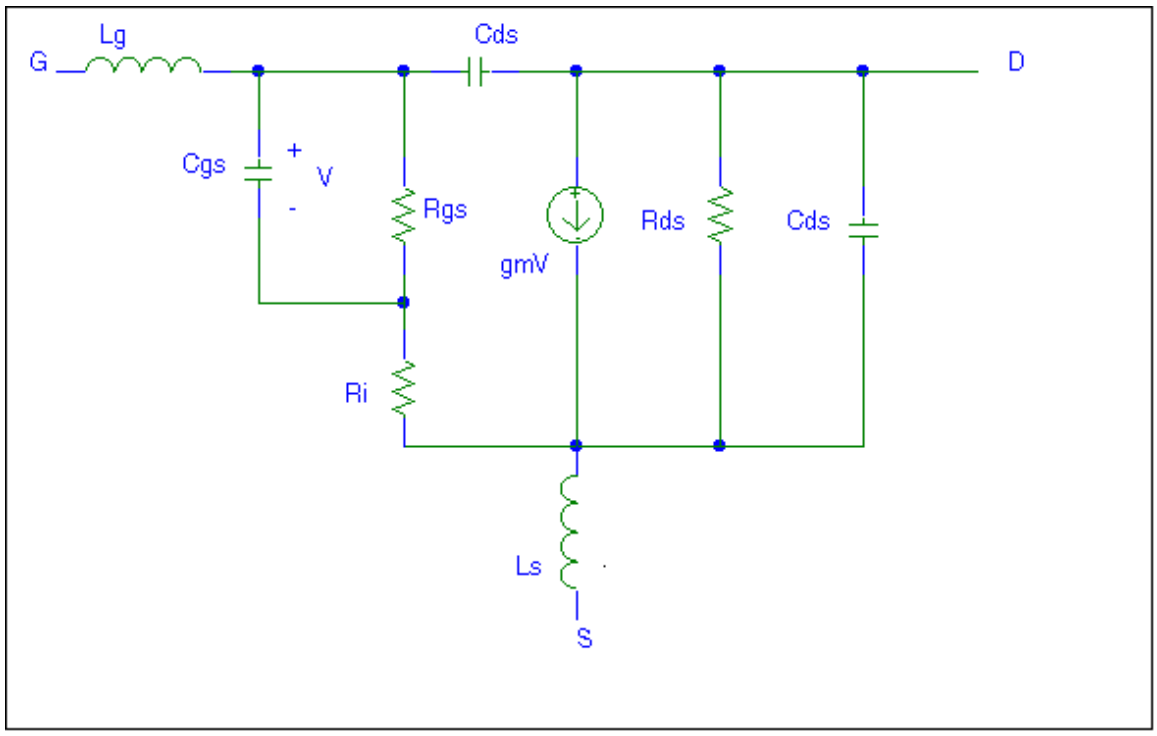

Figure 3.8: Gate-Source Resistor Model [18].

Table 3.1: General Model Results [17].

Quantity	**Value**
C_{gd} (pF)	0.06542
C_{gs} (pF)	0.3965
C_{ds} (pF)	0.1099
R_{ds} (Ω)	291.1
g_m (mS)	46.20
τ (ps)	1.63
L_s (pH)	3.4
L_d (pH)	0.0
L_g (pH)	59.5
R_s (Ω)	3.1
R_d (Ω)	3.6
R_g (Ω)	2.0

Table 3.2: Equivalent Circuit Values For The Liechti Model [9].

Quantity	**Value**
C_{gd} (pF)	0.014
C_{gs} (pF)	0.62
C_{ds} (pF)	0.12
C_{dc} (pF)	0.02
R_i (Ω)	2.6
R_{ds} (Ω)	400
g_m (mS)	53
τ (ps)	5.0
L_s (nH)	0.04
L_d (nH)	0.05
L_g (nH)	0.05
R_s (Ω)	2.0
R_d (Ω)	3
R_g (Ω)	2.9

Table 3.3: Gate-Source Resistor [18].

Quantity	**Value**
C_{gd} (pF)	0.0351
C_{gs} (pF)	0.242
C_{ds} (pF)	0.0802
R_{gs} (kΩ)	1.54
R_i (Ω)	11.3
R_{ds} (Ω)	245
g_m (mS)	34.9
τ (ps)	2.74
L_s (pH)	25.4
L_g (pH)	21.5

CHAPTER IV. EXTRACTION METHODOLOGY

4.1 Introduction [10, 15, 21]

This chapter describes a technique to extract the equivalent circuit parameters from S-parameters data. First, Y-parameters of the intrinsic device are determined. Next, a transformation to a Z-matrix is done so that the series parasitic impedances can be added. Finally, a transformation is done to the Y-parameters model so that the parasitic capacitances can be added. S-parameters are introduced and a conversion from Y-parameters to S-parameters is done. This is an ill-conditioned problem which means that there are too many variables and not enough equations. This problem is solved by the Simplex Method developed by Nelder and Mead [21] which minimizes a cost function, and requires no knowledge of the derivative of the cost function. The equivalent circuit used in this chapter is the General Model of Section 3.3.

4.2 Intrinsic Circuit Extraction [10, 12, 15]

This section describes how the intrinsic circuit which is shown in Figure 4.1 is expressed in terms of Y-parameters. Recall that the intrinisic circuit is the MESFET device excluding the parasitic elements. The intrinsic circuit contains the following elements: C_{gs}, the Gate-Source capacitance; R_i, the charging resistance; C_{dg}, the interelectrode capacitance between the Gate and Drain; g_m, the gain parameter associated with the voltage controlled current source; τ, the delay time associated with the change in the depletion width; R_o, the output resistance of the channel; and C_{ds}, the interelectrode capacitance between the Drain and Source. The equivalent circuit elements can be expressed in terms of Y-parameters. Figure 4.2 shows a Y-parameter representation of three-port network with one port (the Source) being common to the input and output. In the figure, y_{11} and y_{22} represent shunt admittances, and y_{12} and y_{21} represent voltage controlled current sources. The following equations can be written which describe the Y-Parameter network:

$$i_1 = y_{11}v_1 + y_{12}v_2 \tag{4.1}$$

$$i_2 = y_{21}v_1 + y_{22}v_2 \tag{4.2}$$

Short circuits measurements are used to determine the Y-parameters as illustrated in equations (4.3) - (4.6),

$$y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0} \tag{4.3}$$

$$y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1=0} \tag{4.4}$$

$$y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0} \tag{4.5}$$

$$y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1=0} . \tag{4.6}$$

The task now is to convert the intrinsic MESFET equivalent circuit model to a Y-parameters model. First y_{12} is determined. The input is short circuited and a voltage is applied between the drain and the source. This creates a short circuit which bypasses the series combination of C_{gs} and R_i. Because C_{gs} has no voltage across it, the voltage dependent current source is also zero. Figure 4.3 results from this condition.

It is easily determined that

$$v_2 = \frac{-i_1}{j\omega C_{gd}} \tag{4.7}$$

and consequently,

$$y_{12} = -j\omega C_{gd} . \tag{4.8}$$

Next, y_{22} is determined with the same circuit. The voltage v_2 is applied and the current i_2 is measured. The voltage is the same across each circuit element. This determines i_b and i_c in terms of i_a with,

$$y_{22} = \frac{1}{R_o} + j\omega\left(C_{ds} + C_{gd}\right) \tag{4.9}$$

Next, y_{21} is determined by shorting v_2, applying a voltage source, v_1, between the gate and source, and measuring i_2. The short circuit at v_2 shorts C_{ds} and R_o. This also makes the voltage across C_{gd} equal to v_2, so that:

$$i_a\left(\frac{1}{j\omega C_{gs}} + R_i\right) = i_b \frac{1}{j\omega C_{gd}} \tag{4.10}$$

The current i_b can be expressed as:

$$j\omega C_{gd} i_a\left(\frac{1}{j\omega C_{gs}} + R_i\right) \tag{4.11}$$

i_2 is equal to the difference between the current from the voltage controlled current source, $g_m V_{Cgs}\, exp(-j\omega t)$, and i_b. A few more steps of algebra and

$$y_{21} = \frac{g_m\, exp(-j\omega t)}{\left(1 + j\omega C_{gs} R_i\right)} - j\omega C_{gd}\,. \tag{4.12}$$

Figure 4.5 illustrates the circuit used to determine y_{21}. The last y-parameter to be found is y_{11}. v_1 can be expressed as:

$$i_a\left(\frac{1}{j\omega C_{gs}} + R_i\right) \tag{4.13}$$

i_1 can be expressed in terms of i_a:

$$i_a + i_a\left(\frac{1}{j\omega C_{gs}} + R_i\right) j\omega C_{gd}\,. \tag{4.14}$$

Thus,

$$y_{11} = \frac{j\omega C_{gs}}{\left(1 + j\omega C_{gs} R_i\right)} + j\omega C_{gd}\,. \tag{4.15}$$

Finally, the real and imaginary parts can be rearranged so that:

$$y_{11} = \frac{R_i \omega^2 C_{gs}^2}{\left(1 + \omega^2 C_{gs}^2 R_i^2\right)} + j\omega\left(\frac{C_{gs}}{1 + \omega^2 C_{gs}^2 R_i^2} + C_{gd}\right) \tag{4.16}$$

Figure 4.6 illustrates the circuit used to determine y_{11}.

The Y-parameters of the intrinsic MESFET device have been determined in this section by using short circuits. The four Y-parameters have been expressed as functions of the intrinsic equivalent circuit parameters: C_{gs}, R_i, g_m, τ, C_{gd}, R_o, C_{ds}. In the next section, the parasitic inductances and resistances will be added by converting to a Z-parameters representation.

4.3 Parasitic Extraction [10, 15]

In order to determine the effect of the parasitic resistances and inductances, a Z-parameter representation will be used. Figure 4.7 shows the instrinsic MESFET device with the series parasitic impedances. Figure 4.8 shows the equivalent Z-parameter network of the intrinsic MESFET device. The voltages at each of the ports are described as:

$$v_1 = z_{11} i_1 + z_{12} i_2 \tag{4.17}$$

$$v_2 = z_{21} i_1 + z_{22} i_2 \tag{4.18}$$

z_{11} and z_{22} represent series impedances, and z_{12} and z_{21} characterize current controlled voltage sources. Open circuits are used to measure the Z-parameters as illustrated by equations (4.19) - (4.22).

$$z_{11} = \left.\frac{v_1}{i_1}\right|_{i_2=0} \tag{4.19}$$

$$z_{12} = \left.\frac{v_1}{i_2}\right|_{i_1=0} \tag{4.20}$$

$$z_{21} = \left.\frac{v_2}{i_1}\right|_{i_2=0} \tag{4.21}$$

$$z_{22} = \left.\frac{v_2}{i_2}\right|_{i_1=0} \tag{4.22}$$

The Y-parameters must be converted to z-parameters with the following transformation:

$$[z] = \begin{bmatrix} \frac{y_{11}}{|y|} & \frac{y_{12}}{|y|} \\ \frac{y_{21}}{|y|} & \frac{y_{22}}{|y|} \end{bmatrix} \tag{4.23}$$

Where, the determinant $|y|$, is expressed as

$$|y| = y_{11}y_{22} - y_{12}y_{21} \tag{4.24}$$

Using the Z-parameters, the parasitic resistances and inductances are incorporated into the model, as follows,

$$z_{11} = z'_{11} + R_g + R_s + j\omega\left(L_g + L_s\right) \tag{4.25}$$

$$z_{12} = z'_{12} + R_s + j\omega L_s \tag{4.26}$$

$$z_{21} = z'_{21} + R_s + j\omega L_s \tag{4.27}$$

$$z_{22} = z'_{22} + R_d + R_s + j\omega\left(L_d + L_s\right) \tag{4.28}$$

In this case, the prime represents the Y-parameters converted to the Z-parameters.

Now, the parasitic capacitances are placed into the model. Figure 4.9 shows the model with the parasitic capacitances. Y-parameters are used and a transformation must be made between $[Y]$ and $[Z]$:

$$[Y] = \begin{bmatrix} \frac{z_{11}}{|z|} & \frac{z_{12}}{|z|} \\ \frac{z_{21}}{|z|} & \frac{z_{22}}{|z|} \end{bmatrix} \tag{4.29}$$

Where, the determinant $|z|$, is expressed as

$$|z| = z_{11}z_{22} - z_{12}z_{21} \tag{4.30}$$

Now, after Y-parameter analysis, the following expressions can be made which incorporate the parasitic capacitances:

$$Y_{11} = y_{11}' + j\omega\left(C_{gd} + C_{gs}\right) \tag{4.31}$$

$$Y_{12} = y_{12}' - j\omega C_{gd} \tag{4.32}$$

$$Y_{21} = y_{21}' - j\omega C_{gd} \tag{4.33}$$

$$Y_{22} = y_{22}' + j\omega\left(C_{ds} + C_{gs}\right) \tag{4.34}$$

The prime indicates the Z-parameters transformed to the Y-matrix. Finally, an expression can be used to determine the S-parameters in terms of the Y-parameters.

4.4 Scattering Parameters

So far, an equivalent circuit representation has been derived using Z-parameters and S-parameters. These parameters are determined by measurements that are made by researchers; however, they do have limitations. In measuring Z-parameters, open circuit connections are required and at microwave frequencies stray capacitances can cause open circuits to act like short circuits. In measuring Y-parameters, short circuit connections are required and at microwave frequencies stray inductances can cause short circuits to act like open circuits. Therefore, a new network characterization is needed; and that is Scattering parameters, or S-parameters. Scattering parameters measure the incident and reflected waves from both ports of a device. From these measurements, the S-parameters are calculated. The following relationship is evident from Figure 4.10:

$$b_1\left(l_1\right) = S_{11}a_1\left(l_1\right) + S_{12}a_2\left(l_2\right) \tag{4.35}$$

$$b_2\left(l_2\right) = S_{21}a_1\left(l_1\right) + S_{22}a_2\left(l_2\right) \tag{4.36}$$

Where,

$a_1\left(l_1\right)$ is the value of the incident wave at l_1,

$a_2\left(l_2\right)$ is the value of the incident wave at l_2,

$b_1\left(l_1\right)$ is the value of the reflected wave at l_1, and

$b_2\left(l_2\right)$ is the value of the reflected wave at l_2.

S_{11}, S_{12}, S_{21}, S_{22} are the S-parameters and they are defined as different ratios of the reflected waves to the incident waves with the proper terminations,

$$S_{11} = \left.\frac{b_1\left(l_1\right)}{a_1\left(l_1\right)}\right|_{a_2\left(l_2\right)=0} \tag{4.37}$$

S_{11} is the forward reflection coefficient.

$$S_{12} = \left.\frac{b_1\left(l_1\right)}{a_2\left(l_2\right)}\right|_{a_2\left(l_2\right)=0} \tag{4.38}$$

S_{12} is the reverse transmission coefficient. It is also a measure of the isolation of the device.

$$S_{21} = \left.\frac{b_2(l_2)}{a_2(l_2)}\right|_{a_1(l_1)=0} \tag{4.39}$$

S_{21} is the forward transmission coefficient; it also measures the voltage gain of the device.

$$S_{22} = \left.\frac{b_2(l_2)}{a_2(l_2)}\right|_{a_1(l_1)=0} \tag{4.40}$$

S_{22} is the output reflection coefficient.

S-parameters do not require short circuits or open circuits to be measured. They do require that the device be terminated in a matched impedance equivalent to the characteristic impedance of the line. This makes the reflection coefficient zero as evidenced by the relation,

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4.41}$$

Where,

Γ is the reflection coefficient,

Z_L is the impedance of the load,

Z_0 is the characteristic impedance of the line.

Relationships exist between S-parameters and other two-port network parameters. For Y-parameters, the following relationships are used:

$$S_{11} = \frac{\left(1 - y_{11}^{\bullet}\right)\left(1 + y_{22}^{\bullet}\right) + y_{12}^{\bullet} y_{21}^{\bullet}}{\Delta} \tag{4.42}$$

$$S_{12} = \frac{-2y_{12}^{\bullet}}{\Delta} \tag{4.43}$$

$$S_{21} = \frac{-2y_{21}^{\bullet}}{\Delta} \tag{4.44}$$

$$S_{22} = \frac{\left(1 + y_{11}^{\bullet}\right)\left(1 - y_{22}^{\bullet}\right) + y_{12}^{\bullet} y_{21}^{\bullet}}{\Delta} \tag{4.45}$$

Here,

$$\Delta = \left(1 + y_{11}^{\bullet}\right)\left(1 + y_{22}^{\bullet}\right) - y_{12}^{\bullet} y_{21}^{\bullet}, \text{ and} \tag{4.46}$$

$$y_{xy}^{\bullet} = y_{xy} Z_0 . \tag{4.47}$$

Since the MESFET is a three-port device, one should briefly discuss the use of three-port S-parameters. Three port S-parameters do not provide any more information about the Common-Source configuration of the MESFET device. They do, however, provide information about the Common-Gate and Common-Drain configurations [14].

Now, the relationships between the S-parameters and the equivalent circuit elements have been determined via matrix transformations. If one includes the real and imaginary parts of the S-parameters, there are eight equations and sixteen unknowns. The problem can not be solved exactly; there is an infinite number of solutions. The problem is

termed ill-conditioned. Ill-conditioned problems are usually solved using optimizers which are described in the next section.

4.5 Simplex Method [19, 21, 22]

The problem described above is ill-conditioned; there are an infinite number of possible solutions. Thus, it is necessary to use an optimizer; the optimizer varies the parameters of the problem until a minimum is reached. The optimizer is trying to minimize the following cost equation which relates measured S-parameters to modeled S-parameters. If the modeled S-parameters were perfect, this equation would be equal to zero. Equation (4.48) is an expression for the cost function. This cost function was chosen because theoretically it should be zero. That is, if the modeling is perfect, the differences should all go to zero. Also, this cost function is easy to implement and its easy to see what is being minimized. As an extension of this work, weighting factors could be incorporated. Weighting factors would used to emphasize one S-parameter over another.

$$\begin{aligned} E = &\left|S_{11measured(R)} - S_{11modeled(R)}\right| + \left|S_{11measured(I)} - S_{11modeled(I)}\right| \\ &+\left|S_{12measured(R)} - S_{12modeled(R)}\right| + \left|S_{12measured(I)} - S_{12modeled(I)}\right| \\ &+\left|S_{21measured(R)} - S_{21modeled(R)}\right| + \left|S_{21measured(I)} - S_{21modeled(I)}\right| \\ &+\left|S_{22measured(R)} - S_{22modeled(R)}\right| + \left|S_{22measured(I)} - S_{22modeled(I)}\right| \end{aligned} \tag{4.48}$$

Where,

E is the cost function which is being optimized,

$\left|S_{11measured(R)} - S_{11modeled(R)}\right|$ is the absolute value of the difference between the real part of the measured S_{11} and the real part of the modeled S_{11},

$\left|S_{11measured(I)} - S_{11modeled(I)}\right|$ is the absolute value of the difference between the imaginary part of the measured S_{11} and the imaginary part of the modeled S_{11},

$\left|S_{12measured(R)} - S_{12modeled(R)}\right|$ is the absolute value of the difference between the real part of the measured S_{12} and the real part of the modeled S_{12},

$\left|S_{12measured(I)} - S_{12measured(I)}\right|$ is the the absolute value of the difference between the imaginary part of the measured S_{12} and the imaginary part of the modeled S_{12},

$\left|S_{21measured(R)} - S_{21measured(R)}\right|$ is the absolute value of the difference between the real part of the measured S_{21} and the real part of the modeled S_{21},

$\left|S_{21measured(I)} - S_{21measured(I)}\right|$ is the absolute value of the difference between the imaginary part of the measured S_{21} and the imaginary part of the modeled S_{21},

$\left|S_{22measured(R)} - S_{22measured(R)}\right|$ is the absolute value of the difference between the real part of the measured S_{22} and the real part of the modeled S_{22}, and

$\left|S_{22measured(I)} - S_{22measured(I)}\right|$ is the absolute value of the difference between the imaginary part of the measured S_{22} and the imaginary part of the modeled S_{22}.

The Simplex Method is used because it requires no derivatives to reach a minimum; only functional evaluations. For a problem of n variables, n+1 points are needed. If the optimization problem were in only one dimension; with only one starting point, the simplex could not move and find a minimum; therefore, the Simplex needs an extra point. The Simplex uses four moves, illustrated in Figure 4.11 in three dimensions (a tetrahedron).

Move 1: Given the highest point on the Simplex, reflect it through the lowest point.

Move 2: After a reflection, expand in the same direction because a lower point may lie in this direction.

Move 3: Contraction. The Simplex can not expand by reflection, so shrink the size of the simplex.

Move 4: Multiple contraction.

Once the Simplex has started to contract down a minimum, it has no way of getting itself out. Therefore, the Simplex is prone to getting stuck in a local minimum. The Simplex Method terminates when the standard deviation of all the points is less than some tolerance. The method used to move the Simplex can be described in the following quantitative way [21, 22]:

(1) Cost function evaluations of all the points in the Simplex are done and the point with the largest value is determined.

(2) The centroid of the points except the point with the largest functional evaluation is calculated,

$$x^0 = \frac{1}{n}\sum_{\substack{i=1 \\ i\neq h}}^{n+1} x^i \tag{4.49}$$

(3) The highest point is reflected across the centroid according to,

$$x^r = (1+\alpha)x^0 - \alpha x^h, \alpha > 0 \tag{4.50}$$

(4) If this new point gives a cost function less than the lowest point, then an expansion is done in this same direction,

$$x^e = (1-\gamma)x^0 + \gamma x^r, \gamma > 0 \tag{4.51}$$

(5) If after reflection, the value of the new point is less than the value of the second highest point, then the highest point is replaced with the new point and the reflection process is started over again.

(6) If the reflected point is greater than the second highest point, then the Simplex is contracted about the highest point according to:

$$x^c = (1-\beta)x^0 + \beta x^h, 0 < \beta < 1 \tag{4.52}$$

(7) If the contraction fails to produce a new lower point, the whole Simplex is contracted by the following expression:

$$x^i = \frac{1}{2}\left(x^i + x^l\right), \quad i = 1,\text{K}\ ,n+1 \tag{4.53}$$

where i represents the index of each point of the Simplex.

(8) The method is considered to have reached a minimum when the following criteria is met:

$$\sqrt{\left(\sum_{i=1}^{n+1}\frac{\left[M\left(x^i\right)-M\left(x^0\right)\right]^2}{n}\right)} \le \tau, \tau > 0 \qquad (4.54)$$

where M represents a cost function evaluation. $M\left(x^0\right)$ is the cost function evaluation of the centroid of the Simplex without the highest point. $M\left(x^i\right)$ represents the cost function evaluation at each point. τ is the criteria for stopping execution.

4.6 MESFET Device Extraction Tool (MFET)

MFET is an extraction code which was written in FORTRAN for this thesis. MFET inputs the measured S-parameters and a starting set of initial equivalent circuit values. Sixteen other points are generated for the starting Simplex. Next, the cost function is calculated for each point. This involves calculating the Y-parameters, converting to Z-parameters, including the series parasitics, converting back to Y-parameters, including the parasitic capacitors, and finally converting to S-parameters. The Simplex Method subroutine from *Numerical Recipes* [19] is then called. This involves making functional evaluations of the cost function and minimizing the error. Once the error reaches a minimum tolerance the code stops; the best point of the seventeen is used to generate the S-parameters as a function of frequency. Figure 4.12 is a flowchart describing the operation of this code.

4.7 Other Methods Of Extraction [10]

One other method of equivalent circuit extraction involves measuring the parasitic resitances under forward DC bias. Under forward DC bias, the Schottky diode is a short circuit and C_{gs} is bypassed. The parasitic capacitances are assumed to be zero. A low frequency approximation good upto 10 GHz is made with the Y-parameters,

$$\omega^2 C_{gs}^2 R_i^2 << 1 \qquad (4.55)$$

This greatly simplifies the Y-parameter equations for the intrinsic device so that if the parasitics are measured, an optimization is not required. The parasitic inductances are determined from the differences between the measured S-parameters and the modeled S-parameters. These methods are not infallible; designers will change the values of these circuit elements by 50% -100%.

4.8 Conclusion

A method for extracting the equivalent circuit from S-parameter data has been developed. This method involves several matrix transformations and different two-port representations of the MESFET device. The equivalent circuit elements are solved for by using a Simplex Method optimizer. The Simplex Method will choose equivalent circuit

values to minimize the cost function. The advantage of the Simplex Method is that it does not require knowledge of the derivative of a function while the major disadvantage is that it gets stuck in local minima. Finally, an alternate means of extracting the equivalent circuit elements was also briefly introduced.

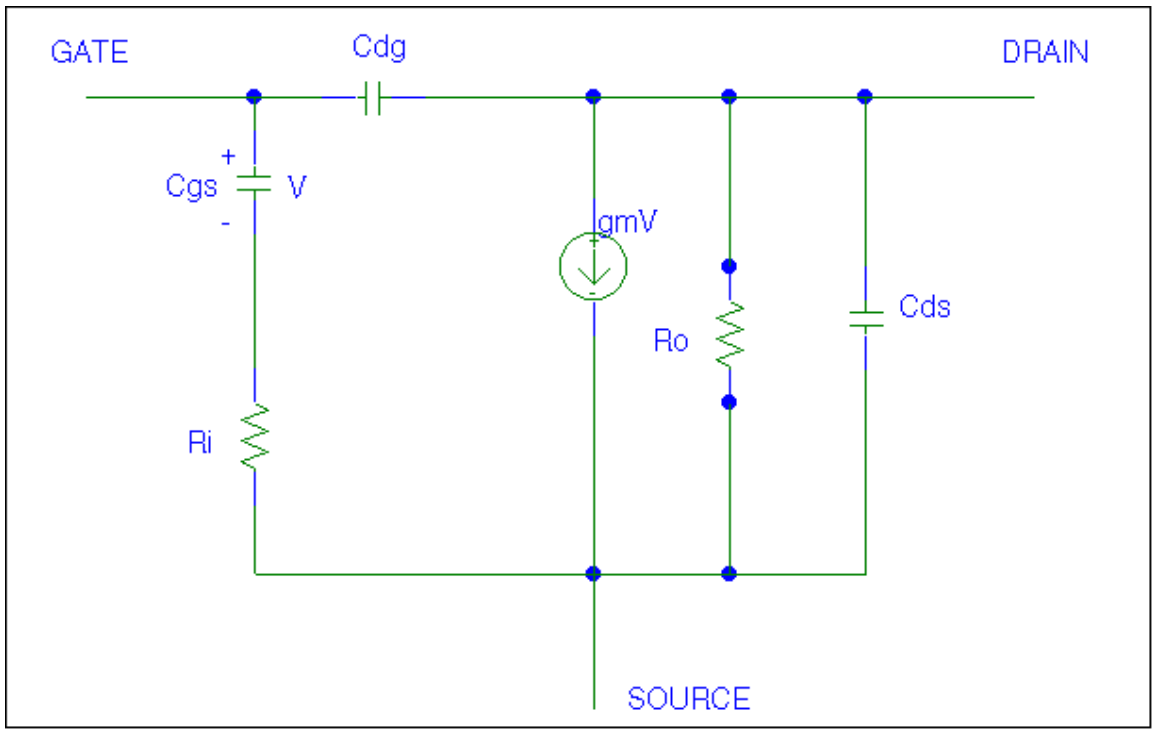

Figure 4.1: Intrinsic MESFET Circuit [10].

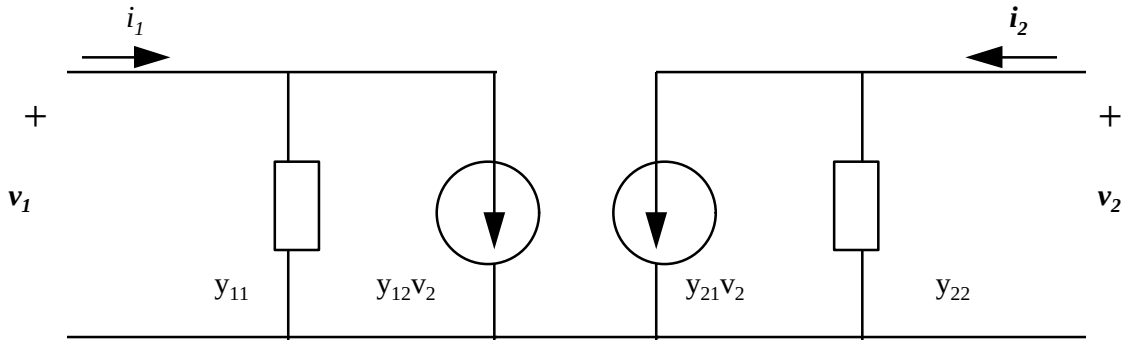

Figure 4.2: Y-Parameter Network.

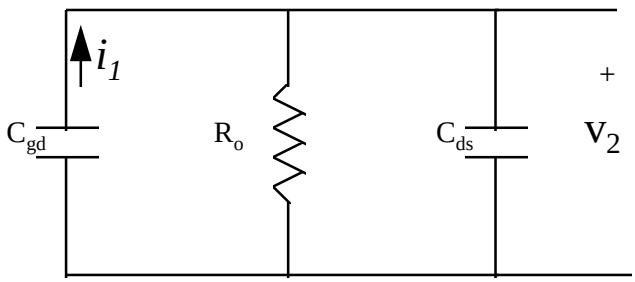

Figure 4.3: Circuit Used to Determine y_{12}.

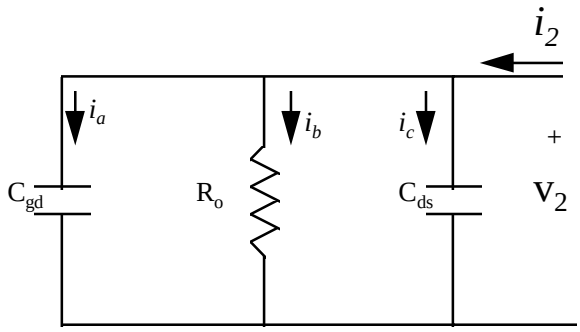

Figure 4.4: Circuit Used to Determine y_{22}.

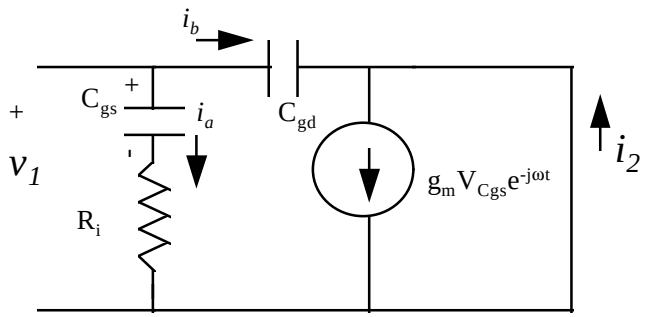

Figure 4.5: Circuit Used To Determine y_{21}.

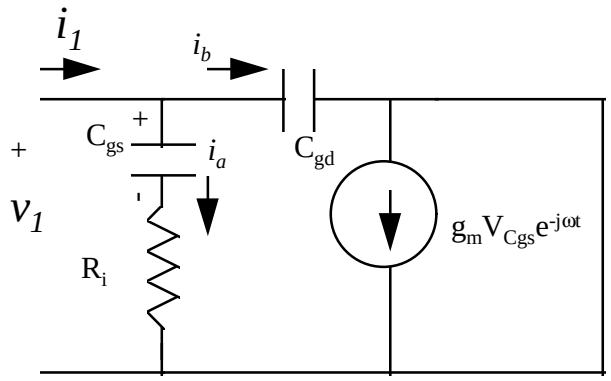

Figure 4.6: Circuit Used To Determine y_{11}.

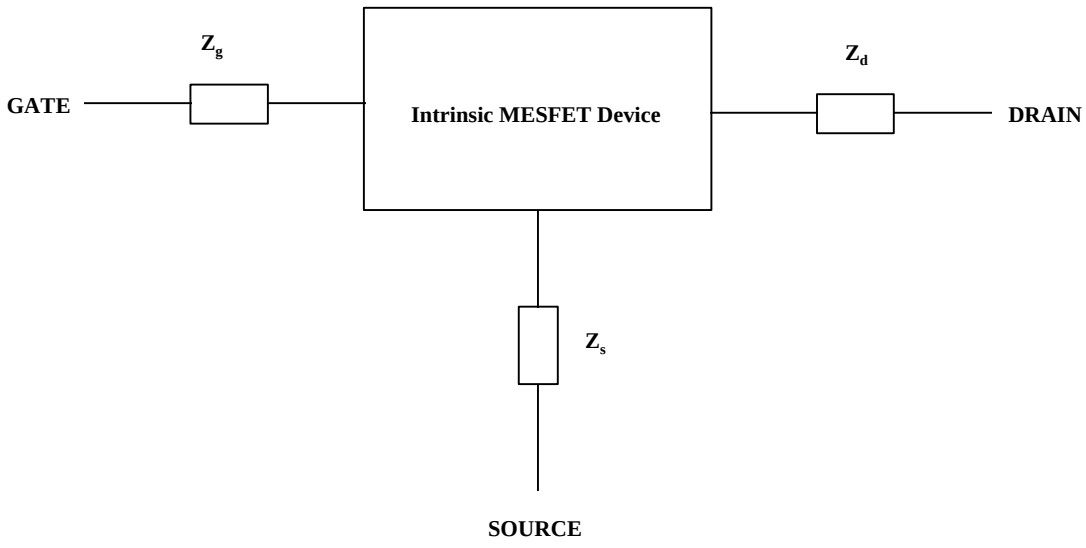

Figure 4.7: Intrinsic Device With Series Parasitics.

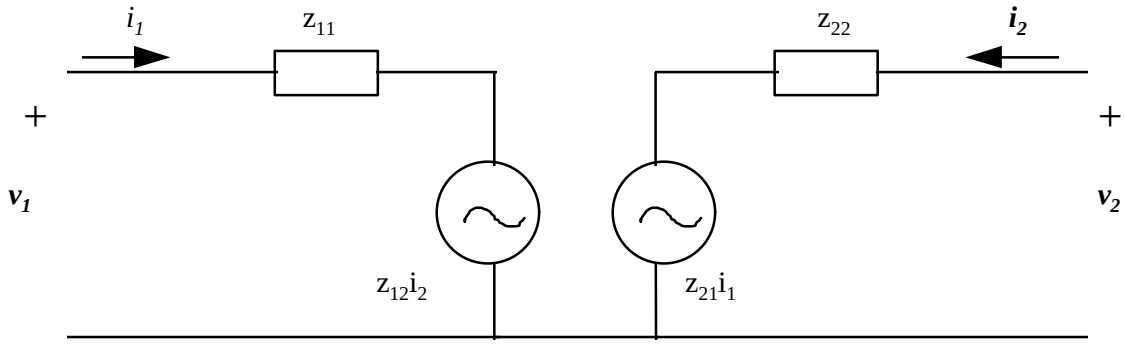

Figure 4.8: Z-Parameter Representation Of Intrinsic MESFET Device.

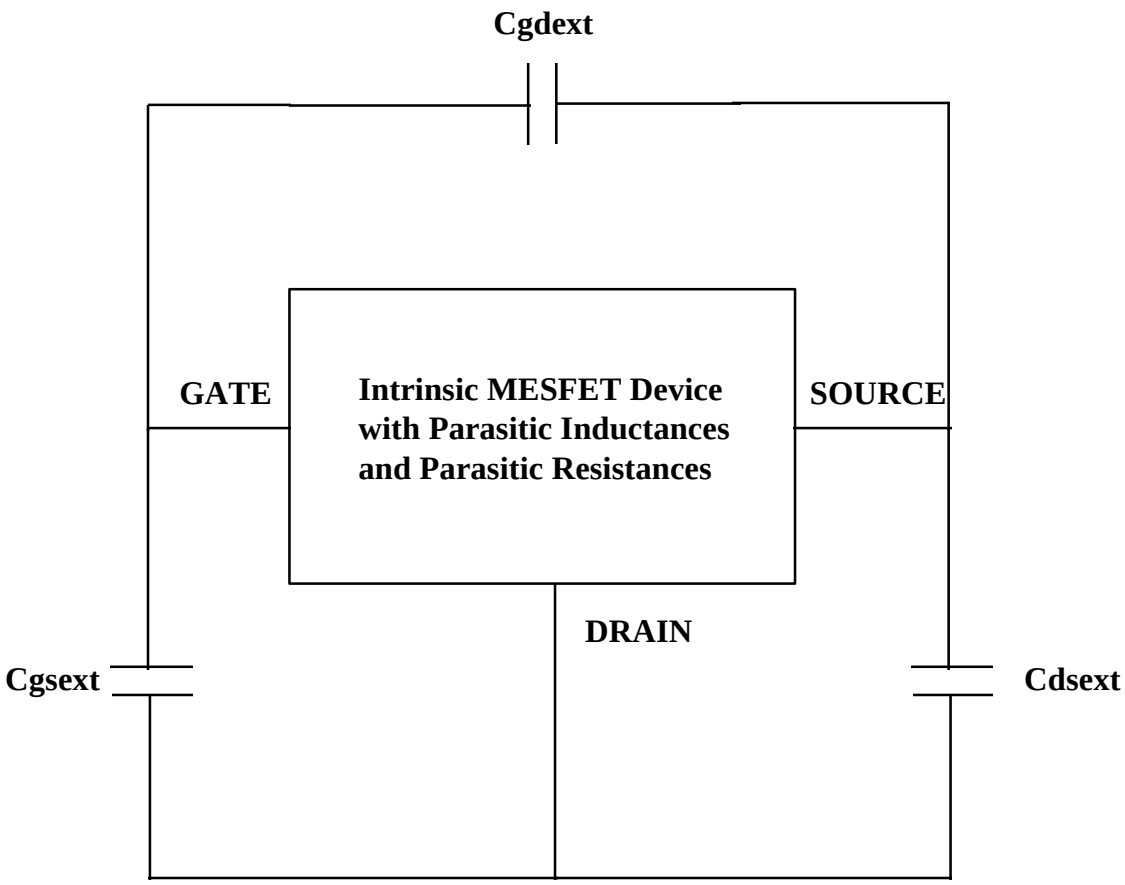

Figure 4.9: MESFET Device With Extrinsic Capacitances.

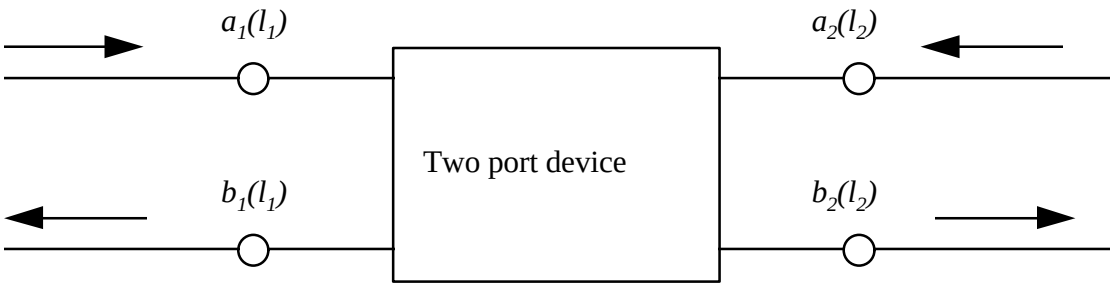

Figure 4.10: Incident And Reflected Waves From A Two-Port Device.

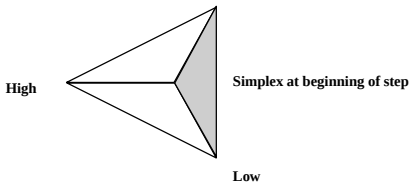

Figure 4.11a: Beginning Position of Simplex [19]

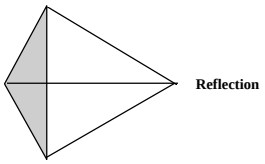

Figure 4.11b: Reflection Move [19]

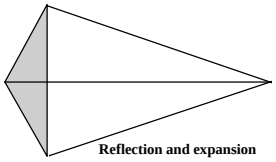

Figure 4.11c: Reflection and Expansion [19]

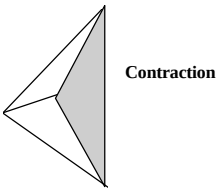

Figure 4.11d: Contraction [19]

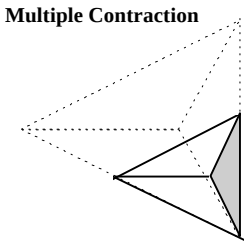

Figure 4.11e: Multiple Contraction [19]

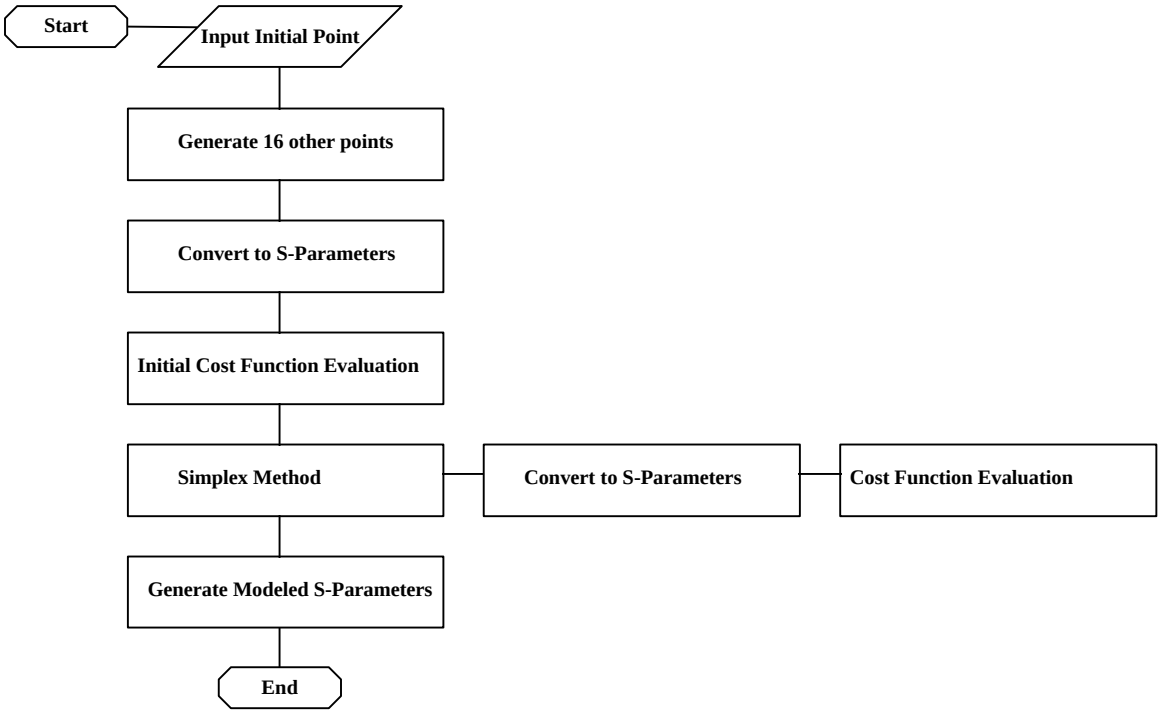

Figure 4.12: Block Diagram of MFET Operation.

CHAPTER V. MEASUREMENTS AND DATA ANALYSIS

5.1 Introduction

This chapter describes the S-parameters measurements conducted on the MESFET device which is analyzed in this thesis. First, the measurement set-up is described. Basically, the measurement set-up involves an HP network analyzer, coplanar waveguide probes, and a wafer-probing station. However, before the measurements were made; the set-up had to be calibrated to remove the effects of the probes. After the experimental set-up and calibration are described, the data will be analyzed by processing them with a FORTRAN code written for this thesis. A broadband equivalent circuit from 0.05 GHz to 6.05 GHz is fit to each of the S-parameters. A narrowband model from 0.05 GHz to 1.85 GHz is then fit to the S-parameters. Finally, the sensitivity of the output equivalent circuit to the initial conditions will be investigated. A key assumption is that the capacitances, the resistances, the inductances, and the voltage controlled current source do not vary with frequency. This is a good assumption for the narrowband model; however, for the wideband model resonances appear in the data which are hard to fit. The code that processes the data uses the Simplex method is described in Chapter IV.

5.2 Equipment And Experimental Set-up

The equipment used for making the measurements was the following: HP 8510B network analyzer, HP 6629A DC power supply system, Electroglass wafer prober, HP 8514B S-parameters test set which went from 45 MHz to 20 GHz, HP 33150A bias tees, and two Cascade coplanar waveguide probes ACP 40. The network analyzer measures the magnitude and the phase of the S-parameters. The S-parameters test set terminates the MESFET device in the required impedance. The S-parameters test set-up used in this thesis is very powerful because it makes the forward terminations and the reverse terminations on the MESFET device automatically. The bias tees consist of an inductor and a capacitor; the inductor keeps the AC signal from leaking into the DC power supply; and the capacitor keeps the DC power from interfering with the network analyzer. Figure 5.1 shows a block diagram of the equipment used in this thesis. The MESFET devices are fabricated on the wafer in reticles. Many devices are contained in each reticle. The devices in the reticles are accessed with Cascade probes. These probes are used to access coplanar waveguide devices and have a Ground-Signal-Ground configuration. Figure 5.2 shows one of the wafer probes. The Electroglass wafer prober is able to move the Cascade probes about the wafer; the prober is also able to raise the wafer probes off the wafer and also lower them. Figure 5.3 shows the wafer with an alignment flat and different reticles. Each reticle contains the same set of MESFET devices.

5.3 Calibration

Before the measurements could be made, the probes had to be calibrated. There are two probes: one accesses the gate side of the device and the other accesses the drain side of the device. Calibration involves removing the effects of the probes, the cables, and the connectors in order to evaluate the S-parameters of the device. Figure 5.4 shows the Short Open Load Thru calibration standards for coplanar waveguide. Only the left probe is shown, but the same procedure is applied to the right probe simultaneously. A set of calibration standards exists on a special wafer. First, the response of the system to a Short is measured. This involves placing the probe on a strip of metallization; all the contacts are shorted. Next, the response of the probe to an Open is measured, and for this, the probe is left in the air and is not contacting anything. The Load calibration involves placing the probe contacts on two 100 Ω resistors which are in parallel. Finally, a 50 Ω thru line is used to measure the response to a Thru. These measurements are applied to an error correction term which has been programmed into the network analyzer. Now, the calibration is verified. The HP vector network analyzer has a Smith Chart display. When the Short is measured now, it shows the Short exactly as a Short should be on the Smith Chart, a dot where the reflection coefficient Γ is, $\Gamma = -1$. Also, when the Open is measured, it is displayed exactly where it would be on the Smith Chart, a dot where $\Gamma = 1$. The Load used is the characteristic impedance of the line and it displays a dot at $\Gamma = 0$. The Thru was very similar to the load having $\Gamma = 0$. Finally, for an independent verification, the calibration is verified with an inductor. This traces out a smooth curve of inductive reactance as the frequency is swept.

5.4 Data Collection

S-parameters measurements were taken from 50 MHz to 6.05 GHz. The Drain bias, V_D, was chosen as 3.3V, and the Gate bias, V_G, was chosen as 0V. On the left side of the MESFET device there are two Source pads; the Ground Contacts of the probe are placed at these locations. In between the Source pads there is a Gate pad; the Signal Contact of the probe is placed at that location. On the right side of the MESFET device there are also two Source pads; the Ground contacts of the left probe are place here. In between the two Source pads is a Drain pad; the Signal Contact of the right probe at this location. Figure 5.5 shows a MESFET device similar to the one measured. The Gate fingers are shown in black. The difference is the total number of gate fingers; the device measured had 56 Gate fingers. The Gate finger width was 300 μm which made the periphery 16.8 mm. The gate pitch was 15 μm. The data were then collected in Magnitude-Angle form and written to an ASCII file.

5.5 Data Processing And Analysis

The equivalent circuit model used to fit the data was the General model of Section 3.3. It is repeated in this section for clarity in Figure 5.6 . The data were then processed using the Simplex Method. It is best to examine the S-parameters in matrix form because with all the Y-parameter and Z-parameter transformations, an algebraic form is very complicated. Since there are 16 equivalent circuit parameters, the exact relationships

between them and the S-parameters are difficult to determine. It should be noted that the Simplex Method will not be able to fit the S-parameters exactly. There are no functions of the form:

$$f(x) = ax + bx^2 + cx^3 + dx^4 + ex^5 + \ldots \tag{5.1}$$

Such a polynomial would allow a better fit to the S-parameters, but it would have no physical meaning.

A very important point to make is that the values of the capacitances, inductances, resistances, and the voltage controlled current source are assumed to be constant over the frequency range. Incorporating a frequency dependence would make the models much more complicated.

The Simplex Method requires coefficients to determine the rates at which it reflects, expands, and contracts. The reflection coefficient used for these runs was $\alpha = 1$, the expansion coefficient used was $\gamma = 2$, and the contraction coefficient was $\beta = 2$. The tolerance as described by equation (4.54) in Section 4.5 used for these runs was $\tau = 10^{-12}$.

5.5.1 Comparison: No Boundaries, Boundaries, Wide-Spread

Three different runs of the Simplex Method are compared: (1) no boundaries are placed on the points of the Simplex, (2) boundaries are placed on the points of the Simplex, (3) the initial starting points of the Simplex are spread out in space. The goal in making these runs is to compare the different curve fits and the final cost function evaluations.

First, the data were processed without using any boundaries; the Simplex was allowed to go anywhere in the sixteen dimensional space to minimize the cost function. The middle column of Table 5.1 shows the starting values for the Simplex. Note that in Table 5.1 the value for C_{gd} is greater than the value for C_{gs}. This is in general nonphysical and is done here only as a mathematical exercise. The Simplex will have seventeen points total; each point will have sixteen coordinates. The initial starting point was used to generate the other sixteen points in the following manner: imagine the sixteen points with their sixteen coordinates as a sixteen by sixteen matrix. Each point is represented as a row. Each diagonal point of the matrix is equal to the initial starting point added to one-tenth the initial starting point. Non-diagonal points are just equal to the initial starting point. As an example, for the first row:

$$L_g = L_g initial + 0.10 \times L_g initial \tag{5.2}$$

All the other points in this first row correspond to the values of the initial starting point. The second point represented by the second row has the following value for L_d

$$L_d = L_d initial + 0.10 \times L_d initial \tag{5.3}$$

All the other points in the second row correspond to the values of the initial starting point. The curves for this run are shown in Figures 5.7 , 5.8 , 5.9 , and 5.10. All curves are plotted on two-dimensional plots because the problem to be analyzed is a curve fit.

Next, bounds were placed on the values of the points of the Simplex. This is an attempt to represent the values of the circuit elements as physical realizable values. These boundaries are labeled as Minimum and Maximum in Table 5.1. The same initial points as

in the case without boundaries were used. When the Simplex tries to reflect or expand through a boundary, that point is replaced by a point 20% smaller than the upper boundary in the case of the upper boundary or 20% larger than the lower boundary in the case of the lower boundary.

Finally, the other sixteen points of the Simplex were spread out to see if this would improve the fit. In the other two cases, the Simplex may have gotten stuck in a local minimum. If the points were spread out more, the Simplex may find a better minimum value for the cost function. The FORTRAN loop structure for this case may be found in Appendix B. In this loop structure, the array p contains the point of the Simplex with the first row containing the initial point. The idea of the loop structure is to spread the other points out with the loop control variable according to the initial value of the equivalent circuit parameter and its range.

The Simplex Method has fit a curve to each of the S-parameters in Figures 5.7, 5.8, 5.9, 5.10. Note that the magnitudes have been plotted in terms of dB. The S-parameters with the best fit are S_{21}. This is because S_{21} is typically larger in magnitude than the other S-parameters, especially at lower frequencies. For example at 50 MHz the magnitudes are: S_{11}=0.9768, S_{12}=0.0081, S_{21}=15.1853, S_{22}=0.8844. S_{21} is 100 times bigger than S_{11} and S_{22}, while it's 10,000 times bigger than S_{12}. After all, S_{21} is a measure of the voltage gain of the device ,and in order to minimize the cost function, the biggest payoff occurs if the magnitude of S_{21} is minimized. In Figure 5.9, all three modeled curves fit the magnitude of S_{21} the best. The phase curve of S_{21} in Figure 5.9 is also fit very well because it is very smooth and does not have any kinks in it. There is some resonance in the measured magnitude of S_{11} in Figure 5.7 at approximately 5.25 GHz. This resonance may be due to a standing wave set-up in the device resulting in less energy being reflected. The Simplex Method will not be able to fit this resonance. In Figure 5.8, the No Bounds curve fits the frequencies which are lower than this resonance in the magnitude of S_{12} the best. The No Bounds curve does not try to fit the resonance in the magnitude of S_{12}. The curves for Bounds and Wide Spread both try to fit the resonance in the magnitude of S_{12}. Of all the Figures, the worst fit is of S_{12} phase. In Figure 5.8, the modeled angle curves go in different directions than the measured curve. Also in Figure 5.8, the measured S_{12} angles are in the first quadrant of the complex coordinate system, while the modeled angles are in the fourth quadrant. In order to analyze this, one must consider the real and imaginary parts of the S-parameters. So, the problem with the modeled S_{12} phase is that the imaginary part is negative when it should have been positive. Note that in the case where the magnitude or phase oscillates with frequency such as the measured angle of S_{22} in Figure 5.10, the modeled S-parameter will take try to take the average.

For the next comparison of these three runs, Table 5.2 shows the values of each of the cost functions and the error terms for S_{11}, S_{12}, S_{21}, S_{22}. The cost function equals the sum of these error terms. The No Bounds case has the lowest value of the cost function. This is reasonable because the Simplex Method is able to find a minimum with no restrictions. When a boundary is placed on the Simplex Method, it is not allowed to find the best minimum. Finally, when the Simplex is spread out throughout the space, it converges to a different local minimum as in the Wide Spread Case. The large value of the cost function in the Wide Spread case indicates that the curve fit is not very good.

The values of the S-parameter error terms are close; the greatest discrepancy is in the values for S_{11}.

Table 5.3 shows the equivalent circuits for the different extractions. With no boundaries on the values, they can go negative as evidenced by C_{dgext} which has a value of -0.899193 pF. A negative capacitance is not physically possible. Note that the numbers in Table 5.3 are just numbers that fit the model and they should not be construed as being able to measure a circuit parameter to six decimal places. Although these extractions give similar fits, the equivalent circuit values have different values. This is especially significant in the case of g_m, C_{gdext}, and C_{dsext}. Because the extraction problem contains so many variables, the Simplex Method is sensitive to initial conditions. Sensitivity will be examined in Section 5.5.3. The next section involves using a narrower frequency band to try to improve the fit.

5.5.2 Narrow Band Model

In order to try to improve the fit of the modeled curves, a narrow band model was applied to the data. This way, the optimizer would not have to fit the resonances that exist in the magnitudes of S_{11} and S_{12}. However, it will still be difficult to fit the oscillations in the magnitude of S_{22}. The frequency range was 0.05 GHz to 1.85 GHz; the actual operating range of the device is 775-900 MHz. The graphs of Figures 5.11, 5.12, 5.13, 5.14 show the Measured MESFET Device, the Narrow Band model, and the Bounds model plotted over a narrower frequency range. The Narrow Band model does have boundaries built into it. The tolerance in both cases was 10^{-12}.

These figures show that the Narrow Band model provides a better fit to the magnitude of S_{11} in Figure 5.11. However, in most cases the fit that the two models provide is very similar; and in the case of the phase of S_{12} in Figure 5.12 and the magnitude of S_{22} in Figure 5.14, the fit is worse. Figure 5.13 shows that the fit of S_{21} of the two cases is very similar. Because the Narrow Band is only fitting over 19 frequencies and not the whole frequency range, the cost function evaluations start out smaller. An indication of the convergence of the Simplex Method is that it is contracting. In the case of the Narrow Band model, as the Simplex Method reaches the tolerance, the Simplex is still expanding and reflecting. The Bounds run ends with the Simplex contracting. In order to remedy this the tolerance should be set smaller for the Narrow Band case.

5.5.3 Sensitivity Analysis

In this section, the sensitivity of the output equivalent circuit to small changes in the initial conditions is studied. For this analysis, the initial values of C_{gs}, g_m, and R_o were changed by 1% to see what the effect on the final values would be; that is C_{gs} was changed to its value in Table 5.3 with the other circuit element values being those in Table 5.1, and so for g_m and R_o.

Table 5.4 shows that the final Cost Function values are very close; however, there are differences in the terms for S_{11}, S_{12}, and S_{21}. These differences equalize in the

expression for the Cost Function. The S-parameters are plotted versus frequency in Figures 5.15, 5.16, 5.17,and 5.18.

Figure 5.15 shows that the fit of the magnitude of S_{11} is very good until about 2.05 GHz when the curve for the sensitivity of C_{gs} passes under the other curves. However, the differences are not very great, only being about a tenth of a dB. The fits of all the curves are close except for S_{12} magnitude. The fit here is not that good due to S_{12} being much smaller than the other S-parameters.

In order to study the sensitivity of the cost function to different initial conditions, different values of C_{gs} were inserted into the model and Figure 5.19 was created. The Simplex method will start its evaluations typically at a cost function value of about 45, that is the sum of differences between the measured S-parameters and modeled S-parameters is 45. The scale of figure 5.19 is significant because the cost function represents four separate error terms: the differences between S_{11}, S_{12}, S_{21}, S_{22}. These four terms could be different and yield a similar value for the cost function. Consequently, the equivalent circuit values are different in most cases. Different equivalent circuit models will provide similar modeled S-parameters. The problem is sensitive because there are only eight equations for sixteen unknowns.

5.6 Conclusion

The Simplex Method has been analyzed in this Chapter. Future work may focus on comparing different cost functions. The best curve fits result when the equivalent circuit parameters are allowed to take on any value. There is very little improvement in applying a narrow band model; however, this is due to the fact that the Simplex has not converged to a local minimum yet. This problem could be solved by making the tolerance for stopping the Simplex Method smaller. Finally, sensitivity to initial equivalent circuit values was investigated in this work. When one initial circuit value was changed by 1%, some of the output equivalent values changed by more than 1%. The Simplex Method still converges to a similar minimum; however the minimum should be viewed as being very flat with many different equivalent circuits possible. The Simplex Method applied to the 16 parameters equivalent circuit model does a satisfactory job fitting the measured S-parameters. If a designer wishes to attribute physical meaning to the output of the Simplex Method, too many equivalent circuit parameter make the Simplex Method unstable in terms of the equivalent circuit output. The next chapter will briefly examine other optimization methods and suggest a way of making the Simplex Method more robust in terms of physical realism.

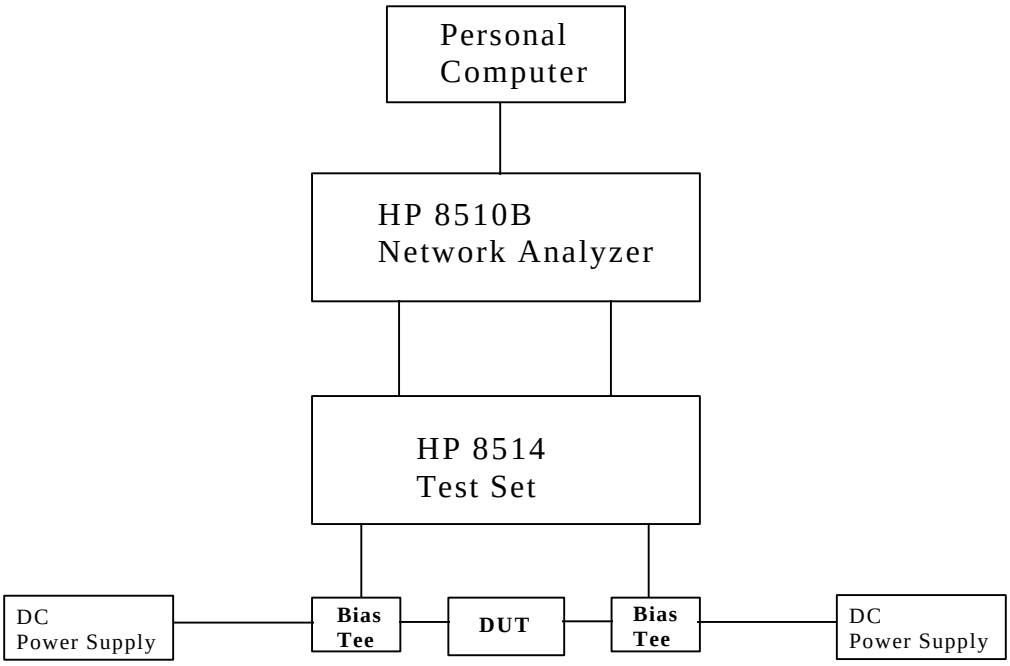

Figure 5.1: Equipment Setup.

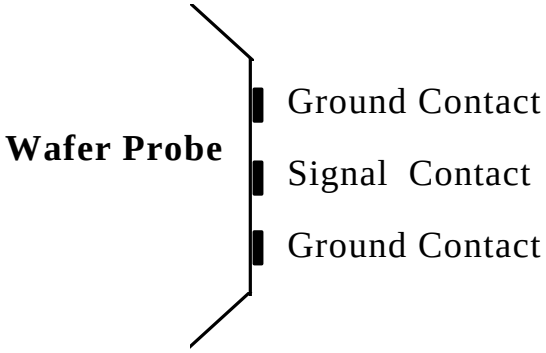

Figure 5.2: Wafer Probe Showing Ground-Signal-Ground Contacts.

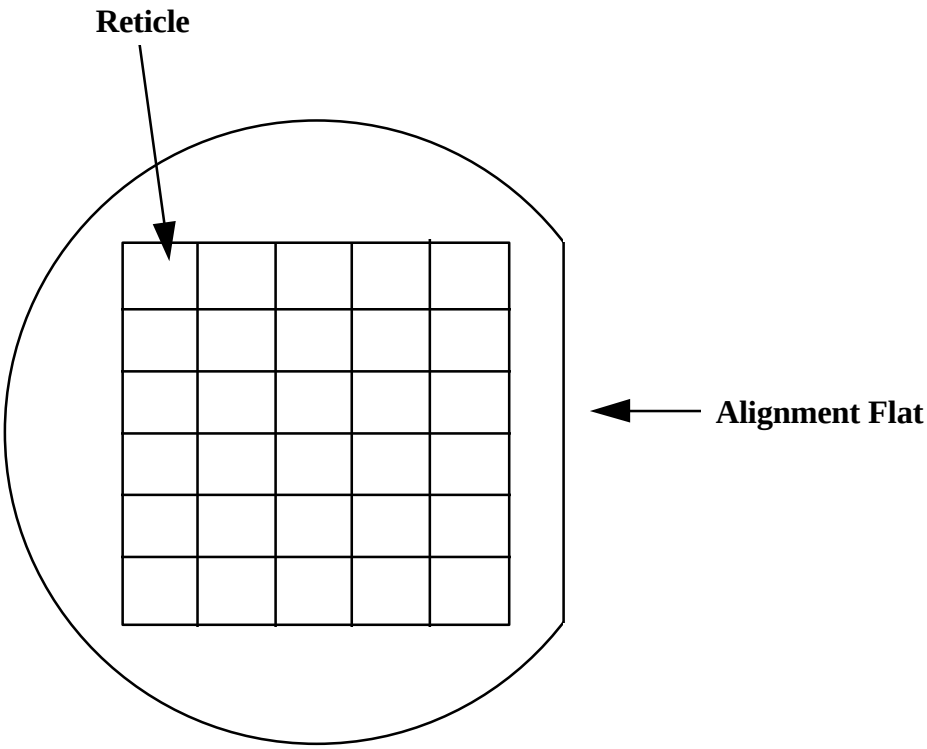

Figure 5.3: Wafer Indicating Reticles and Alignment Flat.

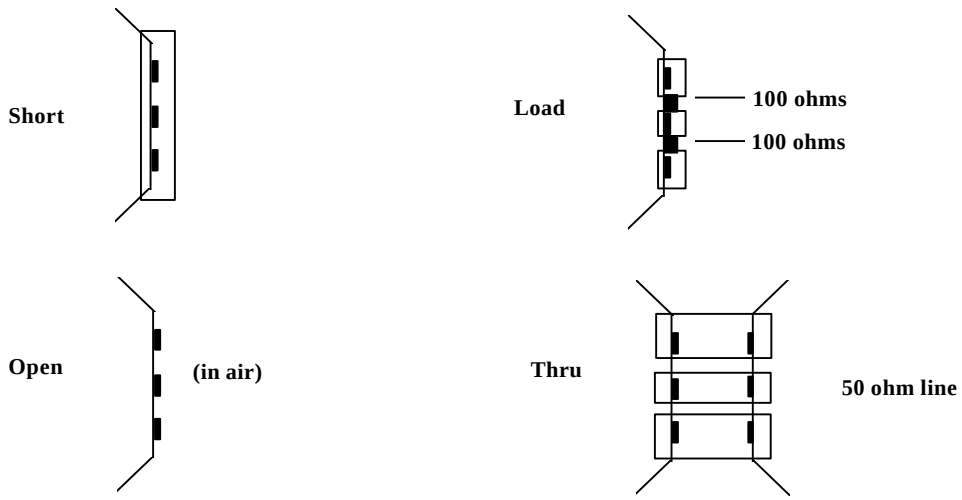

Figure 5.4: SOLT Calibration Standards [23].

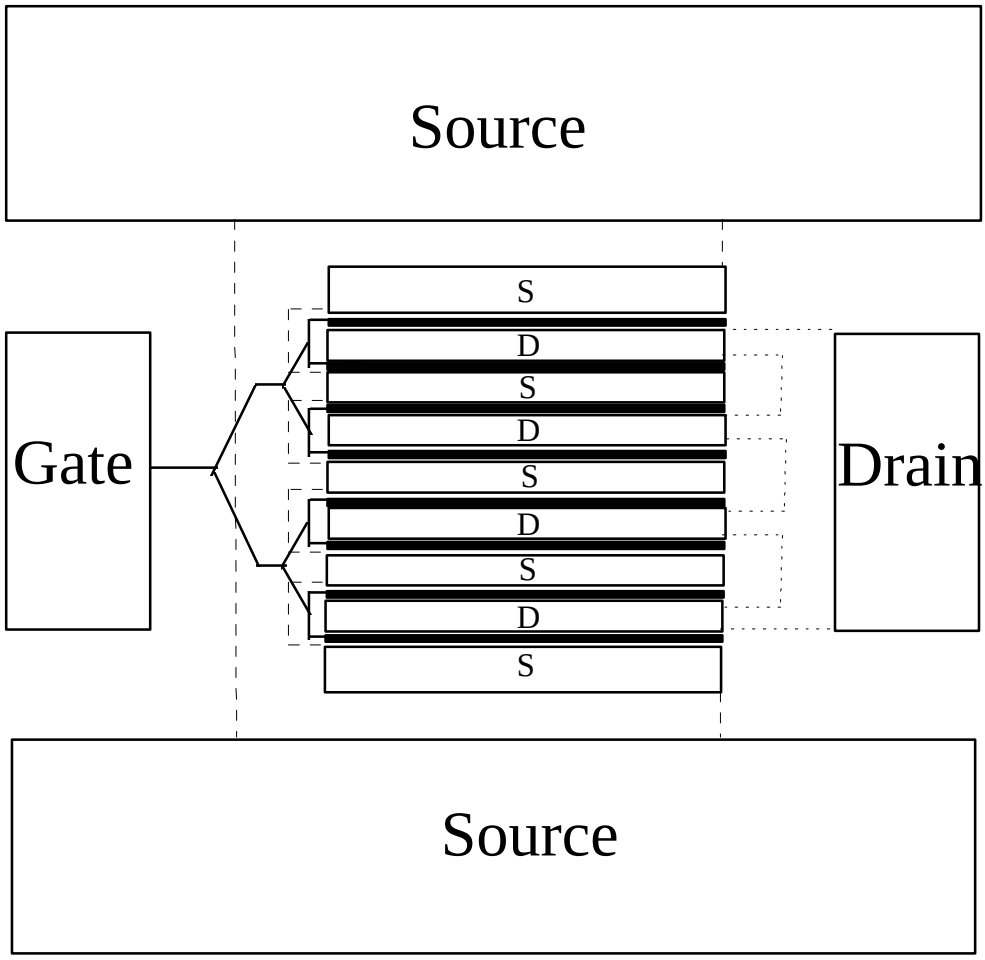

Figure 5.5: Power MESFET Device (Not To Scale).

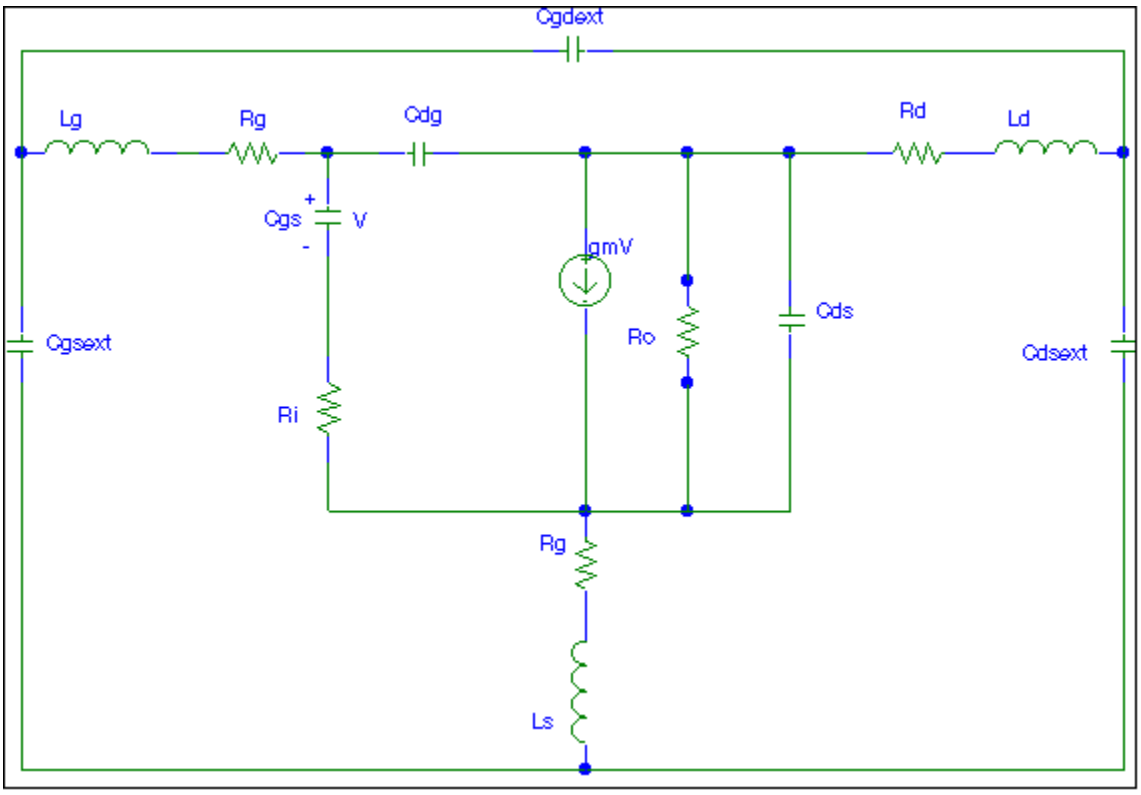

Figure 5.6: General Circuit Model.

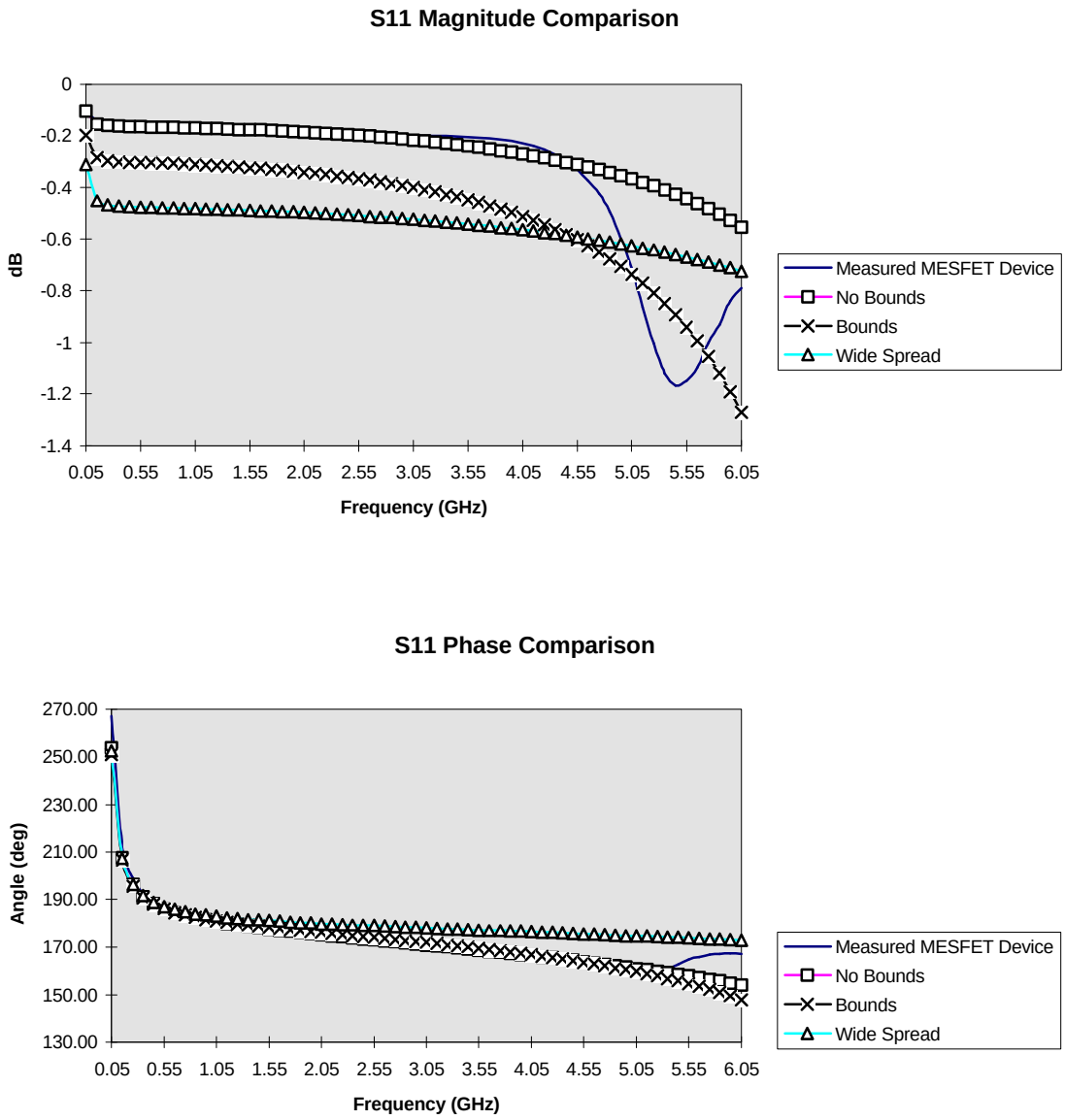

Figure 5.7: S_{11} Boundary Comparison.

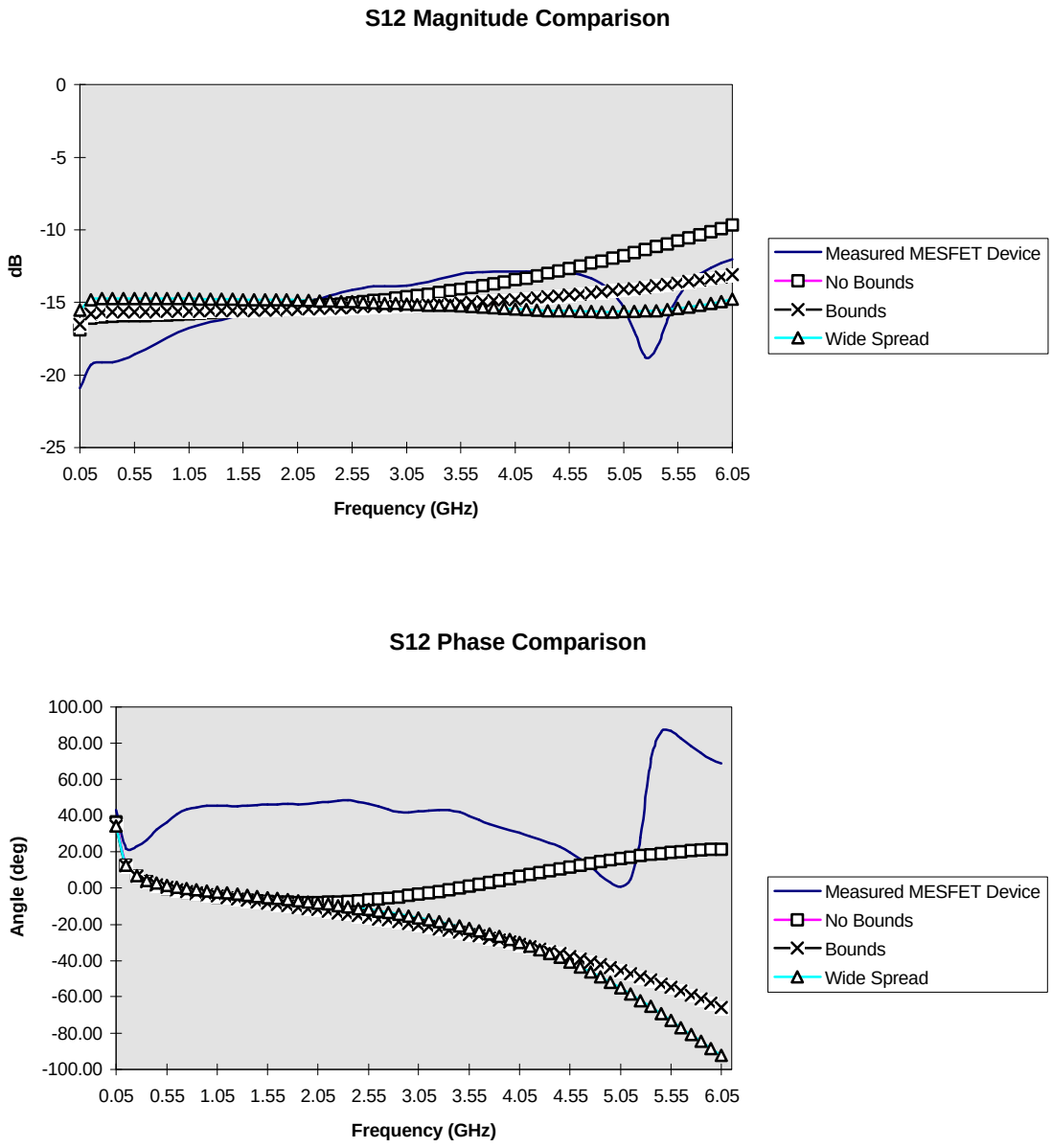

Figure 5.8: S_{12} Boundary Comparison.

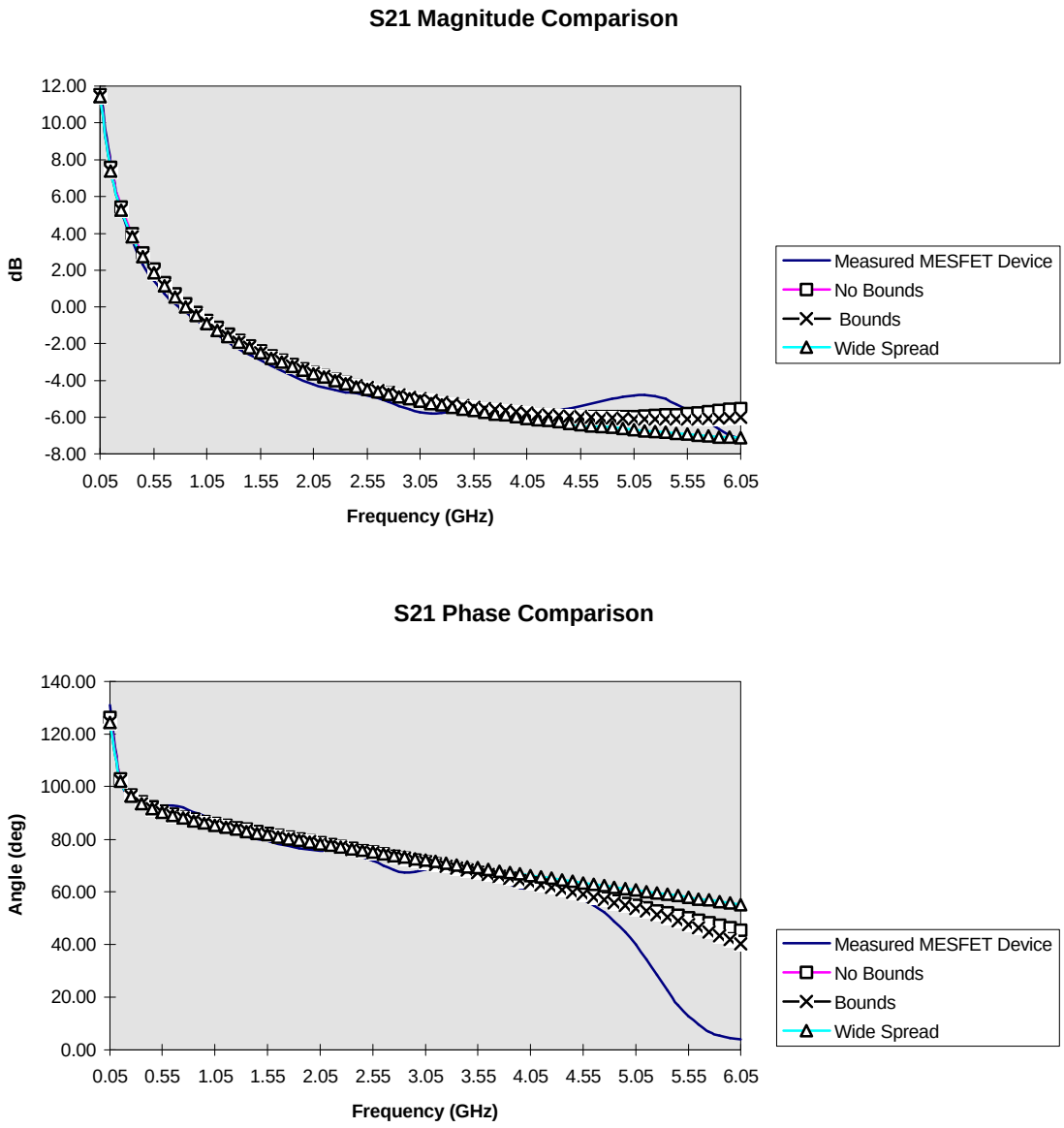

Figure 5.9: S_{21} Boundary Comparison.

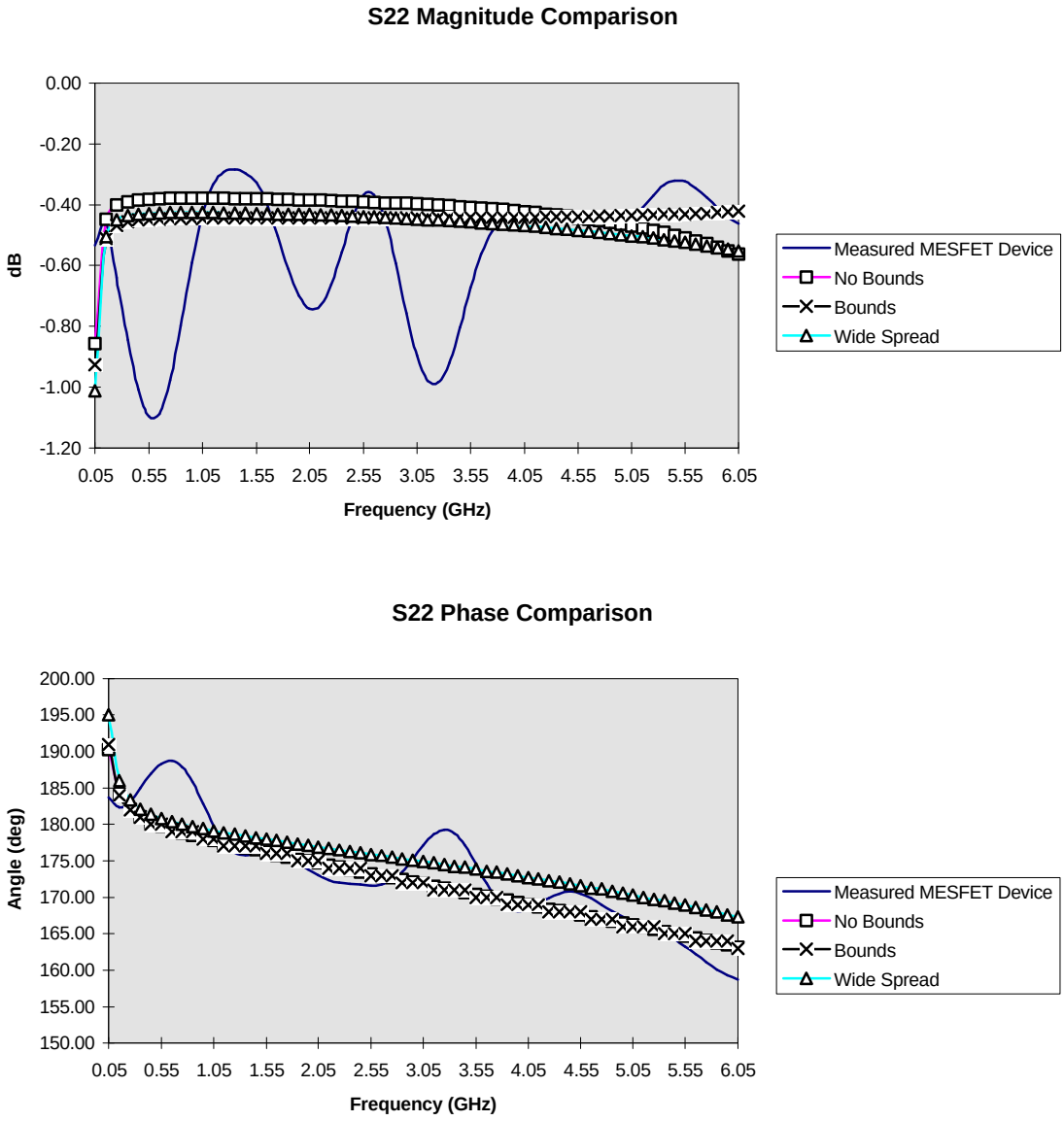

Figure 5.10: S_{22} Boundary Comparison.

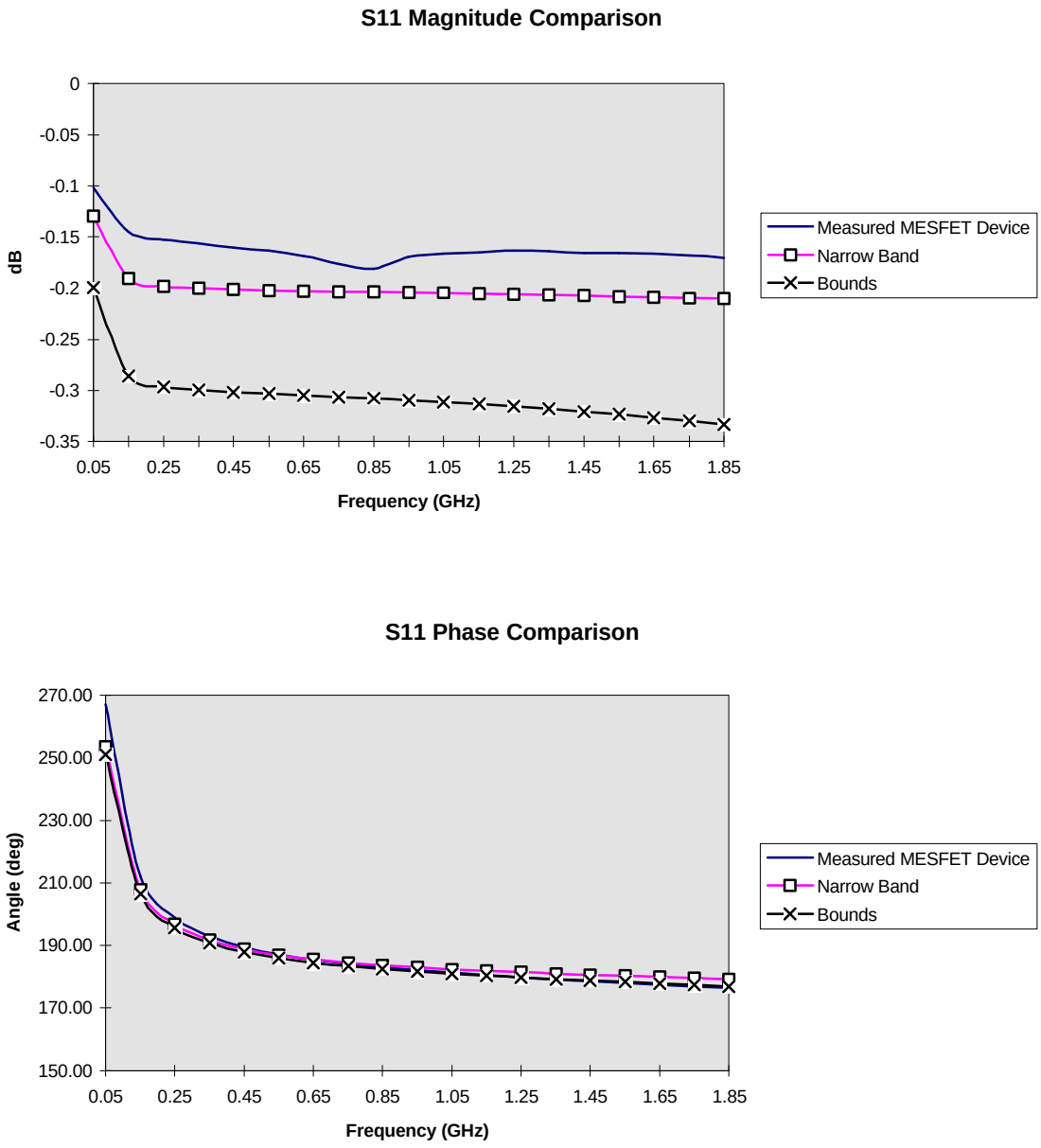

Figure 5.11: S_{11} Narrow Band Comparison.

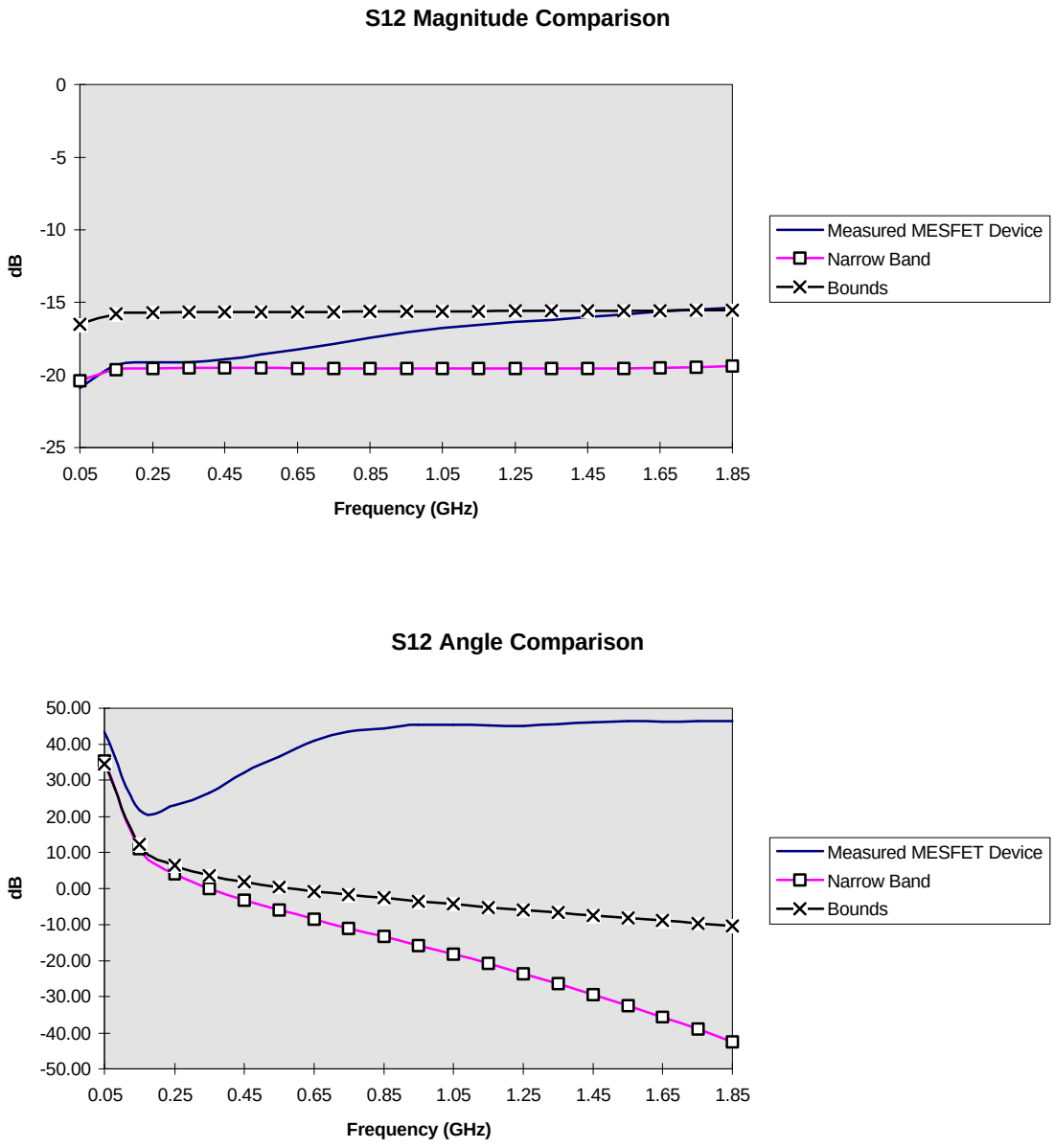

Figure 5.12: S_{12} Narrow Band Comparison.

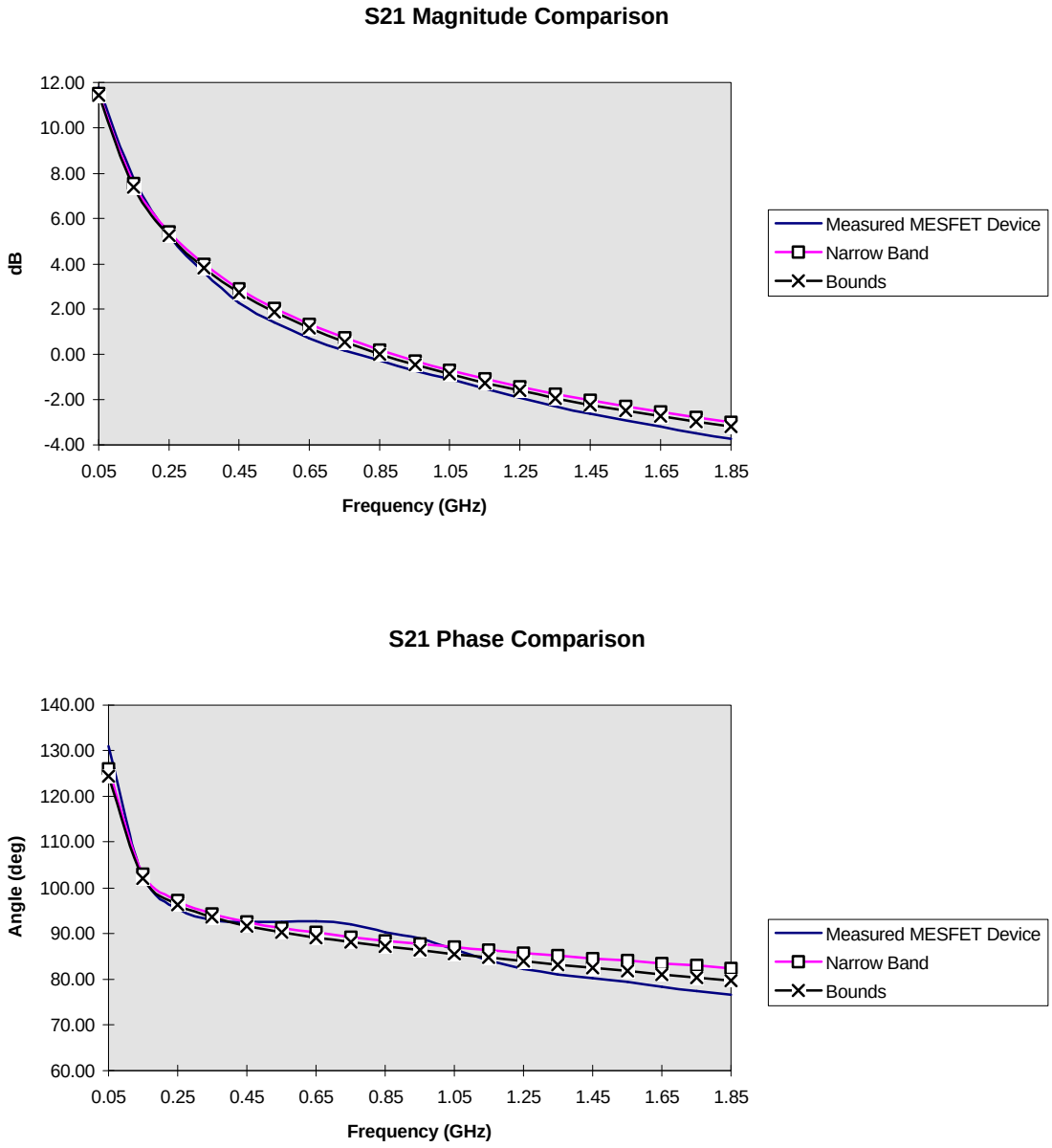

Figure 5.13: S_{21} Narrow Band Comparison.

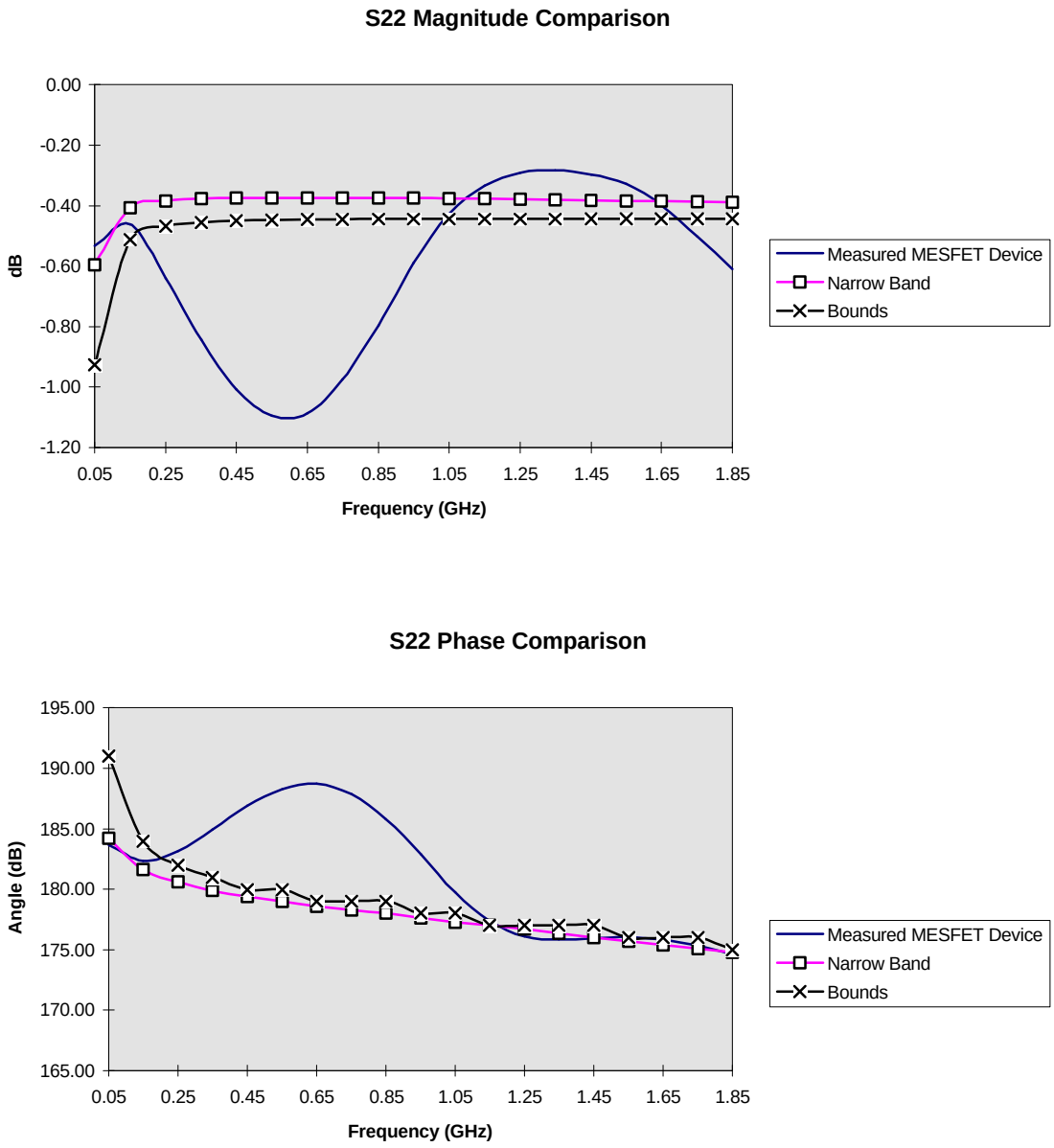

Figure 5.14: S_{22} Narrow Band Comparison.

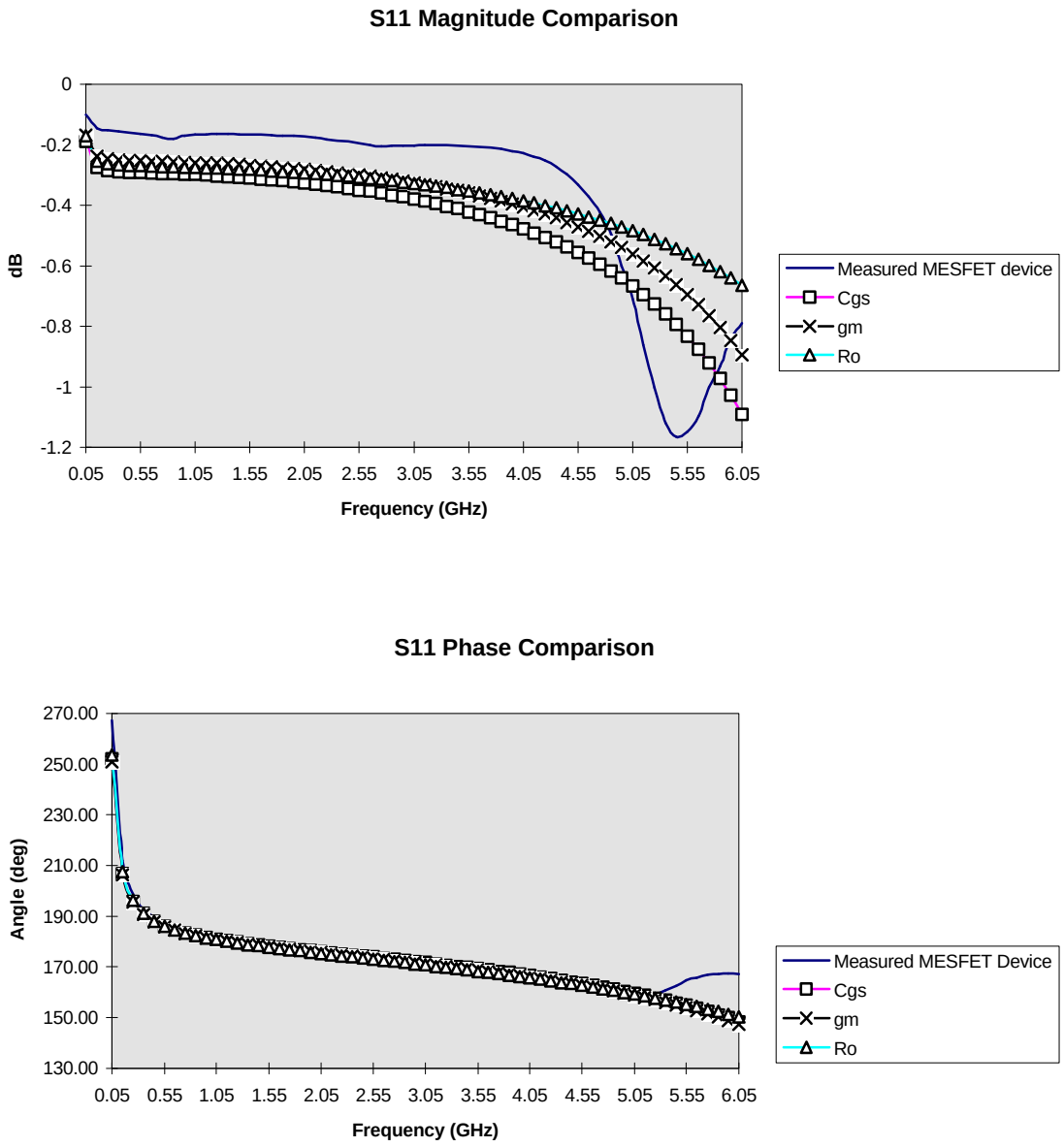

Figure 5.15: S_{11} Sensitivity Comparison.

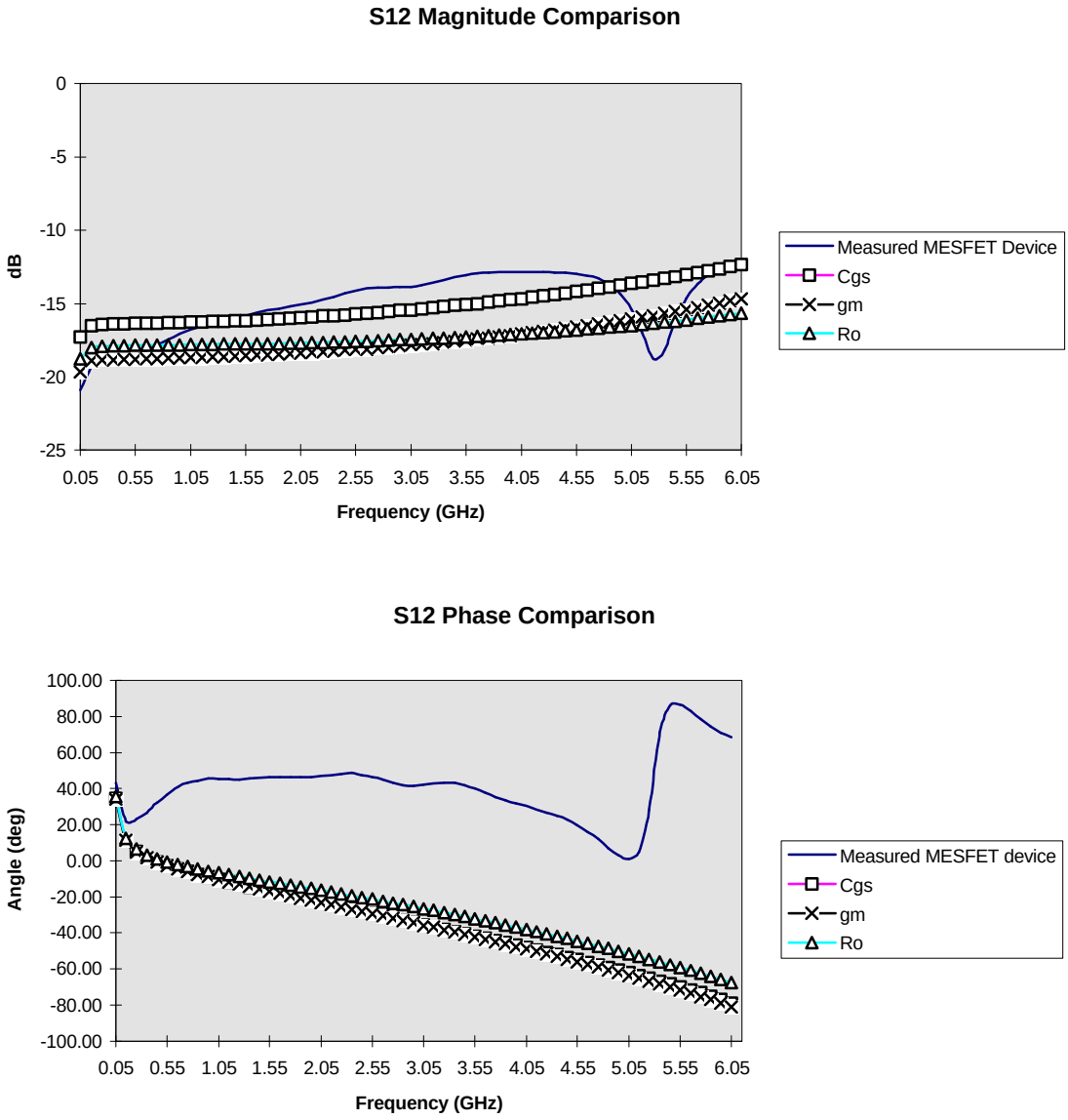

Figure 5.16: S_{12} Sensitivity Comparison.

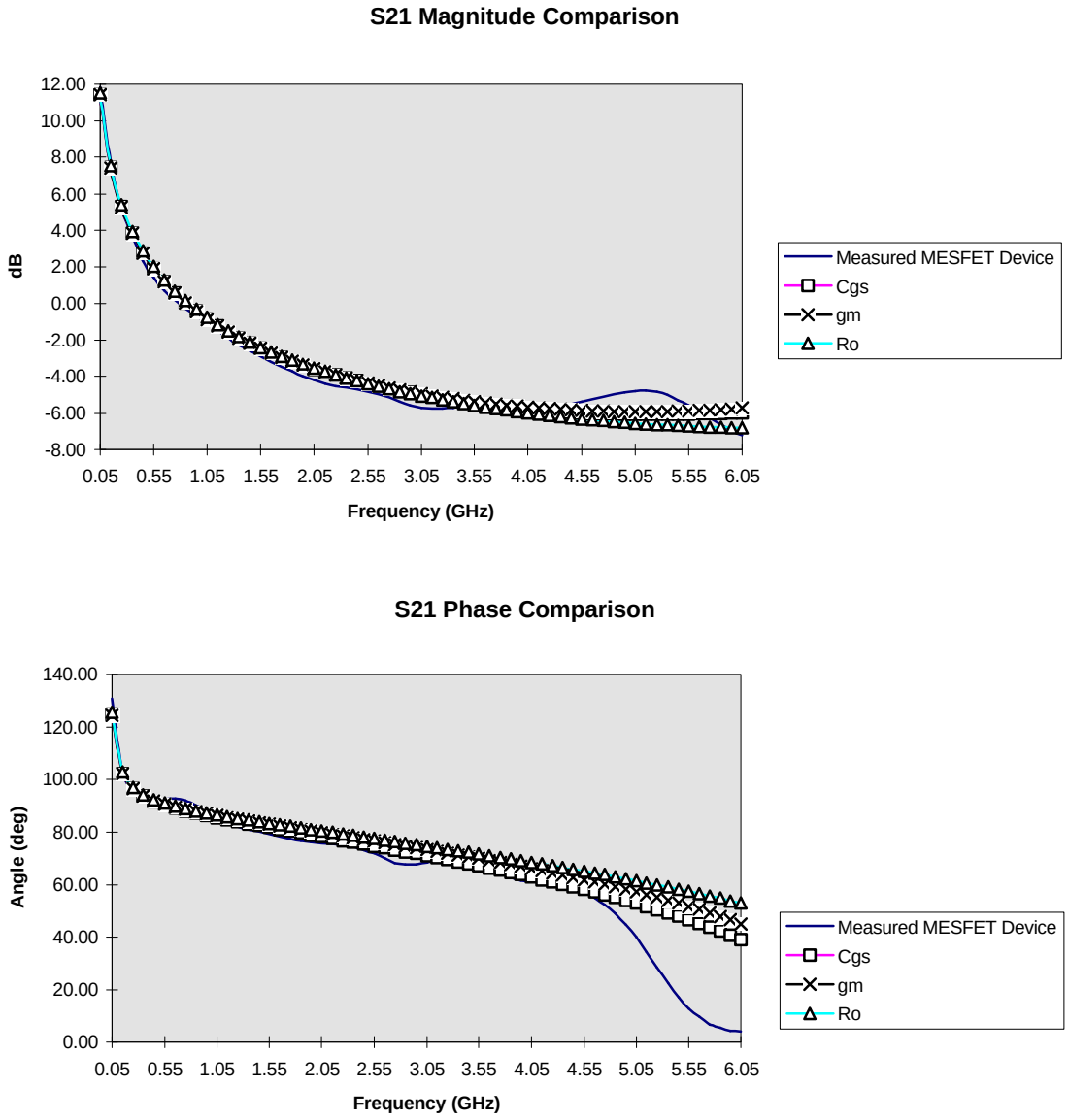

Figure 5.17: S_{21} Sensitivity Comparison.

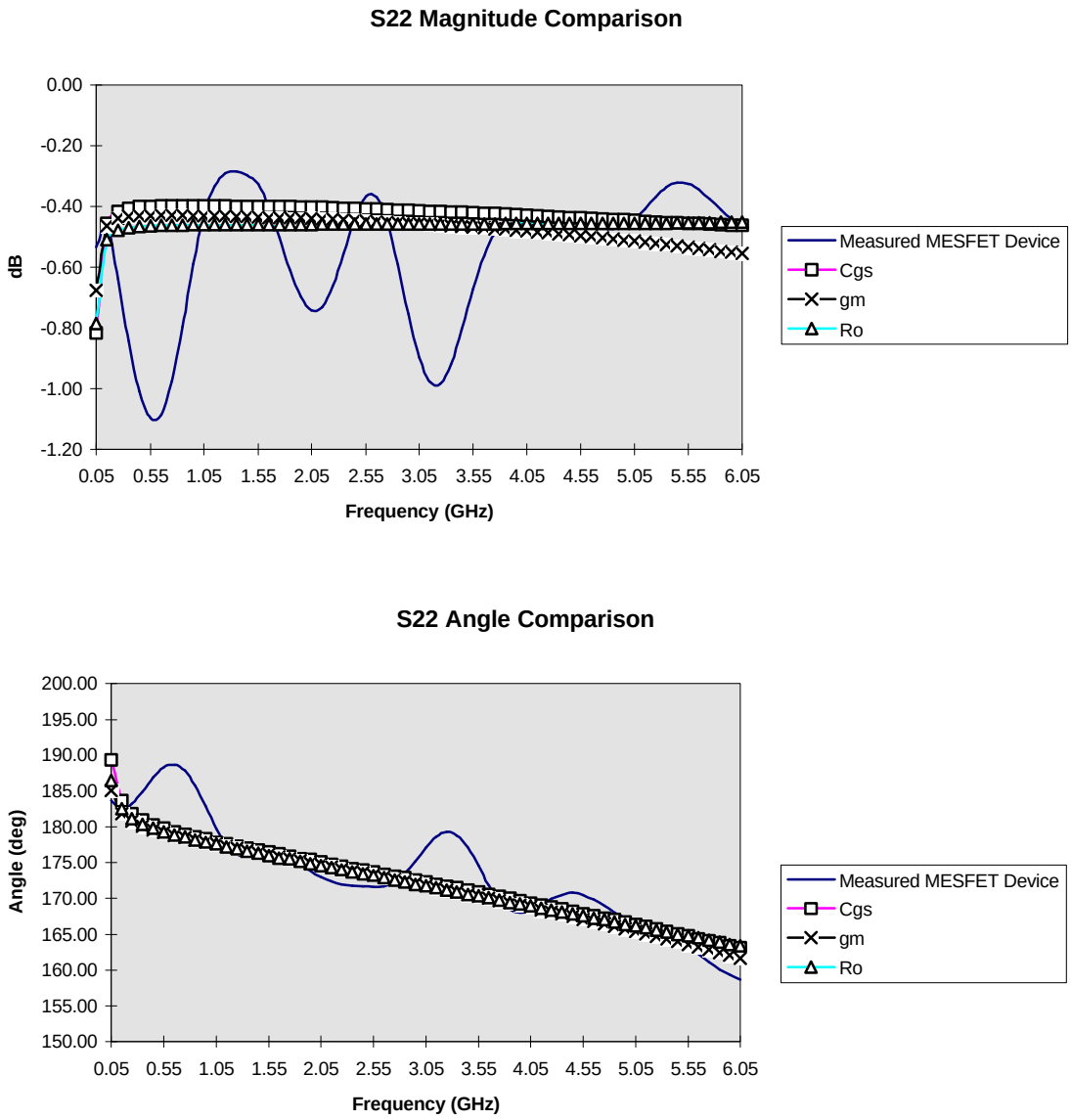

Figure 5.18: S_{22} Sensitivity Comparison.

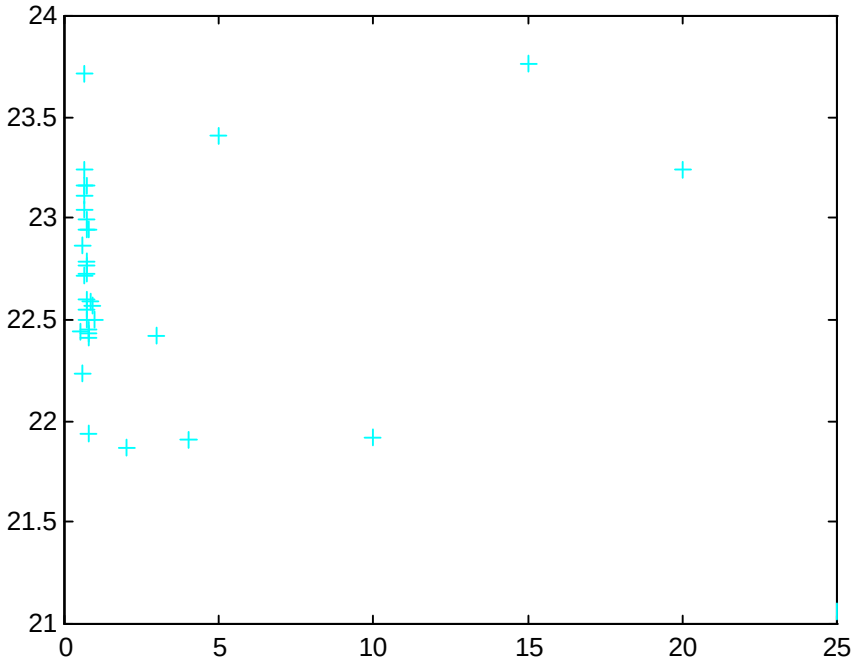

Figure 5.19: Cost Function Versus C_{gs}.

Table 5.1: Circuit Element Bounds and Starting Values.

Circuit element	Minimum	Starting	Maximum
L_g (nH)	0.05	0.123681	1.30
L_d (nH)	0.020	0.084786	1.085
L_s (nH)	0.010	0.010044	1.075
R_g (Ω)	0.1	1.445245	10.0
R_d (Ω)	1.0	2.085451	50.5
R_s (Ω)	0.01	0.010066	0.55
C_{ds} (pF)	0.01	0.024139	0.033
R_i (Ω)	0.05	1.715657	6.0
τ (ps)	2.0	5.321416	9.0
g_m (mS)	20.0	2987.407816	3500
C_{gs} (pF)	0.1	0.703602	30.3
C_{gd} (pF)	0.035	6.902162	30.06
R_o (Ω)	1.0	6.250119	5475
C_{gsext} (pF)	0	1.150036	10.0
C_{gdext} (pF)	0	0.793838	10.0
C_{dsext} (pF)	0	0.408474	10.0

Table 5.2: Cost Function Comparison For Boundary Runs.

Run	**Cost Function**	**S_{11}**	**S_{12}**	**S_{21}**	**S_{22}**
No Bounds	20.2198	3.24457	3.24457	7.95400	6.73666
Bounds	22.5524	5.28662	2.85660	7.88850	6.52073
Wide Spread	29.8436	10.5930	2.86705	8.79711	7.58639

Table 5.3: Equivalent Circuits For Different Extractions.

Circuit element	No Bounds	Bounds	Wide Spread
L_g (nH)	0.157480	0.183875	0.122935
L_d (nH)	0.186913	0.187753	0.0837879
L_s (nH)	0.0110833	0.0101390	0.0108178
R_g (Ω)	1.10155	1.58602	1.43906
R_d (Ω)	0.0101228	1.00104	2.06068
R_s (Ω)	0.0114797	0.0172276	0.0108271
C_{ds} (pF)	0.0311370	0.0201548	0.0241234
R_i (Ω)	0.588542	1.99895	1.71112
τ (ps)	10.04206	7.47925	5.31151
g_m (mS)	1317.12	1223.81	986.892
C_{gs} (pF)	0.558419	0.315232	0.565446
C_{gd} (pF)	7.11441	6.30023	5.54174
R_o (Ω)	11.3039	12.7959	16.8658
C_{gsext} (pF)	1.69517	1.86660	1.14328
C_{gdext} (pF)	-0.899193	0.0793905	0.784166
C_{dsext} (pF)	0.818402	0.00829952	0.403366

Table 5.4: Parameter Values for Sensitivity Analysis.

Circuit Element	Value	Cost Function	S_{11} Difference	S_{12} Difference	S_{21} Difference	S_{22} Difference
C_{gs} (pF)	0.69656598	22.5981	4.88322	3.22892	7.88879	6.59717
g_m (mS)	2957.5337	22.3713	4.38409	2.88839	8.47024	6.62861
R_o (Ω)	6.1876189	22.2905	4.08731	2.66213	9.13103	6.40998

Table 5.5: Equivalent Circuit Extractions for Sensitivity Analysis.

Circuit element	Cgs	gm	Ro
L_g (nH)	0.158124	0.174320	0.178775
L_d (nH)	0.183515	0.199949	0.214615
L_s (nH)	0.0187836	0.0107916	0.0100814
R_g (Ω)	1.42536	1.96111	2.05134
R_d (Ω)	1.00228	1.01971	1.03469
R_s (Ω)	0.0200679	0.0186296	0.0224925
C_{ds} (pF)	0.0114667	0.0257499	0.0165233
R_i (Ω)	0.195231	0.216561	1.09722
τ (ps)	8.99446	8.98977	8.99197
g_m (mS)	1427.26	2441.12	1963.23
C_{gs} (pF)	0.696446	0.720565	0.800504
C_{gd} (pF)	6.34144	6.34363	6.10798
R_o (Ω)	10.33423	5.75443	7.22053
C_{gsext} (pF)	1.77545	1.65752	1.18010
C_{gdext} (pF)	0.00332572	0.0117692	0.0362799
C_{dsext} (pF)	0.484573	0.559462	0.0235261

CHAPTER IV. CONCLUSION

6.1 Introduction

This conclusion sums up the lessons learned in extracting an equivalent circuit model from a MESFET device. The use of the Simplex Method is evaluated in terms of its ability as an optimizer. An indication of the direction of future work is given.

6.2 Simplex Method Evaluation

This thesis has thoroughly evaluated the Simplex Method as it applies to equivalent circuit extraction. The Simplex Method can be used to generate a function that approximates the measured S-parameters very well. However, the Simplex Method is very unstable. Although the S-parameters are satisfactorily modeled, slightly different inputs produce very different outputs. The major problem with the Simplex Method is in its physical realism; the equivalent circuit values fit the S-parameters but they are not necessarily realistic. Other methods of optimization do exist such as direction methods, simulated annealing, and neural networks. Direction methods consider the cost function in one direction at a time; the method finds a minimum and then moves to the next direction and so on until a minimum tolerance is reached. Simulated annealing allows the optimizer to range through space and possibly avoid getting stuck in a local minimum. A neural network would need a training set of data in order to learn what a good circuit extraction should be. These methods should be investigated to see if they can provide a better fit of the modeled S-parameters to the measured S-parameters. A major goal of equivalent circuit modeling is physical realism. This way a designer can predict in advance the properties of the MESFET device and verify them through S-parameters measurements and extraction.

6.3 Future Work

Future work should focus on obtaining a high degree of physical realism. The method used in this section is used by J. Micheal Golio [10]. He does, however, measure the parasitics. (He does not use the parasitic capacitances, though) The final suggestion of this thesis is to use Golio's method to determine reasonable values of seven of the sixteen parameters. Golio considers the intrinsic part of the MESFET device and makes a low frequency approximation which makes the problem solvable. The parasitic resistances are measured under forward bias of the MESFET device, and the parasitic inductances are used to eliminate any errors. If the parasitics are not determined in this way, optimization would be used to determine them and possibly slightly modify the seven other parameters to improve the fit. Another possibility is to use the Simplification of the General Model described in Chapter III. Using Golio's model or the Simplification of the General Model would enable the circuit to be extracted on a smaller scale; there are enough equations and enough unknowns. This would give reasonable bounds to some of the equivalent circuit

parameters. Equivalent circuit optimization is a major part of the semiconductor industry and software companies have teams of engineers dedicated to solving the equivalent circuit problem.

APPENDIX A: MFET FORTRAN MODULES

A.1 Introduction

This section contains a brief explanation of all the FORTRAN modules used in the MFET code. Also included is a listing of all the source code.

A.2 Module Explanation

The modules needed to run this code are: START, MFET, ANG_CHEC, AMEOBA_BC, FUNK, Y_TO_S, DETERM, COMP_MULT, COMP_DIV, COMP_ADD, COMP_SUB, B_CHECK.
START: This module starts the execution of the program. It reads an ASCII file of S-parameters in Magnitude-Angle format. The format of the file is:

frequency S_{11}(mag) S_{11}(ang) S_{21}(mag) S_{21}(ang) S_{12}(mag) S_{12}(ang) S_{22}(mag) S_{22}(ang).

This module converts the S-parameters to real-imaginary format. This module will also take the output equivalent circuit and generate modeled S-parameters by calling the routine Y_TO_S and write them to a a file. Next the MFET routine is called.

MFET: This module reads in the starting point of the equivalent circuit model. The circuit model must be place in a file called FETModel.dat. This module also generates the initial points of the Simplex. It calls the module FUNK and the module AMOEBA_BC.

FUNK: This module has the cost function in it. It also calls the routine Y_TO_S which takes the Y-parameters

AMOEBA_BC: This contains the Simplex Method optimizer. Also include in it is a call to the routine B_CHECK which makes sure the Simplex does not reflect out of the bounded space.

Y_TO_S: This module contains transformations of Y-parameters to Z-parameters and adds the parasitic resistances and inductances. It takes the Z-parameters and transforms them to Y-parameters and then includes the effects of the parasitic capacitances. Finally, it takes these Y-parameters and converts them to S-parameters.

DETERM: This finds the determinant of a 2X2 matrix.

COMP_ADD, COMP_SUB, COMP_DIV, COMP_MULT: These routines perform complex addition, subtraction, multiplication, and division respectively.

ANG_CHEC: This places the phase of the modeled S-parameters in the correct quadrant.
B_CHECK: This makes sure the Simplex does not reflect or expand past the boundaries of a defined space.

A.3 Module Listings

```
      PROGRAM START
      REAL s11x,s11y,s12x,s12y,s21x,s21y,s22x,s22y
      REAL s11mag(100),s11ang(100),s12mag(100),s12ang(100)
     +,s21mag(100),s21ang(100),s22ang(100),s22mag(100),
     +freq(100)
      REAL mags11,mags12,mags21,mags22,mags11m,mags12m,
     +mags21m,mags22m
      REAL angs11,angs12,angs21,angs22,angs11m,angs12m,
     +angs21m,angs22m
      REAL pi,omega(100),ghz,xmod(16),lg,ld,ls,Rg,Rs,Cds,
     +Ri,tau,gm,Cgs,Cgd,Ro,Cgsext,Cdsext,Cgdext,eof
      INTEGER i,nfreq
      COMMON /sparam/ s11x(100),s11y(100),s12x(100),s12y(100)
     +,s21x(100),s21y(100),s22x(100),s22y(100)


      COMMON omega,nfreq

      Open(15,file='model.dat',status='old')
      Read(15,*,end=20)lg,ld,ls,Rg,Rd,Rs,Cds,Ri,tau,gm,Cgs,Cgd,Ro,
     +Cgsext,Cgdext,Cdsext,eof

   20 close(15)



      xmod(1)=lg
      xmod(2)=ld
      xmod(3)=ls
      xmod(4)=rg
      xmod(5)=rd
      xmod(6)=rs
      xmod(7)=cds
      xmod(8)=ri
      xmod(9)=tau
      xmod(10)=gm
      xmod(11)=cgs
      xmod(12)=cgd
      xmod(13)=ro
      xmod(14)=cgsext
      xmod(15)=cgdext
      xmod(16)=cdsext
```

```
nfreq=1
      OPEN(11,FILE='f4_d31.dat',status='old')
    5 READ(11,*,end=30) freq(nfreq),s11mag(nfreq),s11ang(nfreq)
     +,s21mag(nfreq),s21ang(nfreq),
     +s12mag(nfreq),s12ang(nfreq),s22mag(nfreq),s22ang(nfreq)
      nfreq=nfreq+1
      print*,nfreq
      goto 5
   30 continue
      ghz=1e9


      pi=2*ACOS(0.0)
      do j=1,nfreq
        omega(j)=2*pi*freq(j)*ghz

      enddo



C     CONVERT MAG-ANG to xy

      CLOSE(11)

      do j=1,19
        s11x(j)=s11mag(j)*cos(s11ang(j)*pi/180.0)
        s11y(j)=s11mag(j)*sin(s11ang(j)*pi/180.0)
        s12x(j)=s12mag(j)*cos(s12ang(j)*pi/180.0)
        s12y(j)=s12mag(j)*sin(s12ang(j)*pi/180.0)
        s21x(j)=s21mag(j)*cos(s21ang(j)*pi/180.0)
        s21y(j)=s21mag(j)*sin(s21ang(j)*pi/180.0)
        s22x(j)=s22mag(j)*cos(s22ang(j)*pi/180.0)
        s22y(j)=s22mag(j)*sin(s22ang(j)*pi/180.0)
      enddo

      CALL MFET(xmod)
      open(12,file='allMA',status='new')
      open(13,file='allRI',status='new')
      do jj=1,19
      om=omega(jj)
      CALL Y_TO_S(xmod,om,S11R_M,S11I_M,S12R_M,
     +S12I_M,S21R_M,S21I_M,S22R_M,S22I_M)
      write(13,100)freq(jj),S11R_M,S11I_M,S12R_M,
     +S12I_M,S21R_M,S21I_M,S22R_M,S22I_M,s11x(jj),
```

```
     +s11y(jj),s12x(jj),s12y(jj),s21x(jj),s21x(jj),
     +s22y(jj)
C
C    CONVERT to magnitude,angle
C

      mags11m=SQRT(S11R_M**2 + S11I_M**2)
      mags12m=SQRT(S12R_M**2 + S12I_M**2)
      mags21m=SQRT(S21R_M**2 + S21I_M**2)
      mags22m=SQRT(S22R_M**2 + S22I_M**2)

      angs11m=(180.0/pi)*atan(S11I_M/S11R_M)
      call ang_chec(angs11m,S11I_M,S11R_M)

      angs12m=(180.0/pi)*atan(S12I_M/S12R_M)
      call ang_chec(angs12m,S12I_M,S12R_M)

      angs21m=(180.0/pi)*atan(S21I_M/S21R_M)
      call ang_chec(angs21m,S21I_M,S21R_M)

      angs22m=(180.0/pi)*atan(S22I_M/S22R_M)
      call ang_chec(angs22m,S22I_M,S22R_M)

      mags11=SQRT(s11x(jj)**2 + s11y(jj)**2)
      mags12=SQRT(s12x(jj)**2 + s12y(jj)**2)
      mags21=SQRT(s21x(jj)**2 + s21y(jj)**2)
      mags22=SQRT(s22x(jj)**2 + s22y(jj)**2)

      angs11=(180.0/pi)*atan(s11y(jj)/s11x(jj))
      angs12=(180.0/pi)*atan(s12y(jj)/s12x(jj))
      angs21=(180.0/pi)*atan(s21y(jj)/s21x(jj))
      angs22=(180.0/pi)*atan(s22y(jj)/s22x(jj))

      write(12,100)freq(jj),mags11m,angs11m,mags12m,angs12m,
     +mags21m,angs21m,mags22m,angs22m,mags11,angs11,mags12,
     +angs12,mags21,angs21,mags22,angs22
      enddo
      close(12)
      close(13)
      open(12,file='FETModel.new',status='new')
      write(12,*)xmod
      close(12)
```

```
      print*,'meas',s11x(1),s11y(1)
      print*,'meas',s12x(1),s12y(1)
      print*,'meas',s21x(1),s21y(1)
      print*,'meas',s22x(1),s22y(1)
  100 FORMAT(17(E12.4,2x))

      END
```

```
SUBROUTINE MFET(xmod)
      REAL p(17,16),ftol,y(17),xmod(16)
      REAL p1(16),p2(16),p3(16),p4(16),p5(16)
     +,p6(16),p7(16),p8(16),p9(16),p10(16),p11(16),
     +p12(16),p13(16),p14(16),p15(16),p16(16)
     +,p17(16),pn,qn,z
      REAL lg,ld,ls


      integer iter,mm


      do mm=1,16

        p(1,mm)=xmod(mm)
        print*,p(1,mm)
      enddo



      ndim=16
      z=16.0
      s=0.1
      s1=.2
C     pn=((sqrt(z+1)-1+z)/(z*SQRT(2.0)))*s
C     qn=((sqrt(z+1)-1)/(z*SQRT(2.0)))*s
      do jj=2,ndim+1

        do kk=1,ndim
          if (kk.eq.(jj-1)) then
            p(jj,kk)=p(1,kk) + s*p(1,kk)
          else
            p(jj,kk)=p(1,kk)
          endif




        enddo


      enddo
```

```
ftol=1e-12


iter=0
do ll=1,ndim
   p1(ll)=p(1,ll)
   p2(ll)=p(2,ll)
   p3(ll)=p(3,ll)
   p4(ll)=p(4,ll)
   p5(ll)=p(5,ll)
   p6(ll)=p(6,ll)
   p7(ll)=p(7,ll)
   p8(ll)=p(8,ll)
   p9(ll)=p(9,ll)
   p10(ll)=p(10,ll)
   p11(ll)=p(11,ll)
   p12(ll)=p(12,ll)
   p13(ll)=p(13,ll)
   p14(ll)=p(14,ll)
   p15(ll)=p(15,ll)
   p16(ll)=p(16,ll)
   p17(ll)=p(17,ll)
enddo



y(1)=funk(p1)


y(2)=funk(p2)

y(3)=funk(p3)

y(4)=funk(p4)

y(5)=funk(p5)

y(6)=funk(p6)
y(7)=funk(p7)
y(8)=funk(p8)

y(9)=funk(p9)
```

```
      y(10)=funk(p10)
      y(11)=funk(p11)

      y(12)=funk(p12)
      y(13)=funk(p13)
      y(14)=funk(p14)
      y(15)=funk(p15)
      y(16)=funk(p16)
      y(17)=funk(p17)




      CALL AMOEBA(p,y,17,16,16,ftol,funk,iter)
      do ii=1,16
        xmod(ii)=p(1,ii)
      enddo

C     print*,y
C     print*,iter
C     print*,term1,term2,term3,term4
      END
```

```
SUBROUTINE amoeba(p,y,mp,np,ndim,ftol,funk,iter)
      INTEGER iter,mp,ndim,np,NMAX,ITMAX,i2,i1,kk
      REAL ftol,p(mp,np),y(mp),funk,psave(16),qw(16)
      LOGICAL bound
      PARAMETER (NMAX=20,ITMAX=5000)
      EXTERNAL funk
C Uses amotry, funk




      INTEGER i,ihi,ilo,inhi,j,m,n,q,r,s
      REAL rtol,sum,swap,ysave,ytry,psum(NMAX),amotry,sumy,sume
      REAL psum2(NMAX),sum2,qr(16)
      bound=.true.



      iter=0
      ncount=0
      tcount=0
      qcount=0
    1 do n=1,ndim
          sum=0.
          do m=1,ndim+1
              sum=sum+p(m,n)

          enddo
          psum(n)=sum

      enddo
    2 ilo=1


      if (y(1).gt.y(2)) then
         ihi=1
         inhi=2
      else
         ihi=2
         inhi=1
      endif
      do i=1,ndim+1
          if (y(i).le.y(ilo)) ilo=i
          if (y(i).gt.y(ihi)) then
```

```
        inhi=ihi
        ihi=i
    else if(y(i).gt.y(inhi)) then
        if (i.ne.ihi) inhi=i
    endif
enddo

sumy=0
sume=0

do q = 1,ndim
  sum2=0
  do r=1,ndim+1
  if (r.ne.ihi) then
    sum2=sum2+ p(r,q)

  endif
  enddo

  psum2(q)=sum2/ndim
enddo


sumy=funk(psum2)

do s=1,m
  sume=sume+ (y(s)-sumy)**2
enddo



rtol=sqrt(sume/ndim)
print*,'rtol=',rtol


if (rtol.lt.ftol) then
    swap=y(1)
    y(1)=y(ilo)
    y(ilo)=swap
    do n=1,ndim
      swap=p(1,n)
      p(1,n)=p(ilo,n)
      p(ilo,n)=swap
    enddo
```

```
          return
        endif

        if (iter.ge.ITMAX) then


          print*, 'ITMAX exceeded in amoeba'
          return
        endif
        iter=iter+2
C
C     This saves the old high point
C
        do i1=1,ndim

          psave(i1)=p(ihi,i1)
          print*,psave(i1)
        enddo
        ytry=amotry(p,y,psum,mp,np,ndim,funk,ihi,-1.0)
        do ii=1,ndim
          print*,p(ihi,ii)
          qr(ii)=p(ihi,ii)
        enddo

        call b_check(qr,bound)
        if (bound) then

          if (ytry.le.y(ilo)) then

            ytry=amotry
     +(p,y,psum,mp,np,ndim,funk,ihi,2.0)

            do kk=1,ndim
              qw(kk)=p(ihi,kk)
            enddo
            call b_check(qw,bound)
            if (bound) then
              goto 2
            else
              do k1=1,ndim
                p(ihi,k1)=qw(k1)
              enddo
              ysave=y(ihi)
```

```
            call contract(p,y,psum,mp,np,ndim
     +,funk,ihi,ysave,more)
            if (more) then
               iter=iter+ndim
               goto 1
            else
               iter=iter-1
               goto 2
            endif
           endif
         elseif (ytry.ge.y(inhi))then
            ysave=y(ihi)
            print*,mp,np,ndim,ihi
            call contract(p,y,psum,mp,np,ndim
     +,funk,ihi,ysave,more)

            if (more) then
               iter=iter+ndim
               goto 1
            else
               iter=iter-1
               goto 2
            endif

         endif
       else
C
C    This puts the old high point back
C

       do i2=1,ndim
         print*,psave(i2)
         print*,p(ihi,i2)
         p(ihi,i2)=psave(i2)
       enddo
       do j2=1,ndim
         print*,p(ihi,j2)
       enddo
       stop
            ysave=y(ihi)
            call contract(p,y,psum,mp,np,ndim
     +,funk,ihi,ysave,more)
            if (more) then
```

```
              iter=iter+ndim
              goto 1
            else
              iter=iter-1
              goto 2
            endif
          endif

          END

          FUNCTION amotry(p,y,psum,mp,np,ndim,funk,ihi,fac)
          INTEGER ihi,mp,ndim,np,NMAX
          REAL amotry,fac,p(mp,np),psum(np),y(mp),funk
          PARAMETER (NMAX=20)
          EXTERNAL funk
      C Uses funk
          INTEGER j
          REAL fac1,fac2,ytry,ptry(NMAX)
          fac1=(1.-fac)/ndim
          fac2=fac1-fac

          do j=1,ndim
            ptry(j)=psum(j)*fac1-p(ihi,j)*fac2

          enddo
          ytry=funk(ptry)
          if (ytry.lt.y(ihi)) then
            y(ihi)=ytry
            do j=1,ndim
              psum(j)=psum(j)-p(ihi,j)+ptry(j)
              p(ihi,j)=ptry(j)
            enddo
          endif
          amotry=ytry
          return
          END
          REAL FUNCTION funk(x)
          REAL x(16),omega
          REAL s11x,s11y,s12x,s12y,s21x,s21y,s22x,s22y
          integer nfreq
          REAL S11R_M,S11I_M,S12R_M,S12I_M,S21R_M,
         +S21I_M,S22R_M,S22I_M
          common /sparam/ s11x(100),s11y(100),s12x(100),
         +s12y(100),s21x(100),s21y(100),s22x(100),s22y(100)
```

```
      common omega(100),nfreq



      term1=0.0
      term2=0.0
      term3=0.0
      term4=0.0


      do j=1,19

      om=omega(j)


      CALL Y_TO_S(x,om,S11R_M,S11I_M,S12R_M,S12I_M,S21R_M,
     +S21I_M,S22R_M,S22I_M)




        term1=term1 + abs(s11x(j)-S11R_M)
     +   + abs(s11y(j)-S11I_M)
        term2=term2 + abs(s12x(j)-S12R_M)
     +   + abs(s12y(j)-S12I_M)
        term3=term3 + abs(s21x(j)-S21R_M)
     +   + abs(s21y(j)-S21I_M)
        term4=term4 + abs(s22x(j)-S22R_M)
     +   + abs(s22y(j)-S22I_M)
      enddo
funk=term1+term2+term3+term4
      print*,funk,term1,term2,term3,term4


      return

      end
```

```
      SUBROUTINE B_CHECK(ptry,np)

      REAL ptry(np),lb(16)
      REAL ub(16)

      lb(1)=0.05
      lb(2)=0.020
      lb(3)=0.010
      lb(4)=0.1
      lb(5)=1
      lb(6)=0.01
      lb(7)=0.01
      lb(8)=0.05
      lb(9)=2
      lb(10)=20
      lb(11)=0.1
      lb(12)=0.035
      lb(13)=1
      lb(14)=0
      lb(15)=0
      lb(16)=0

      ub(1)=1.30
      ub(2)=1.085
      ub(3)=1.075
      ub(4)=10
      ub(5)=50.5
      ub(6)=0.55
      ub(7)=0.033
      ub(8)=6
      ub(9)=9.0
      ub(10)=3500
      ub(11)=30.3
      ub(12)=30.06
      ub(13)=5475
      ub(14)=10.0
      ub(15)=10.0
      ub(16)=10.0

      do j=1,16

         if (ptry(j).GT.ub(j)) then
C             bound=.false.
ptry(j)=ub(j) - .2*ub(j)
```

```
        elseif (ptry(j).LT.lb(j)) then
C             bound=.false.
ptry(j)=lb(j) + .2*lb(j)
        endif
     enddo

      RETURN
      end
```

```
 SUBROUTINE Y_TO_S(xmod,om,S11R_M,S11I_M,S12R_M,
+S12I_M,S21R_M,S21I_M,S22R_M,S22I_M)
 REAL y11R,y11I,y12R,y12I,y21R,y21I,y22R,y22I
 REAL xmod(16),pf,nH,ms

 REAL om,cgs,cgd,ri,gm,cds,tau,ro,D
 REAL ld,ls,lg,rg,rd,rs
 REAL z11R,z11I,z12R,z12I,z21R,z21I,z22R,z22I
 REAL Z11R_,Z11I_,Z12R_,Z12I_,Z21R_,
+Z21I_,Z22R_,Z22I_
 REAL Y11R_,Y11I_,Y12R_,Y12I_,Y21R_,
+Y22R_,Y22I_
 REAL y11_nR,y11_nI,y12_nR,y12_nI,
+y21_nR,y21_nI,y22_nR,y22_nI
 REAL det1R,det1I,det2R,det2I,st1R,st1I,
+st2R,st2I,st3R,st3I,st4R,st4I
 REAL S11R_M,S11I_M,S12R_M,S12I_M,S21R_M
+,S22R_M,S22I_M

 nH=1e-9
 pf=1e-12
 ms=1e-3
 ps=1e-12

 lg=xmod(1)
 ld=xmod(2)
 ls=xmod(3)
 rg=xmod(4)
 rd=xmod(5)
 rs=xmod(6)
 cds=xmod(7)
 ri=xmod(8)
 tau=xmod(9)
 gm=xmod(10)
 cgs=xmod(11)
 cgd=xmod(12)
 ro=xmod(13)
 cgsext=xmod(14)
 cgdext=xmod(15)
 cdsext=xmod(16)


 D=1+(om*cgs*ri*pf)**2
```

```
      y11R=ri*((cgs*pf*om)**2)/D

      y11I=om*(cgs*pf/D +cgd*pf)

      y12R=0.0

      y12I=-om*cgd*pf

      y21R=gm*ms*(cos(om*tau*ps)-sin(om*tau*ps)*ri*
     Kcgs*pf*om)/D


      y21I=-gm*ms*cos(om*tau*ps)*ri*cgs*pf*om/D
     K-sin(om*tau*ps)*gm*ms/D - om*cgd*pf

      y22R=1/ro
      y22I=om*(cds +cgd)*pf




C     Convert the y-matrix to the z-matrix

C     Compute the determinate of y

      CALL DETERM(y11R,y11I,y12R,y12I,y21R,y21I
     +,y22R,y22I,det1R,det1I)

C     Results of the multiplication are stored in e3,f3



C     Divide each y by the determinant of the matrix

C     FIRST y11

      CALL COMP_DIV(y11R,y11I,det1R,det1I,z11R,z11I)
```

```
C     y12

      CALL COMP_DIV(y12R,y12I,det1R,det1I,z12R,z12I)

C     y21

      CALL COMP_DIV(y21R,y21I,det1R,det1I,z21R,z21I)



C     y22


      CALL COMP_DIV(y22R,y22I,det1R,det1I,z22R,z22I)


C     Now add the parasitic inductances


      Z11R_=z11R + rg +rs
      Z11I_=z11I + om*(lg+ls)*nh

      Z12R_=z12R +rs
      Z12I_=z12I +om*ls*nh

      Z21R_=z21R +rs
      Z21I_=z21I +om*ls*nh

      Z22R_=z22R +rd +rs
      Z22I_=z22I +om*(ld+ls)*nh



C     Now convert to y parameters

      CALL DETERM(Z11R_,Z11I_,Z12R_,Z12I_,Z21R_,
     +Z21I_,Z22R_,Z22I_,det2R,det2I)


      CALL COMP_DIV(Z11R_,Z11I_,det2R,
     +det2I,y11_nR,y11_nI)

      CALL COMP_DIV(Z12R_,Z12I_,det2R
     +,det2I,y12_nR,y12_nI)
```

```
      CALL COMP_DIV(Z21R_,Z21I_,det2R,
     +det2I,y21_nR,y21_nI)

      CALL COMP_DIV(Z22R_,Z22I_,det2R
     +,det2I,y22_nR,y22_nI)


C     Now subtract the parasitic capacitances

      Y11R_=50.0*y11_nR

      Y11I_=50.0*(y11_nI + om*(cgdext + cgsext)*pf)

      Y12R_=50.0*y12_nR

      Y12I_=50.0*(y12_nI - om*(cgdext*pf))

      Y21R_=50.0*y21_nR

      Y21I_=50.0*(y21_nI - om*(cgdext*pf))

      Y22R_=50.0*y22_nR

      Y22I_=50.0*(y22_nI + om*(cgdext + cdsext)*pf)


C     Now convert to s-parameters

      CALL COMP_MULT(Y12R_,Y12I_,Y21R_,Y21I_,st1R,st1I)

      Y11R_=Y11R_ + 1.0

      Y22R_=Y22R_ + 1.0

      CALL COMP_MULT(Y11R_,Y11I_,Y22R_,Y22I_,st2R,st2I)


      CALL COMP_SUB(st2R,st2I,st1R,st1I,deltR,deltI)
```

```
      Y11R_=-(Y11R_ - 1.0) + 1.0

      Y11I_=-Y11I_

      CALL COMP_MULT(Y11R_,Y11I_,Y22R_,Y22I_,st3R,st3I)


      CALL COMP_ADD(st3R,st3I,st1R,st1I,st4R,st4I)

C     Figure out S11

      CALL COMP_DIV(st4R,st4I,deltR,deltI,S11R_M,S11I_M)

C     Figure out S12

      Y12R_=-2*Y12R_

      Y12I_=-2*Y12I_

      CALL COMP_DIV(Y12R_,Y12I_,deltR,deltI,S12R_M,S12I_M)

C     Figure out S21

      Y21R_=-2.0*Y21R_

      Y21I_=-2.0*Y21I_

      CALL COMP_DIV(Y21R_,Y21I_,deltR,deltI,S21R_M,S21I_M)

C     Figure out S22

      Y22R_=1.0-(Y22R_ - 1.0)
      Y22I_=-Y22I_

      Y11R_= -Y11R_ +2
      Y11I_= -Y11I_


      CALL COMP_MULT(Y11R_,Y11I_,Y22R_,Y22I_,st5R,st5I)

          CALL COMP_ADD(st5R,st5I,st1R,st1I,st6R,st6I)
```

```
      CALL COMP_DIV(st6R,st6I,deltR,deltI,S22R_M,S22I_M)

      RETURN

      END
SUBROUTINE DETERM(r,s,t,u,w,x,y,z,det1,det2)
      REAL w,x,y,z,det1,det2,st1,st2,r,s,t,u

      CALL COMP_MULT(r,s,y,z,st1,st2)

      CALL COMP_MULT(w,x,t,u,st3,st4)

      CALL COMP_SUB(st1,st2,st3,st4,det1,det2)

      RETURN

      END

      SUBROUTINE COMP_ADD(a3,b3,e3,f3,r1,r2)

      REAL a3,b3,e3,f3,r1,r2

      r1=a3+e3

      r2=b3+f3

      RETURN

      END


      SUBROUTINE COMP_SUB(a3,b3,e3,f3,r1,r2)

      REAL a3,b3,e3,f3,r1,r2

      r1=a3-e3

      r2=b3-f3

      RETURN

      END
```

```
      SUBROUTINE COMP_MULT(a1,b1,a2,b2,a3,b3)
      REAL a1,b1,a2,b2,a3,b3
      a3=a1*a2 - b1*b2
      b3=a1*b2 + a2*b1
      RETURN
      END

      SUBROUTINE COMP_DIV(a1,b1,a2,b2,a3,b3)
      REAL a1,b1,a2,b2,a3,b3
      a3=(a1*a2 + b1*b2)/(a2**2 +b2**2)
      b3=(a2*b1 - b2*a1)/(a2**2 +b2**2)
      RETURN
      END
      SUBROUTINE ang_chec(ang,y,x)
      REAL x,y,ang
C
C     Check for first quadrant
C
      if (y.gt.0.AND.x.gt.0) then
         ang=ang
C
C     Check for the second quadrant
C
      elseif(y.gt.0.and.x.lt.0) then
         ang=ang+180.0
      elseif(y.lt.0.and.x.lt.0) then
         ang=ang+180.0
      else
         ang=ang+360.0

      endif
      RETURN
      END
```

APPENDIX B. LOOP STRUCTURE FOR WIDE SIMPLEX

```
do mm=2,ndim+1
        y1=float(mm)
        p(mm,1)=p(1,1) + (y1/2)*p(1,1)
        p(mm,2)=p(1,2) + y1*p(1,2)
        p(mm,3)=p(1,3) + y1*p(1,3)
        p(mm,4)=p(1,4) + (y1/3)*p(1,4)
        p(mm,5)=p(1,5) + y1*p(1,5)
        p(mm,6)=p(1,6) + y1*2.0*p(1,6)
        p(mm,7)=p(1,7) + (y1/64.0)*p(1,7)
        p(mm,8)=p(1,8) + (y1/5.0)*p(1,8)
        p(mm,9)=p(1,9) + (y1/6.0)*p(1,9)
        p(mm,10)=p(1,10) -y1*40.0*p(1,10)
        p(mm,11)=p(1,11) +16.0*y1*p(1,11)
        p(mm,12)=p(1,12) + 16.0*y1*p(1,12)
        p(mm,13)=p(1,13) + 100*y1*p(1,13)
        p(mm,14)=p(1,14) + (y1/2.0)*p(1,14)
        p(mm,15)=p(1,15) + y1*p(1,15)
        p(mm,16)=p(1,16) + y1*p(1,16)

    enddo
```

APPENDIX C. MEASUREMENT DATA FILE

The data file has the following format:
frequency S_{11}(mag) S_{11}(ang) S_{21}(mag) S_{21}(ang) S_{12}(mag) S_{12}(ang) S_{22}(mag) S_{22}(ang)

0.05 0.9768 -92.89 15.1853 130.93 0.0081 43.27 0.8844 -176.34
0.15 0.9672 -148.03 5.9971 102.36 0.0117 21.81 0.8995 -177.65
0.25 0.9655 -161.16 3.344 95.33 0.0122 23.08 0.8631 -176.83
0.35 0.9647 -167.1 2.3046 92.91 0.0122 26.47 0.8234 -175.04
0.45 0.9638 -170.53 1.6982 92.44 0.0128 32.18 0.7929000000000001 -173.12
0.55 0.963 -173.03 1.384 92.57000000000001 0.0139 36.52 0.7771 -171.73
0.65 0.962 -174.56 1.177 92.74 0.015 40.87 0.7786 -171.28
0.75 0.9602000000000001 -175.91 1.0395 92.04000000000001 0.0164 43.41 0.7989000000000001 -172.13
0.85 0.9592000000000001 -176.94 0.9403 90.3 0.018 44.29 0.8325 -174.2
0.95 0.9617 -177.75 0.8487 88.82000000000001 0.0196 45.42 0.873 -177.12
1.05 0.9624 -178.67 0.7803 86.43000000000001 0.0211 45.34 0.9061 179.76
1.15 0.9627 -179.4 0.7065 84.01000000000001 0.0222 45.16 0.9262 177.4
1.25 0.9631 179.82 0.6446 82.21000000000001 0.0232 45.03 0.9350000000000001 176.12
1.35 0.9629 179.2 0.5904 81.06 0.0241 45.56 0.9369 175.82
1.45 0.9626 178.54 0.5484 80.24 0.0251 45.99 0.9341 175.99
1.55 0.9626 178.01 0.5119 79.36 0.0262 46.34 0.9274 176.07
1.65 0.9624 177.43 0.4794 78.31 0.0273 46.21 0.9123 175.84
1.75 0.9621 176.89 0.4479 77.39 0.0284 46.39 0.8909 175.35
1.85 0.9615 176.38 0.4227 76.58 0.0292 46.31 0.869 174.67
1.95 0.9612000000000001 175.91 0.3988 76.07000000000001 0.0301 46.58 0.8516 173.84
2.05 0.9607 175.38 0.3808 75.72 0.0311 47.05 0.8429 173.02
2.15 0.96 174.92 0.3643 75.46000000000001 0.0322 47.38 0.8452 172.34
2.25 0.9589 174.44 0.354 75.17 0.0335 48.09 0.8587 171.99
2.35 0.9581 174.01 0.3454 74.57000000000001 0.0352 48.63 0.8799 171.82
2.45 0.9574 173.51 0.3385 73.23 0.0371 47.51 0.9032 171.75
2.55 0.9562000000000001 173.08 0.3302 71.81 0.0385 46.39 0.9189000000000001 171.59
2.65 0.9548 172.62 0.319 69.91 0.0399 44.87 0.9187 171.73
2.75 0.9535 172.31 0.3051 68.24 0.0408 43.39 0.9023 172.29
2.85 0.9542000000000001 171.99 0.2892 67.56 0.0409 41.88 0.8728 173.45
2.95 0.9545 171.52 0.2769 67.64 0.041 41.65 0.8405 175.2
3.05 0.9542000000000001 171.15 0.2684 68.48 0.0412 42.27 0.8137 177.08
3.15 0.9547 170.62 0.2645 69.51000000000001 0.0422 42.91 0.7984 178.62
3.25 0.9546 170.17 0.2652 70.57000000000001 0.0438 43.19 0.7975 179.26
3.35 0.9549 169.68 0.2688 70.55 0.0457 43.06 0.8092 178.77
3.45 0.9542000000000001 169.22 0.2745 70 0.0477 41.96 0.8312000000000001 177.08
3.55 0.9539 168.74 0.2782 68.31 0.0495 39.94 0.8567 174.58
3.65 0.9533 168.19 0.28 66.45 0.0507 37.84 0.8787 171.93
3.75 0.9527 167.59 0.2769 64.3 0.0514 35.38 0.8939 169.72
3.85 0.9519 167.03 0.2734 62.76 0.0518 33.54 0.9018000000000001 168.42
3.95 0.9505 166.41 0.2676 61.57 0.0519 31.83 0.9055 168.04
4.05 0.9488 165.79 0.267 61.13 0.0518 30.4 0.9065 168.4
4.15 0.9463 165.09 0.266 61.04 0.0516 28.43 0.9062 169.07
4.25 0.9434 164.46 0.2696 60.52 0.0515 26.73 0.9047 169.91
4.35 0.9391000000000001 163.71 0.2736 60.05 0.0512 24.97 0.903 170.52
4.45 0.9335 162.97 0.2807 58.82 0.0513 22.77 0.9016 170.79

4.55 0.9266 162.11 0.29 57.13 0.0504 19.9 0.9005 170.51
4.65 0.9177 161.28 0.2993 54.83 0.0491 16.14 0.899 169.88
4.75 0.9069 160.39 0.3087 52.34 0.0468 11.86 0.8974 168.97
4.85 0.8923 159.54 0.317 48.86 0.0424 7.01 0.897 168.08
4.95 0.8709 158.79 0.3249 44.74 0.0367 3.05 0.8986 167.29
5.05 0.8491 158.33 0.3307 39.98 0.029 1.06 0.9028000000000001 166.7
5.15 0.8197 158.46 0.3332 34.47 0.0202 4.74 0.9103 166.21
5.25 0.7934 159.23 0.3288 28.52 0.0133 28.03 0.9184 165.74
5.35 0.7727000000000001 160.86 0.3158 22.56 0.0152 71.15000000000001 0.9257 165.06
5.45 0.7645 162.6 0.2952 17.02 0.0243 86.03 0.9288 164.3
5.55 0.7677000000000001 164.62 0.2754 12.72 0.0344 86.59 0.9281 163.27
5.65 0.7765 165.83 0.2561 9.700000000000001 0.0429 82.79000000000001 0.9236 162.22
5.75 0.7943 166.86 0.236 6.74 0.0496 78.51000000000001 0.9174 161.12
5.85 0.8069 167.13 0.2177 5.46 0.0546 74.58 0.9098000000000001 160.14
5.95 0.8242 167.32 0.2005 4.46 0.0592 71.17 0.9035 159.36
6.05 0.8336 167.06 0.1895 3.98 0.0629 68.57000000000001 0.8994 158.71

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VITA

Mark C. Lau was born at Wright-Patterson Air Force Base, Ohio in 1965. He received the B. S. degree in Physics in 1989 from George Mason University. Soon after he joined Nichols Research Corporation in Vienna, Virginia and applied his talents to solving problems in radar, laser radar, infrared data analysis, ballistic missile defense, and air traffic control. The highlight of his career at Nichols Research was participating in the On-Orbit Calibration of the Infrared Background Signature Survey (IBSS) Space Shuttle Mission. He has been a full-time student at Virginia Tech since January 1995. Mark was a Graduate Teaching Assistant and thoroughly enjoyed interacting with Virginia Tech's overachieving undergraduate engineers. He has attended every major university in the Commonwealth of Virginia except UVA, and will finally matriculate there in the Fall to further his study of semiconductor devices.