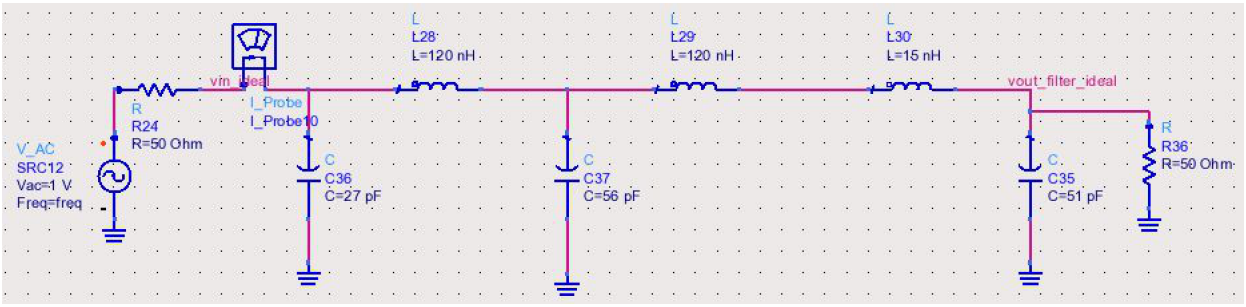
1 EE 242A Lab 2 Postlab

1.1 Measurement vs. Simulation

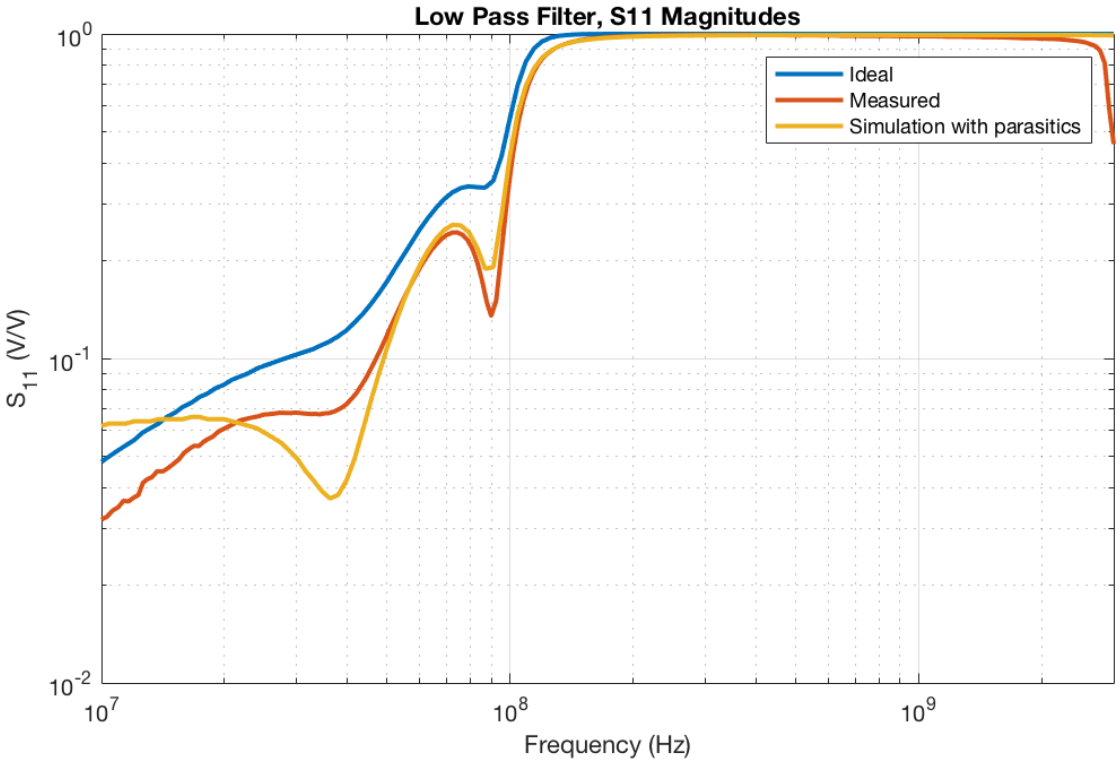
Compare measurement and simulation results by overlapping the measured S_{11} and S_{21} of your filter with the simulations. Explain differences.

1.1.1 Low Pass filter

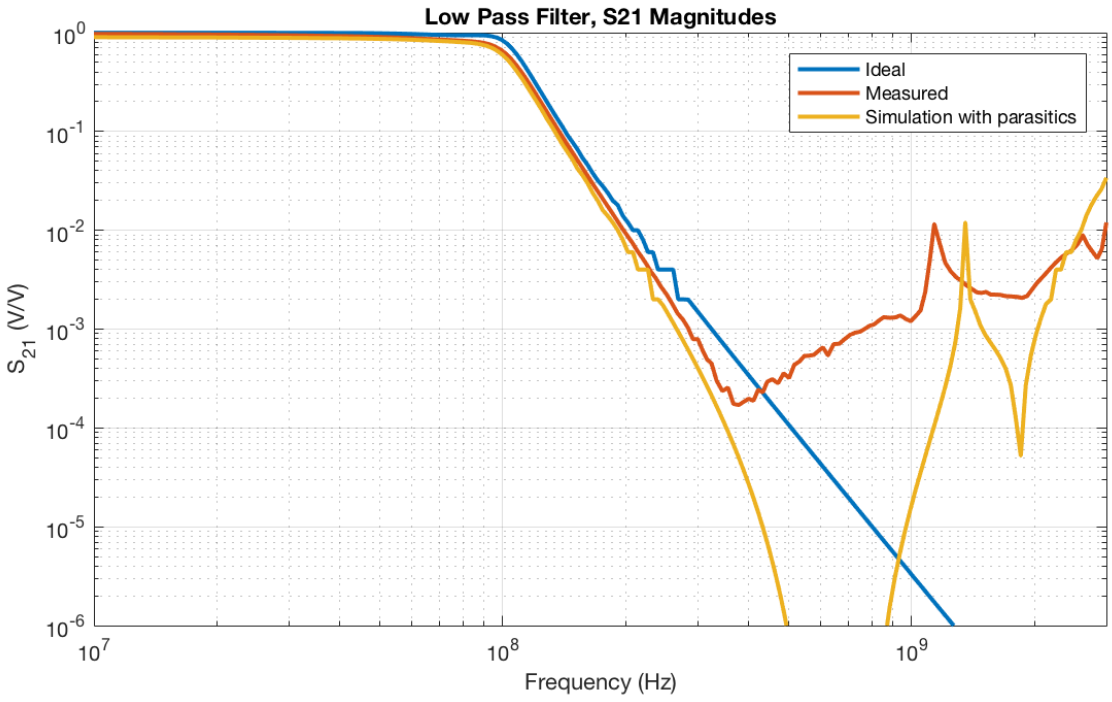
Our low pass filter was constructed in ADS to prioritize the 40 dB roll-off requirement, followed by the low ripple. Finite Q simulation flatted the roll off, giving about 2 dB attenuation at 100 MHz.



Ideal Low-Pass Filter Schematic



LPF: S11



LPF: S21

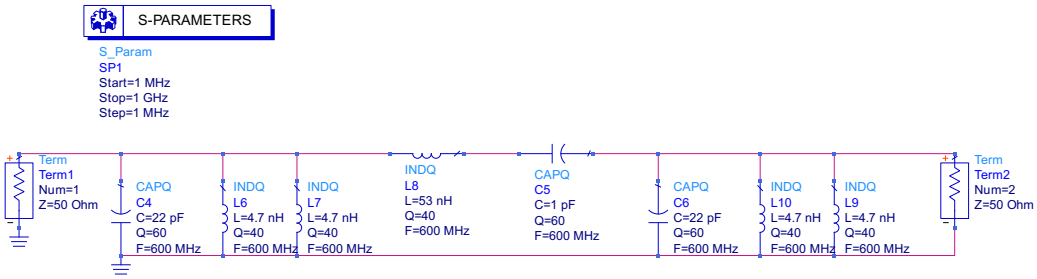
Note, the jagged edge in the S21 plot around 220 MHz are due to rounding errors in the simulation export from ADS.

The corner frequency and rolloff of our measured filter matched very well with our simulation. The rolloff is slightly greater after the corner, which we attribute to our simulation Q being overly pessimistic.

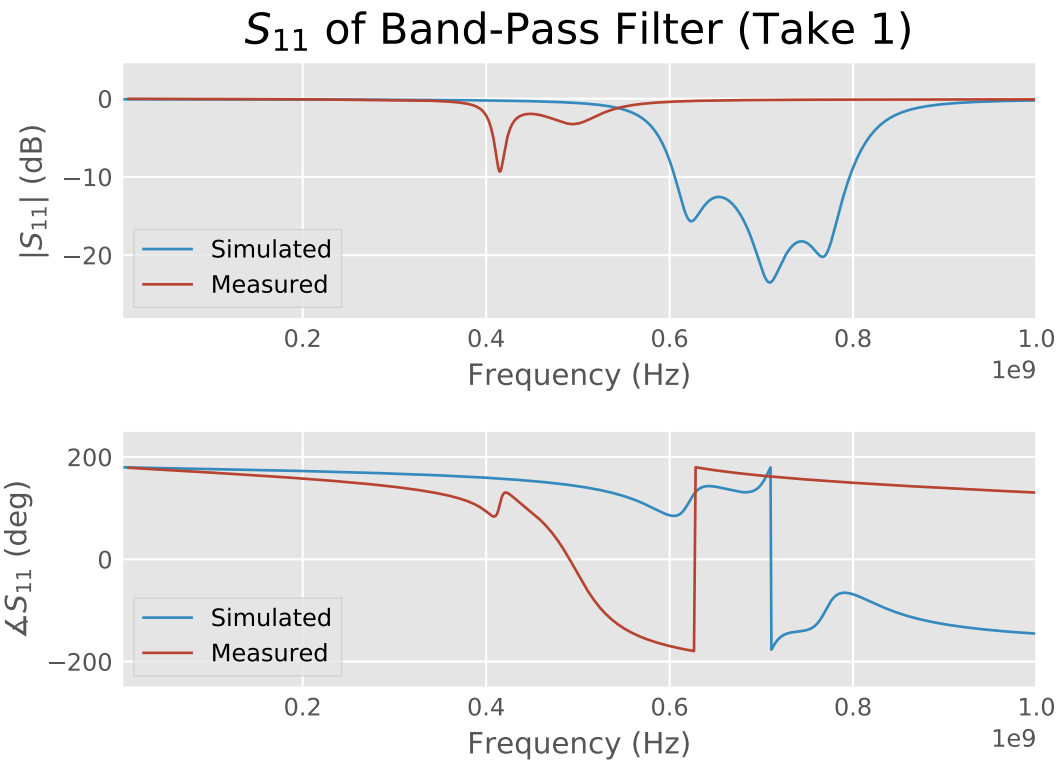
The largest difference we saw is expected inversion at higher frequency, where component self-resonance takes over. We were able to partially model this behavior, but not sufficiently well. We also see a spike around 1 GHz caused by further self-resonance with the packages and vias. We will discuss these in the later section.

1.1.2 Band Pass Filter

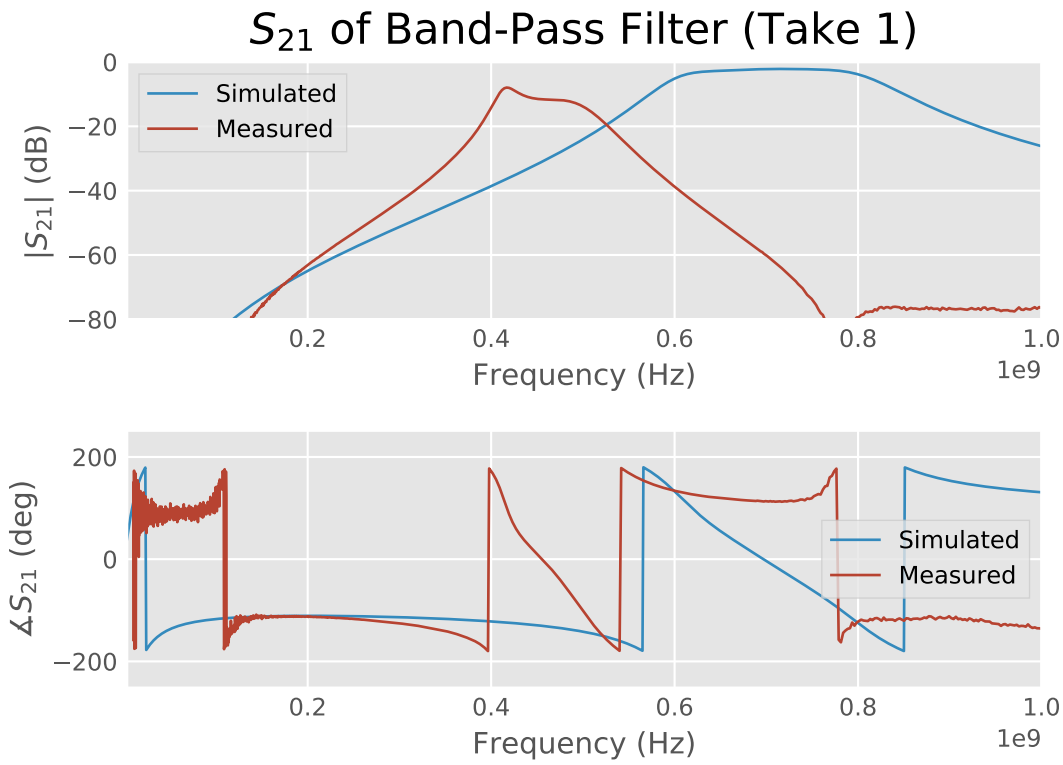
Our first band-pass filter was constructed in ADS to meet all the specs desired. We simulated it in ADS with finite Q components and constructed the circuit. The measured result was very different from simulation.



Original Band-Pass Filter Schematic



Take 1 BPF: S11



Take 1 BPF: S21

The main issue is that the center frequency of the filter doesn't match simulation. The component Q values we simulated with were also excessively pessimistic compared to what seems like a sharper response that we measured.

The reasons for this discrepancy are parasitics of the board, 0603 packages, and component tolerance variations. We were able to explain this result with the addition of via inductance, component parallel plate capacitance, and manufacturing variations ($\pm$ 10% tolerance) of very small components like the 1 pF capacitor used in series.

1.2 Filter Non-Idealities

In the design of a communication system, which filter non-ideality would you consider to be most important?

Here are some non-idealities of filters, some of which we contended with:

- Selectivity/Q of bandpass filter
- Group Delay
- Passband Ripple

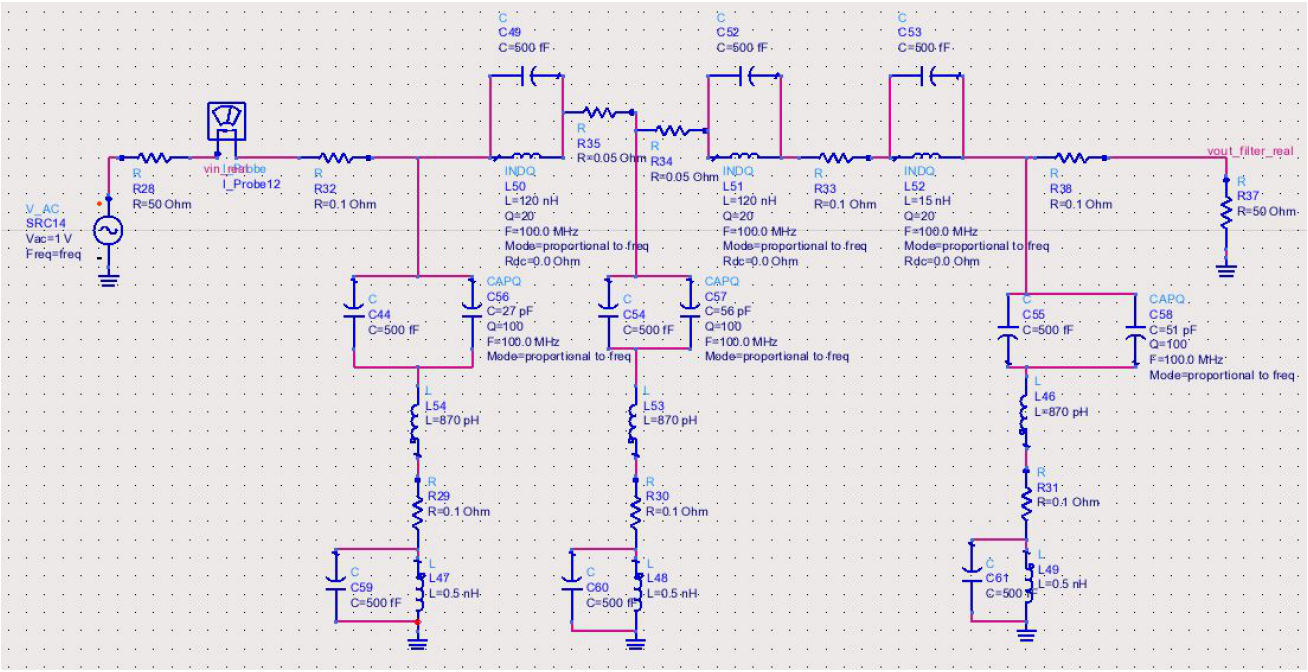
- Interference/out of band rejection
- Harmonic Distortion
- Step Response (transient behavior)
- Insertion Loss
- Input referred noise

A communication system is likely very sensitive to interference, so we think the selectivity of the filter and it's out-of-band rejection are the most important characteristics in a communication system.

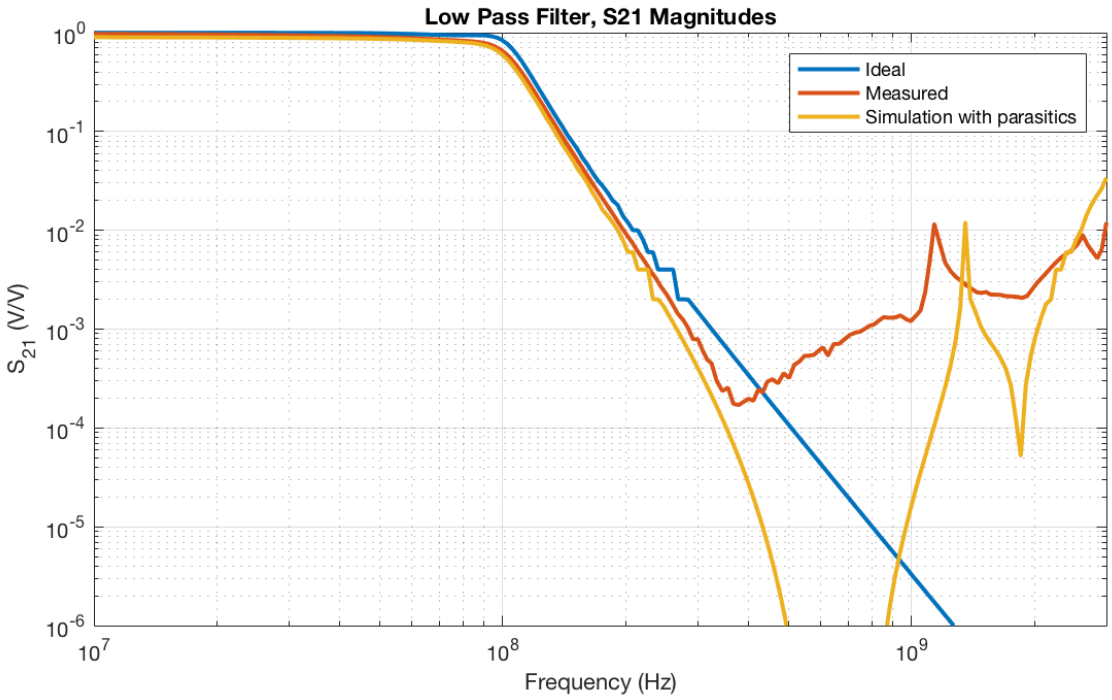
1.3 Parasitics

1.3.1 Low Pass filter

Our low pass filter measurement was nearly exactly at spec. The spec required 1dB passband ripple. We had nearly no ripple, but 3dB attenuation at 100 MHz corner frequency. The spec required 40dB attentuation at 200 MHz, which we met. As such, we chose not to redesign our filter.



Low-Pass Filter Schematic with Parasitics



LPF S21, repeated for convenience

We attempted to model the inductive inversion around 400 MHz using our parasitic model. Unfortunately, between all our parasitic models, we were unable to find this. We conjecture that the behavior should come from some resistance or finite Q that we were not able to model. Even at high frequency, our model's gain slope is too great compared to the measurement.

We were able to partly model the spike around 1 GHz. We found this to arise from package parasitics. While the spike's gain is correct, the exact frequency is off. This is likely due to component tolerances, which are 10% for inductors and 5% for capacitors.

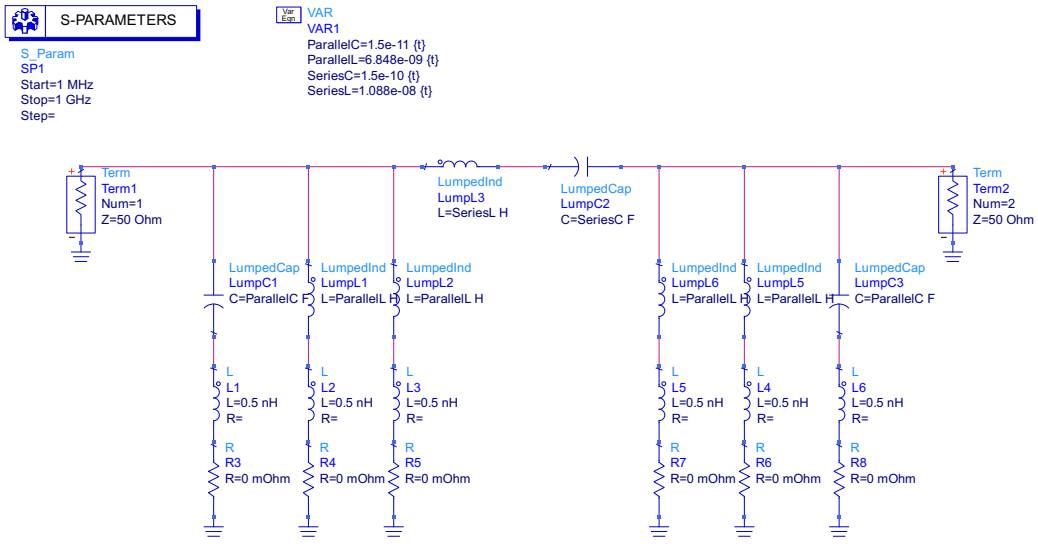
1.3.2 Band Pass filter

The bandpass filter was redesigned using a re-extracted parasitic model from lab 1. The model included as its main components:

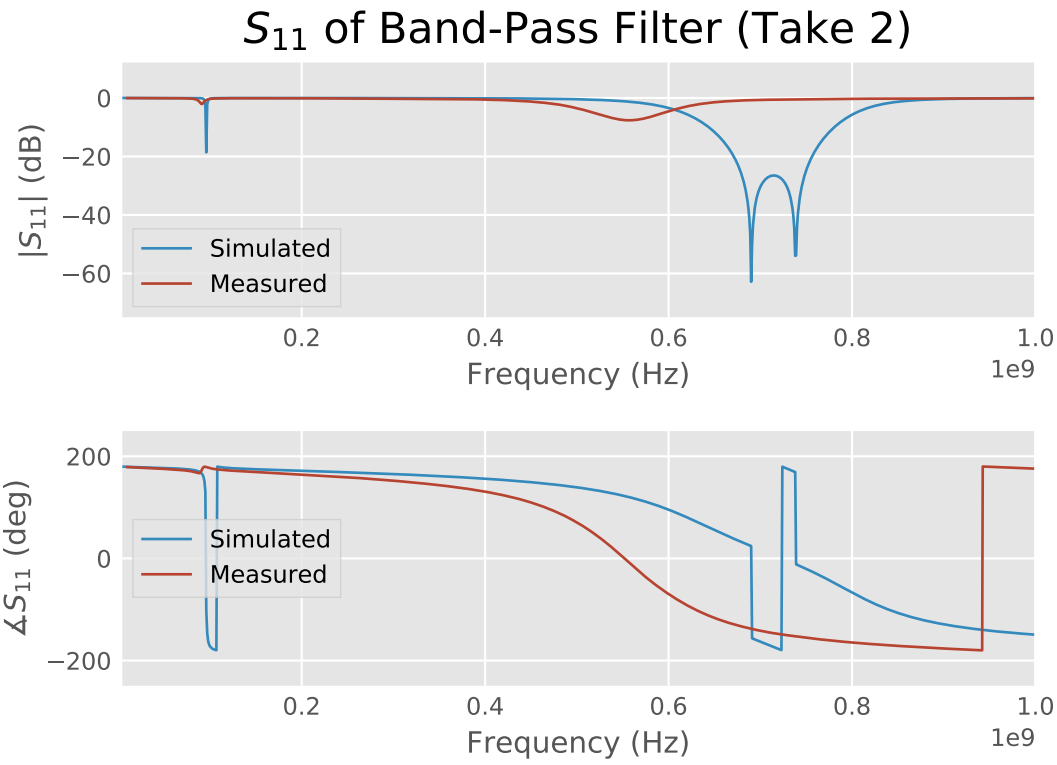
- Via inductance of 0.5 nH
- Via parallel plate capacitance of 0.4 pF
- 0603 pad parallel plate capacitance of 0.5 pF
- Capacitor self-resonance at 1.5 Ghz
- Inductor self-resonance at 1 Ghz

as well as several DC resistances.

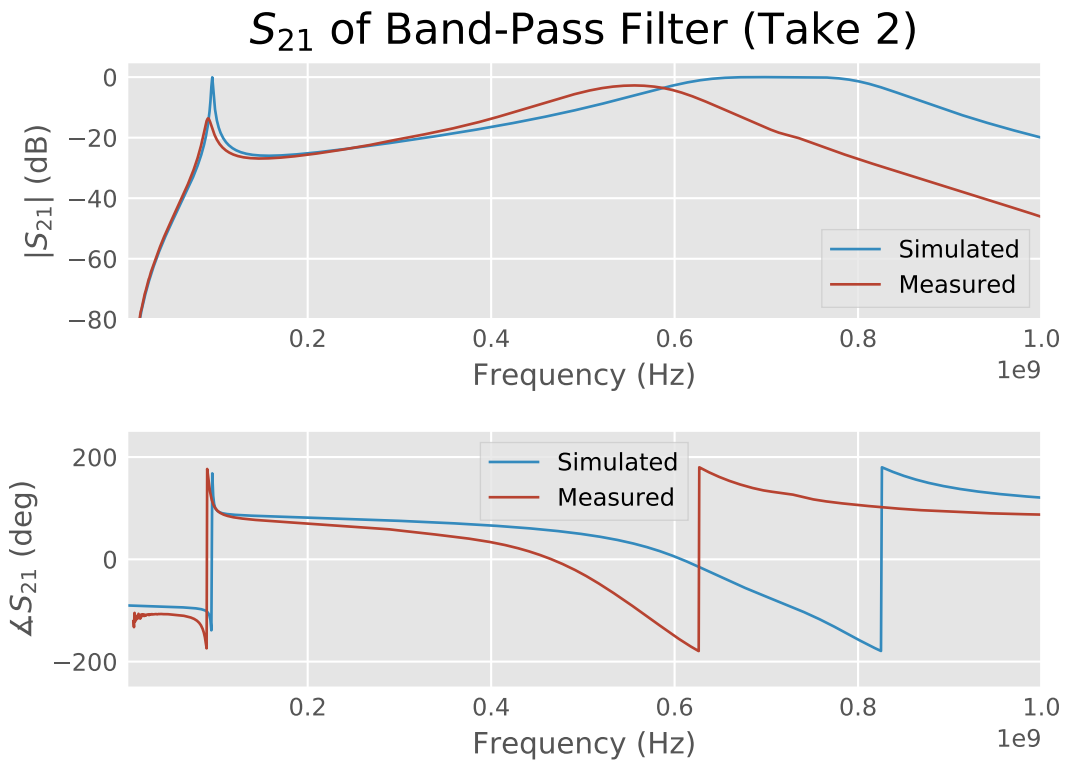
The filter was redesigned with the intention of moving the passband to 700 Mhz or higher. Unfortunately, this wasn't achieved.



New Band-Pass Filter Schematic



Take 2 BPF: S11



Take 2 BPF: S21

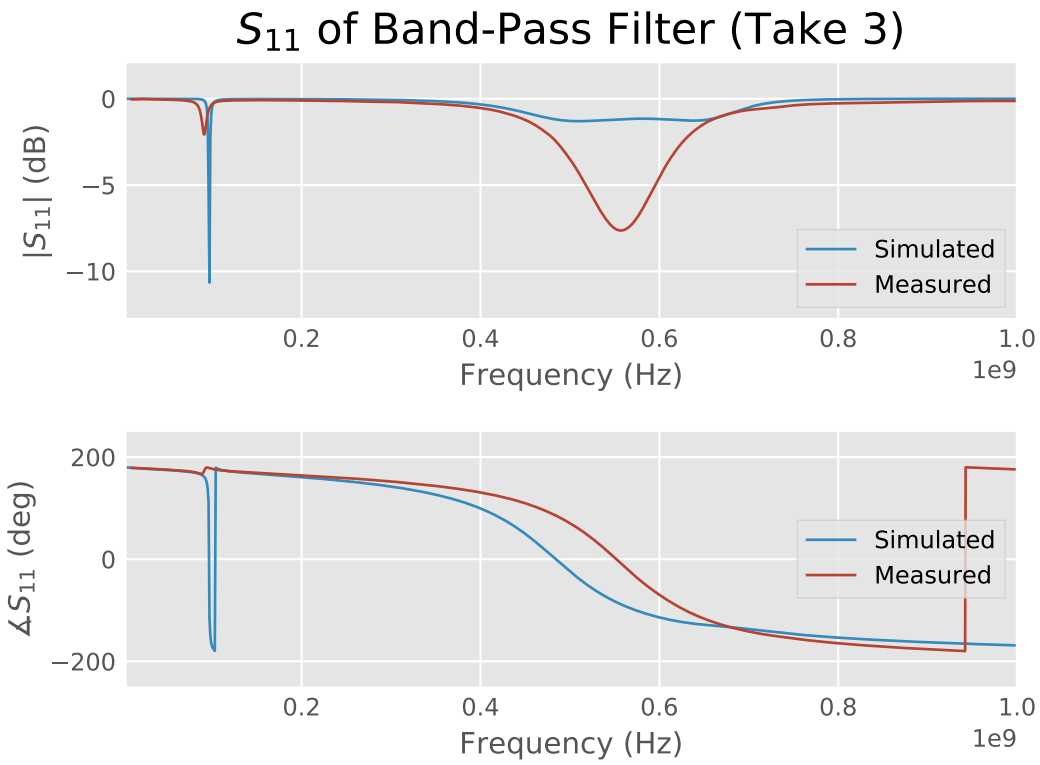
While we did succeed in moving the passband to a higher frequency around 550 Mhz, and while the parasitic model accurately predicted the S_{21} spike around 100 Mhz, we didn't have a sufficiently rigorous model to explain the passband deviation.

It is very likely that the component tolerances are affecting our designed circuit since we likely have 10% inductors and 5% capacitors. We ought to run a Monte Carlo analysis to see if this could explain our center frequency deviation.

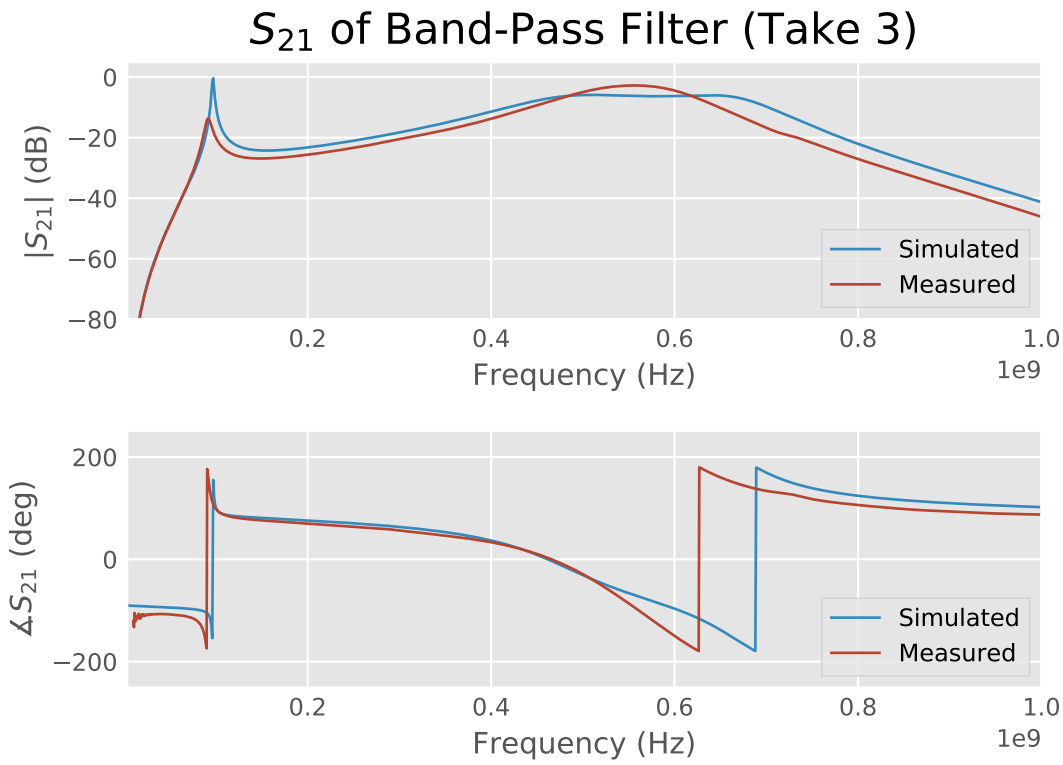
In a final effort, we modified our parasitic model to account for the following:

- We used a small piece of wire to short 2 pads. We added it's inductance of 3 nH.
- Boosted via parasitic inductance to 1 nH.
- Set self-resonance of L and C models to 1.5 Ghz

We managed to get our modified simulation to better fit the measured data.



Take 3 BPF: S11



Take 3 BPF: S21

1.4 Trace Width

Consider different board layouts employing either wider or narrower traces. Explain how each layout should affect the overall response of the filter.

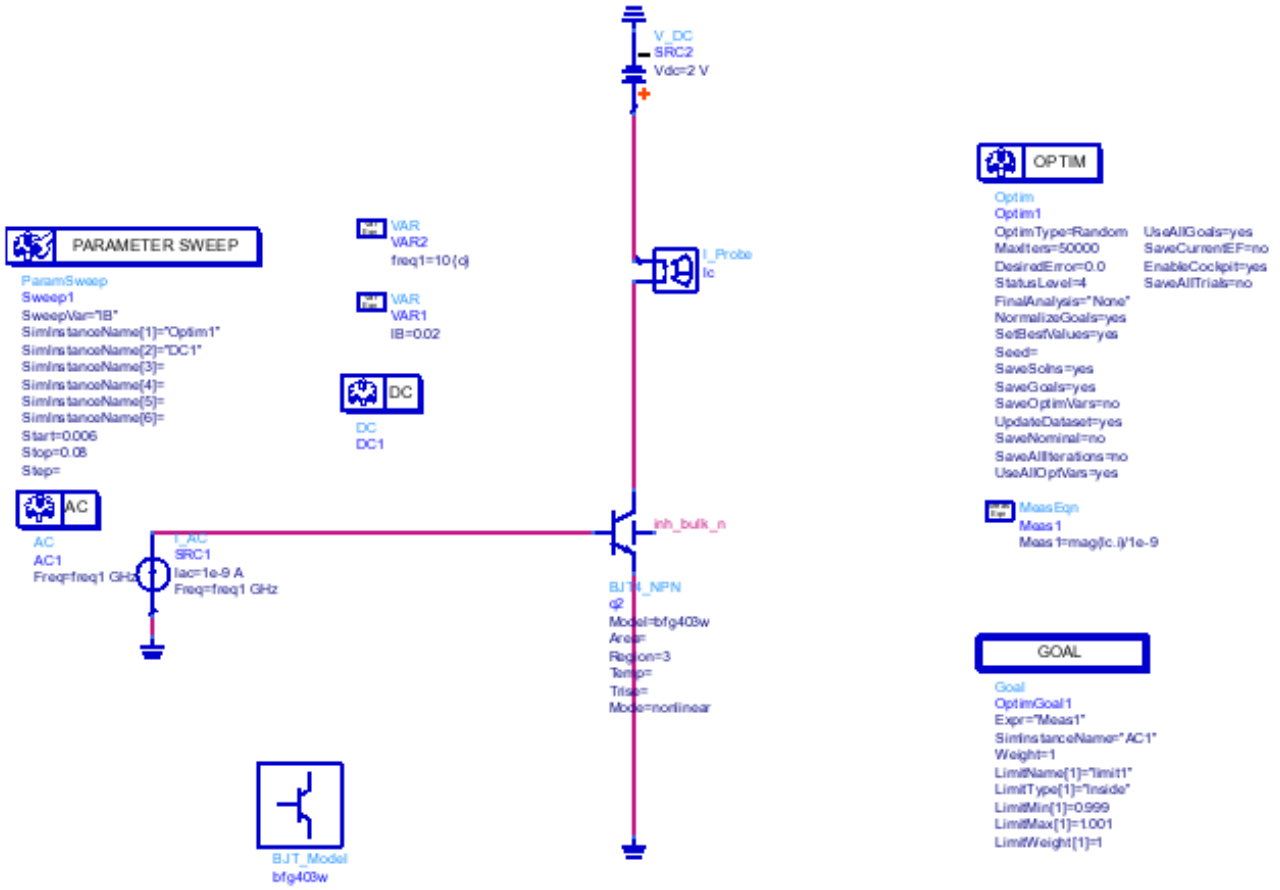
Wider and narrower traces would affect the characteristic impedance of the transmission lines on the board. This would probably affect the input match (S_{11}).

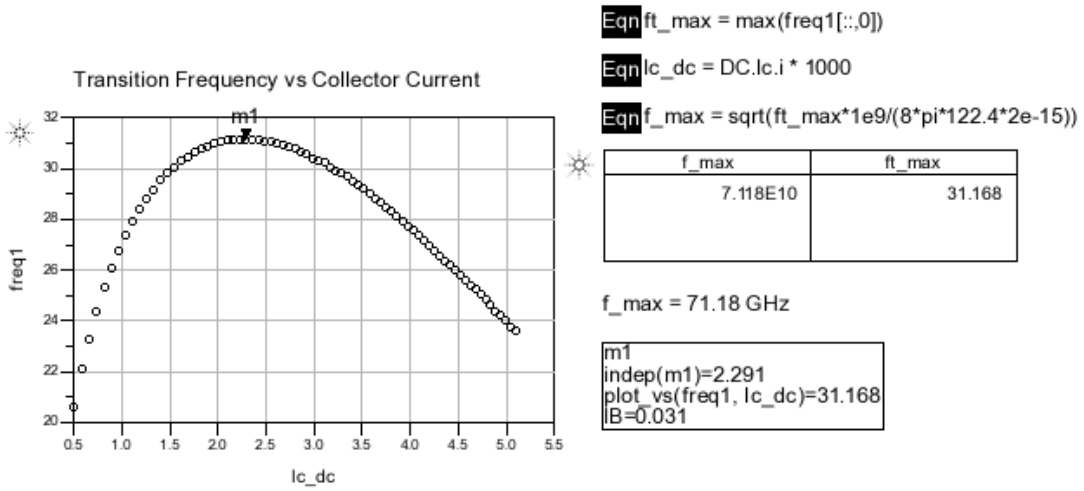
In addition, wider traces will have a greater parasitic contribution in the form of parallel plate capacitance and, to a lesser extent, loop inductance.

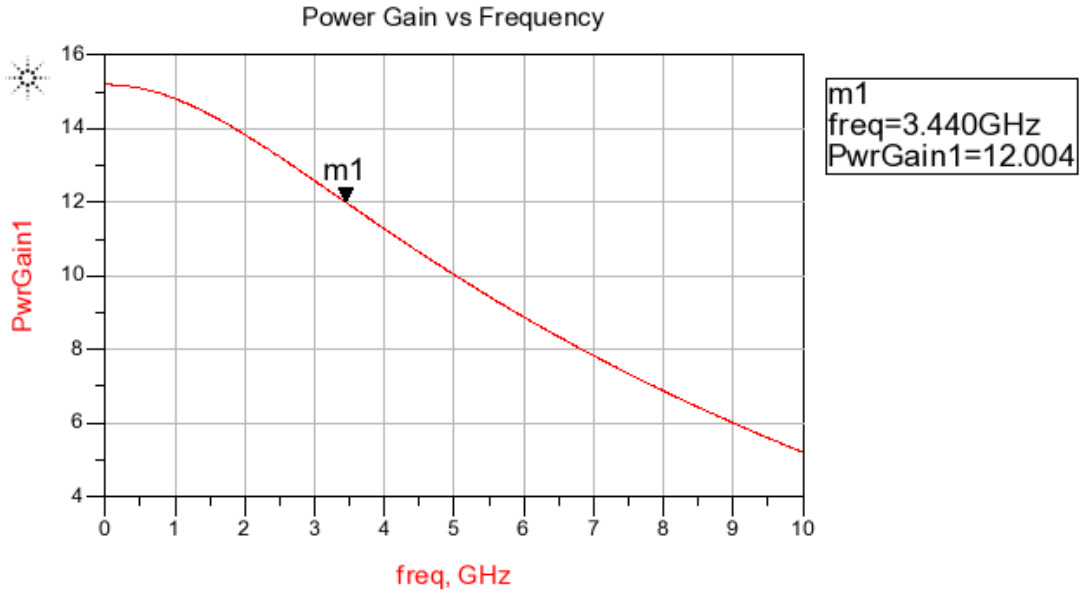
EE 242A Lab 3 Prelab

1. The collector current is 2.29 mA when $f_T = 31.131$ GHz is maximum. Using the formula for f_{max}, we get $f_{max} = \sqrt{\frac{f_T}{8\pi R_b C_{bc}}} = 71.13$ GHz. Doing a *PwrGain* simulation, we get $12dB$ at 3.44 GHz.

   Schematic:

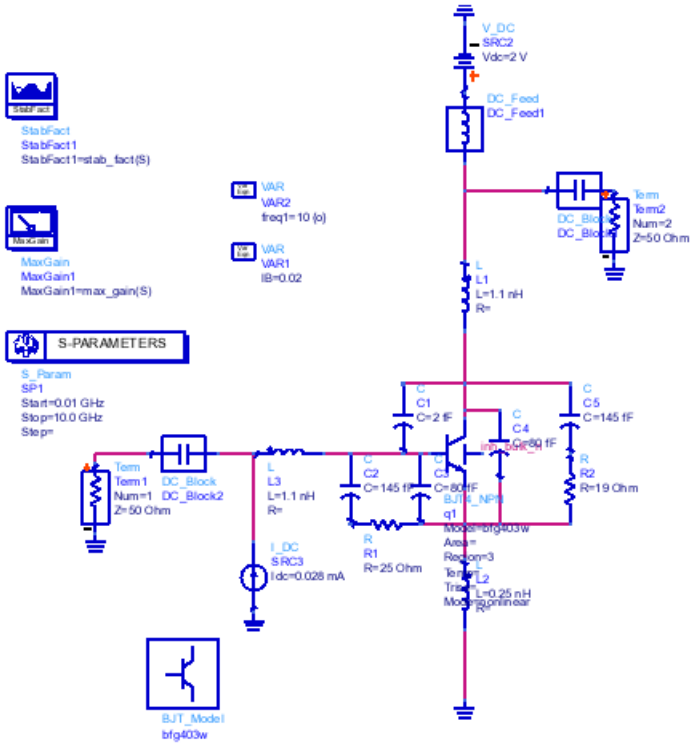


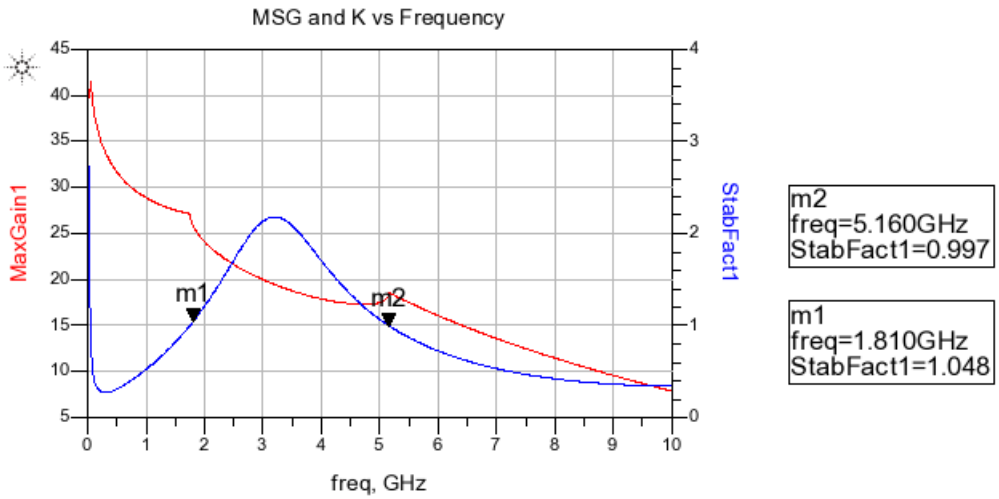

Transition Frequency vs Collector Current
m1
freq1
Ic_dc
Eqn ft_max = max(freq1[::,0])
Eqn Ic_dc = DC.Ic.i * 1000
Eqn f_max = sqrt(ft_max*1e9/(8*pi*122.4*2e-15))
f_max
ft_max
7.118E10
31.168
f_max = 71.18 GHz
m1
indep(m1)=2.291
plot_vs(freq1, Ic_dc)=31.168
IB=0.031


Power Gain vs Frequency
m1
PwrGain1
freq, GHz
m1
freq=3.440GHz
PwrGain1=12.004

2. Schematic Testbench:

   The frequencies at which the device is unconditionally stable are 1.8 to 5.1 GHz.





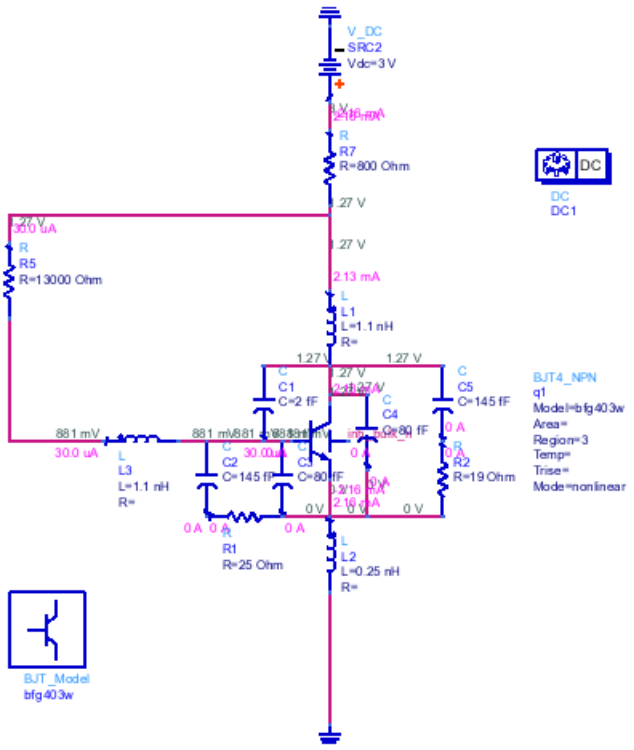
3. We want to bias the transistor to have a collector current of around 2.2 mA. We wanted to use a resistor from collector to the supply and a resistor from collector to base. We add caps to both ends of the feedback resistor to short the AC signal. We used $\beta \approx 100$. We referenced the biasing network of the 900 MHz LNA design in the application notes of the transistor and used $R_{fb} = 13\ k\Omega$ and $R_{bias} = 400\ \Omega$

   Our equations are:

$$\begin{aligned} I_c &= 2.2\text{ mA} \\ I_b &= 22\text{ uA} \\ V_b - V_e &= 0.7 \\ I_{sup} &= I_c + I_b \\ V_c &= V_{dd} - I_{sup}R_{bias} \\ V_{dd} - I_bR_{fb} &= V_b \end{aligned}$$

$$V_b = 1.8,\ V_c = 1.8$$

   We originally designed for emitter degeneration but it decreased stability.



   We then wanted to match our input and output impedances for power match.

   Since $BW = 100\text{ MHz} \approx \frac{600\text{ MHz}}{Q}$, $Q \approx 6$, for our networks. We decided to match a 2 section L-network at both output and input to have a $Q = 4$.

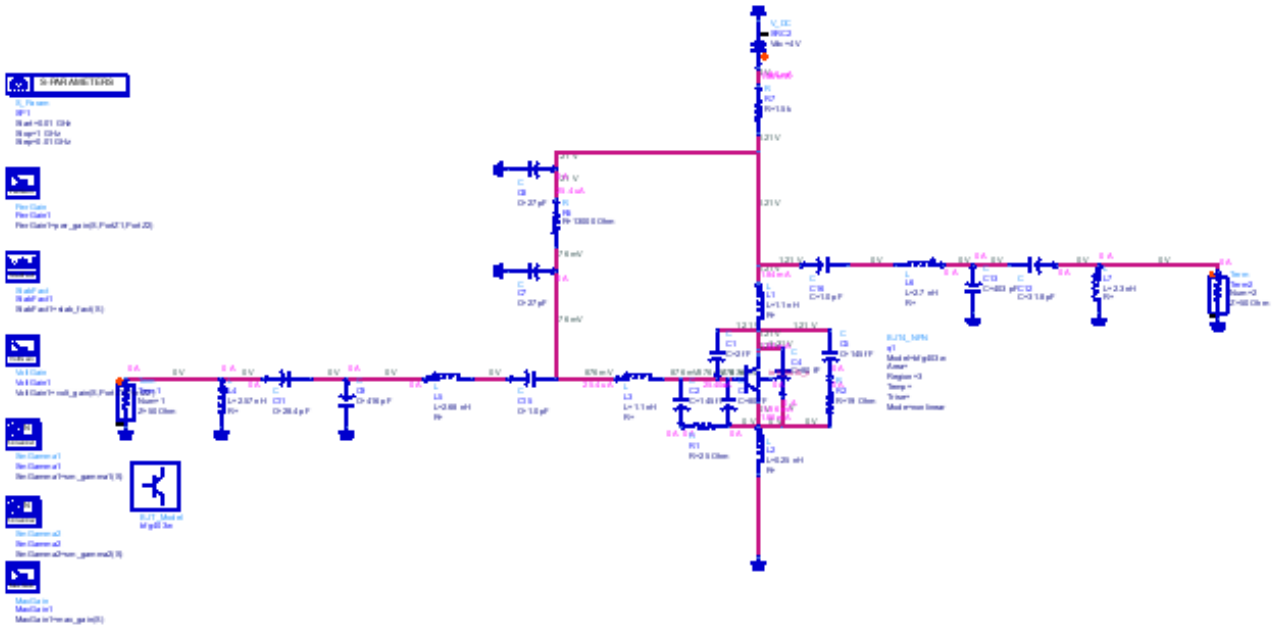
SmGamma1 and SmGamma2 reported that our input wants to see $Z_s = 50(0.004 + j0.191)$ and our load wants to see $Z_L = 50(0.005 + j0.193)$.

For our 2 section L-network:

$$Q = \frac{1}{2}\left(\sqrt{R_i/RL - 1} + \sqrt{Rs/Ri - 1}\right)$$

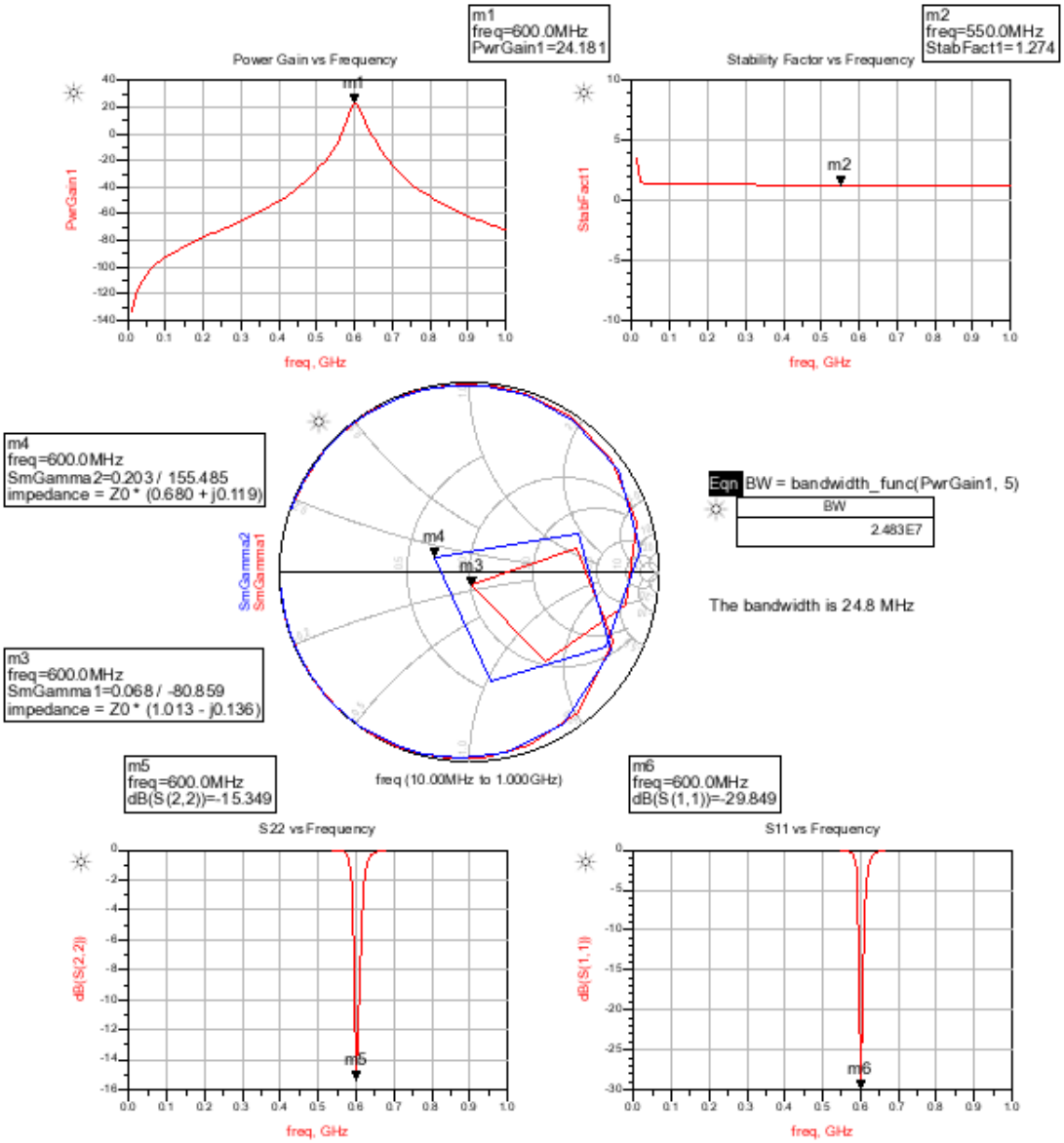
We got $R_i = 0.412$ and $R_i = 1.43$ for the input and output intermediate resistances.

Using a python and MATLAB script that solves for the L-matching network, we get the values shown in the schematic:

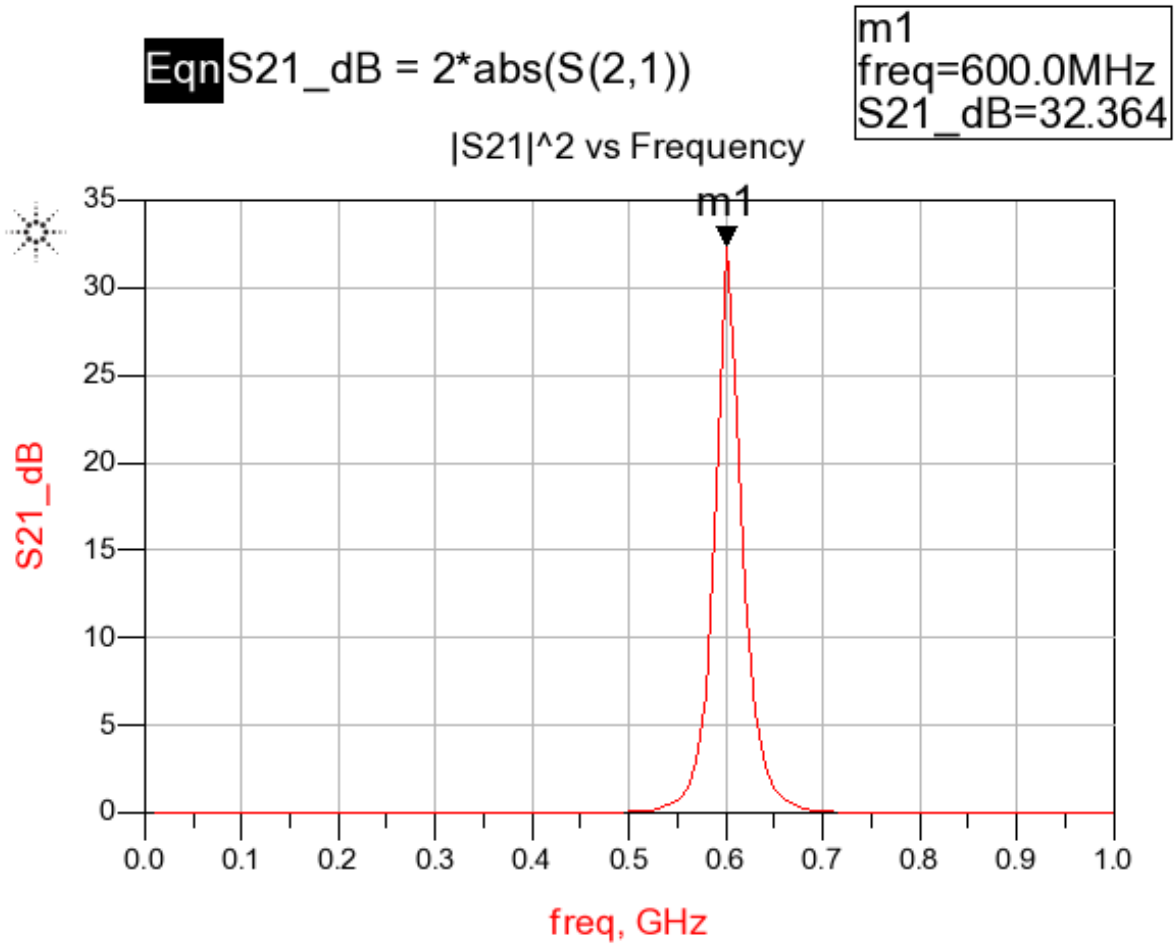


4. Our bias network was considered first (so that we matched impedance with it).

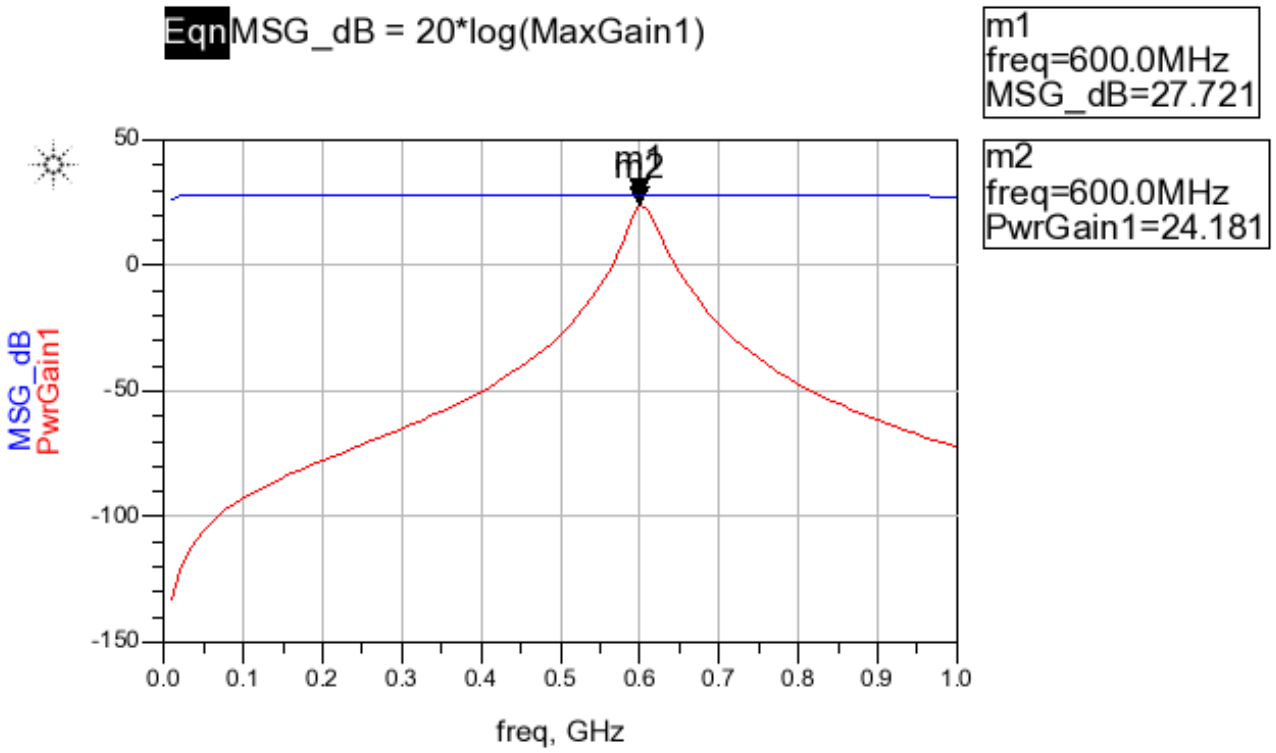
5. The plots of our design:



6. With the input/output match we realized a gain of 24.2 dB. The maximum possible gain assuming perfect match is 32.4 dB.



7. According to MSG, we can realize a maximum possible gain of 27.7 dB. With finite Q, our bandwidth increased by roughly 20 MHz.



8. Doing Monte Carlo, these were our Power Gain and Stability plots: