EE 242A Lab 3 Postlab

1. Explain the importance of bypass capacitors in the design. Why does the supply VCC need to be bypassed to ground? Where is the best location to place bypass capacitors?

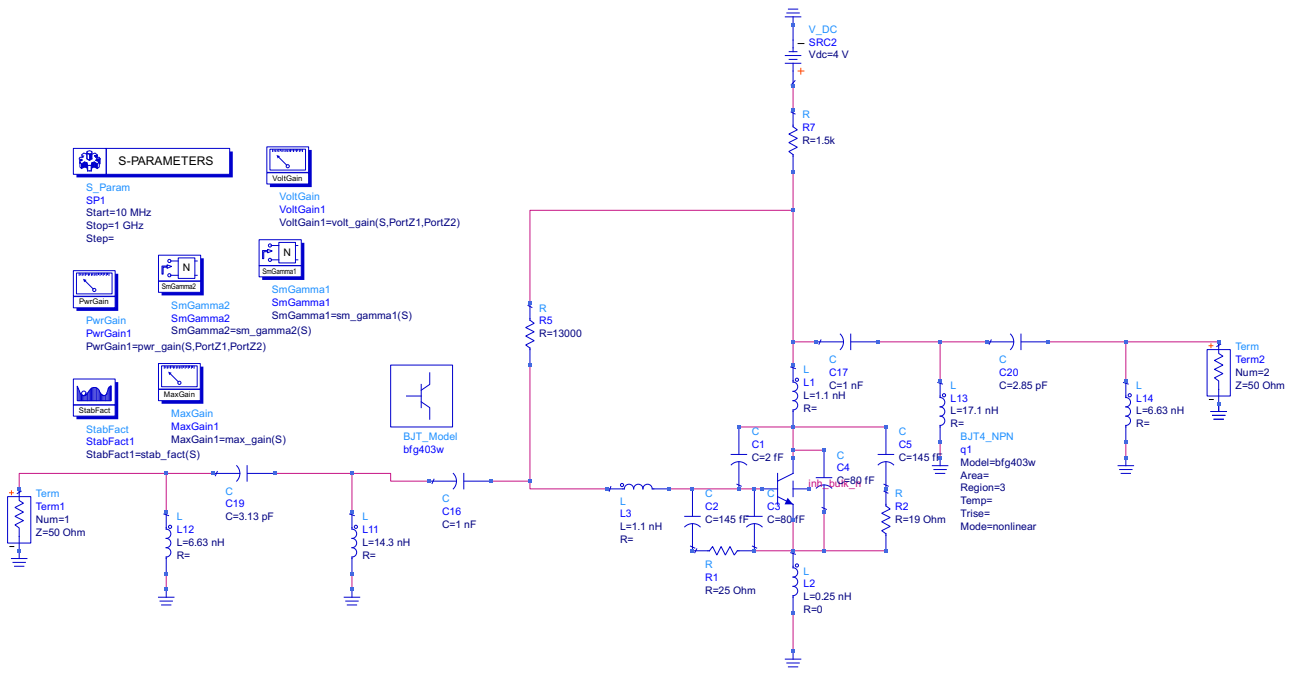
Bypass capacitors serve as a local tank of energy storage that an active device can draw on. The goal is to reduce the supply voltage ripple for active devices and allow them to source the current they need when switching quickly. The power supply can't respond fast enough to sudden current spikes due to the wire inductance, so a series of bypass capacitors are used to mitigate the voltage drops that would occur without them. Usually bypass capacitors of various capacitance values are placed in parallel: the larger valued capacitors usually have a higher ESR, but can store more charge, whereas the smaller valued capacitors have lower ESR which gives them better high frequency performance.

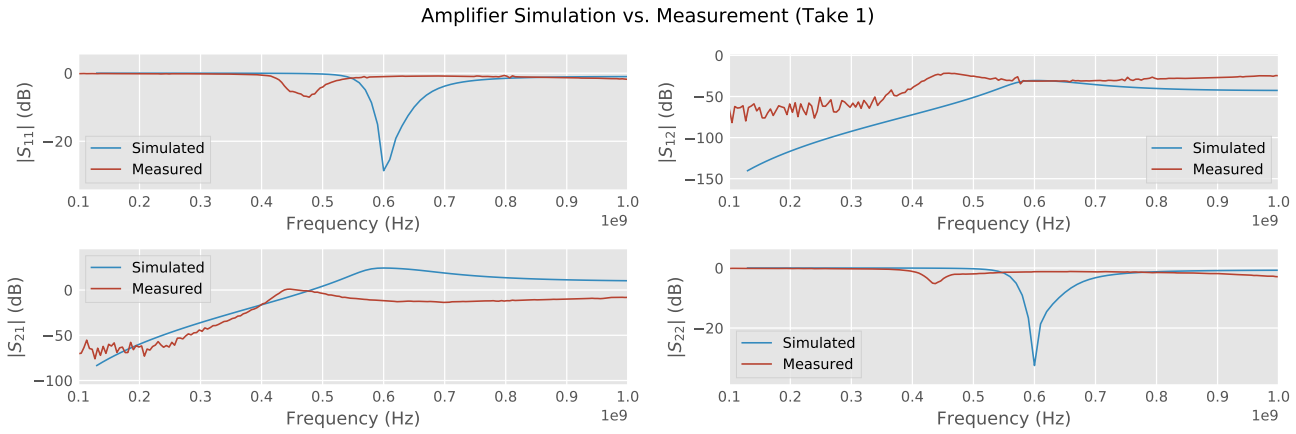
The best location to place bulk bypass is across V_{DD} and GND planes where the supply wires are soldered onto the PCB. Smaller bypass caps should be placed near the active component as close as possible to the pin (BJT collector resistor) which is sourcing current.

2. Compare measurement and simulation results by overlapping the measured S11, S22, and S21 of your amplifier with the simulations. Explain differences.

Take 1

Our first amplifier used resistive feedback for self-biasing, a 4V supply, 1 nF AC coupling caps, and Π matching networks on the input and output. It was designed with roughly 1.8 mA of bias current.

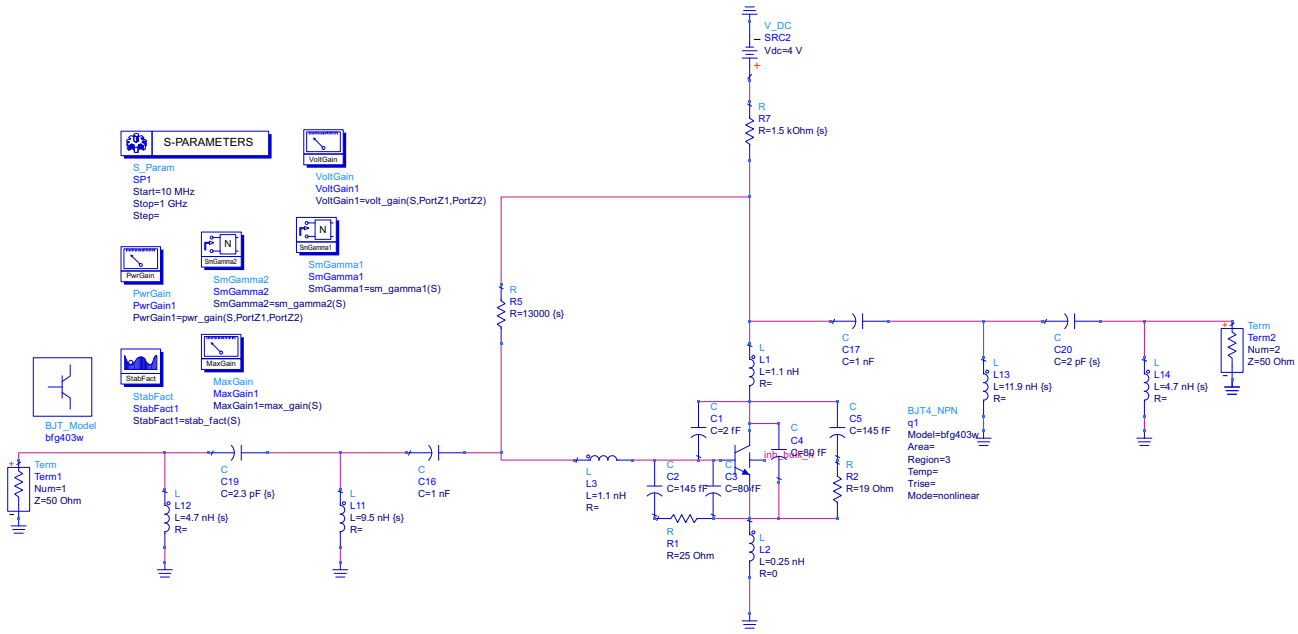


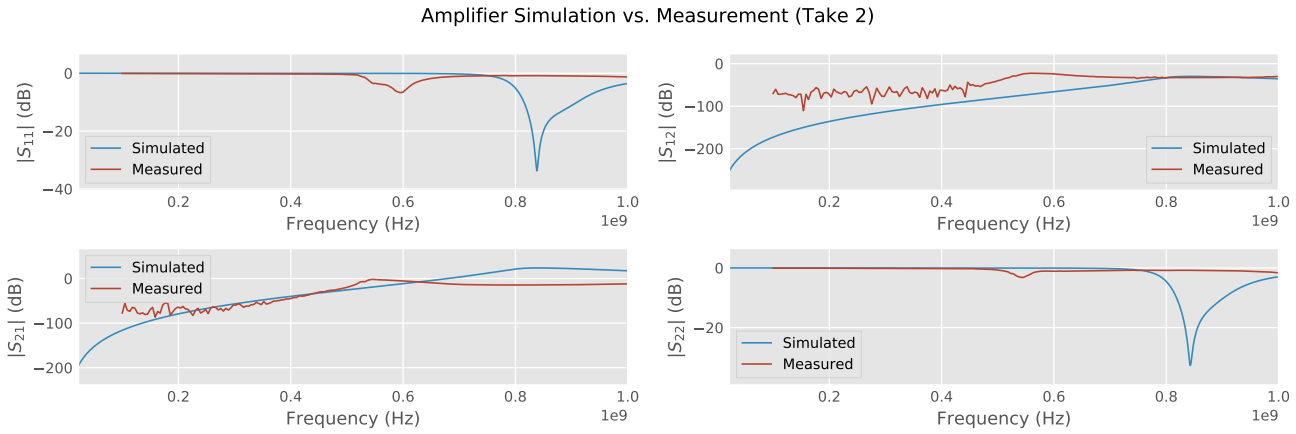


It is evident that the measured dips in S_{11} and S_{22} don't match the simulation in both depth and center frequency. This is due to board and component parasitics. This caused the gain (S_{21}) to be close to 0dB (at 450 MHz) as the input and output match didn't have an equal center frequency.

Take 2

The amplifier was redesigned to achieve a center frequency of 850 MHz. The ingenious idea was to design for a higher center frequency in the hope that the parasitics would reduce the center frequency to what we wanted. The only difference in this take was the matching network (the bias was left the same).





The center frequency on S_{21} was now around 540 MHz which is better, but still not what we wanted. The dip on S_{11} was deadset on 600 MHz, but the dip on S_{22} was closer to 565 MHz, which meant a poor output match giving us an achieved gain of 0 dB (again).

3. Explain the significance of S12 in the design. Compare the measured and simulated S12, especially at higher frequencies. Explain the mismatch between the simulation and measurements.

S_{12} has been plotted in the previous section: it represents the 'unilateral-ity' of the amplifier. When the amplifier is connected backwards it shouldn't have any gain, but there is still an AC path for current to flow out of port 1.

The measured and simulated results show a S_{12} which is roughly 20 dB down from S_{21}, as expected. At high frequencies, the measured S_{12} appears to slightly increase as the parasitic AC coupling across the BJT (collector to base) makes the amplifier less unilateral.

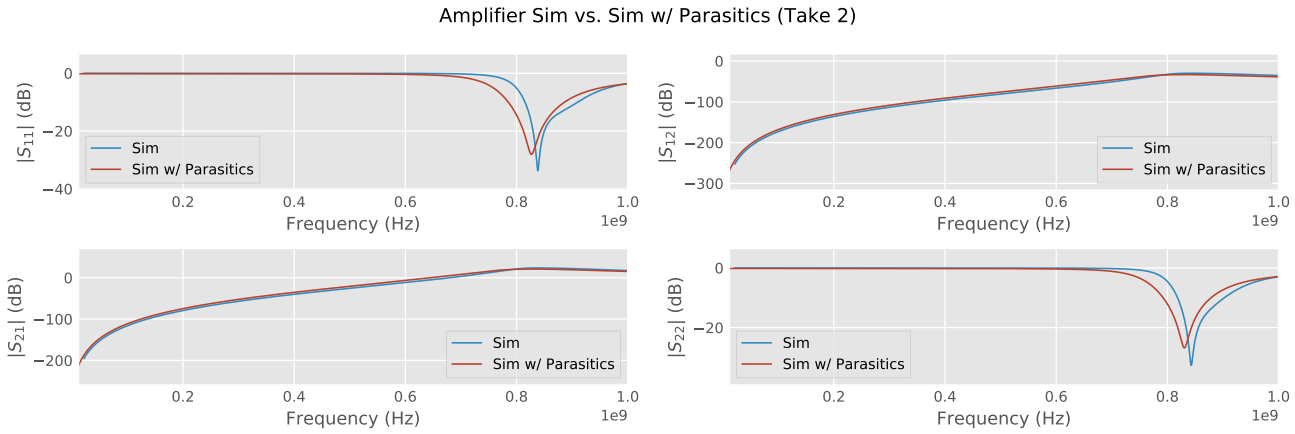
4. Which board level or component level parasitics were the most detrimental? Explain.

From experimentation, it appears the via inductance is the most significant parasitic, adding around 1nH to each component connected to ground. Additionally, through Monto Carlo simulations, it appears that component value variations can have a large impact on the accuracy of the input and output match.

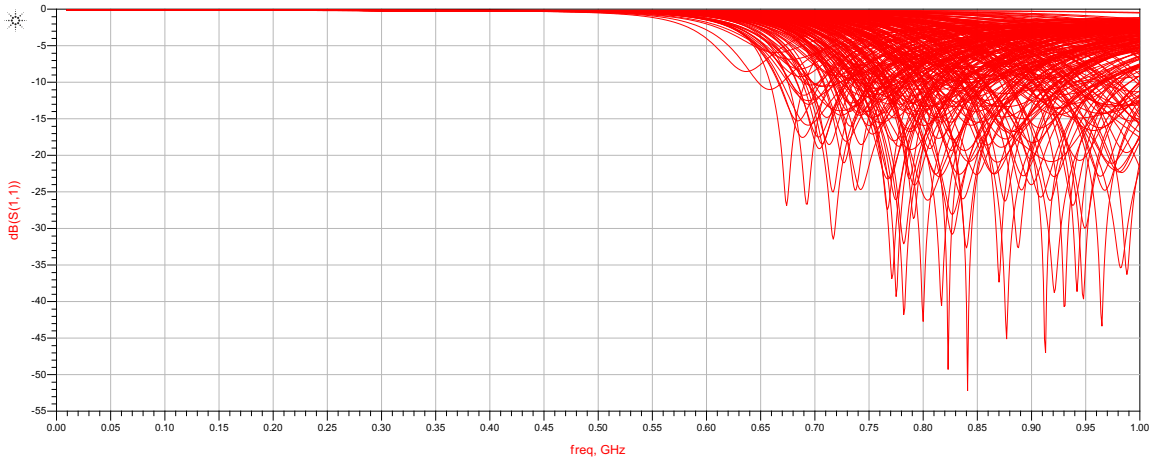
After going through the lab several times, we finally came upon the parasitic that contributed the most to simulation and measurement mismatch: **board transmission lines**. This is elaborated on in section 6.

5. Modify schematic to match measurements. You should use your knowledge of the board level parasitics and component parasitics. If you did not measure the components and the board, the GSI can provide you the appropriate data. Make sure you understand the various measurements of the board level parasitics. The component models can also be obtained from the manufacturer.

Adding parasitic models of components (modeling finite Q, self-resonance, and pad capacitance), and via parasitics (1nH inductor to ground with 500 $m\Omega$ DC resistance), did little to change the results of our simulation.



We then run Monte Carlo simulation to see if component variation could explain the discrepency between simulation and measurement. We use very aggressive variation values on inductors and capacitors (20% and 10%), and look at S_{11}.



Even with these unrealistically high component variations, we don't observe the S_{11} center frequency shift to the measured 540 MHz. The same observation is made with the other S-parameters.

Clearly, there are some board or component variations that we aren't taking into account. There are some zero-Ohm resistors and solder bridges used in the actual board layout, but they should have little effect on the overall circuit. We also aren't modeling transmission lines and power supply inductance, but they should have little impact at our frequencies of operation. (*We later found out that transmission lines have a huge impact*)

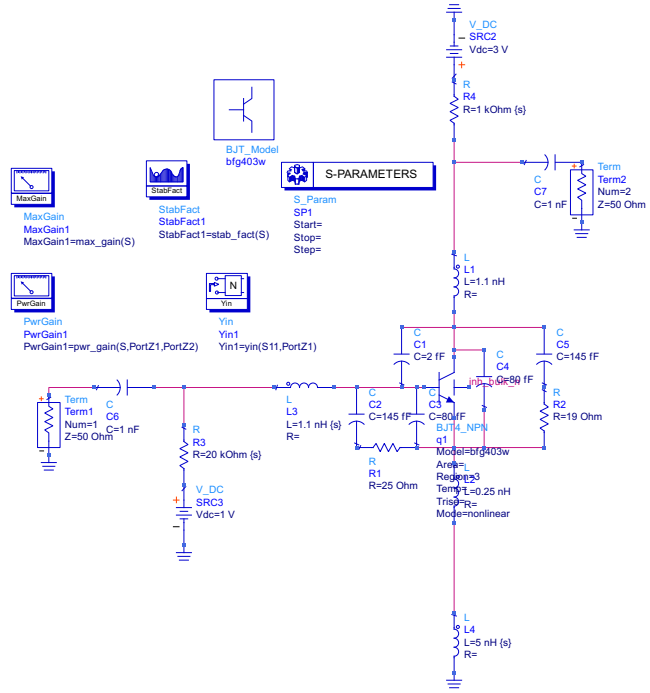
6. Based on your experience in the lab, comment on any changes in the design of the amplifier which may improve performance or make the amplifier more realizable. If time permits, feel free to redesign and rebuild the amplifier.

The major issue is the mismatch between the input and output matching network center frequen-

cies. Another issue is the need to use a Π or T network to boost the Q of the matching network, when using cascaded L sections would place less strict requirements on component variation and parasitics to contend with. Also, our parasitic models don't match reality.

Take 3

We decided to redesign the amplifier to make the matching network more insensitive to component Q and parasitics. This was done with inductive degeneration to make the input/output impedance of the BJT as real as possible and by biasing the amplifier using a second supply applied to the BJT's base.



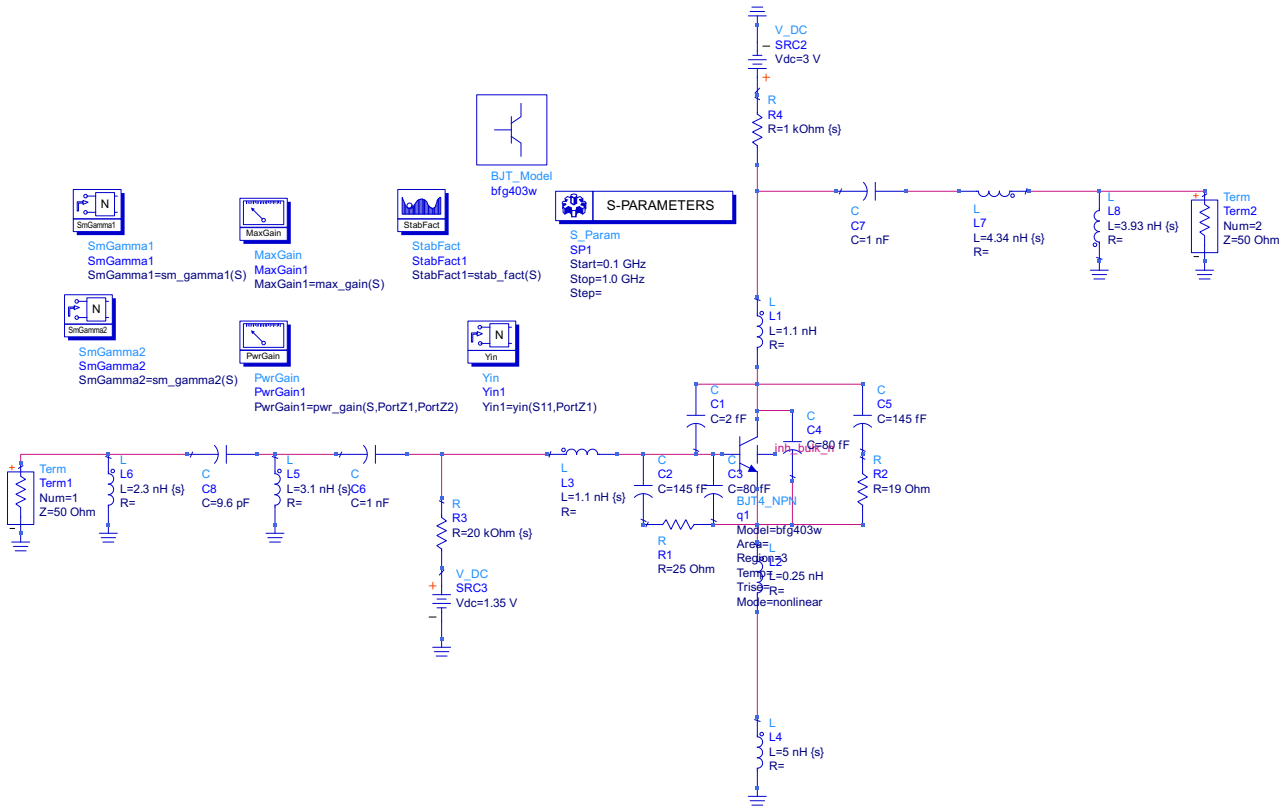
The goal is to design the matching network using the VNA and it's Smith Chart empirically rather than through simulation since the parasitic models we are using aren't predictive.

After building this circuit and measuring its response, **we noticed immediately that the VNA reported an input impedance Z_{in} that was substantially different than what ADS reported.** We observed that the VNA was reporting a Z_{in} close to a short (3Ω) around 600 MHz, while ADS reported a Z_{in} that had an impedance of around 420Ω around 600 MHz. This is very likely due to the transmission line from the SMA connector to the AC coupling capacitor, which isn't modeled in the schematic, and based on physical measurements is close to a $\lambda/4$ line.

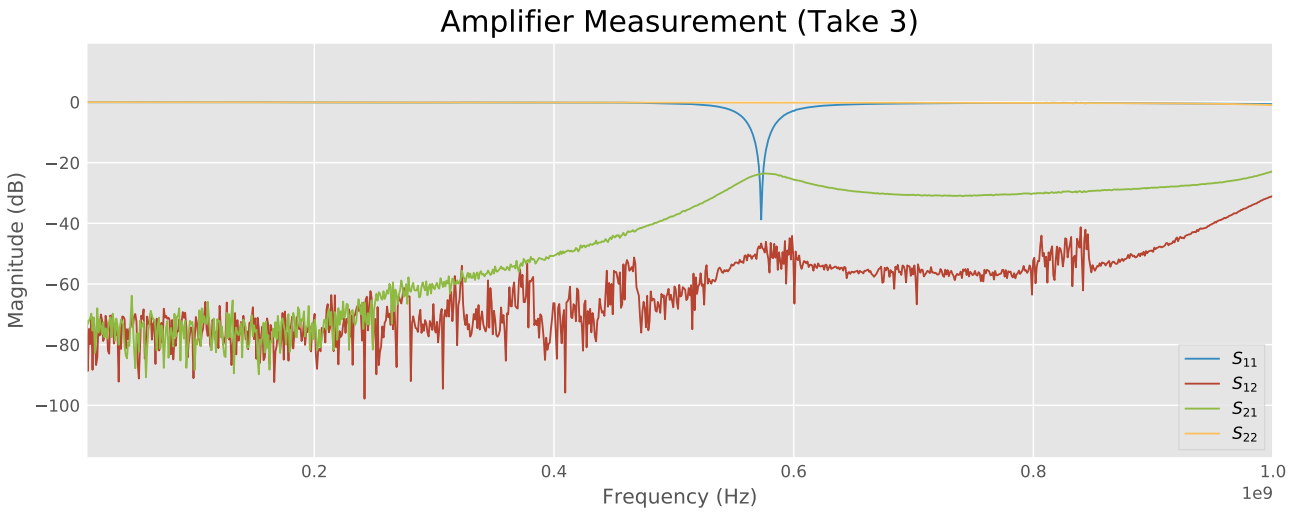
The missing parasitic is identified as: **board transmission lines**.

However, the VNA includes this in its calculation, so we just directly designed input and output matching networks based on the reported S_{11} and S_{22}.

Here is the final schematic (as constructed on the board):



Here are the final results:



We were able to match S_{11} around 570 MHz, but weren't able to match S_{22} after repeated attempts. As a result S_{21} is still below 0 dB.

7. How much time did you spend on this lab? Any feedback is appreciated.

Several hours.

EE 242A Lab 4 Prelab

1. Begin by calculating a power series representation for the in-band performance of the amplifier design. Assume that the amplifier is operating in resonance so that many LC elements resonant out and only the resistive parasitic effects remain.

We maintain our DC bias current at resonance, for $I_{c0} = 1.74mA$. We use the equation power series expansion equation for a CE BJT amplifier:

$$i_c = I_{c0}(\tfrac{v_b}{V_{TH}}) + \tfrac{1}{2}(\tfrac{v_b}{V_{TH}})^2 + \tfrac{1}{6}(\tfrac{v_b}{V_{TH}})^3 + \cdots)$$

At high frequency, we can the output voltage v_c to be the the small signal current times the 50 Ohm output termination and the 19 Ohm parasitic resistance. We also take the base voltage to be the input times a voltage divider.

$$\begin{aligned} v_b &= \tfrac{25}{25+50} = \tfrac{1}{3} \\ v_c &= i_c \times \tfrac{19*50}{19+50} = i_c \times 13.8\Omega \\ v_c &= (0.308)v_b + (1.97)v_b^2 + (8.43)v_b^3 + \cdots) \end{aligned}$$

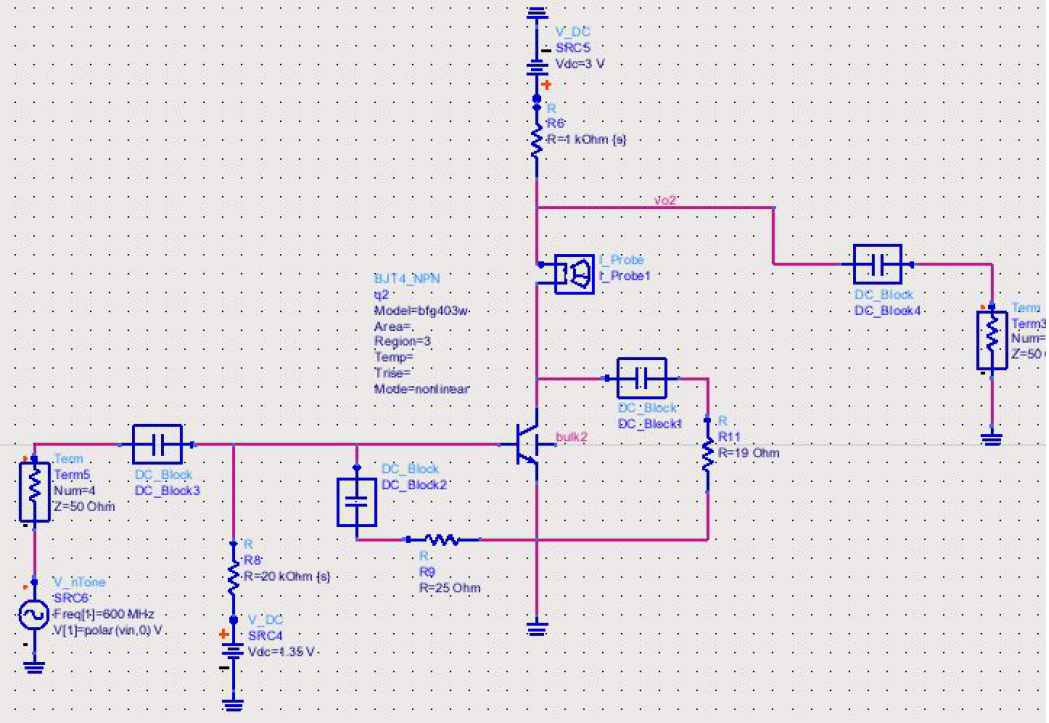
2. From the power series, predict the harmonic powers (2nd, 3rd) and intermodulation powers for a 600 MHz input(s) with -30 dBm input power. If your amplifier center frequency is different, use the actual center frequency for the measurements..

-30 dBm equates to 1uW. Under 50 Ω load, using RMS power, we get $S_{in} = \sqrt{\frac{1uW*50\Omega}{2}} = 5mV$

$$\begin{aligned} HD_2 &= \frac{\alpha_2}{2}S_{in} = \frac{1.97}{2}(5mV) \\ &= 4.9mV = 0.96uW = -32dBm \\ HD_3 &= \frac{\alpha_3}{4}S_{in}^2 = \frac{8.43}{4}(5mV)^2 \\ &= 53uV = 0.11pW = -69dBm \\ IM_2 &= HD_2 + 6dB = -26dBm \\ IM_3 &= HD_3 + 10dB = -59dBm \end{aligned}$$

3. Simulate the large signal behavior of the amplifier by applying a single tone at the center frequency at the input and measuring the output power. Vary the input power level and find the 1 dB-compression point. Compare the simulated compression point to the calculated point.

We simulated a simplified version of the circuit, under the assumptions of perfect match and DC bias.



We found $a_1 = 0.230$, which is reasonable close to our model.

-1dB compression will occur when $a_1 = 0.205$, which we found to be around $V_{in} = 85mV$. Hand calculation suggests it to be $\sqrt{abs(10^{-1/20} - 1) * 4/3/8.43} = 131mV$.

4. Compare the distortion products for a -30 dBm input between the simulation and the calculations.

For -30 dBm, our ω_0 gain is 0.230. Our $2\omega_0$ gain is 0.420. Our $3\omega_0$ gain is 0.403.

Our ω_0 gain is reasonable close to our hand calculation.

5. Simulate and make a plot of the amplifier intermodulation powers IM2 and IM3 versus input power. Compare the calculated extrapolated IIP points to the extrapolations from simulations.

6. Suppose you cascade your amplifier with itself. What is the overall gain, compression point, and iIP2 and iIP3? Use the cascade formulas to estimate these quantities and then simulate the amplifier to verify.

7. Calculate the noise figure of your amplifier. Verify the results with simulation.

8. Convert your amplifier into a mixer. If the output stage uses a tuned network, assume that the output network is converted into a low-pass filter (for instance by removing the inductor from the tank). Assume a strong signal is applied to the input of your amplifier which modulates its operating point. Calculate the conversion gain of the amplifier if a small RF signal is added to the LO. Through simulation find a good LO power level which results in nearly the optimal

conversion gain. The LO signal should be at 600 MHz (or your amplifier's center frequency) and the IF should be selected to be in the pass-band of the output network.