EE219C HW2: SMT

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1 Bit-Twiddling Hacks

(a) Are the functions `f1` and `f2` in Figure 1 equivalent?

```c
int f1(int x) {
  int v0;
  if (x > 0) v0 = x;
  else v0 = -x;
  return v0;
}
```

```c
int f2(int x) {
  int v1, v2;
  v1 = x >> 31;
  v2 = x ^ v1;
  return (v2 - v1);
}
```

`f1` is an absolute value function. `f2` is first isolating the sign bit in `v1` then performing a 2s complement inversion if the sign bit is 1. So these functions should be equal. I encoded this validity question using the Z3 Python API:

```python
x, v0, v1, v2 = BitVecs('x v0 v1 v2', 32)
s = Solver()
s.add(v0 != v2 - v1, v0 == If(x > 0, x, -x), v1 == x >> 32, v2 == x ^ v1)
print(s.check())
print(s.sexpr())
```

The equality between the return values of `f1` and `f2` was inverted to check for validity. The results were:

```
unsat
(declare-fun v0 () (_ BitVec 32))
(declare-fun x () (_ BitVec 32))
(declare-fun v2 () (_ BitVec 32))
(declare-fun v1 () (_ BitVec 32))
(assert (distinct v0 (bvsub v2 v1)))
(assert (= v0 (ite (bvsgt x #x00000000) x (bvneg x))))
(assert (= v1 (bvashr x #x00000020)))
(assert (= v2 (bvxor x v1)))
(model-add v0
           ()
           (_ BitVec 32)
           (bvmul x (ite (bvsle x #x00000000) #xffffffff #x00000001)))
(model-add v2 () (_ BitVec 32) (bvxor x v1))
```

Showing that `f1` and `f2` are functionally equivalent.

(b) Are the functions `f3` and `f4` in Figure 1 equivalent?

```c
int f3(int x, int y) {
  int v0;
  if (x >= y) v0 = x;
  else v0 = y;
  return v0;
}
```

```c
int f4(int x, int y) {
  int v1, v2, v3;
  v1 = x ^ y;
  v2 = (-(x >= y));
  v3 = v1 & v2;
  return (v3 ^ y);
}
```

`f3` is a max function. I used Z3 in the same manner:

```python
x, y, v0, v1, v2, v3 = BitVecs('x y v0 v1 v2 v3', 32)
s = Solver()
s.add(v0 != v3 ^ y,
      v0 == If(x >= y, x, y),
      v1 == x ^ y,
      v2 == If(x >= y, BitVecVal(-1, 32), BitVecVal(0, 32)),
      v3 == v1 & v2
     )
print(s.check())
print(s.sexpr())
```

These two functions are also equivalent:

```
unsat
(declare-fun v0 () (_ BitVec 32))
(declare-fun y () (_ BitVec 32))
(declare-fun x () (_ BitVec 32))
(declare-fun v1 () (_ BitVec 32))
(declare-fun v2 () (_ BitVec 32))
(declare-fun v3 () (_ BitVec 32))
(assert (distinct v0 (bvxor v3 y)))
(assert (= v0 (ite (bvsge x y) x y)))
(assert (= v1 (bvxor x y)))
(assert (= v2 (ite (bvsge x y) #xffffffff #x00000000)))
(assert (= v3 (bvand v1 v2)))
(model-add v0 () (_ BitVec 32) (ite (bvsle y x) x y))
(model-add v1 () (_ BitVec 32) (bvxor x y))
(model-add v2 () (_ BitVec 32) (ite (bvsle y x) #xffffffff #x00000000))
(model-add v3
           ()
           (_ BitVec 32)
           (let ((a!1 (bvor (bvnot (bvxor x y))
                            (bvnot (ite (bvsle y x) #xffffffff #x00000000)))))
             (bvnot a!1)))
```

2 Sum-Sudoku

(a) Describe your SMT encoding and list the constraints in it. Then encode the formulation using the Z3 API by implementing `var`, `val`, and `valid` in `sumsudoku.py`.

We are working in the theory of `QF_LIA`.

$$x_{i,j} \quad \forall i \, 0 \leq i < n \, , 0 \leq j < n$$

Declare variables representing the value in each square. Also declare variables $r_i \forall i 0 \leq i < n$ and $c_i \forall i 0 \leq i < n$ representing the row and column sums.

(b) Use the pigeonhole principle, forall numbers there is only 1 place it can go into.