

EE 240B – Spring 2019

Advanced Analog Integrated Circuits

Lecture 1: Introduction



Ali Niknejad
Dept. of EECS

Course Focus

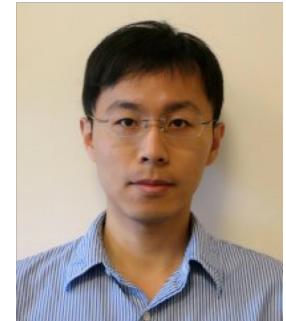
- **Focus is on analog design methodology**
- **Methodology = how to translate a set of specs in to a circuit (topology + sizing)**
 - Note that also need to understand where the specs came from
- **Especially in analog, some things are much “easier” to do than others**
 - Concrete methodology helps to make tradeoffs more clear
 - Sometimes (often) the right thing to do is change the specs

Course Goal

- **Learn how to create systematic methodologies to analog design**
 - Based on fundamental principles
 - For a wide variety of applications
 - And that can be captured within an executable program (generator)
- **Will develop increasingly more complete design methodology examples**
 - And will introduce additional topologies/circuits as we realize the need for them

Teaching Staff

- **Ali's office hours**
 - 511 Cory Hall
 - Office hours TBA
- **GSI: Yi-An Li**
 - Office hours TBA



Administrative

- **Everything is on bCourses**
 - You should be enrolled automatically
- **No lecture videos**
- **All announcements made through piazza**
 - In case you weren't already enrolled:
<http://www.piazza.com/berkeley/spring2019/ee240b>

Lecture Notes

- **Compilation from offerings by multiple faculty/instructors:**
 - Prof. Bernhard Boser, Prof. Ali Niknejad, Dr. Simone Gambini, Dr. Lingkai Kong, Prof. Elad Alon
- **Primary source of material for the class**
 - No required text – reference texts on next slide
- **Notes posted on the bCourses**

Reference Texts

- **Analysis and Design of Integrated Circuits,**
Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer,
4th Ed., Wiley, 2001.
- **Design of Analog CMOS Integrated Circuits,**
Behzad Razavi, McGraw-Hill, 2000.
- **Analog Integrated Circuit Design,**
D. Johns and K.Martin, Wiley, 1997.
- **The Designers Guide to SPICE & SPECTRE,**
K. S. Kundert, Kluwer Academic Press, 1995.
- **Operation and Modeling of the MOS Transistor,**
Y. Tsividis, McGraw-Hill, 2nd Edition, 1999.

Grading

- **HW: 20%**
 - One HW roughly every two weeks
 - You will be “graded” purely by on-time submission
 - You should “self-grade” and make sure you understand the solutions – falling behind/not doing this will doom you to failure everywhere else.
- **Project: 25%**
 - Groups of 2 – find a partner ahead of time
- **Midterm: 25%**
- **Final Exam: 30%**

Homework

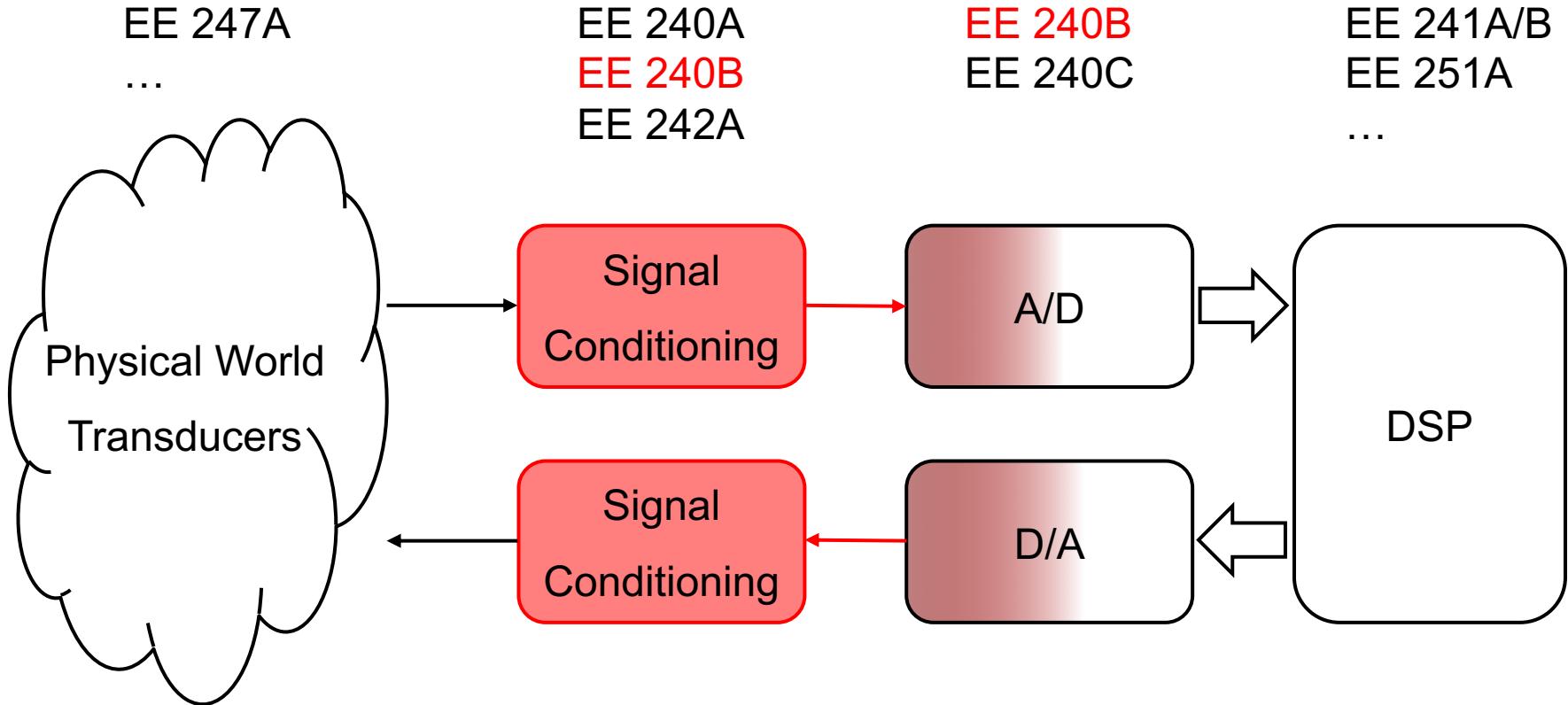
- **Can discuss/work together**
 - But write-up must be individual
- **Submission via bCourses**
 - **PDF is the only acceptable format**
- **Generally due 5pm on Thursdays**
- **No late submissions**
 - **Start early!**

Schedule Notes

- **ISSCC Week:** 2/18 - 2/22 (no lectures)
- **Midterm:** March 5 (mark your calendars)
- **Spring break:** 3/25 – 3/29
- **Project (tentative)**
 - Part 1 due Mar. 12
 - Part 2 due Apr. 2
 - Part 3 due May 2
- **Final: Monday, May 13, 11:30am – 2:30pm**

Course Material Introduction

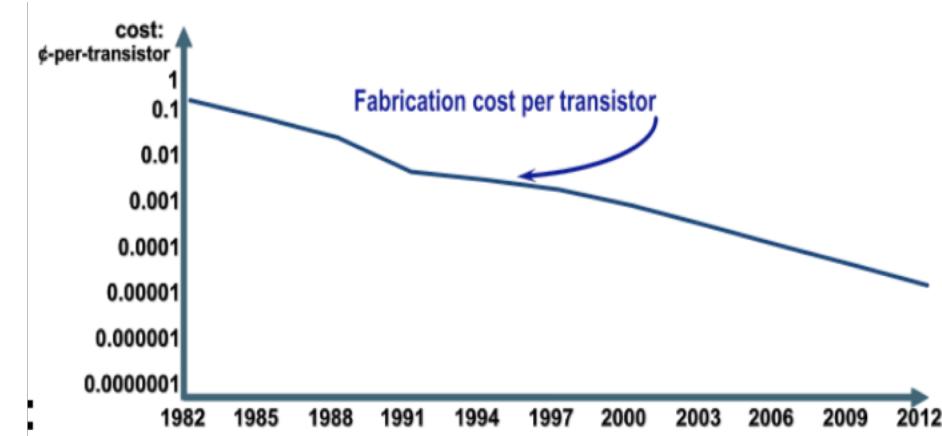
Analog and Mixed-Signal Circuits



Analog ICs in a “digital” World?

Digital circuitry:

- Cost/function decreases by 29% each year
- That's 30X in 10 years



Ref: International Technology Roadmap for Semiconductors (ITRS),
<http://public.itrs.net>

Analog circuitry:

- **Cost/function is constant**
- **Dropping supply voltages threaten feasibility**
- **Common complaints about scaling analog:**
 - Supply voltage is too low, device gain is low, horrible matching...
- **“Analog will die – everything will be digital!”**
- **Who agrees?**

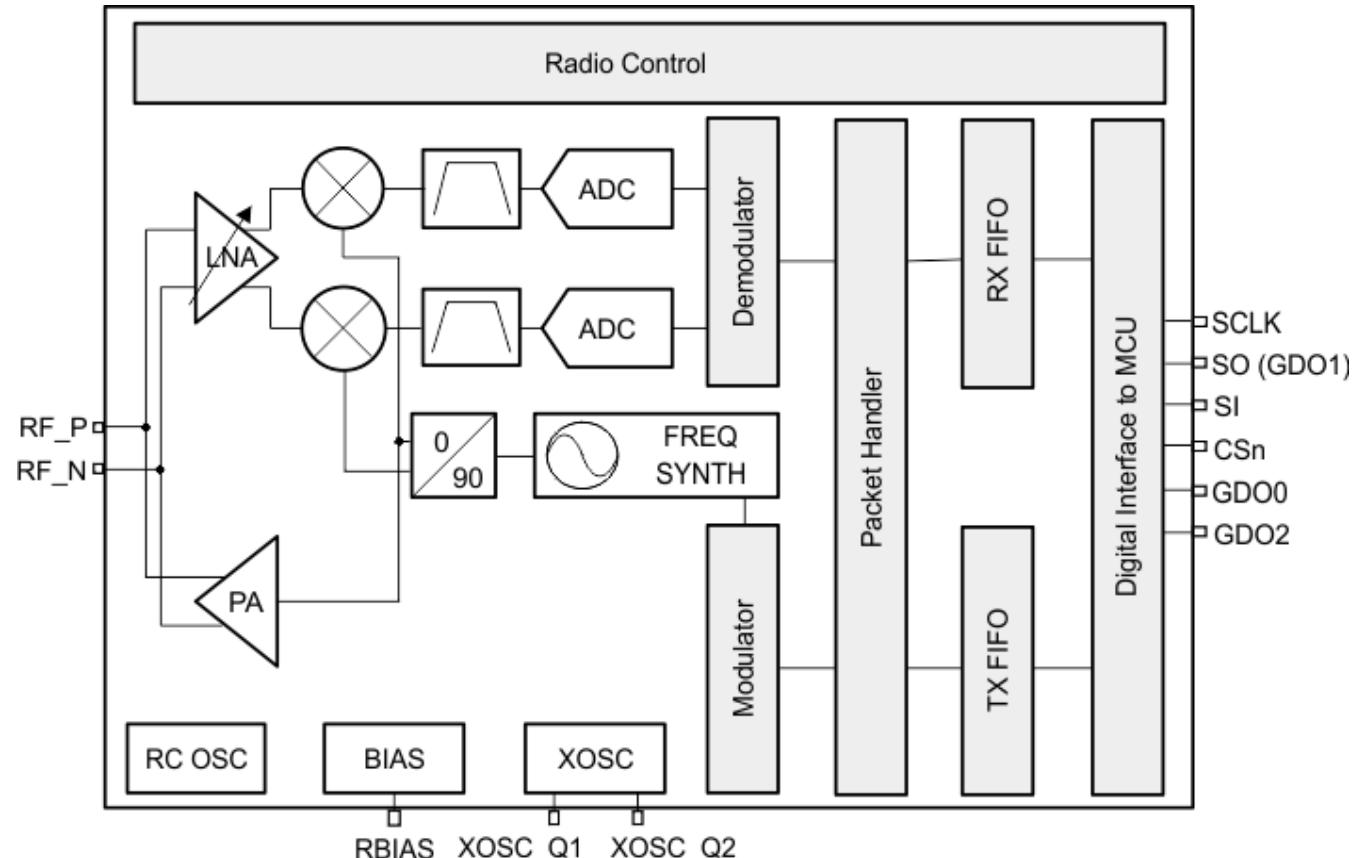
(Good) Digital Design Needs Analog Insights

- **Can synthesize large blocks at “medium” frequencies in ASIC flow, but**
 - Need to know transistors to design the cells
 - Really need to know transistors to design memories
- **Lots of analog issues to deal with when push digital performance, power, etc.**
 - Charge sharing, interconnect parasitics, etc.
- **Matching growing concern in advanced CMOS technologies**
 - Especially in memories

Why Analog Circuits?

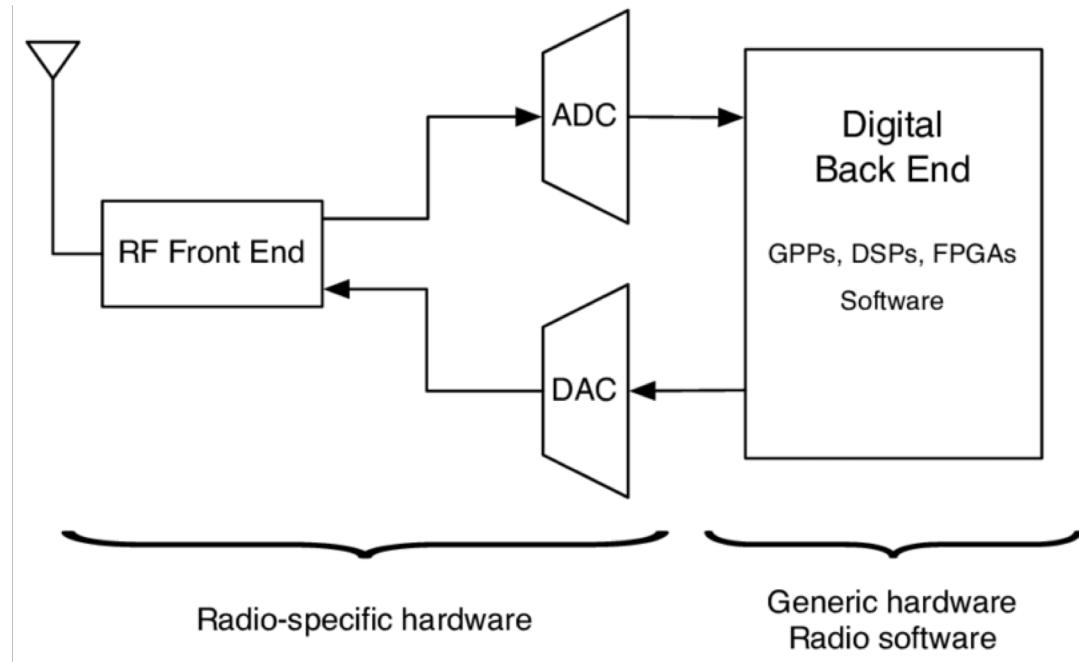
- **The “real” or “physical” world is analog**
 - Analog is required to interface to just about anything
 - Digital signals have analog characteristics too...
- **In many applications, design of analog components is in the critical path**
 - More later

Example: RF Transceiver



<http://www.ti.com/product/CC110L>

Can we replace the transceiver with an ADC / DAC?



- Is analog design going to become ADC/DAC design ?

Another Example

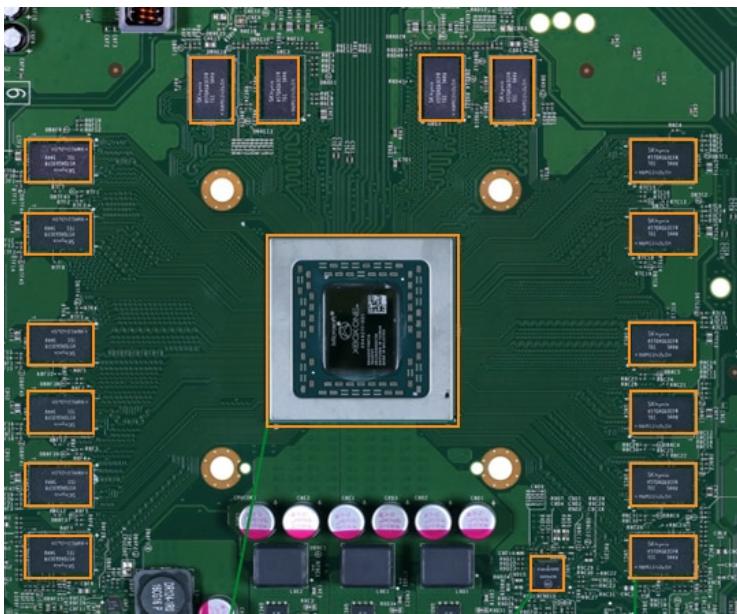
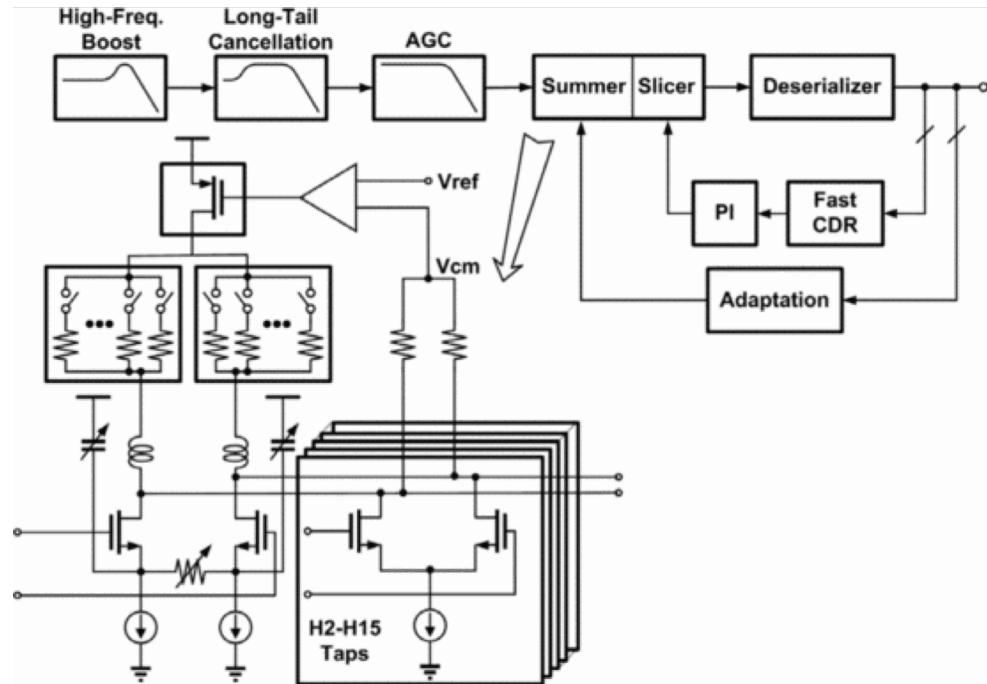


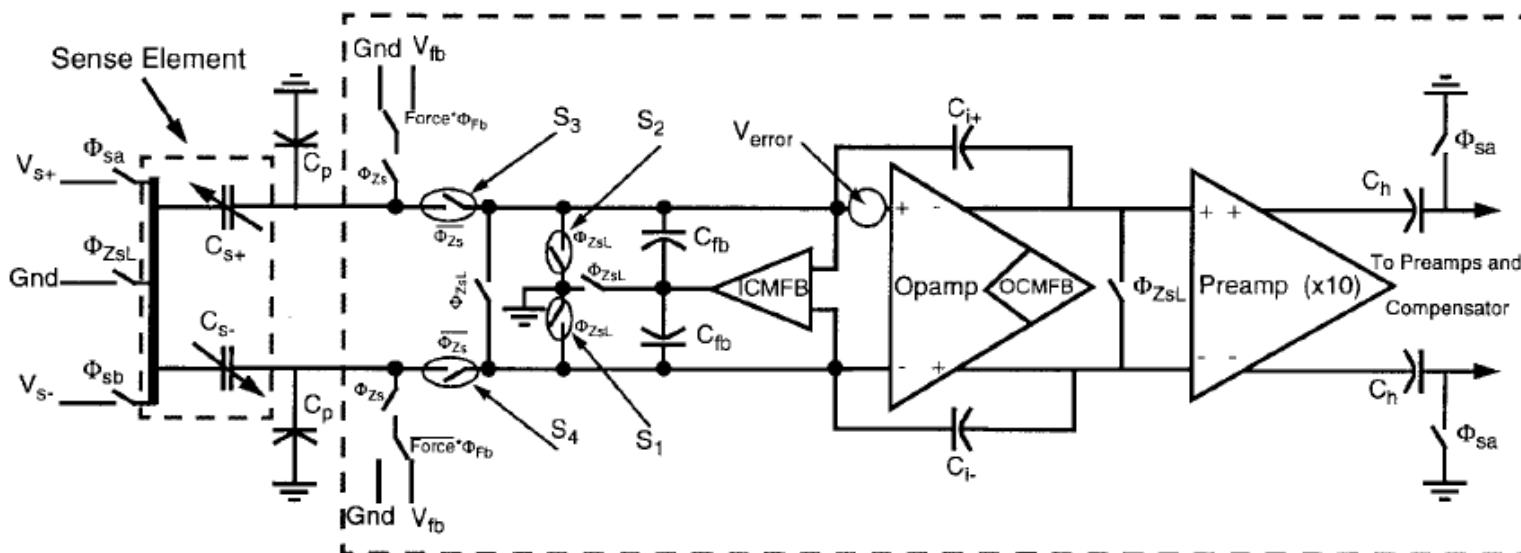
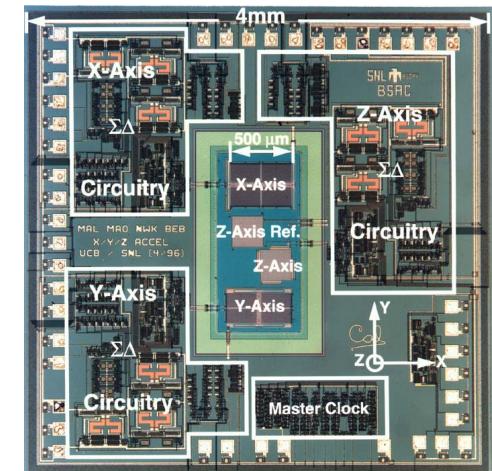
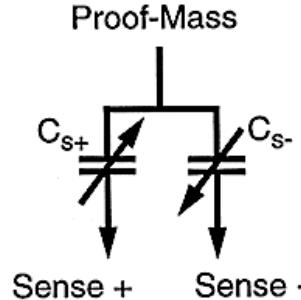
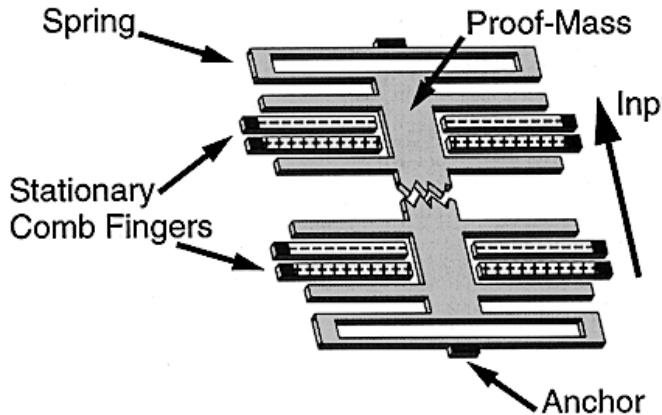
Image from <http://ihsmarkit.com>



From P. Upadhyaya, ISSCC 2015

- Power is once again the key motivating factor

Not Just Communications



Some Important Context

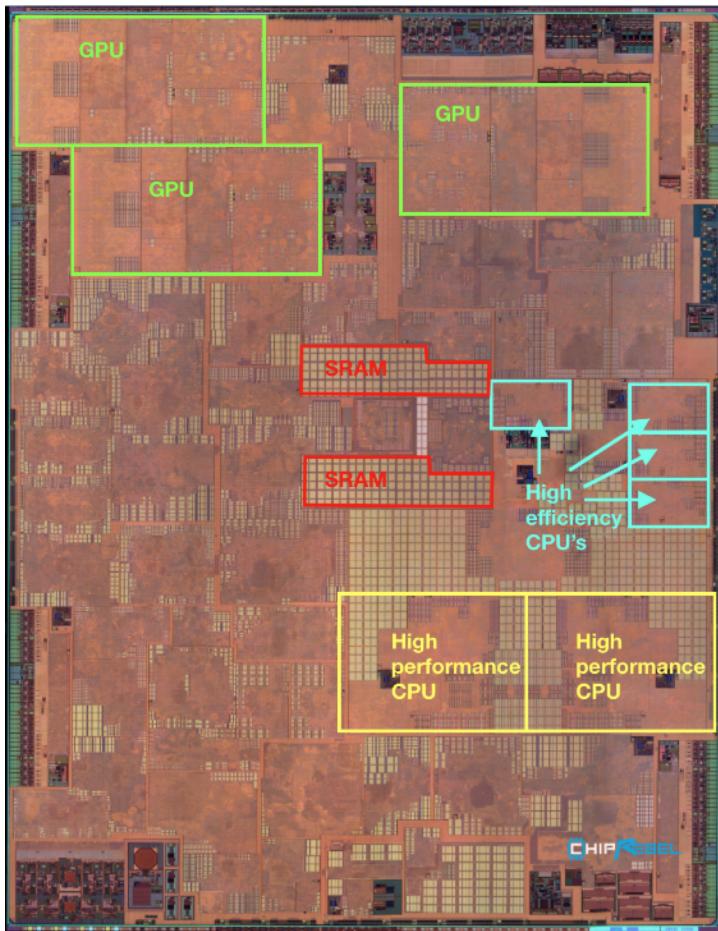


Image from chiprebel.com

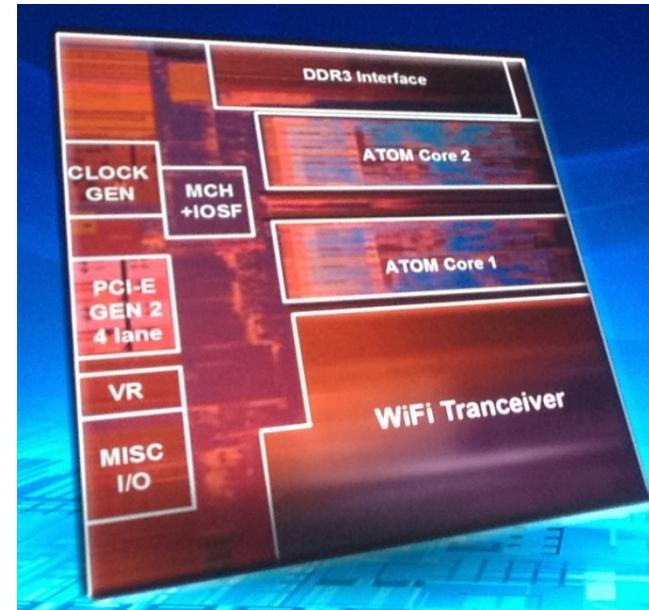
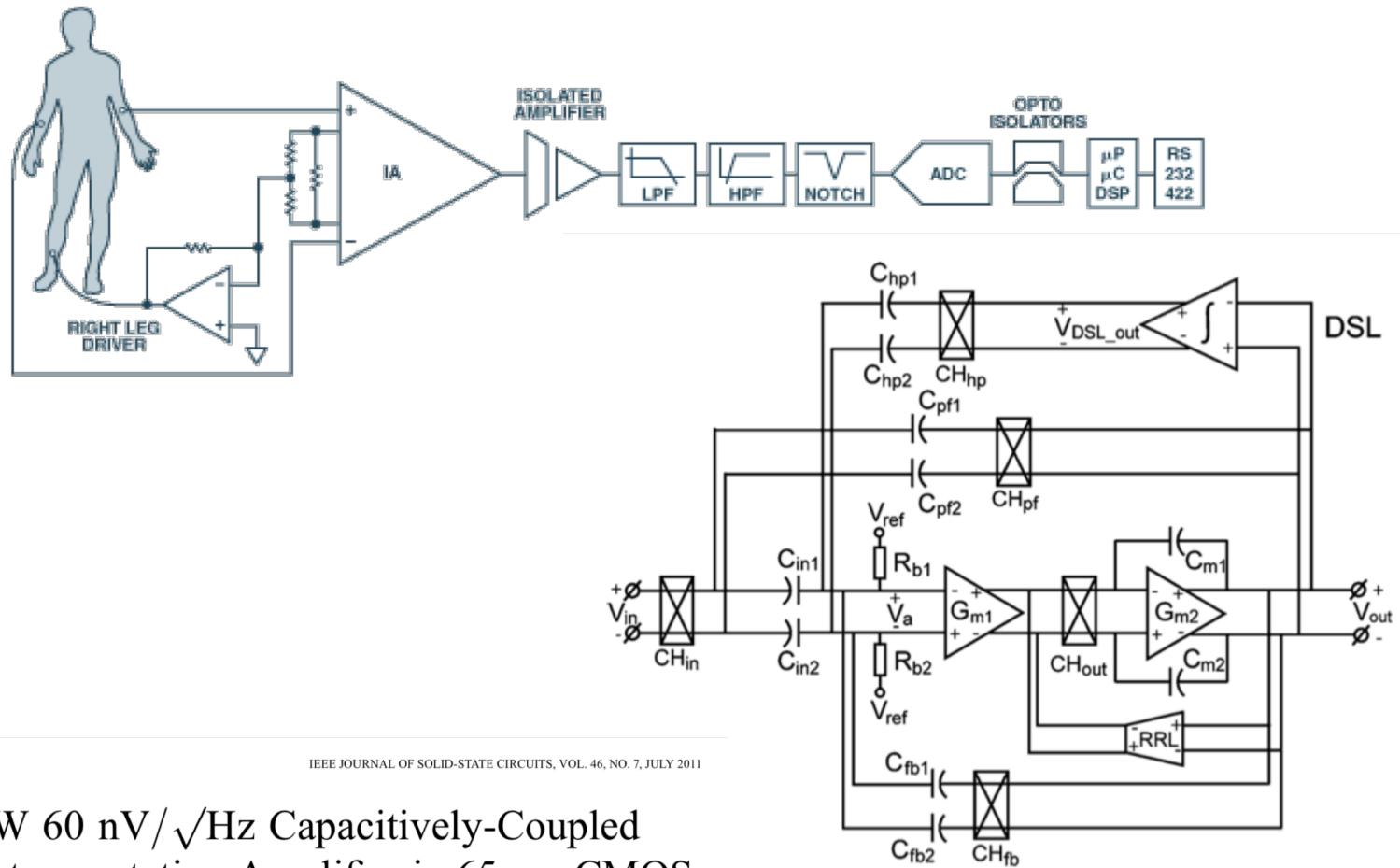


Image from moorinsightsstrategy.com

Biomedical Transceivers



1534

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 7, JULY 2011

A $1.8 \mu\text{W}$ $60 \text{ nV}/\sqrt{\text{Hz}}$ Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes

Qinwen Fan, Student Member, IEEE, Fabio Sebastian, Student Member, IEEE, Johan H. Huijsing, Life Fellow, IEEE, and Kofi A. A. Makinwa, Fellow, IEEE

Digital Versus Analog

- Abstraction in digital is Boolean logic (1's, 0's)
- At a higher level, it's gates and registers (RTL)
- Abstraction in analog is the device model
(BSIM is a few thousand lines long)
- At a higher level, it's the op-amps and OTAs
- Digital layout is often automated
- Analog layout is traditionally hand crafted for precision and accuracy
 - This is changing ! (BAG)

Analog versus RF

- **What is RF?**
 - It's analog with inductors! (+ T-lines and resonators)
- **Signal is usually narrowband sinusoidal modulation.** Tuned circuit techniques are used for signal processing.
- **RF impedance levels are relatively low for wideband operation.**
- **Analog impedances are high (low) for voltage (current) gain.**
- **Voltage/current gain versus power gain.**
- **Analog can be discrete time (sampled).**
 - RF is usually continuous → “digital” RF

Digital Assisted Analog

- Take advantage of “free” horsepower in a modern CMOS process to perform as much signal processing as possible.
- One RF inductor ($200\mu \times 200\mu$) can be replaced by a microprocessor in 90nm technology!
- Use digital calibration to tune out offsets, to center the filter cutoff frequencies, to tune the frequency of oscillators, etc.

Mixed Signal Design

- The design of some communication circuit building blocks, such as PLL (phase-locked loops), PLL based frequency synthesizers, analog to digital converters, involves the co-design of several analog/digital building blocks.
- In a PLL, the prescalars and programmable dividers and phase detectors are high speed digital circuits. Increasingly the loop filter and VCO are adopting digital techniques.

What You Will Therefore Be Doing

- **You will be tasked with building many different variants of the same function/block**
- **You will be tasked with building many different blocks**
- **You will be tasked with putting many different blocks together to realize a (sub-) system**
- **How do you do this efficiently without (re-)introducing any known errors?**

Re-Use is the Key

- **Today: Integrate pre-designed blocks (IP)**
 - But re-use is still limited – IP is blackbox, so if ever need to extend/modify, usually end up building your own
- **Berkeley view: Capture designer's knowledge (methodology) as an executable generator**
 - Good methodologies will be parameterized (i.e., support variants)
 - New features supported by incrementally extending the code

In Other Words...

- Your goal as an analog designer should not be to deliver a specific *instance*.
- Instead, you should strive to realize the best *generator* that you can
 - So that the generator can be executed to realize any instance you are tasked with building
 - And so that you can actually effectively re-use your colleagues work (and they can re-use yours)

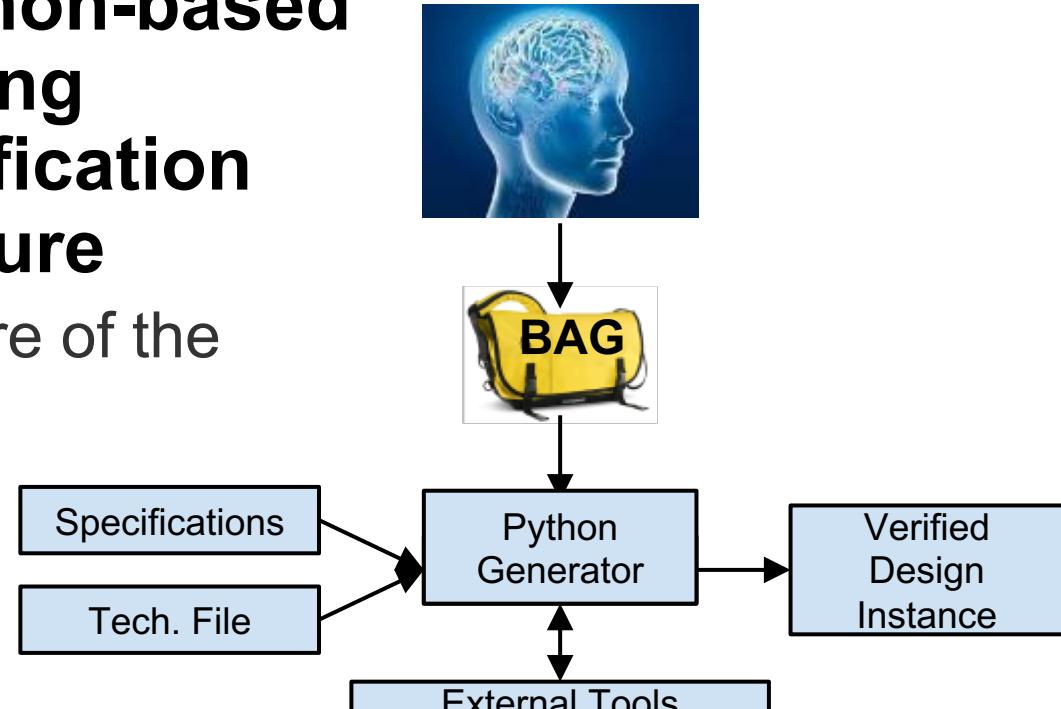
Berkeley Analog Generator (BAG)

- Hierarchical, Python-based framework allowing executable specification of design procedure

- I.e., BAG takes care of the “plumbing”

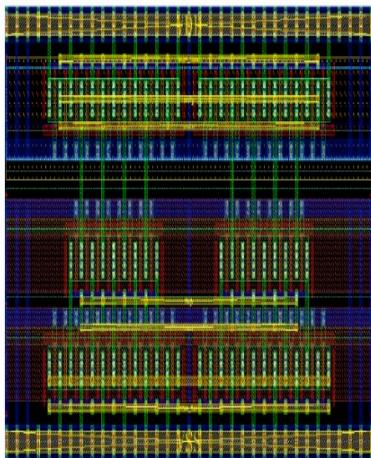
- Will not require you to use BAG in this class

- But forcing yourself to codify your methodology is an outstanding way to check and develop your understanding

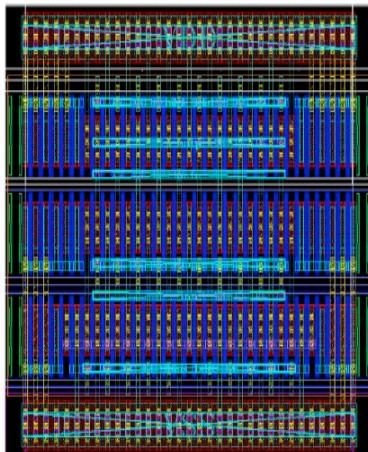


J. Crossley et al., ICCAD Nov. 2013

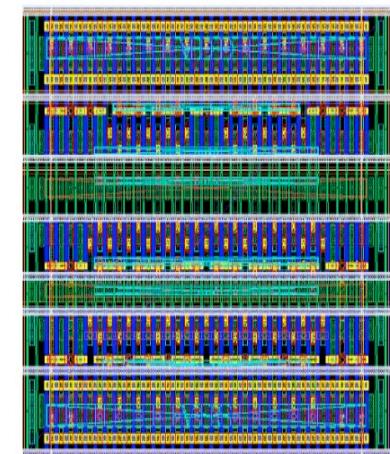
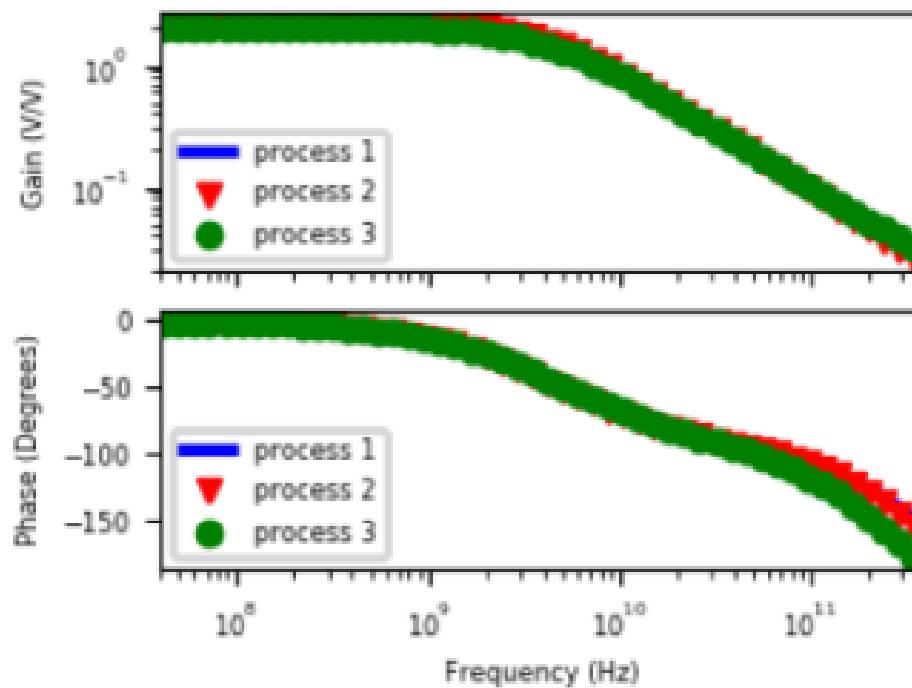
BAG Example



SOI



Bulk



FinFET

Course Outline (approx.)

- **Module 1: Analog design core**
 - “Modeling” MOS transistors
 - Electronic noise and noise analysis
 - GBW- and noise-limited amplifier design
- **Module 2: MOS amplifier implementation**
 - OTA topologies and design
 - Time-domain behavior (settling)
 - Interference mitigation
 - Common-mode feedback

Course Outline (approx.)

- **Module 3: AFE system (Photonic Link) design**
 - Link circuit components and analysis
 - Comparators
 - Layout and matching effects
 - Offset cancellation
- **Module 4: Wrap-up**
 - Discrete time analog circuits
 - Sampling
 - Biasing and references
 - Design strategies/motifs

EECS 240 versus 247

- **EECS 240**
 - Transistor level building blocks
 - Device and circuit fundamentals
 - Little abstraction
 - SPICE
- **EECS 247**
 - Macro-models, behavioral simulation, large systems
 - Signal processing fundamentals
 - High level of abstraction
 - Matlab

240 versus 242/142

- 142/242 are concerned mostly with narrowband amplification (tuned circuits) and sinusoidal response. Circuits are often non-linear (mixers, oscillators, power amplifiers). Feedback is seldom used in classical RF.
- 240 focuses on highly linear precision amplifiers. These amplifiers are usually realized using high gain and feedback.

240 versus 231

- In 240 we review important device physics and CMOS process. But the focus of the course is on circuits and not on devices. For the most part, we treat the transistors as black boxes described by complicated equations. But this is only a concern when determining the DC operating points and the voltage swing of the amplifier.
- Small signal models are very handy for understanding analog circuits. No matter how complicated the transistor (IV, CV), the AC models we use are easy and lend well to hand analysis.

What's Missing?

- PLL's and DLL's are key analog building blocks that are extensively used in almost all systems
- PLL's are truly mixed signal and involve digital, analog, and RF blocks
- If time permits, will spend a week on analog aspects of PLL design