EE240B HW 1

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February 8, 2019

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1. For a transistor in strong inversion, the current is dominated by drift rather than diffusion. The channel profile is nevertheless non-uniform which means there is a drift current even in strong inversion. Assuming the square law model (which ignores drift) is a good estimate of the channel charge profile, calculate the diffusion current and compare it to the drift current.

2. For your technology DK, what is the compact model used? Which version number? Does the model use binning? If so, by which parameters?

   I'm using GPDK 45nm. The compact model is BSIM v4 based. Binning is done using the $l_{min}, l_{max}, w_{min}, w_{max}$ parameters present in each model. There are 30 different bins for NMOS transistors. Binning changes V_{th}-related parameters (like vth0, lvth0, wvth0, pvth0), mobility-related parameters (like u0, lu0, wu0, pu0), subthreshold-related parameters (like voff, lvoff, wvoff, pvoff), and output resistance-related parameters (like pdiblc2, lpdiblc2).

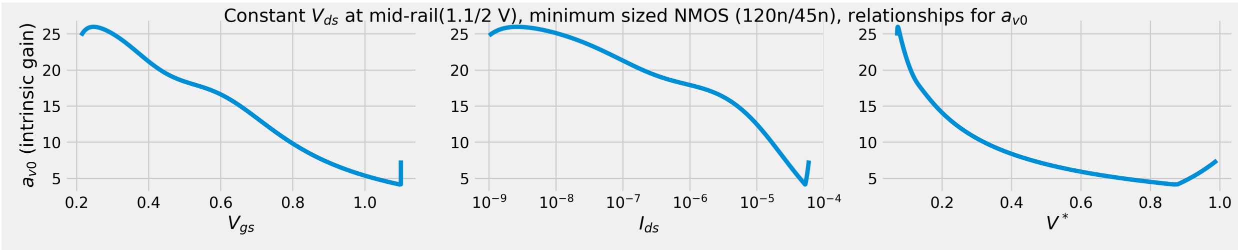
3. Besides W and L, what are the supported instance parameters for your model? Why are detailed layout dependent parameters (such as distance to well edge) used in some models?

   - finger width (W)
   - number of fingers (W)
   - folding threshold (finger width at which to apply device folding in layout)
   - S/D metal width (width of metal used to short source and drain)
   - some other ones I don't think matter

   The layout dependent parameters are auto-derived from the basic instance parameters (I guess for the PDK-reference layout of this transistor). These layout dependent parameters can be overridden as instance parameters. These detailed layout parameters can be used to estimate device parasitics at schematic-design time.

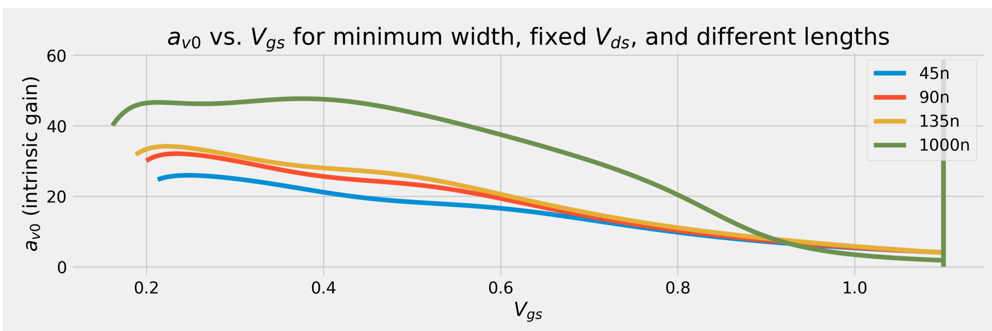
4. Set up a schematic (don't rely on the simulator to output small-signal parameters) and plot the intrinsic gain (a_{v0}) of the minimum sized transistor versus V_{gs}. Make sure you hold V_{DS} constant (use an ideal op-amp - VCVS) to setup the simulation. Plot the intrinsic gain versus I_{ds} and V^*. What is your conclusion? Do you expect a strong bias current dependence? Explain.

   I'm holding V_{DS} at mid rail $= \frac{1.1}{2}$ and sweeping I_{ds}. I'm using a SVT transistor with minimum size ($L_{min} = 45n, W_{min} = 120n$). Here are the plots:



- a_{v0} has an inverse relationship to drain current I_{ds} (logarithmic) and V_{gs} (linear)
  - This is expected because the r_o of the device decreases more rapidly than the g_m increases as I_{ds}, V_{gs} increase.
- a_{v0} versus V^*, follows the V_{gs} relationship and this is one reason for using the V^* design methodology to choose the transistor's operating point.

5. Now re-plot the instinsic gain a_{v0} for a few non-minimum length devices. Try $2L_{min}$, $3L_{min}$, and L_{max}. Does the gain depend on W? Explain why you should avoid using a very small W. L_{max} is the longest channel length supported by the DK.



In this process $L_{max} = 10\mu m$, but this gave weird simulation results, so I'm using $L_{max} = 1\mu m$.

- The intrinsic gain also doesn't depend on L after the transistor is strongly saturated since the r_o vs g_m relationship begins to look similar across lengths.
- The intrinsic gain generally doesn't depend on W since r_o and g_m both scale linearly with the transistor width.
- A very small W however has a proportionally larger C_{dd} and C_{gg} than a wider transistor, which can lead to significant schematic/layout mismatches post-layout and extraction (and frequency dependent gain differences too).

6. Which capacitance model does your model use? What is the charge partition scheme?

   Look at capmod, xpart (in the capacitance parameter section), look these up the bsim manual

7. Setup a simulation to plot the normalized input capacitances seen from the gate (C_{gs}, C_{gd}, C_{gb}) of a MOS device as you vary V_{gs} and hold V_{ds} constant in triode and saturation (normalize by C_{ox}). Are the expected symmetry properties upholding? Specify as many physical constraints as possible and check to see they are upheld by the model

   Hold off on this until the SS gain parameters are done.

8. Plot $\frac{g_m}{I_d}$ versus V_{gs} for the minimum, $2L_{min}$, $3L_{min}$, and L_{max} of your technology. Superimpose the expected sub-threshold and square-law behavior and compare.

   I can do this with the data I already have.

9. Plot V^* versus V_{gs} for the minimum, $2L_{min}$, $3L_{min}$, and L_{max} of your technology. Superimpose the expected sub-threshold and square-law behavior and compare.

   Same data can be analyzed.

10. Plot f^T vs V^*. Make sure to set up a schematic to extract f^T rather than using the SS-parameters of the model. Use L_{min}, $2L_{min}$, $3L_{min}$, and L_{max} of your technology. Explain the trends.

    I need to update the schematic to include f^T calculation.

11. Plot the product of f^T and a_{v0} vs V^* for L_{min}, $2L_{min}$, $3L_{min}$, and L_{max}. For which V^* is the product maximum for each case? Once I have f^T this is easy.

12. Design an amplifier that achieves a DC gain of 20 and a unity gain frequency of 500 Mhz while driving a load of 1pF. Specify the required V^*, bias current, V_{gs}, and device dimensions. Use the results of the previous problems to guide the design choices. Verify with SPICE.