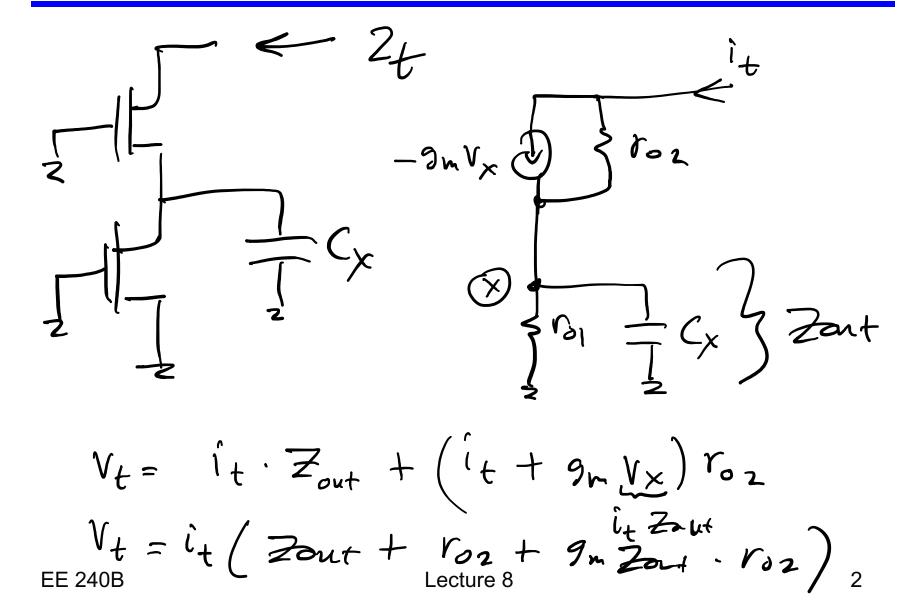
EE 240B - Fall 2019

Advanced Analog Integrated Circuits Lecture 8: Operational Transconductance Amplifiers (II)

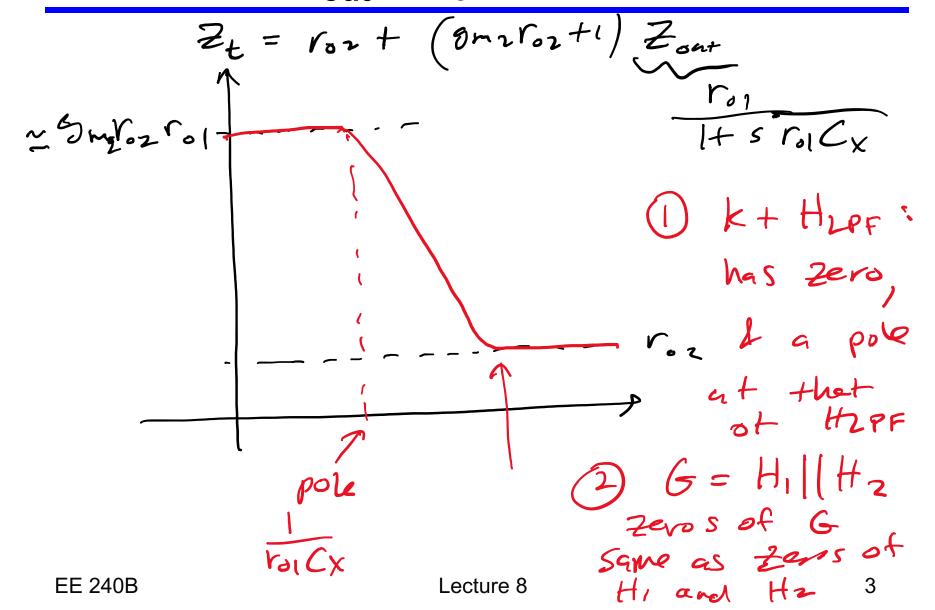


Ali M. Niknejad Dept. of EECS

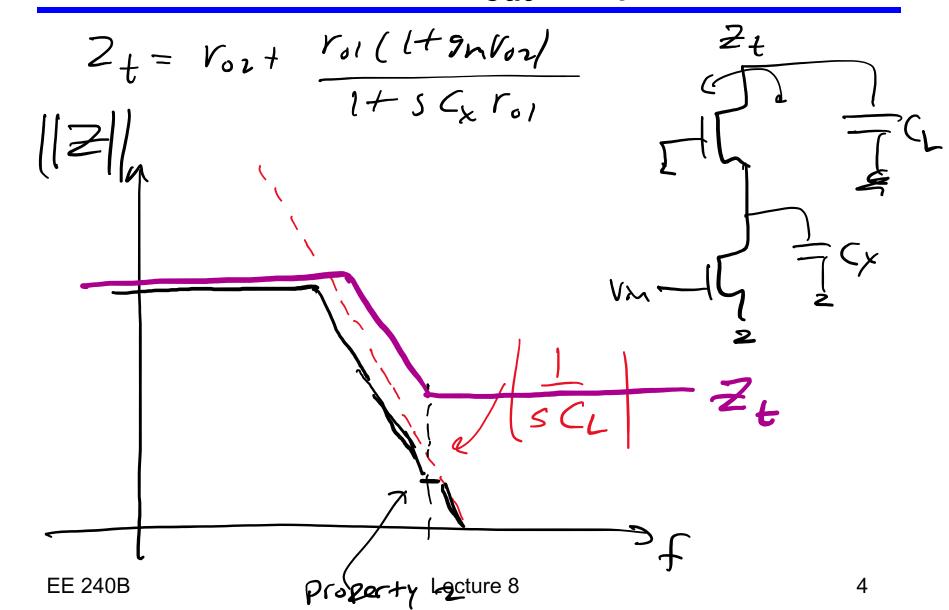
Closer Look at Cascode Dynamics



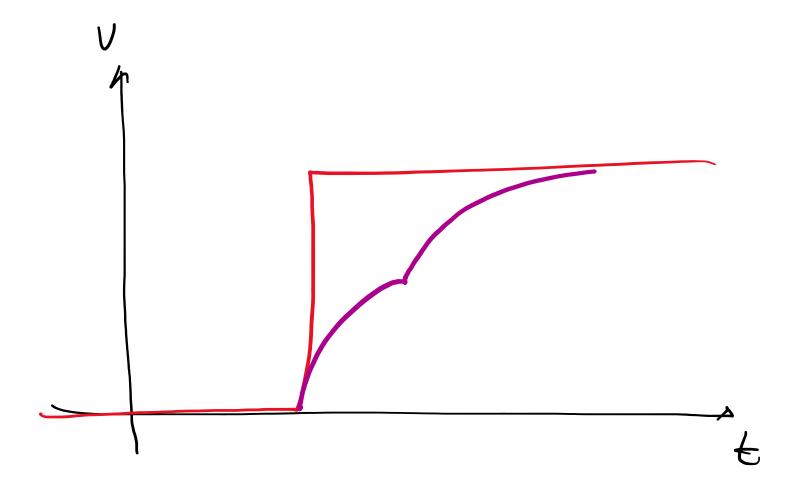
Cascode Z_{out} vs. f



Load + Cascode Z_{out} vs. f



Pole-Zero Doublets

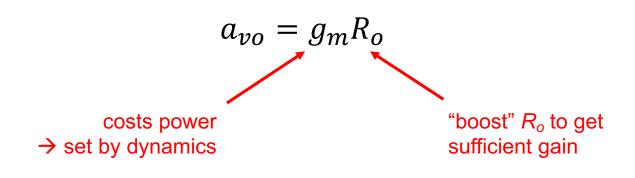


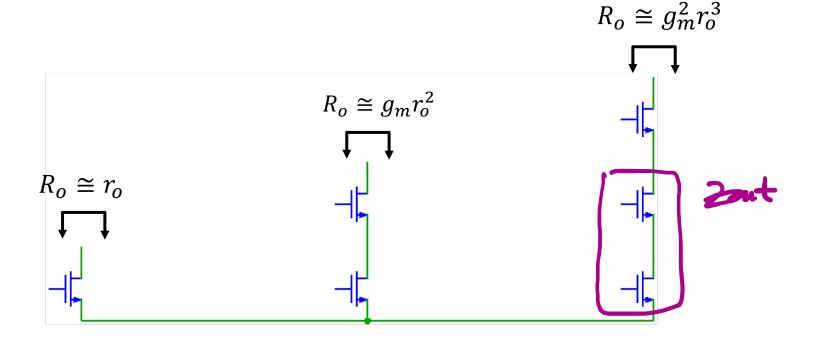
Discussion

- Doublet generally not important in "simple" cascode since it shows up at high frequencies
- But, doublets can show up in similar circuits
 - In particular, when you try and increase the gain beyond what a simple cascode can support

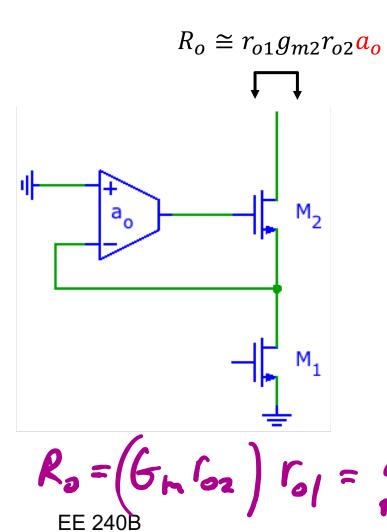
Openloop Gain







Gain Boosting



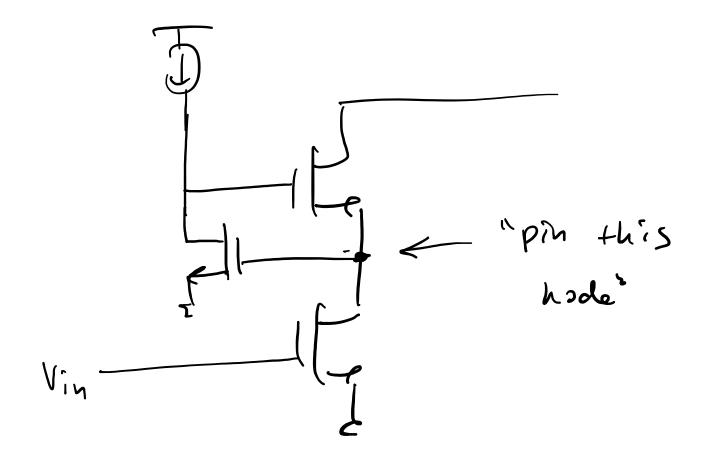
Use feedback to further increase R_{out}

 No increase of V_{min} (unlike double cascode)

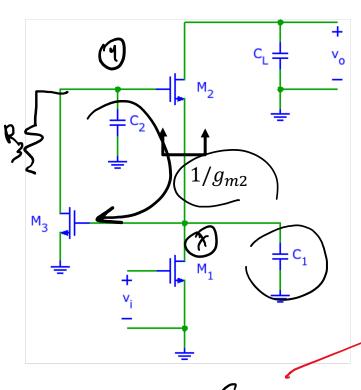
References:

- B. J. Hosticka, "Improvement of the gain of MOS amplifiers," JSSC, Dec. 1979, pp. 1111-4.
- E. Sackinger and W.
 Guggenbuhl, "A high-swing high-impedance MOS cascode circuit",
 JSSC, Feb. 1990, pp. 289-298.
- K. Bult, G. Geelen, "A fast-settling CMOS op-amp for SC circuits with 90-dB DC gain," JSSC, Dec. 1990, pp. 1379-84.

8



High Frequency Analysis



Loop gain
$$|T|=1$$
 \mathbb{C} $\omega_{\infty} \frac{g_m}{C_2}$

$$T(s) = \frac{g_{m3}}{sC_2} \frac{1}{1 + s\frac{C_1}{g_{m2}}} = \frac{\omega_{u3}}{s} \frac{1}{1 + s\frac{C_1}{g_{m2}}}$$

For acceptable phase margin

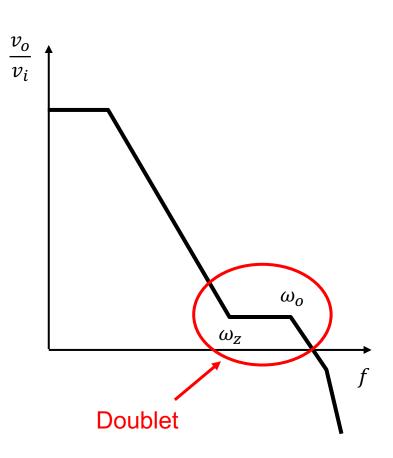
$$\frac{g_{m2}}{C_1} = \omega_{p2} > k\omega_{u3}$$

Overall Amplifier Response

$$\frac{v_o}{v_i} = \frac{g_{m1}}{sC_L} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_o^2}}$$

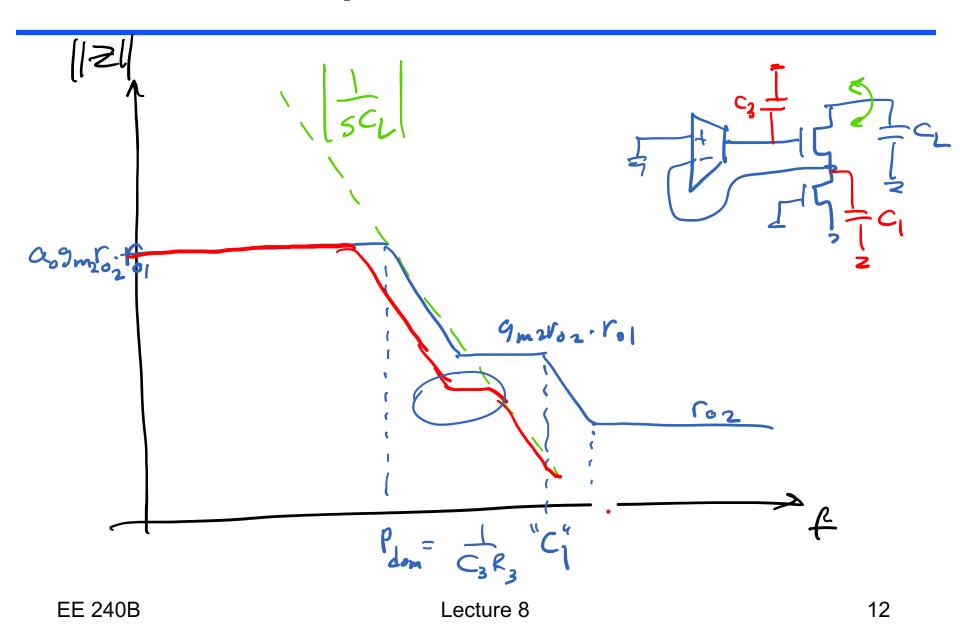
$$\omega_z = \omega_{u3}$$
 $\omega_o = \sqrt{r}\omega_{u3}$ $Q = \frac{1}{\sqrt{r}}$

for
$$Q < 0.5 \implies r > 4$$



Ref: M. Das, "Improved design criteria of gain boosted CMOS OTA with high-speed optimizations," IEEE CAS II, March 2002, pp. 204-7.

Graphical Derivation



Pole-Zero Doublets

- Often "closely spaced"
 - May miss in Bode plot!
- Origins
 - Feedforward (e.g. Miller capacitance, C_{qd} , ...)
 - Frequency dependent degeneration (series feedback, e.g. cascode)
- Concerns
 - Ringing (if high Q)
 - Slow settling

Ref: Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits*, pp. 347–352, Dec. 1974.

Doublet Settling

• Amplifier model: replace G_{mo} with

$$G_m(s) = G_{mo} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \qquad \text{with} \qquad \begin{aligned} \omega_p &= \beta \omega_{-3dB}, & \omega_{-3dB} & \text{is bandwidth of } T(s) \\ \omega_z &= \frac{\omega_p}{\alpha} \\ \alpha &= 1 + \varepsilon & \text{with} & |\varepsilon| << 1 \end{aligned}$$

Closed-loop response

$$\frac{V_o}{V_{in}} = -c \frac{1}{1 + s \frac{C_{Leff}}{FG_m(s)}} \cong -\frac{c}{1 + \frac{s}{\omega_{-3dB}}} \left(\frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_{pp}}} \right) \qquad \text{with} \qquad \omega_{-3dB} = \frac{FG_{mo}}{C_{Leff}} \\ \omega_{pp} \cong \omega_p$$

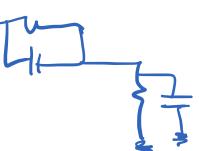
Notation from Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits*, pp. 347–352, Dec. 1974.

Doublet Step Response

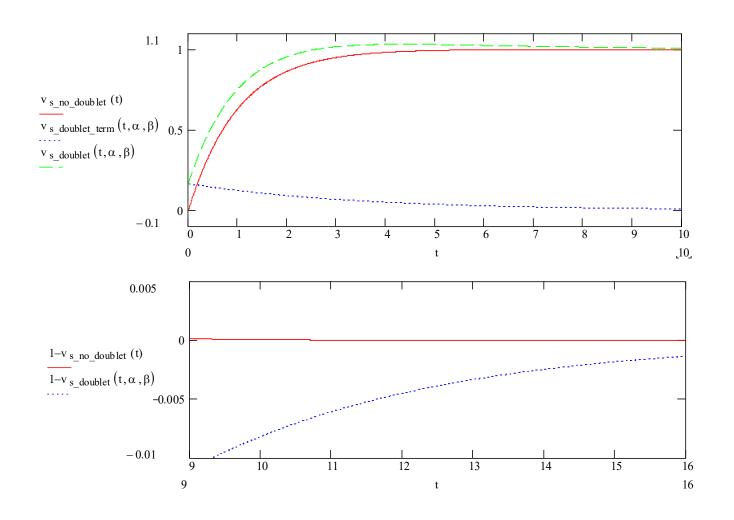
$$v_{o,step}(t) = -cV_{step}\left(1 + Ae^{-t\omega_{-3dB}} + Be^{-t\omega_{pp}}\right) \qquad \text{with} \qquad \qquad B \cong \varepsilon \frac{\beta}{1 - \beta^2}$$

$$\text{main amplifier}$$

- Case A: $\omega_{pp} > \omega_{-3dB}$
 - Doublet settles faster than main amplifier
 - Has no impact on overall settling time (unless B>>A)
- Case B: $\omega_{pp} < \omega_{-3dB}$
 - Doublet settles more slowly than main amplifier
 - Determines settling time unless B<<A
 - Acceptable in "low precision" applications (e.g. oscilloscope probes)
 - Avoid when precise settling is required



Doublet Example



$$\alpha = 1.5$$
 $\beta = 0.3$

Gain Boosting – Doublets

Doublet is near ω_{u3}

$$\omega_{u3} > \beta \frac{g_{m1}}{c_{Ltot}}$$
 for fast settling
$$\frac{g_{m2}}{g_{m2}}$$
 (large r)

$$\omega_{u3} < \frac{g_{m2}}{c_1}$$
 (large r)

Parasitic pde

of feedback loop

- Practical designs show 20-30% power penalty for booster
 - Since usually $C_2 < C_L$

If it works, do it again!

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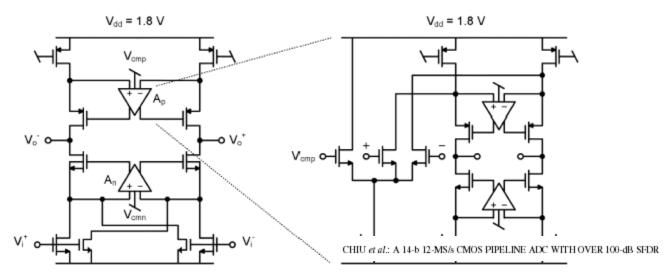
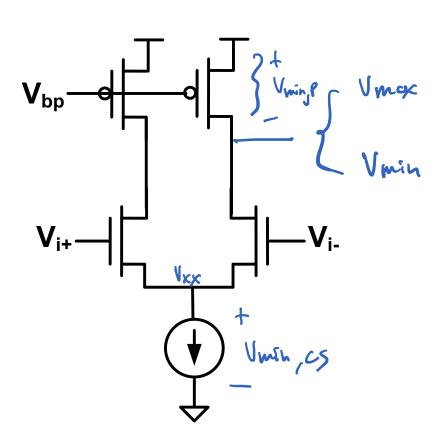


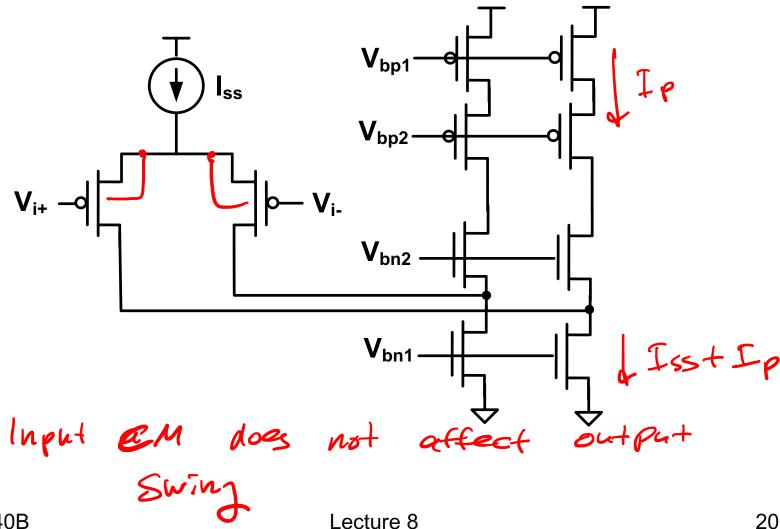
Fig. 8. Nested CMOS gain-boosting technique.

- Since in advanced scaled CMOS $g_m r_o$ is small, we can use nested gain boosting for higher output impedance.
- Watch out for pole-zero doublets!

Telescopic OTA: Common Mode vs. Swing

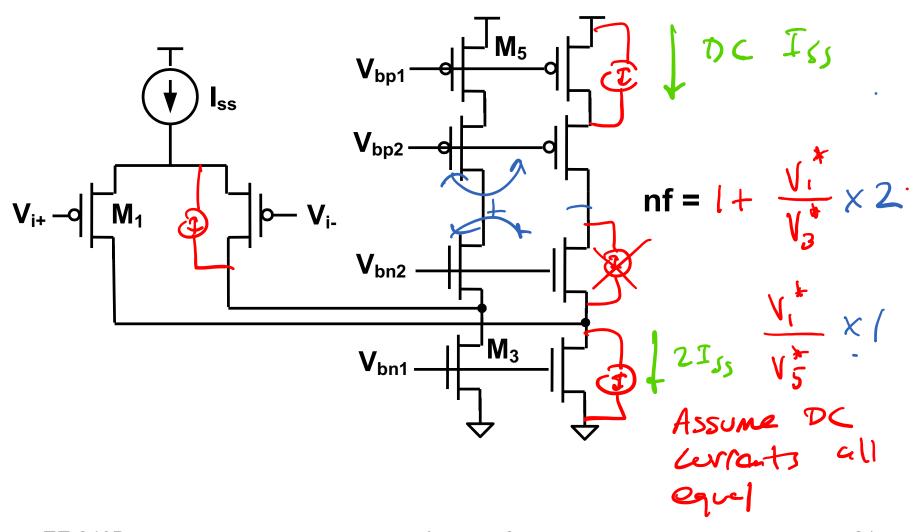


Folded-Cascode Schematic

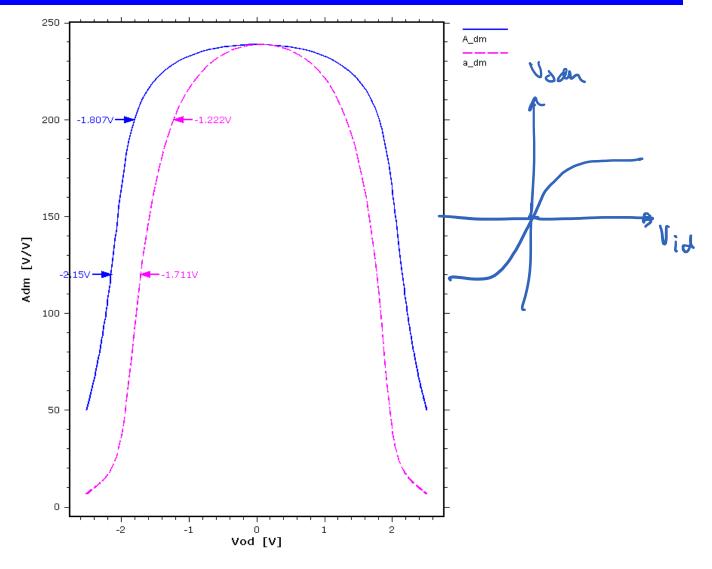


EE 240B

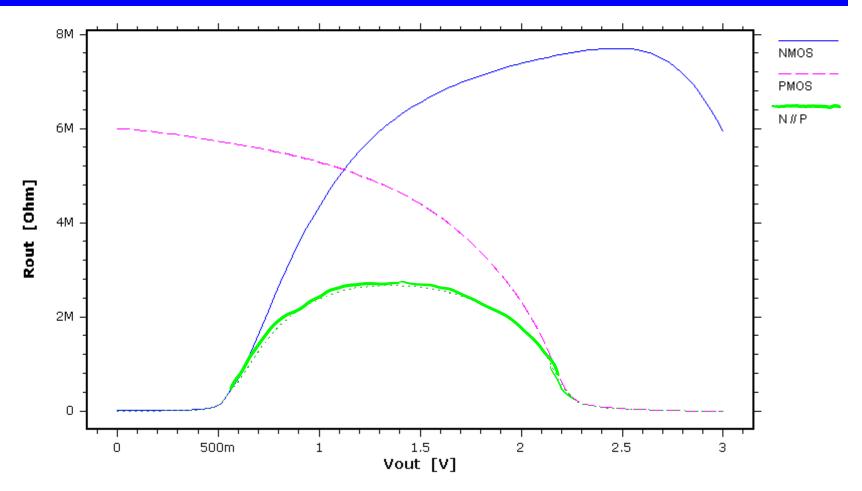
Folded-Cascode Noise



Low Frequency Gain: a_v and A_v

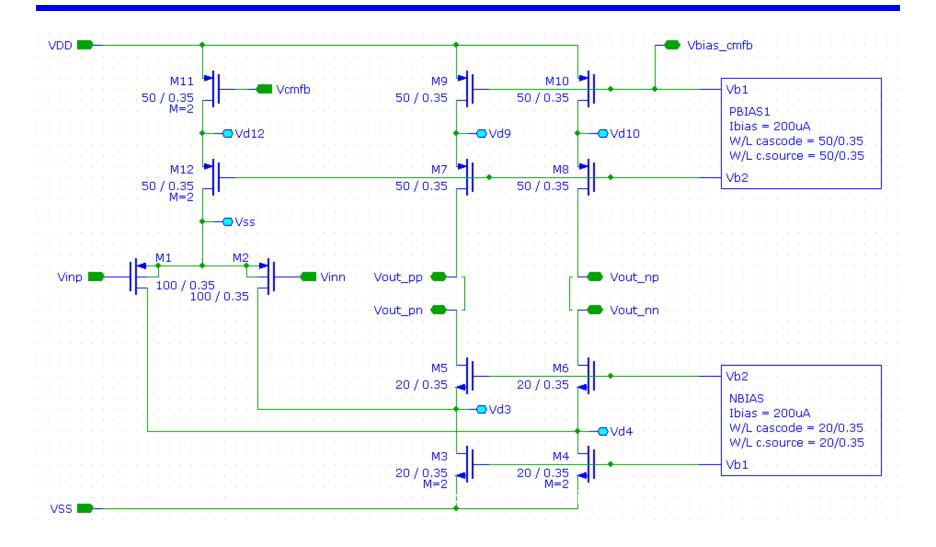


Output Resistance

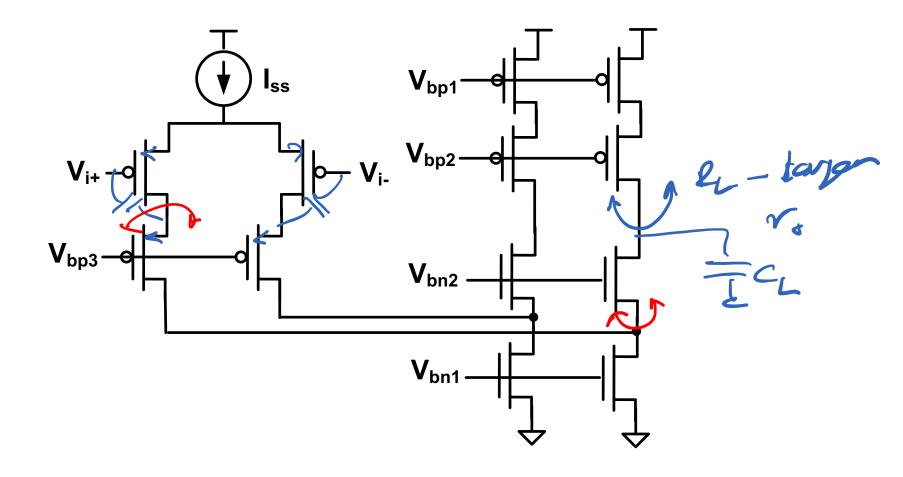


Beware of r_o imbalance between NMOS and PMOS current sources

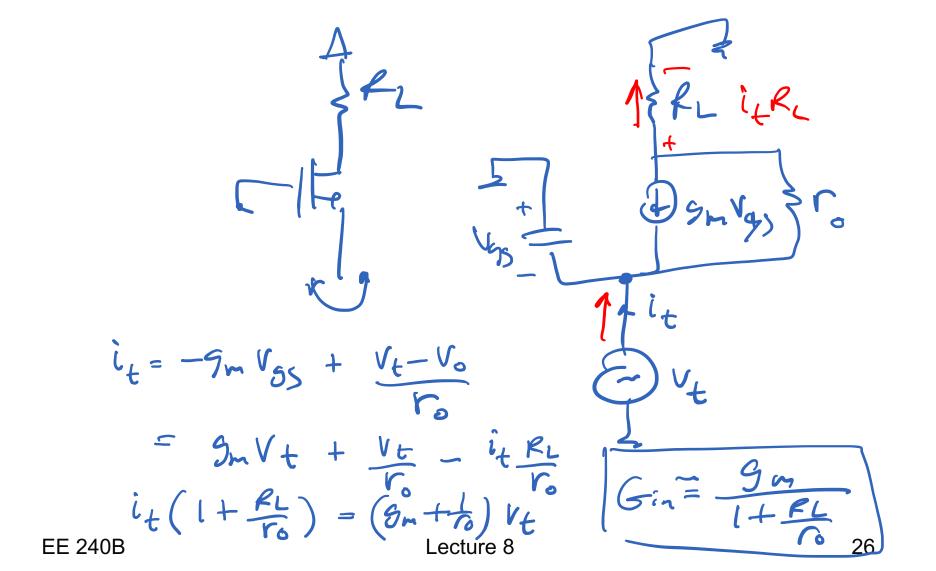
Simulation Schematic



Input Cascode



Reminder: Cascode Zin



Biasing and Parasitic Feedback

