UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 240B
Spring 2019

Homework Assignment #1
Due date: Midnight on Friday, 2/8/2019

1. For a transistor in strong inversion, the current is dominated by drift rather than diffusion. The channel profile is nevertheless non-uniform which means there is a drift current even in strong inversion. Assuming the square law model (which ignores drift) is a good estimate of the channel charge profile, calculate the diffusion current and compare it to the drift current.

2. For your technology DK, what is the compact model used? Which version number? Does the model use binning? If so, by which parameters?

3. Besides W and L, what are the supported instance parameters for your model. Why are detailed layout dependent parameters (such as distance to well edge) used in some models?

4. Setup a schematic (do not rely on the simulator to output small-signal parameters) and plot the intrinsic gain of the minimum sized transistor versus V_{gs}. Make sure you hold V_{DS} constant (use an ideal op-amp – a voltage-controlled voltage source) to setup the simulation. Also plot the intrinsic gain versus I_{ds} and V^*. What is your conclusion? Do you expect a strong bias current dependence? Explain.

5. Now re-plot the intrinsic gain for a few non-minimum length devices. Try $2*L_{min}$, $3*L_{min}$, and L_{max}. Does the gain depend on W? Explain why you should avoid using a very small W. L_{max} is the longest channel length supported by the DK.

6. Which capacitance model does your model use? What is the charge partition scheme?

7. Setup a simulation to plot the normalized input capacitances seen from the gate (C_{gs}, C_{gd}, C_{gb}) of a MOS device as you vary V_{gs} and hold V_{ds} constant in triode and saturation (normalize by C_{ox}). Are the expected symmetry properties upholding? Specify as many physical constraints as possible and check to see that they are upheld by the model.

8. Plot g_m/I_d versus V_{gs} for the minimum, $2*L_{min}$, $3*L_{min}$, and L_{max} of your technology. Superimpose the expected sub-threshold and square law behavior and compare.

9. Plot V^* versus V_{gs} for the minimum, $2*L_{min}$, $3*L_{min}$, and L_{max} of your technology. Superimpose the expected square law behavior and compare.

10. Plot f_T versus V^*. Make sure you setup a schematic to extract f_T rather than using the small-signal parameters of the model. Use L_{min} , $2*L_{min}$, $3*L_{min}$, and L_{max} of your technology. Explain the trends.

11. Plot the product of intrinsic gain and f_T for L_{min} , $2*L_{min}$, $3*L_{min}$, and L_{max}. For which V^* is the product maximum for each case?

12. Design an amplifier that achieves a DC gain of 20 and a unity gain frequency 500 MHz while driving a load of 1pF. Specify the required V^*, bias current, V_{gs}, and device dimensions. As much as possible, use the results of the previous problem to guide your design choices. Run SPICE to verify.