EE240B Project: Checkpoint 1 & 2

See our Github repo

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Contents

1 Checkpoint 1: System-Level Design

1.0 Top-Level Specs

To begin, we transcribe the specs given in the project description into a more formal form to reference later.

$$\omega_{pass} = 20 \text{ Mhz} \tag{1}$$
$$A_{v,dc} = 0 \text{ dB} \tag{1}$$
$$A_v(\omega_{pass}) \geq -3 \text{ dB} \tag{1}$$
$$\omega_{stop} = 200 \text{ Mhz} \tag{2}$$
$$A_v(\omega_{stop}) \leq -55 \text{ dB} \tag{2}$$
$$\text{Group Delay } = \tau_g(\omega) = \frac{d\angle H(j\omega)}{d\omega} \tag{3}$$
$$[\max(\tau_g(\omega)) - \min(\tau_g(\omega))]\Big|_{\omega=0}^{\omega=\omega_{pass}} \leq 3 \text{ ns} \tag{3}$$
$$\text{Dynamic Range } = DR = \frac{P_{sig,max} + P_{noise}(s)}{P_{noise}(s)}\Big|_{\omega=1\cdot 2\pi}^{\omega=\omega_{pass}} \geq 50 \text{ dB} \tag{4}$$
$$C_{load} = 40 \text{ fF} \tag{5}$$
$$V_{dd} = 1.2 \text{ V} \tag{6}$$
$$\text{minimize}(P_{static}) \tag{7}$$
$$\text{Passband Ripple } = Rip_{max} \leq 1 \text{ dB} \tag{8}$$
$$\text{Stable when driven by a 200mV differential step} \tag{9}$$

1.0.1 Methodology

We approached this design problem with a generator-centric methodology. As an even higher-level than using BAG, we incorporate open-source tools based in Python. First, filter transfer functions are synthesized `scipy` and the given filter specs. Concurrently, a real model of the active filter is generated using `ahkab`, which also synthesizes symbolic transfer functions that include OTA nonidealities. We quickly fit the synthesized filter to the circuit topology using naive design equations, and then use a optimizer to refit the filter resistance and capacitance after adjusting for real non-idealities extracted from transistor-level characterization. After constraining the space of design parameters, we verify that the noise and power meet specifications, and iterate as necessary.

1.1 Filter Type Selection

Given the gain and passband spec 1, the stopband spec 2, and the group delay spec 3, we can synthesize transfer functions for various filter types that minimally meet these specs (in terms of order and extension of passband frequency). We perform this iterative synthesis using the `scipy` Python library.

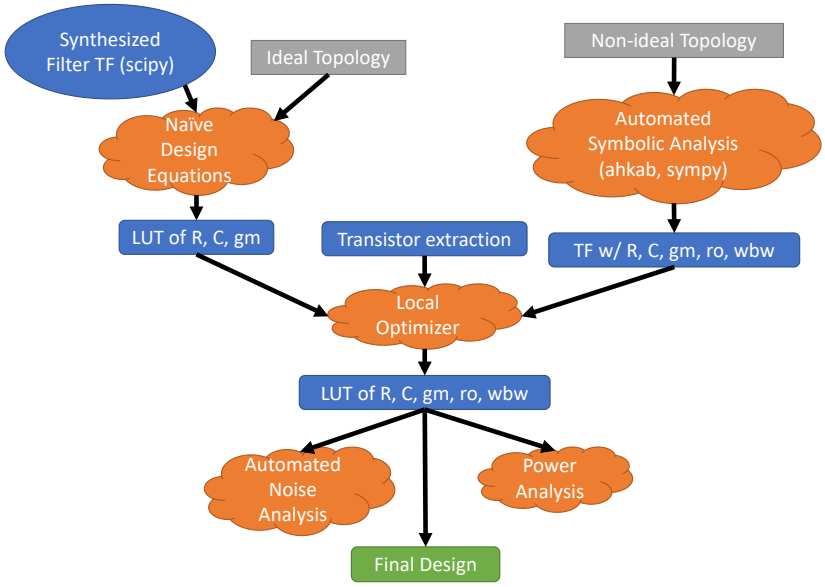

Figure 1: The flow to go from filter specs to a system-level design with parameterized blocks

Algorithm 1 Filter TF Synthesis

procedure SYNTHESIZETF($\omega_{pass}, \omega_{stop}, A_v(\omega_{stop}), Rip_{max}, \tau_{g,max}$)
  $O \leftarrow 1$
  $\omega_{pass,i} \leftarrow \omega_{pass}$
  while True do
    $BA \leftarrow$ SCIPY.IIRFILTER(N $\leftarrow O$, Wn $\leftarrow \omega_{pass,i}$, rp $\leftarrow Rip_{max}$, rs $\leftarrow A_v(\omega_{stop})$)
    if $A_v(BA, \omega_{stop}) < A_v(\omega_{stop})$ **then**
      $O \leftarrow O + 1$ ▷ Increase the filter order if stopband attenuation spec isn't met
    else if $A_v(BA, \omega_{pass}) < -3$ dB **then**
      $\omega_{pass,i} \leftarrow \omega_{pass,i} + 1$ Mhz ▷ Bump the passband corner if there's too much attenuation
    else if Passband Variation($\tau_{g,BA}$) $> \tau_{g,max}$ **then**
      $\omega_{pass,i} \leftarrow \omega_{pass,i} + 1$ Mhz ▷ Bump the passband corner if the group delay variation is excessive
    else
      return BA

This procedure returns a filter transfer function. Using this technique we can find optimal filter polynomial coefficients BA for each filter type. We plot the transfer functions' magnitude gain (Figure 2) and group delay (Figure 3) over frequency to show they meet the specs.

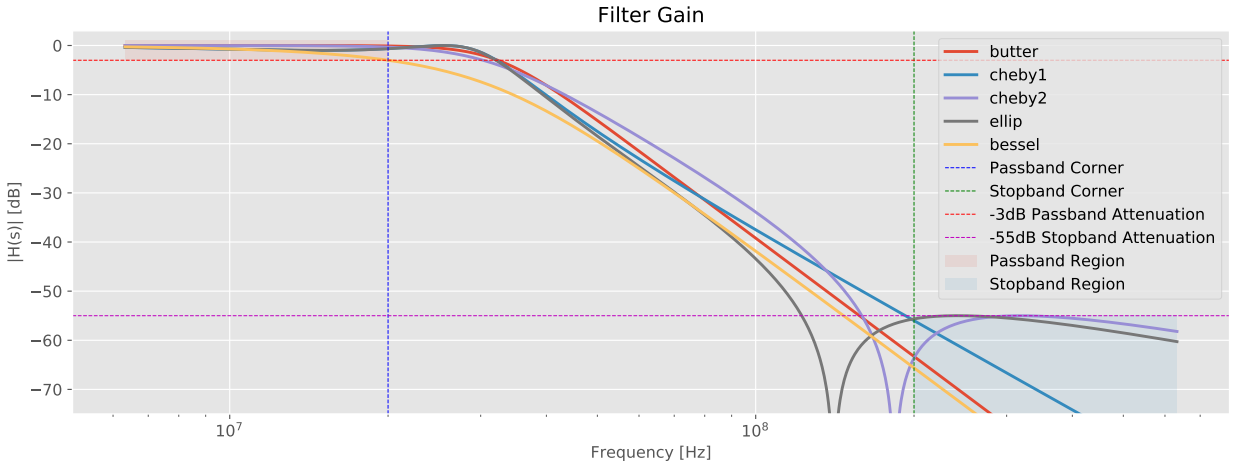

Figure 2: Magnitude gain for synthesized filter transfer functions

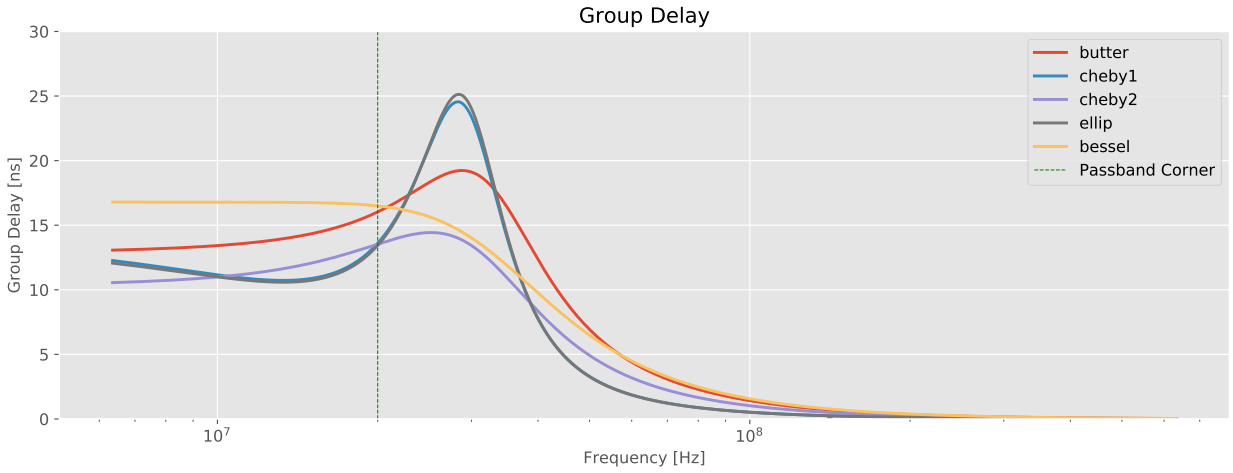

Figure 3: Group delay for synthesized filter transfer functions

We believe the *Butterworth filter* with order = 4 best fits the specifications and is the easist to design for because the passband frequency needs to be minimally pushed out to achieve the group delay spec and contains no zeros in the transfer function. The *Bessel filter* can also work, but may need to be redesigned to push forward the passband corner for the real design to not exceed -3dB attenuation at the corner frequency.

The other filter types either have zeros in the transfer function or have too much group delay variation forcing the passband corner too far up. They have the advantage of only needing an order = 3, but odd orders don't simplify the circuit topology anyways.

1.2 Filter Topology Selection

We initially considered the Sallen-Key and Multiple Feedback topologies using op-amps since they are straightforward to implement and cascading 2 stages will give us 4 poles as desired.

Later, we switched to using OTAs and decided on this simple 2 pole lowpass topology:

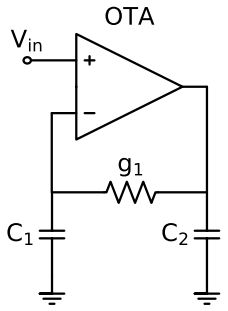

Figure 4: OTA-based lowpass filter with 2 poles and 3 passives, assuming the OTA's $R_{out} = \infty$. The output is taken from the top of C_1

The transfer function is:

$$H_{ideal}(s) = \frac{g_m g_1}{s^2 C_1 C_2 + s g_1 (C_1 + C_2) + g_m g_1}$$

The standard design equations are:

$$\omega_o = \sqrt{\frac{g_m g_1}{C_1 C_2}}$$
$$Q = \sqrt{\frac{g_m}{g_1}} \frac{\sqrt{C_1 C_2}}{C_1 + C_2}$$

Now assuming $C_1 = C_2 = C$, we can spec g_1 and g_m:

$$g2 = \frac{\omega_o C}{2Q}$$
$$g_m = 2Q\omega_o C$$

Since we are using a Butterworth filter, we set $Q = 1/\sqrt{2}$, and we extract ω_o from the transfer function provided by `scipy`.

These design equations are used to generate a table of (R, C, g_m) design points which will be refined in the next step. The rest of the analysis below considers a single-ended filter; a fully differential filter will to first-order have the same transfer function.

1.3 Op-Amp or OTA?

We initially chose op-amps as the active stage, but later realized that the output stage of op-amps is unnecessary for a filter with a capacitive load and just burns extra current. OTAs are more economical and have enough free variables to support the chosen filter family. We plan to cascade 2 of the lowpass OTA circuits (Figure 4) to form the filter.

1.4 Spec Out OTA Stages

The OTA non-idealities we consider are finite output resistance G_o, limited g_m, and finite bandwidth. We still assume that no DC current flows into the OTA.

$$g_m = \frac{g_{m0}}{1 + s/\omega_{bw}}$$
$$G_o = \frac{1}{R_o}$$

We choose to neglect output capacitance C_o and input capacitance C_i, since the parasitic caps are small compared to the filter capacitors and the parasitic caps can be lumped into the filter caps anyways once two filter stages are cascaded.

The transfer function is modified slightly after accounting for the non-idealities:

$$H_{nonideal}(s, r_o, \omega_{bw}) = \frac{g_{m0} r_o}{\left(-\frac{s}{\omega_{bw}} + 1\right)\left(C^2 R r_o s^2 + CRs + 2Cr_o s + \frac{g_{m0} r_o}{-\frac{s}{\omega_{bw}} + 1} + 1.0\right)}$$

The new ω_0 has slightly shifted and the DC gain is now slightly offset from 0 as $\frac{g_{m0} r_o}{1 + g_{m0} r_o}$. The Q factor has increased due to the bandwidth restriction of g_m, but comes at the cost of the poles being shifted towards the RHP. Also the finite output resistance greatly influences the passband loss which means either the filter's passband corner should be bumped up or more bias current is needed to boost the g_m.

We take the table of (R, C, g_m) produced by the design equations in the earlier section and resolve for their optimal values given the OTA non-idealities.

To get an idea of the space of transistor non-idealities we will encounter, we extracted transistor parameters from HW#1. Since most of the design parameters are dependent on the input differential pair, we want to bound all the relevant transistor specs for a variety of transistor bias points. By simulating a L=135nm and W=150nm NMOS over a range of bias current, we grab about 20 bias points (for $V*$ ranging from 0.1 to 0.5V) and generate a LUT containing parameters such as $g_m, r_o, w_b w, I_d, and V*$, all of which will be used for adjusting the optimizer and calculating noise and power.

With a table of realizable r_o and ω_{bw} values, we run a local optimizer which attempts to fit the non-ideal $H(s)$ to the ideal-case $H(s)$.

$$\min_{R,C,g_{m0}} \|H_{ideal}(s) - H_{nonideal}(s, r_o, \omega_{bw})\|_2^2 \Big|_{s=\omega_{pass}-\epsilon}^{s=\omega_{stop}+\epsilon}$$

The initial guess of R and C is provided by the table from section 1.2 and the local optimizer figures out how these variables should be adjusted.

As an example, for these specific non-ideality values and initial guesses for R, C:

$$A_{v0} = 20 \text{ V/V}$$
$$\omega_{bw} = 25.3 \text{ Ghz}$$
$$g_{m0} = 0.744 \text{ mS}$$
$$R = 6 \text{ k}\Omega$$
$$C = 1.32 \text{ pF}$$

We get these modifications of R, C, g_{m0} after optimization:

$$R' = 3.23 \text{ k}\Omega$$
$$C' = 2.82 \text{ pF}$$

1.5 Resistor Sizing and Noise Analysis

For a single OTA filter stage, we can calculate the output noise of R_1 and the OTA itself (thermal and flicker noise of a g_m cell). In the circuit, we model the resistor and OTA's noise as noise currents, for which we calculate a symbolic transfer function for the input-referred noise voltage. In this analysis, we can neglect the OTA's finite bandwidth, as it is too high to shape noise in the passband. We also make the assumption that cascode devices in the OTA do not contribute any noise, and current source/CMFB circuits do not contribute any differential noise.

$$H_{ni,R}(s) = \frac{R\left(sC_2 r_o + 1\right)}{g_m r_o}$$
$$H_{ni,OTA}(s) = \frac{1}{g_m}$$

Intuitively, this makes sense, because R's current noise at DC (where the caps are AC ground) circulates solely in R, and as the frequency increases past the zero created by C_2 and r_o, noise current flows into the OTA as well and gets amplified. The OTA's noise current is simply input-referred by its own transconductance as expected, and is therefore constant with bias. As the g_m of the OTA is decreased, C_2 increases, so we should expect the filter to be noisier at lower OTA bias.

If we use the following noise currents, setting $\gamma = 2$ for a relatively short channel device, and using the optimized R for a given g_m, we integrate over the passband for one stage:

$$v_{ni,T} = \int_{1Hz}^{20MHz} \left[\frac{4kT}{R}|H_{ni,R}(s)|^2 + (4kT\gamma g_m + \frac{K_f I_D}{L^2 C_{ox} f})|H_{ni,OTA}(s)|^2\right] df$$

Now if 2 stages are cascaded, we can similarly calculate the total output noise assuming isolation between the two stages. The first stage's R and OTA will have the same input-referred noise, while the second stage's input-referred noise will be attenuated by Av_0 of the first stage. Since the component values should not change much, and the DC gain is unity, the noise power should be about double that of a single stage.

Taking some values for R and g_m from the previous section, we can calculate the absolute output noise power. With the dynamic range requirement 4, we have a hard limit on this quantity:

$$P_{sig,max} = \frac{V_{sig,max}^2}{2} = \frac{0.2^2}{2} = 0.02W$$
$$P_{ni,max} = \frac{P_{sig,max}}{10^{50/10}} = 200nW$$

We run all the component values in our LUT through this noise calculation to find out which OTA bias points can satisfy the noise spec. We use the following constants in the noise calculations:

$$\gamma = 2$$
$$K_f = 6 \times 10^{-29} \text{ A*F}$$
$$L = 135 \text{ nm}$$
$$C_{ox} = 97 \text{ aF}$$

Figure 5 confirms that at low bias currents, noise is dominated by the filter resistor, and asymptotically approaches the OTA noise at high bias currents. With one stage, we have at least a 20dB margin on the dynamic range. This suggests to us that the choice of bias point is essentially input swing-limited: the V^* must be at least 100mV.

Later on, if we discover that the OTA's noise and nonidealities are much worse than we calculate in this analysis and/or we require additional stages, we can introduce an optimizer once again to adjust all component values at higher OTA bias currents to meet the dynamic range spec.

1.6 Power Estimation

We estimate the static power of the filter circuit as:

$$P = I_{ds} \cdot N_{stages} \cdot N_{branches} \cdot V_{dd} \cdot 2$$

where N_{stages} is 2 representing the number of OTAs, $N_{branches}$ is 2 estimating the number of bias current branches within each OTA, V_{dd} is from the spec, and the factor of 2 accounts for the differential OTA. I_{ds} is derived using 1-transistor simulations and it is collected along with all the OTA non-idealities we considered earlier.

We find the following plot:

All the noise numbers meet our required spec, so we are primarily concerned with getting the required output swing and minimizing distortion. To that end, we can increase V^* and by consequence I_{ds} incrementally until those specs are met without worrying too much about noise.

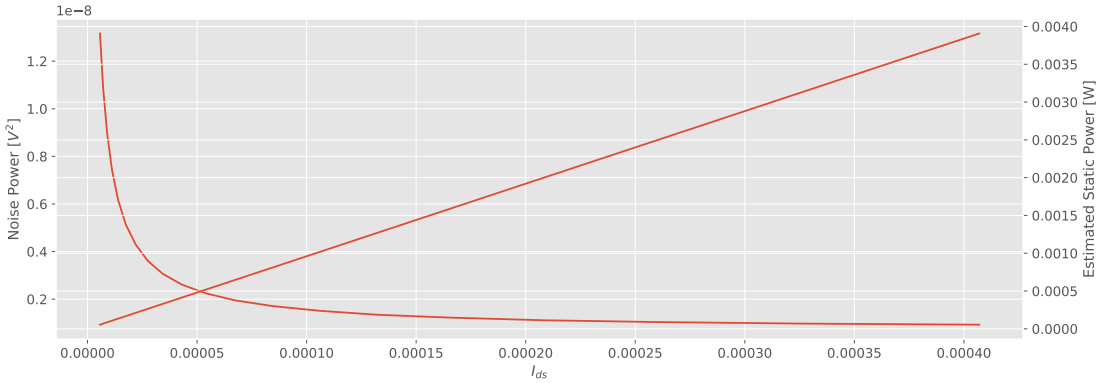

Figure 5: Considering various I_{ds} values for a fixed dimension transistor, we find the total input referred noise and estimated power consumption

1.7 Chosen Design Parameters

Here is one design point which meets our specs:

$$
\begin{aligned}
V^* &= 0.115 \text{ V} \\
I_{ds} &= 112\mu\text{A} \\
g_m &= 0.195 \text{ mS} \\
r_o &= 12.7\text{k}\Omega \\
w_{bw} &= 43.3 \text{ GHz} \\
R &= 12 \text{ k}\Omega \\
C &= 746.25 \text{ fF}
\end{aligned}
$$

This is the output of our optimization program:

```
Total input referred noise power: 7.424237673893265e-09 V^2
Min reqd voltage swing for DR: 0.0385337194516524 V
Passes dynamic range!
Power: 0.00010751999999999999 W
```

2 Checkpoint 2: OTA Design

2.1 Schematic Design

2.1.1 Pseudo-Differential Filter

The 3-passive single-ended OTA filter from section 1.2 was modified to form a psuedo-differential filter section as shown in Fig. 6. This filter uses 2 single-ended OTAs, and with ideal OTAs, implements the same transfer function as the single-ended filter designed in checkpoint 1.

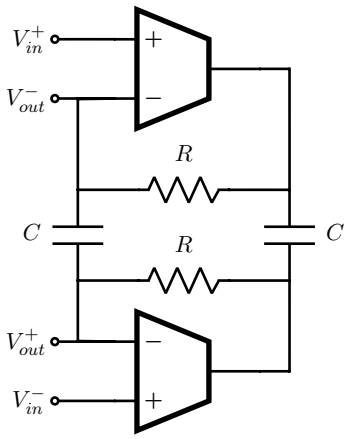

Figure 6: A single stage of the psuedo-differential OTA filter.

We cascade 2 to 3 of these stages to achieve the required attenuation and group delay specs. This psuedo-differential filter doesn't provide any common mode rejection, but that is solved by using a fully differential OTA in unity gain before the filter stages with the necessary CMRR.

2.1.2 OTA

The single-ended OTA uses a simple telescopic cascoded topology with a cascoded mirror load. Only 1 stage is required to get enough g_m and bandwidth to meet the filter specs. Fig. 7 is the OTA schematic which is sized with these constants:

$$\begin{aligned} I_{bias} &= 50\mu\text{A} \\ L &= 180 \text{ nm} \\ W &= 500 \text{ nm} \\ V_{b,cas,n} &= 1.1 \text{ V} \\ V_{b,cas,p} &= 450 \text{ mV} \end{aligned}$$

With this biasing for all LVT transistors, we achieve ≈ 140mV of V^* in the input pair transistors. Because this is a single stage OTA, the dominant pole is from the mirror, and thus the mirror's sizing relative to the secondary pole at the unloaded output node determines the phase margin. The cascode devices use min. L to reduce parasitic capacitance with a V^* of ≈ 130mV. The input pair was most important for meeting the dynamic range spec because noise is dominated by their flicker noise; we chose the minimum area possible while achieving a differential G_m of about 80μ S. Finally, our R_{out} is approx. 1GΩ, which is high enough to not affect the filter response.

2.1.3 CM Reject Stage

The CMMR reject stage is structurally similar to the OTA to have common output common mode and is shown in Fig. 8. The only differences between the two circuits are:

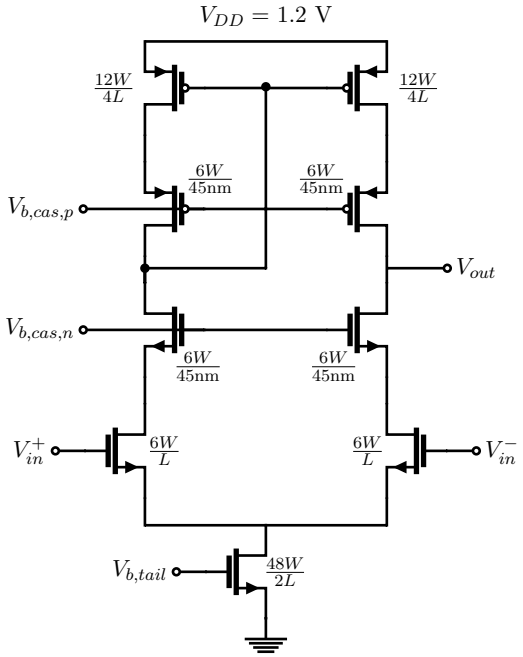

Figure 7: Schematic and sizing of single-ended OTA

- Both loads are diodes, such that $g_{m,p} \approx g_{m,n}$ for unity gain (this was tested across different P/N corners with only 1dB impact on the DC gain). The sizing must be matched with the PMOSs of the OTAs for the common mode to remain equal, as will be explained below.
- The NMOS cascode is moved down above the tail current source to increase the tail's R_{out}, which is the primary contributor to CMRR. The bias voltage is 700mV instead.
- An ideal CMFB circuit senses the desired common mode from a replica OTA, and adjusts the tail current bias as referenced against the gate voltage of a diode sinking the same current as the OTAs.

This stage has the following biases as a result of the different cascode structure:

$$V_{b,cas,n} = 700 \text{ mV}$$
$$V_{b,cas,p} = 450 \text{ mV}$$
$$V_{in,cm} = 900 \text{ mV}$$

2.1.4 Replica Biasing

The DC bias point of each OTA's output and negative terminal is set by the resistive feedback of the filter. However, the DC bias point of the OTA's input needs to be matched with the output common mode bias point of the CMRR stage. To make all common mode voltages equal, we recognize that we can just place a replica OTA with its output and both inputs shorted, thereby creating a structure that has two current mirrors back-to-back as shown in Fig. 9. The resulting

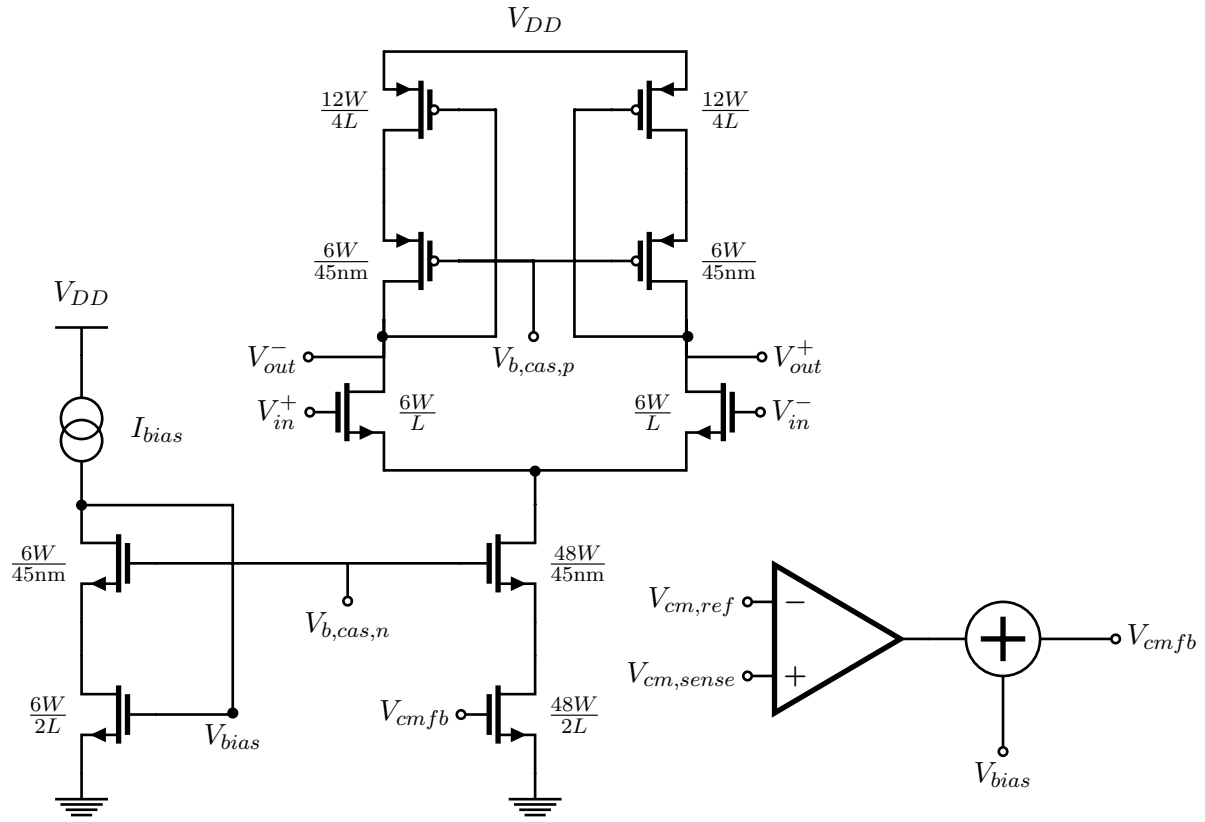

Figure 8: Schematic and sizing of the CMRR stage. $V_{cm,sense}$ is sensed from the common mode voltage across V_{out}^- and V_{out}^+.

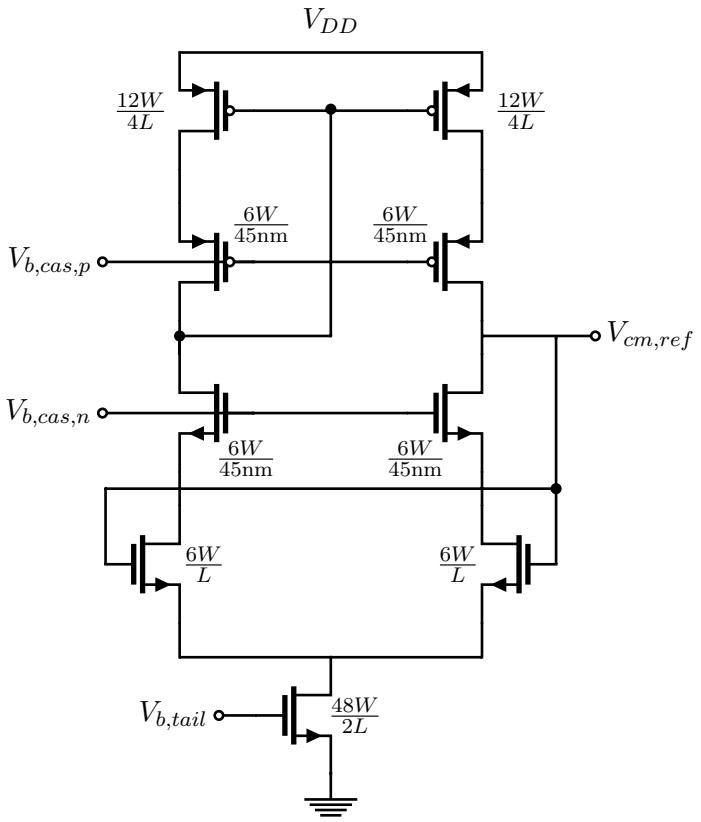

Figure 9: Schematic and sizing of the replica circuit

self-biased voltage feeds the common reference of the CMFB circuit in the CMRR stage. Startup could be an issue, but transient sims show that leakage current prevents the circuit from staying locked in a 0 current state as the supply is quickly or slowly ramped. If certain startup time is required, a small startup circuit could be attached. The sizing of this stage can be made much smaller than the OTAs if common mode noise is not a concern.

2.2 Testbench

Testbenches were made at each stage of the design process, measuring specs such as open loop gain and bandwidth, unity gain step response, and CMRR. Here we describe the system-level testbench as shown conceptually in Fig. 10 and in detail in 11, which contains:

- 2 filter stages, a CMRR stage, and a replica bias circuit for the real filter
- A filter with ideal OTAs
- Ideal current source to mirror to all OTA tail current sources
- Ideal voltage sources for the cascode biases and input common mode
- Ideal balun to convert differential and common-mode components of the stimulus for AC & transient sims

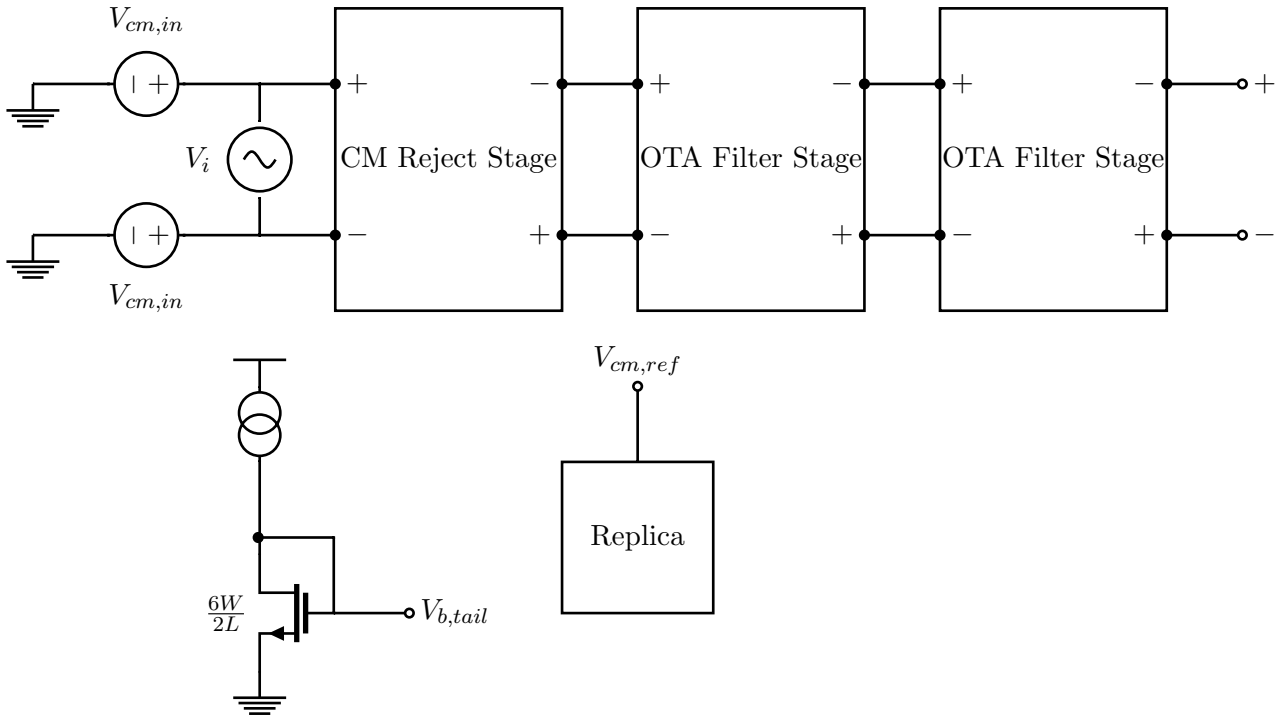

Figure 10: The system-level testbench with bias

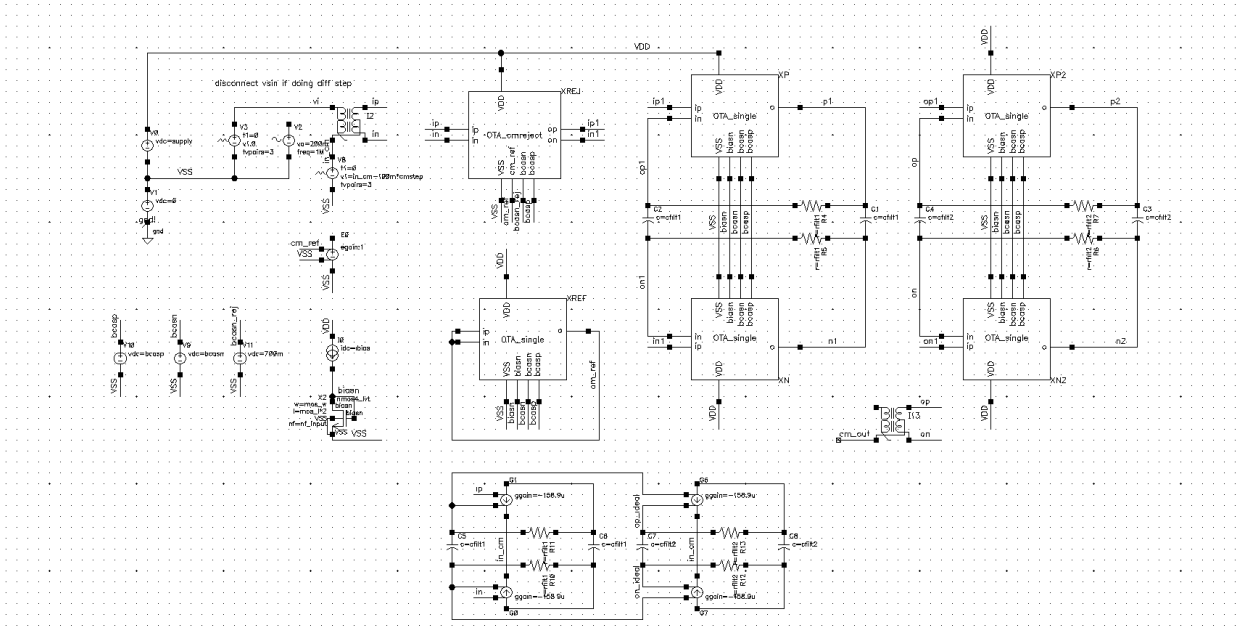

Figure 11: The detailed system-level testbench schematic

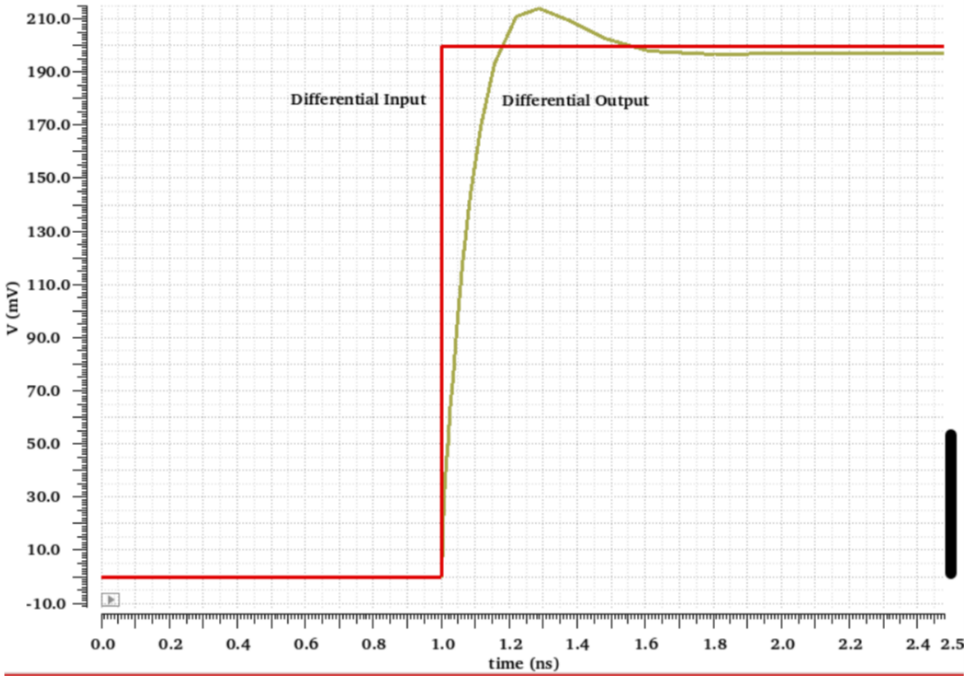

Figure 12: OTA stability with 200mV differential step

2.3 OTA Stability

The transient simulations on the pseudo-differential OTA in unity gain feedback in response to differential and common-mode steps with rise time of 1ps are shown in Figs. 12 and 13, respectively. Both are demonstrated to be stable, and we must note that the common-mode step is not rejected because the CM rejection is performed by a separate CM reject stage, in front of the filter stages, whose CM step response will be shown later.

Fig. 14 shows that the pseudo-differential OTA in open-loop has a phase margin of about **62 degrees**.

2.4 Noise

Fig. 15 shows the input and output noise density. It is clear that the noise is dominated by flicker noise, and analysis of the noise contributors shows that it comes mostly from the input pair. We sized the W and L of the OTA such that we would meet the dynamic range requirement with the CM reject stage and 3 filter stages.

2.5 Comparison with Ideal

To compare our filter to a filter with an ideal OTA, we note that the CMRR would be infinite and it will be perfectly linear. Thus, we will just show comparisons in the frequency response, differential step settling, and noise.

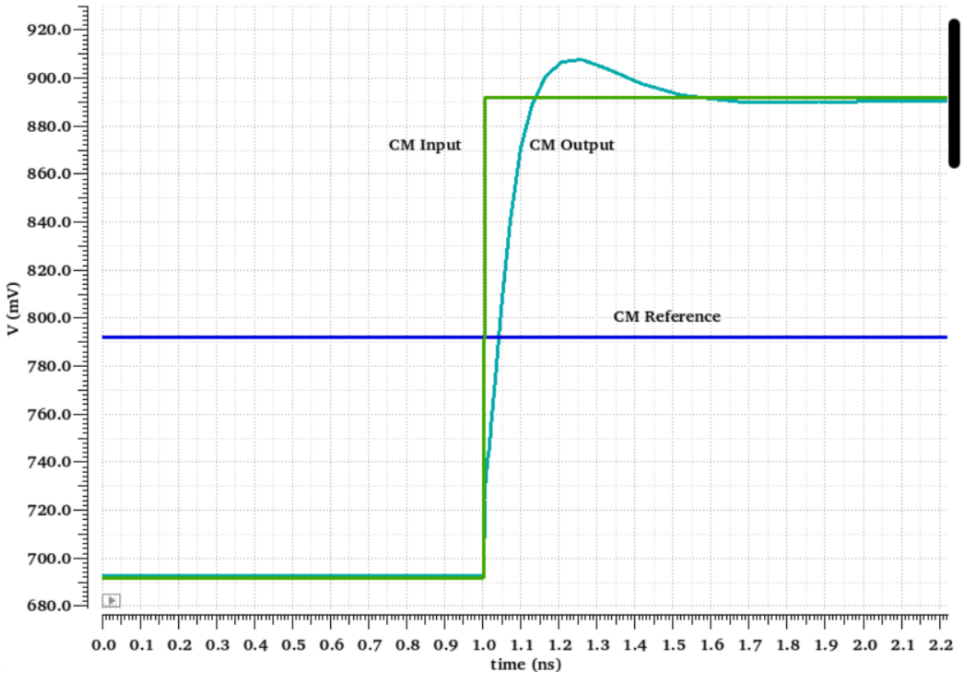

Figure 13: OTA stability with 200mV common-mode step

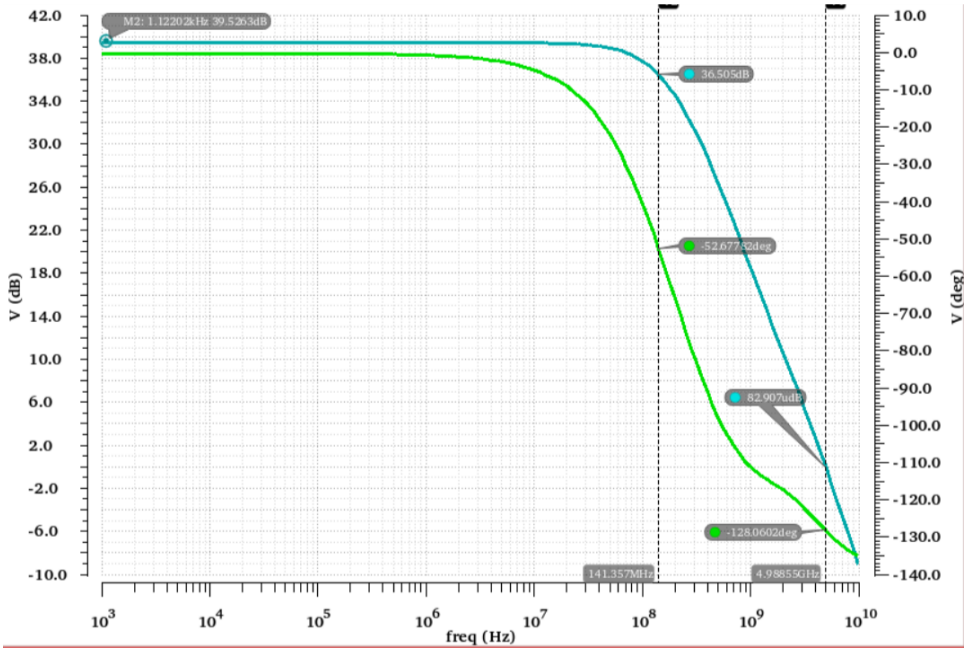

Figure 14: OTA phase margin

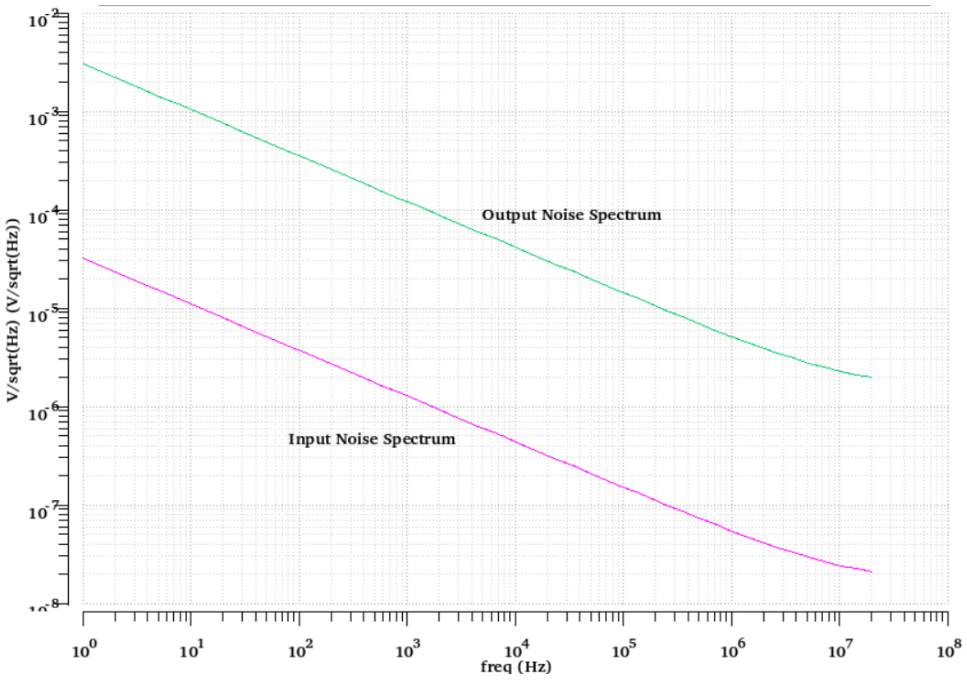

Figure 15: OTA input and output noise spectrum from 1Hz to 20MHz

2.5.1 Filter Passives

To meet the required pole frequency and quality factor, the following filter passives values were chosen:

$$R_{filt,1} = 8.05\ \text{k}\Omega$$
$$C_{filt,1} = 390\ \text{fF}$$
$$R_{filt,2} = 3.4\ \text{k}\Omega$$
$$C_{filt,2} = 670\ \text{fF}$$

2.5.2 Frequency Response

Fig. 16 shows the simulated filter frequency response of our real filter and the filter with the OTA replaced by an ideal VCCS. The transconductance of the ideal OTA is set from the extraction of G_m of our real OTA in open loop simulations. The real filter was tuned to meet both the passband and stopband attenuation specifications with 2 stages at the moment. Due to additional zeros and other parasitic effects, the resulting transfer function looks much closer to a type-II Chebyshev filter than the ideal Bessel. Pole Q's and the corner frequency had to be tuned for the real filter to try to meet the group delay spec (which we still *do not yet* meet - a 3rd filter stage will help), hence why the filter with the ideal OTA does not appear to have a correct corner frequency.

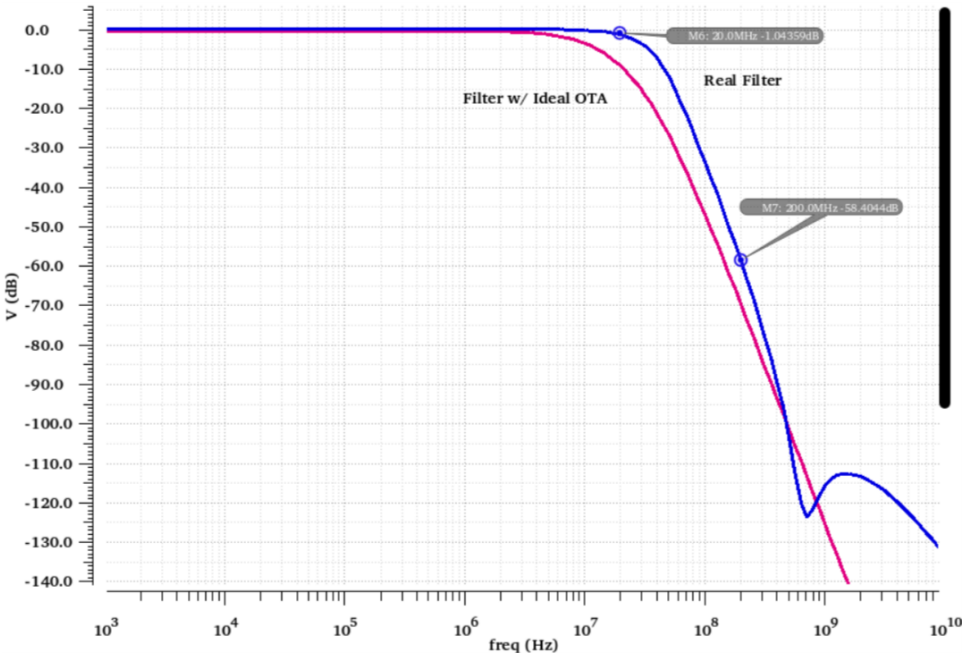

Figure 16: Filter frequency response

2.5.3 Step Response

Figs. 17 and 18 show the response to 200mV differential and common-mode steps with rise time of 1ps. The differential step response is very similar to that of the OTA stages in unity gain feedback, as expected, whereas the filter with ideal OTA has no overshoot because it has infinite bandwidth. Discrepancy in the final output differential voltage is caused by the slight DC gain in our CM rejection amplifier. The first common-mode rejection stage is also stable (albeit with an ideal CMFB circuit). Slight ripple in the common mode is caused by feedthrough in the CMRR stage's input pair due to the 1ps rise time and infinite bandwidth of the ideal CMFB circuit. A real CMFB circuit would show a more realistic CM step response. As long as the CMFB circuit has at least double the bandwidth of the filter itself, we should meet the settling spec. An additional plot of the CMRR over frequency is shown in Fig. 19, and we are currently achieving almost **68dB** of rejection and it remains above 60dB over the entire passband.

2.5.4 Noise

The input referred noise power integrated from 1 to 20MHz is:

- Real filter: **90** nV^2 or **300** μV differential
- Filter w/ ideal OTA: **2.6** nV^2 or **51.4** μV differential

The noise of the real filter is **56.6dB** lower than the 200mV differential input that we are expected to receive. Both filter's output noise spectrums are shown in Fig. 20, and once again, we are dominated by flicker noise from the input pairs of all amplifiers in the passband.

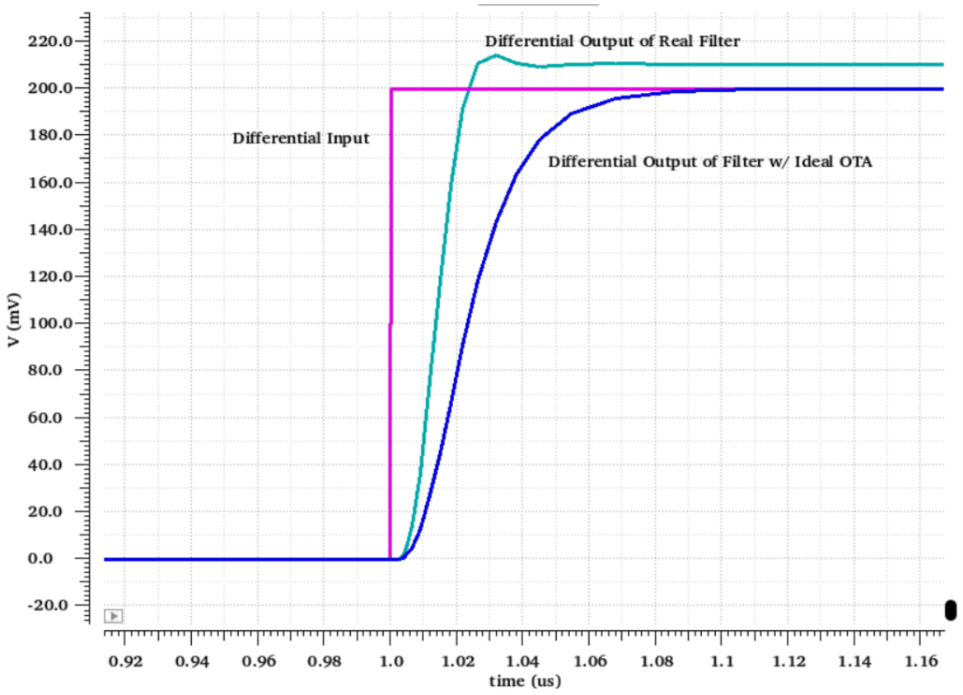

Figure 17: Filter response to 200mV differential step

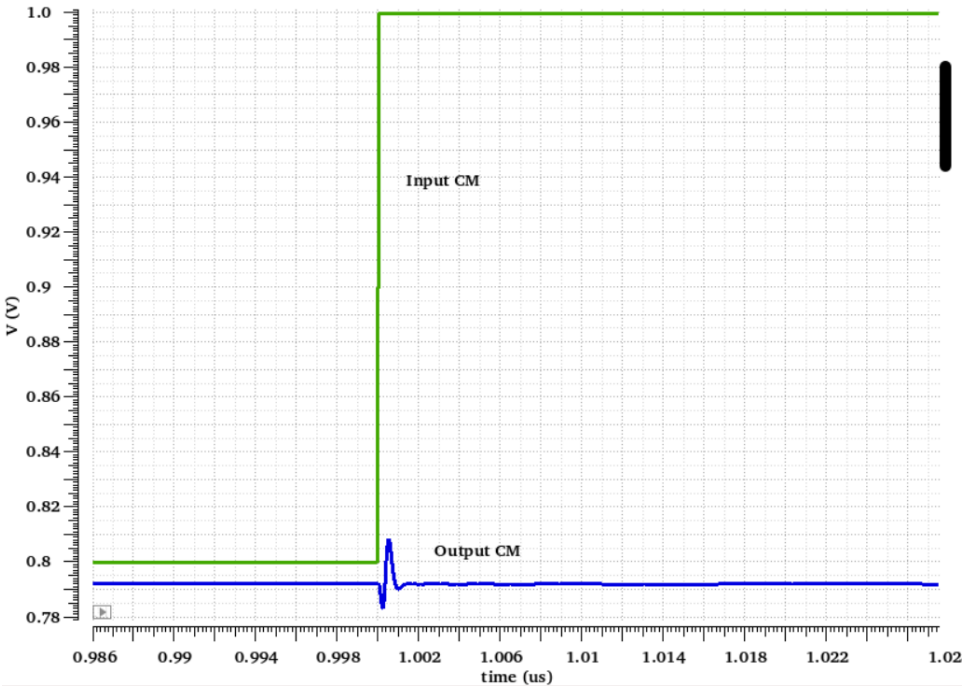

Figure 18: Filter response to 200mV common-mode step

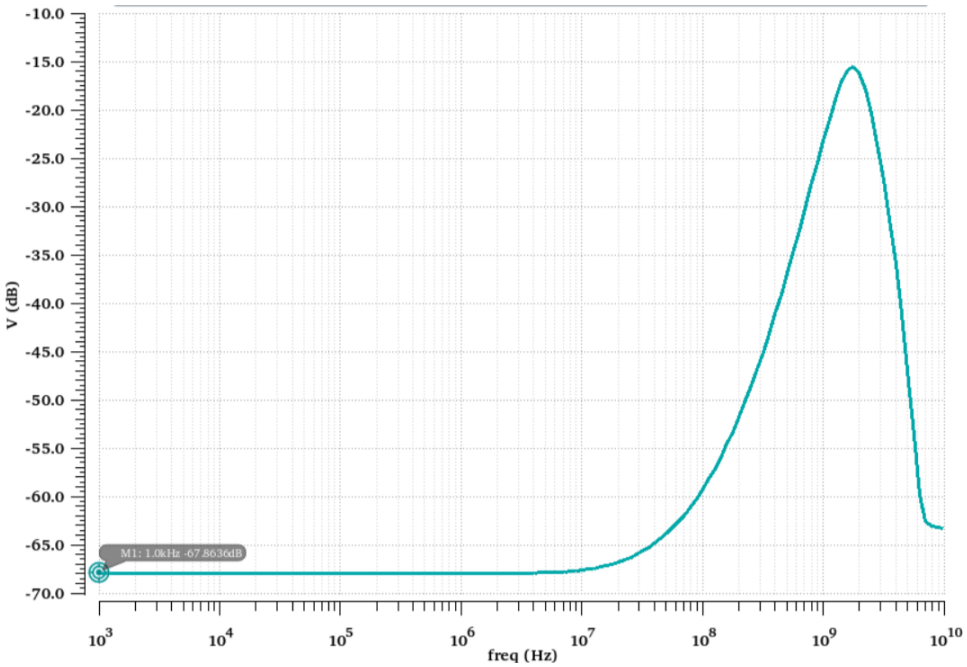

Figure 19: Filter CMRR vs. frequency

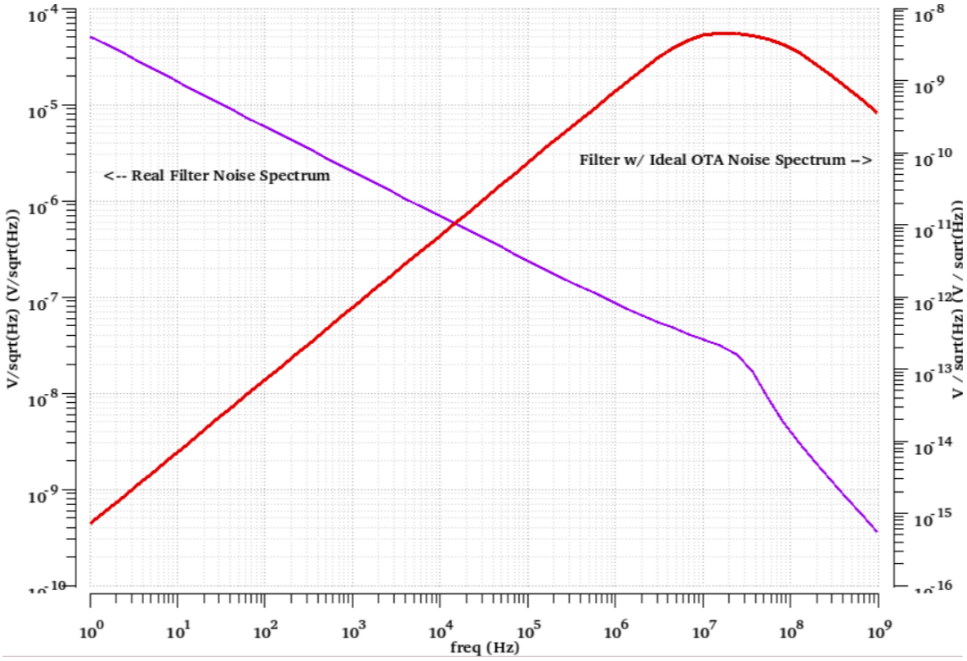

Figure 20: Filter output noise spectrum

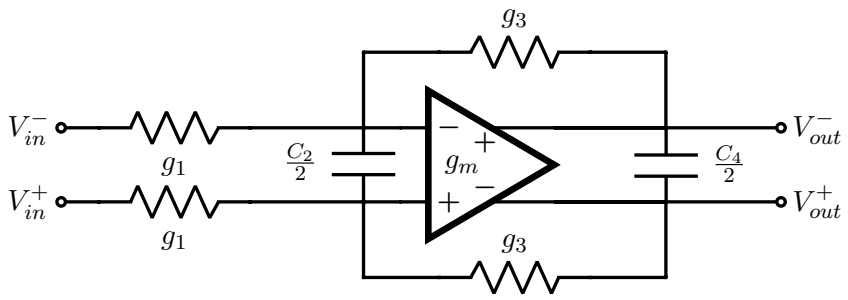

Figure 21: Schematic of the OTA filter stage with 4 passives

2.5.5 Linearity

The linearity for a 200mVpp input at 1MHz is calculated by performing a harmonic balance simulation with 9 harmonics and probing the expression, `drplPssHarmThd((vh('hb "/op") - vh('hb "/on")) 1)`. The balanced structure removed the even-order harmonics as expected, and our bias points leave plenty of headroom on each transistor to accommodate additional input or output swing. The resulting THD = **0.1835%**.

3 Checkpoint 3

3.1 Schematic Design

The original single-ended OTA design in 2.1.1 (figure 7) was improperly configured. We neglected to tie the tail nodes between the single-ended stages together, resulting in an effective degeneration of the input pair due to the tail current source. Once this was fixed, we found that it suffered from 2 poles at the same frequency, because each single-ended OTA's mirror pole was at the same frequency. Furthermore, the filter was incompatible with a ±30% variation in power supply due to the 5-high transistor stack. In the quest to address these issues without burning significantly more power, we elected to change to a fully-differential filter topology.

3.1.1 Fully-Differential Filter

The new filter stage topology now uses 4 passives: 2 resistors and 2 capacitors. The extra series resistor decouples the common modes between each stage and moves the differential output to the output of the OTA instead of its negative terminal. As a result, we can make a fully-differential OTA instead.

Each stage of this filter is shown in Fig. 21. The capacitors are chosen to be equal (with the output capacitance absorbing parasitic capacitances). The design equations for this topology are as follows, assuming an ideal OTA with infinite R_o:

$$H_{ideal}(s) = \frac{g_1(g_3 - g_m)}{s^2 C_2 C_4 + s[g_3 C_2 + (g_1 + g_3)C_4] + (g_1 + g_m)g_3}$$

The DC gain K of the filter is tunable using the resistors, which helps counteract finite R_o in the OTA. However, this still requires the OTA's $R_o \gg R_1, R_3$. Once a suitable ratio between R_1 and R_3 is found, matching the pole frequency and its Q factor are accomplished by selecting the capacitance and base resistance to satisfy the following design equations:

$$K = \frac{g_1 g_3 - g_1 g_m}{g_1 g_3 + g_1 g_m}$$
$$\omega_0 = \sqrt{\frac{(g_1 + g_m) g_3}{C_2 C_4}}$$
$$Q = \frac{\sqrt{(g_1 + g_m) g_3 C_2 C_4}}{g_3 C_2 + (g_1 + g_3) C_4}$$

In designing the OTA stages, we found that we are able to meet all of the specifications with a 5th-order Bessel filter. This minimizes power by requiring only two active filter stages shown here followed by a single real RC pole. Furthermore, keeping the pole Q's low keeps the filter's resistors small, reducing their thermal noise contribution.

The values for the filter passives were calculated using our equation solver with K slightly larger than 1 to offset the OTA's finite R_o, a target bandwidth of 25MHz, and target group delay of less than 2.5ns and produced the following results. No tuning was required to get the filter to meet specs:

$$R1_{filt,1} = 17.4 \text{ k}\Omega$$
$$R3_{filt,1} = 33.8 \text{ k}\Omega$$
$$C_{filt,1} = 322 \text{ fF}$$
$$R1_{filt,2} = 5 \text{ k}\Omega$$
$$R3_{filt,2} = 15.2 \text{ fF}$$
$$C_{filt,2} = 632 \text{ fF}$$
$$R_{filt,3} = 10 \text{ k}\Omega$$
$$C_{filt,3} = 352 \text{ fF}$$

3.1.2 Fully-Differential Folded Cascode OTA

The new OTA is shown in Fig. 22, and the base transistor sizing is as follows:

$$L = 360 \text{ nm}$$
$$W = 500 \text{ nm}$$

The PMOS load resistor is selected to be a standard-Vt device in contrast to the other low-Vt devices and sized to satisfy the requirement that the input common mode will be equal to the output common mode for all but the first filter stage; i.e., $V_{GS} \approx 2V_{DS}$. The input pair is sized for sufficient V^* to satisfy linearity specs for a g_m that limits the filter resistors to less than a few 10's of kΩ, the NMOS current source is sized to minimize and balance thermal and flicker noise, and the cascode transistors are unchanged as before.

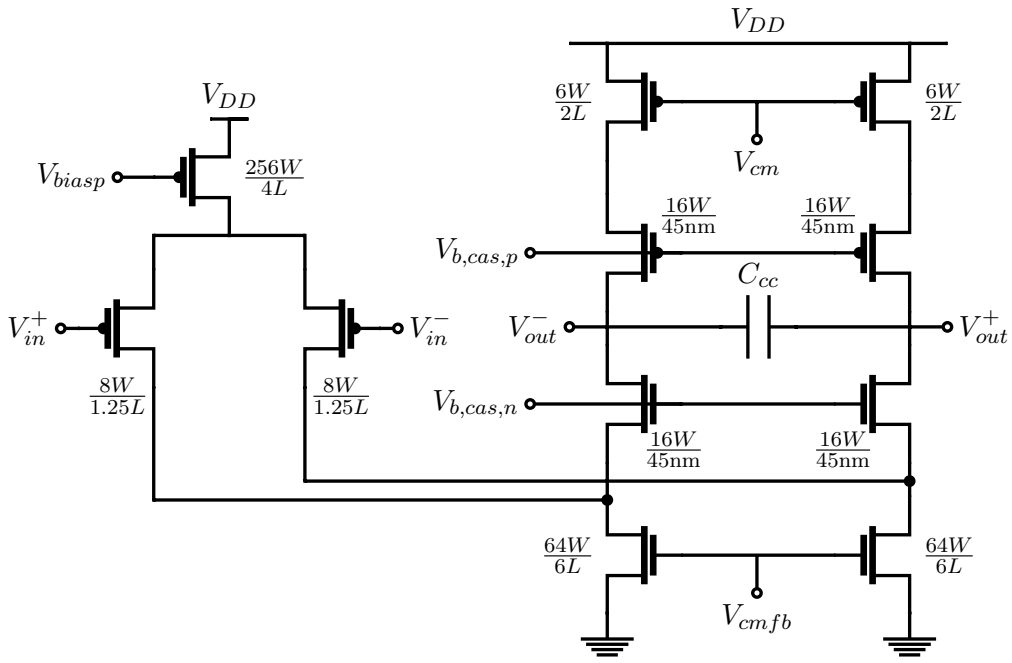

Figure 22: Schematic of the FD-OTA

In switching to the full-differential folded cascode OTA, the power penalty of having the extra input branch offset the power reduction when going from pseudo- to fully-differential. Furthermore, the fully-differential OTA's need for CMFB builds in CM rejection already, negating the need for a separate CM reject stage in the filter. All in all, the total power consumption is essentially the same as the filter in checkpoint 2.

Lastly, the gain and phase margin specification for the open-loop OTA is easily met in this single-stage OTA by providing a small compensation capacitor in between the differential output to lower the dominant pole. When placed into the filter stage, this compensation capacitor is fully absorbed.

3.1.3 Constant-gm Reference and Biasing Circuits

Due to the g_m appearing in the design equations, it is imperative that this filter employ a constant-gm reference as shown (minus a startup circuit) in Fig. 24 to maintain filter performance over temperature. Because the input pair is a PMOS transistor, a reference current of approx. 6.5μA at nominal supply and temperature with respect to the PMOS current source requires an off-chip precision 11kΩ resistor, a very standard component. This reference circuit provides *biasp* and *biasn* for the OTA. The rest of the biasing circuit is shown in Fig. 23 to generate the remaining voltages for the cascode transistors and common-mode reference. It is a simple replica of the OTA's half-circuit and is self-biased such that:

- V_{GS} of the cascode transistors are forced equal
- The common-mode reference voltage is set by the cascode PMOS diode

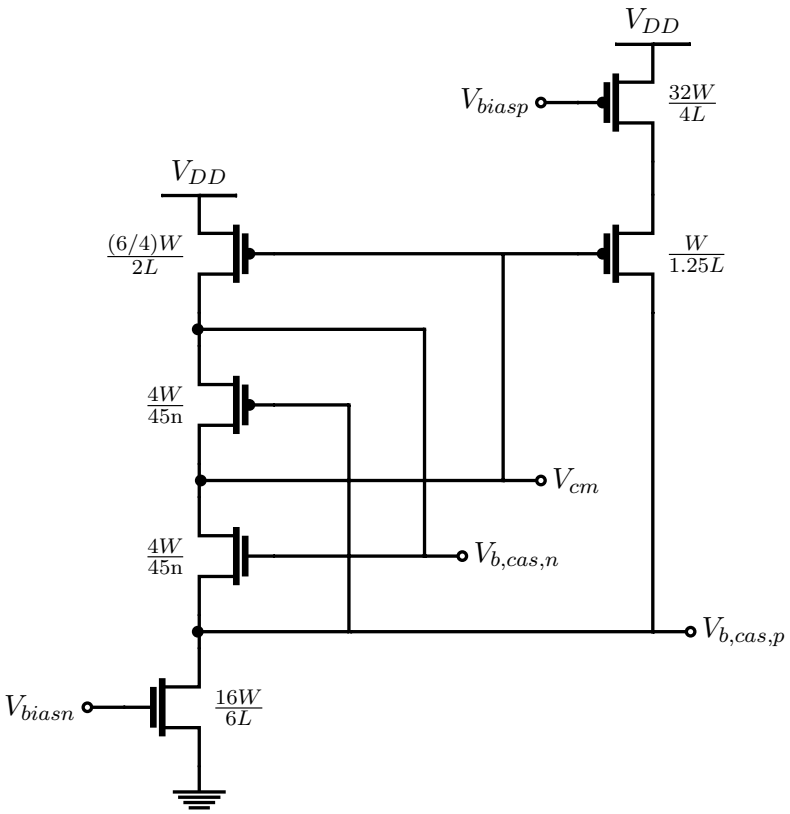

Figure 23: Cascode voltage biasing circuit

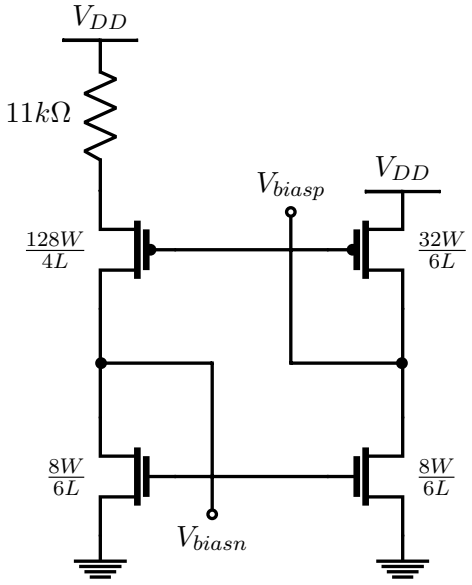

Figure 24: Constant-gm reference schematic

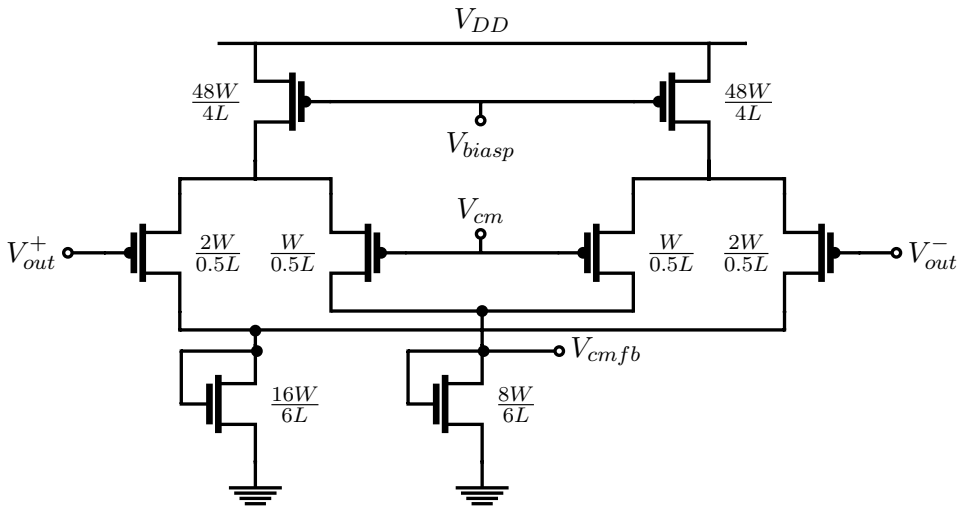

Figure 25: Common-mode feedback circuit schematic with sizing

- The cascode voltages are generated from the common-mode reference using the balance of r_o between the cascode transistors
- The bias voltages *biasp*, V_{CM}, *bcasp*, and *bcasp* all move together and make the OTA's current supply independent

3.1.4 Common-Mode Feedback Circuit

In contrast to an op-amp, common-mode feedback for an OTA must fundamentally not load down the OTA's output. Thus, in lieu of resistive feedback which would greatly degrade the OTA's R_o and factor into the filter response, a double-differential pair sense amplifier is employed instead, sized proportionally to the structure of the OTA's input branch as shown in Fig. 25.

Since the output common mode should be equal to the input common mode, the sense amp mimics the input branch of the OTA, such that output common mode variation generates a differential current in the sense circuit that raises or lowers $vcmfb$ to adjust the OTA's NMOS current source. This in turn pulls or pushes excess current in or out of the OTA to maintain the output common mode. Gain is achieved by adjusting the current ratios in the sense amp and stability is easy to achieve because the dominant pole is at the output of the OTA, where it sees the capacitance of the sense amp and the R_o of the OTA itself. The capacitive loading of the input pair conveniently helps the open-loop differential-mode stability of the OTA and can also be lumped into the filter's capacitance.

3.2 Testbench

Testbenches were made similarly to checkpoint 2, measuring all the filter specifications along the way. Due to the new topology and real biasing circuits, the top-level filter testbench no longer contains the CM reject stage and ideal biasing circuits. Fig. 26 shows the detailed system-level

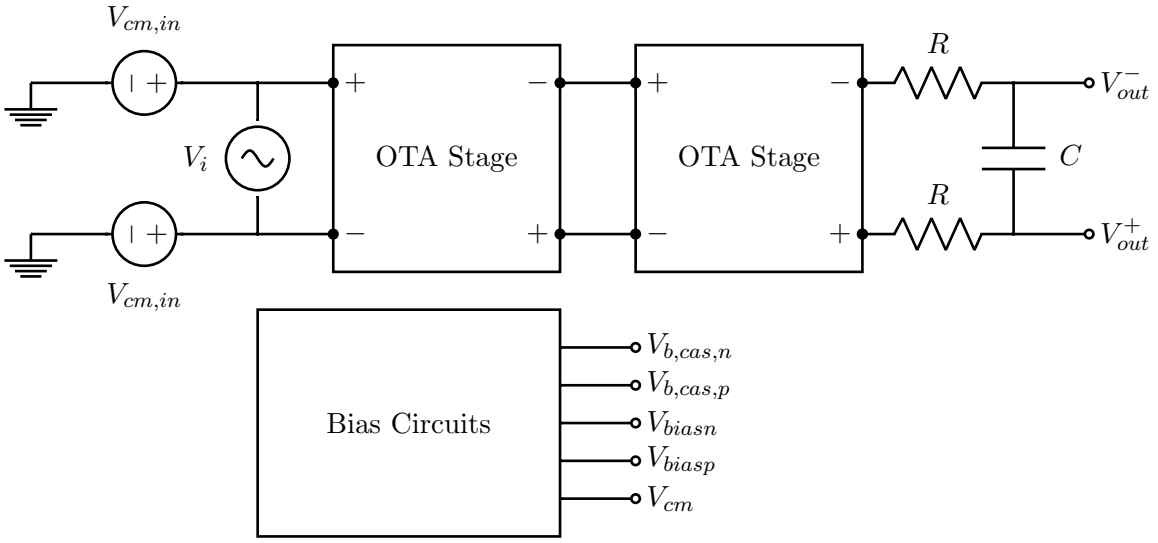

Figure 26: The top-level testbench

testbench schematic. The only ideal components left in the filter are the resistors and capacitors. Voltage sources and baluns generate the stimulus.

3.3 Results

3.3.1 Filter Response

This 5th order Bessel filter has the transfer function shown in Fig. 27. It achieves:

Specification	Result
DC gain	1.9 dB
Stopband attenuation	-56.1 dB
-3dB frequency	29 MHz
Passband group delay variation	0.3ns
Power consumption (@1.2V)	462 μW

3.3.2 Stability

We repeated stability simulations on this new OTA. Figs. 28 and 29 show that the phase margin of the OTA and CMFB circuits are both greater than 60 degrees. Stability analysis was used for the CMFB loop, and additional filtering capacitance on the bias voltages will smooth out the response.

3.3.3 Power Supply Variation

The filter was tested and suffers no catastrophic effects when operating at ±30% supply variation. The only major difference was in the output swing, as shown in Fig. 30.

Supply	DC Gain
0.84 V	-0.65 dB
1.56 V	4.1 dB

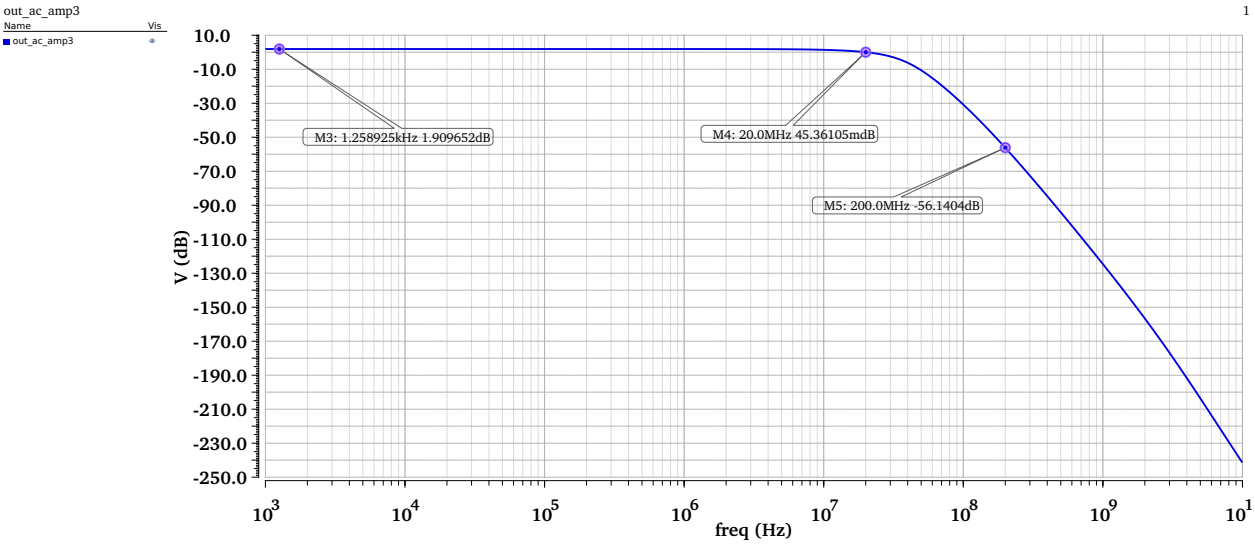

Figure 27: Frequency response of the full filter

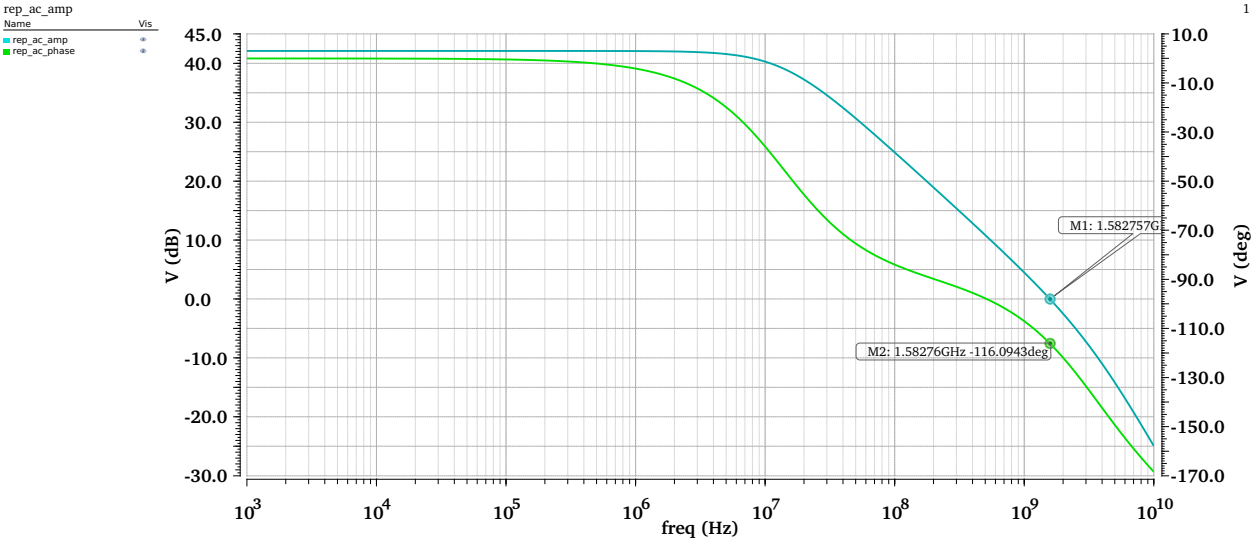

Figure 28: AC response of OTA in open-loop

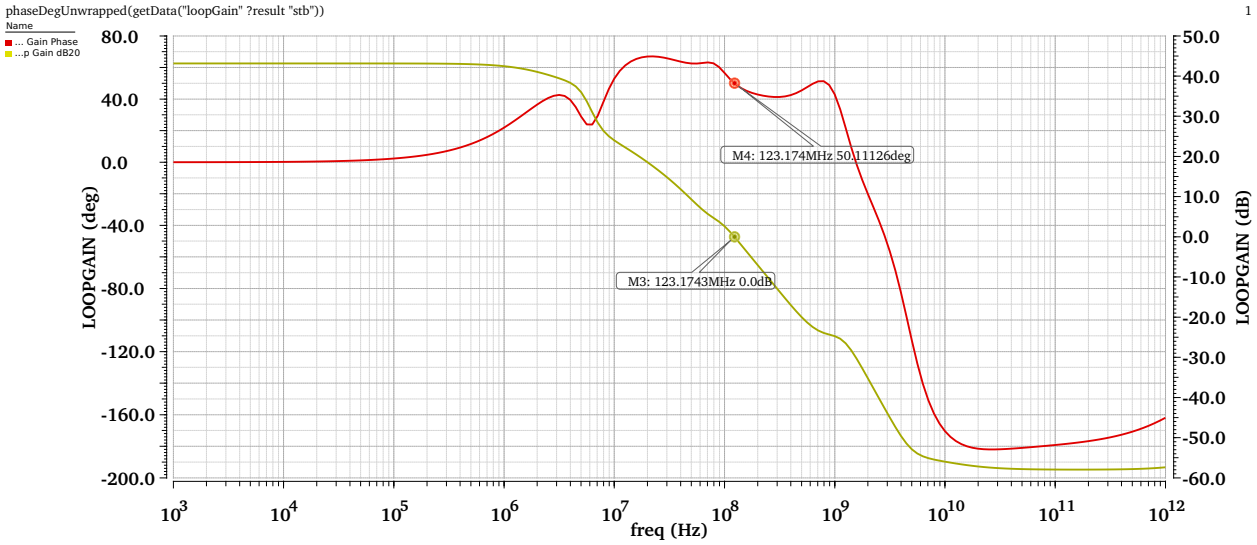

Figure 29: Stability analysis of CMFB loop

The only main specification that did not meet with variation was the stopband attenuation at 1.56 V. However, tuning the filter resistors can easily offset the observed excess DC gain.

We also replot the phase margins for the OTA and its CMFB at 0.84 V supply to verify stability in Figs. 31 and 32. Phase margin is degraded down to about 50 degrees, which is still stable.

3.3.4 Common-Mode Rejection

The CMRR achieved using AC simulation was **61 dB** as shown in Fig. 33, with a larger rejection from the first stage due to the larger filter resistors not loading down the R_o of the OTA needed for the CMFB loop gain. Fig. 34 shows the transient CMRR for a 400mVpp sinusoidal common-mode input at 100kHz. We set the input common mode to be 100mV below the nominal output common mode to accommodate this input CM swing.

3.3.5 Settling

Transient simulations in response to differential and common-mode steps of 200mV with a rise time of 1ps are shown in Figs. 35 and 36, respectively. The common-mode settling time is much shorter than required to meet the settling spec, and can be attributed to the very simple yet effective CMFB circuit we employed.

Step Mode	Settling time (ns)
Differential	35
Common-Mode	6

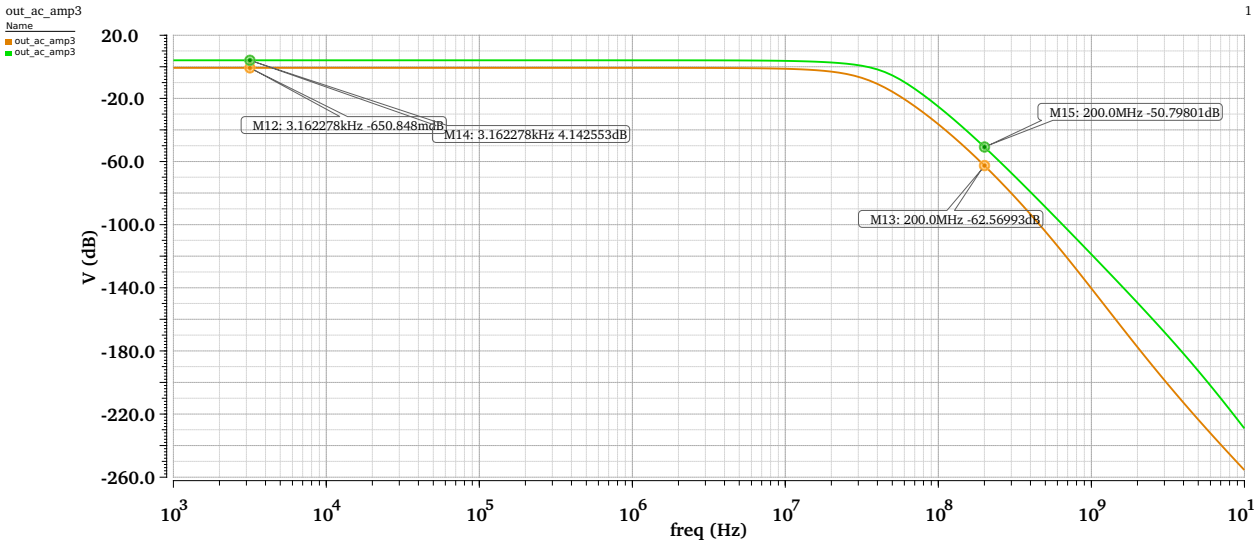

Figure 30: Change in DC gain over supply variation

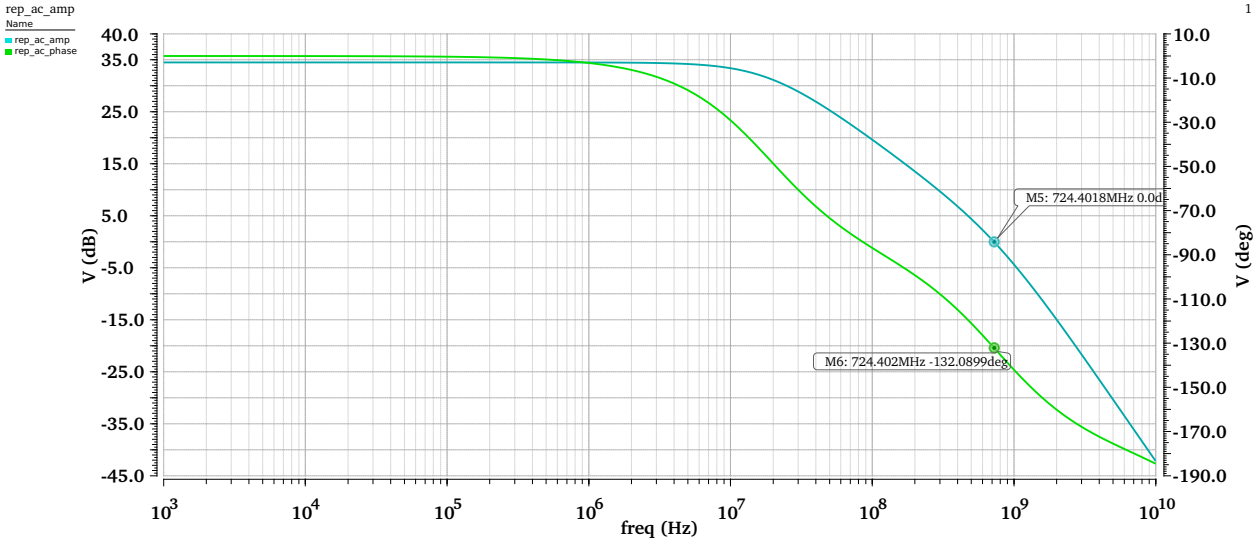

Figure 31: AC response of the OTA in open-loop with $V_{DD} = 0.84$ V

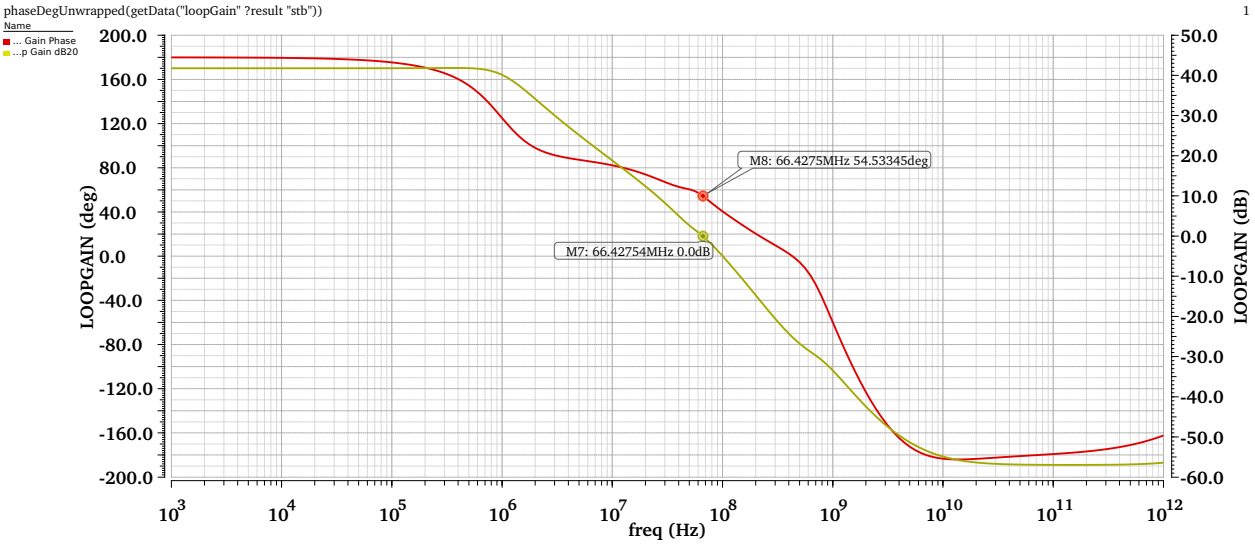

Figure 32: Stability analysis of CMFB circuit with $V_{DD} = 0.84$V

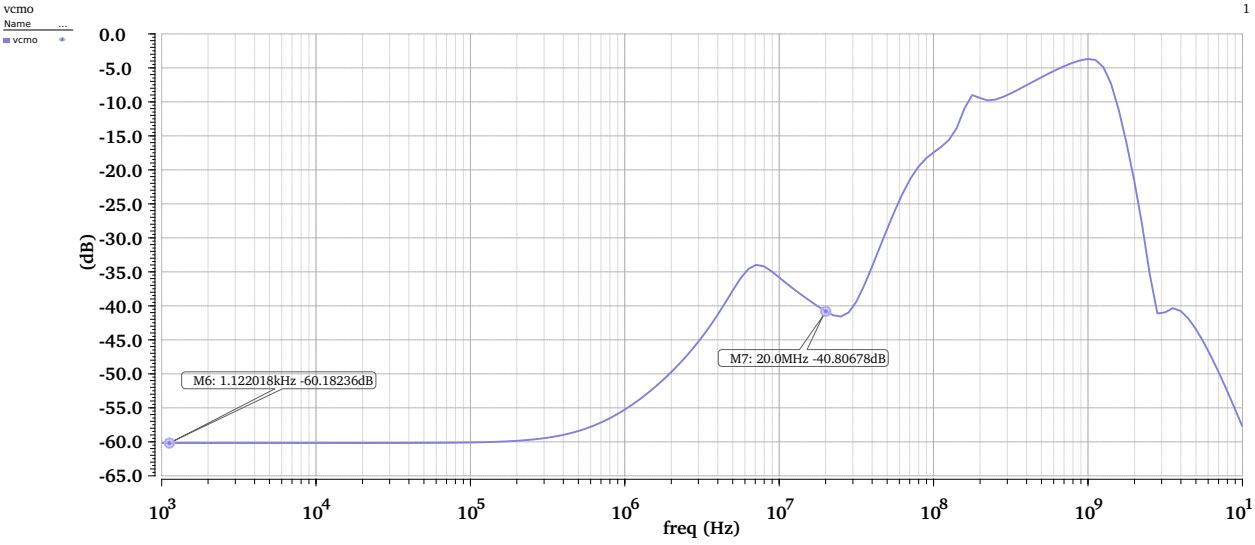

Figure 33: Filter AC CM Rejection

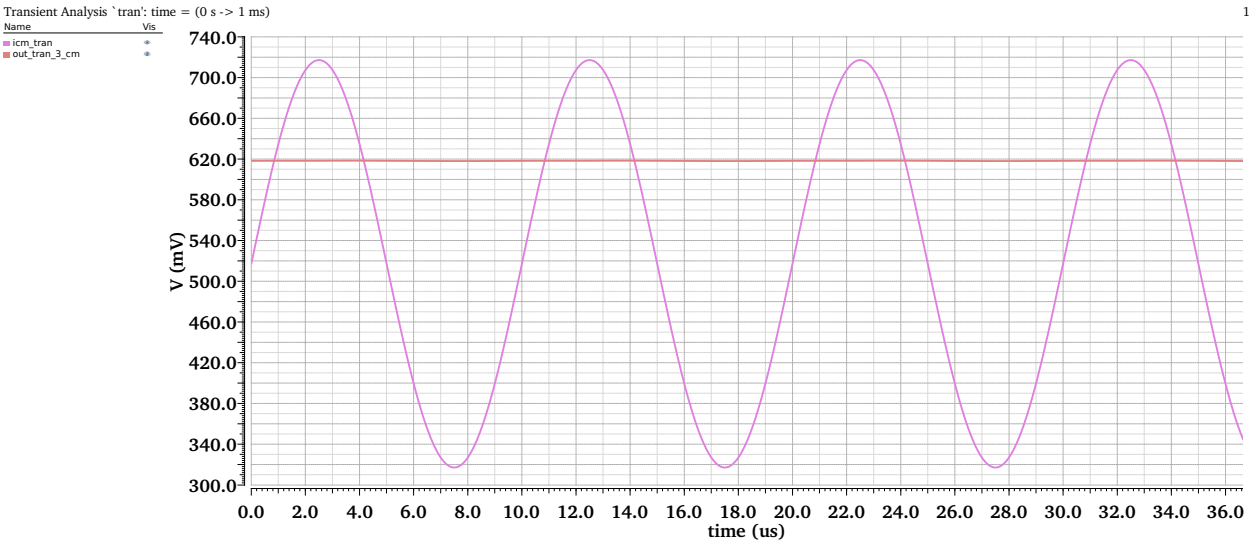

Figure 34: CM Rejection of a 400mVpp CM input

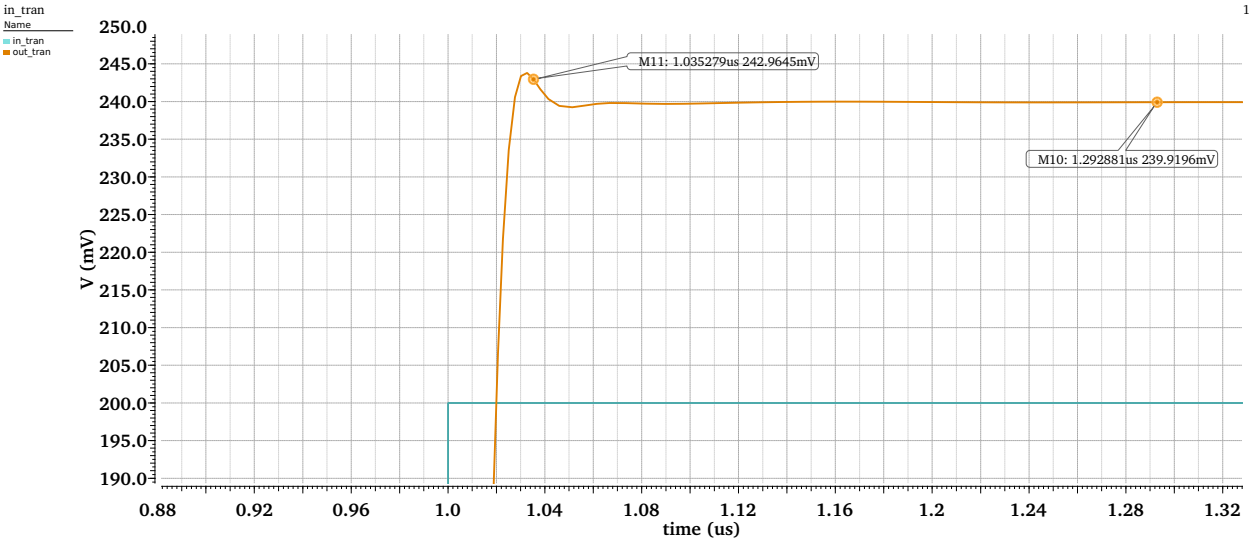

Figure 35: Transient simulation of 200mv differential step (settling to within 1% shown)

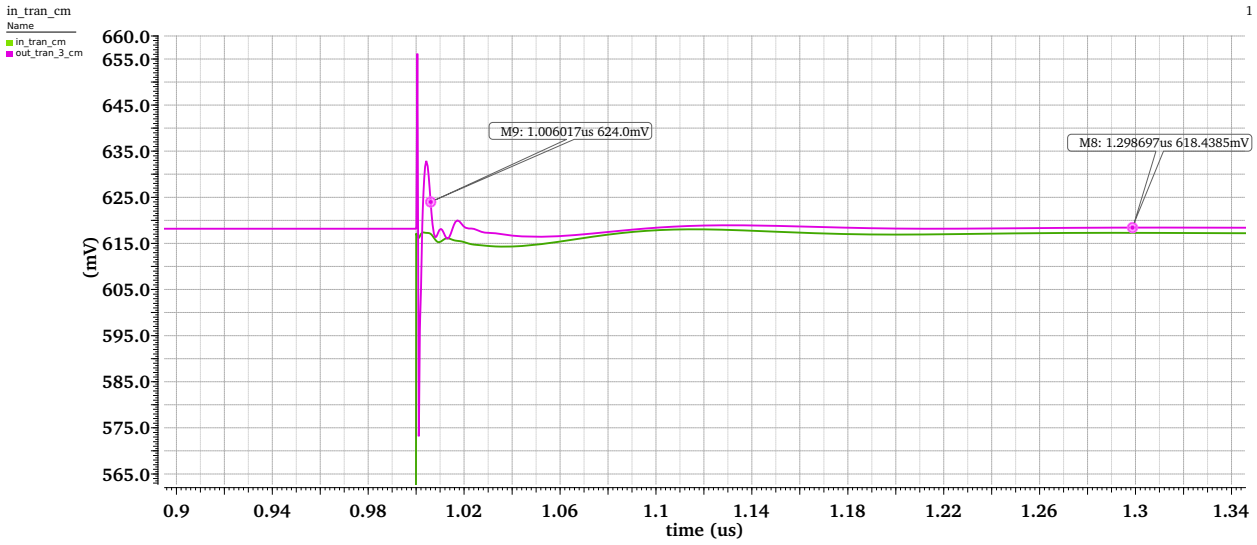

Figure 36: Transient simulation of 200mv common mode step (settling to within 1% shown)

3.3.6 Noise

Due to slight DC gain in the filter at nominal supply, we report both input- and output-referred noise power integrated from 1 to 20MHz, and the output noise spectrum is shown in Fig. 37.

Referred to	Noise Power (nV^2)
Output	88.2
Input	64.2

With this, we still meet the dynamic range specification just as easily as with the pseudo-differential filter. However, the noise contributions are very different this time around. With the filter resistors in series with the signal path, they become the dominant contributor to output noise. The second highest contribution is the thermal noise from the NMOS current sources in the OTA. The input pair and load transistors fall further down in the list of contributors.

3.3.7 Linearity

To maximize the performance under ±30% supply variation, we had to compromise on the linearity of the filter by optimizing the V^* of the input pair and the allowable swing at the output to achieve a THD of **0.966**%. If the filter is tuned to not have DC gain, the linearity would be slightly better. The spectrum of the output from harmonic balance simulation is shown in Fig. 38

4 Checkpoint 4

4.1 Schematic Design Testbench

For this checkpoint, the design is unchanged from Checkpoint 3. Please refer to Section 3.1 for the circuit design and Section 3.2 for the testbench.

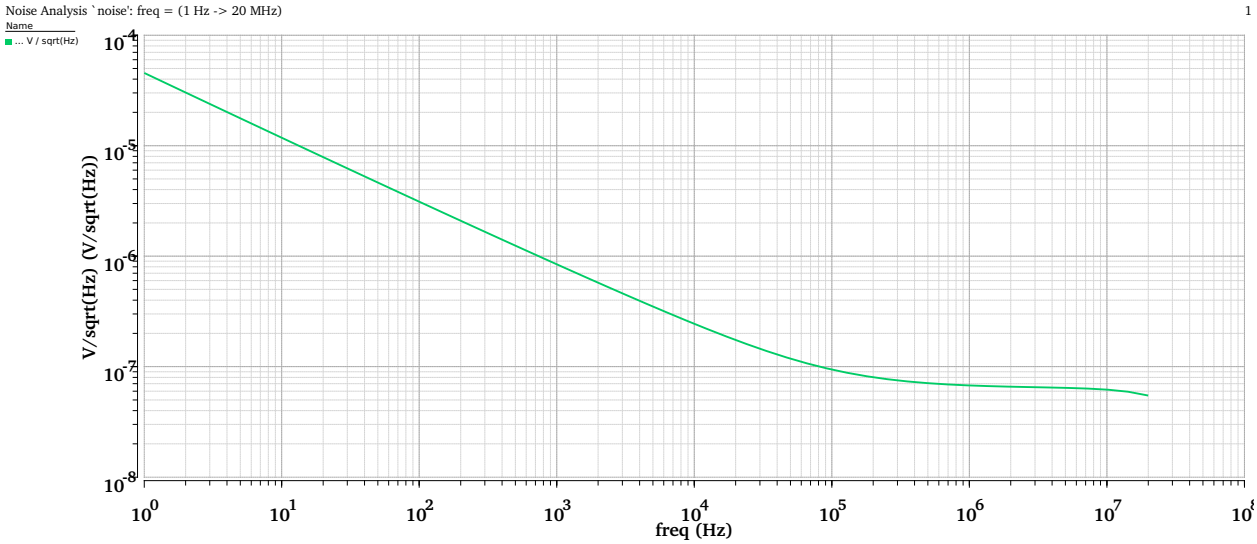

Figure 37: Output noise spectrum of full filter at nominal supply.

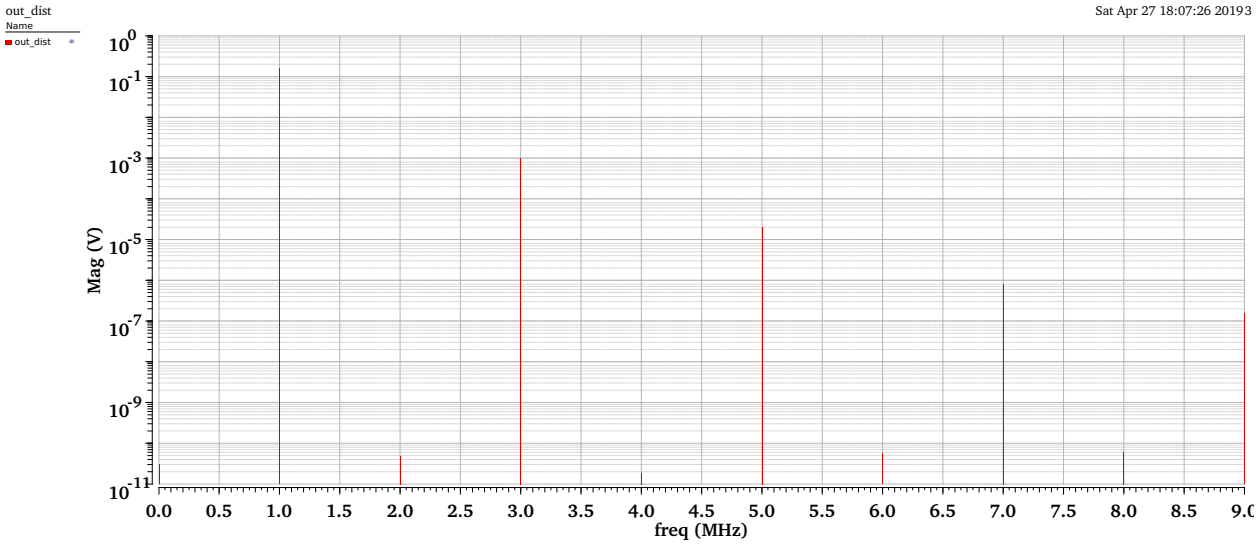

Figure 38: Harmonic balance simulation results

Corner	DC gain (dB)	Stopband Att.(dB)	Group Delay Variation (ns)	CMRR (dB)
nominal	1.91	-56	0.301	-60.2
0.96 V	0.265	-59.7	0.403	-54.7
1.44 V	3.57	-52.1	0.290	-67.6
-40 C	4.39	-50	0.322	-70
85 C	0.781	-58.5	0.385	-57.5

Table 1: AC response over corners

4.2 Performance

The filter is simulated over the following corners:

- 1.2 V, 25 C (nominal)
- 0.96 V, 25 C
- 1.44 V, 25 C
- 1.2 V, -40 C
- 1.2 V, 85 C

4.2.1 AC Response

The AC response and group delay is plotted in Figs. 39 and 40 and the CMRR is plotted in Fig. 41. The performance over corners is tabulated in Table 1. The filter is Bessel, so there are no gain ripples in the passband and it is excluded from the table. Furthermore, attenuation at the passband corner is >-3dB across all corners as well because the corner frequency is above 20MHz.

We find that the stopband attenuation is the specification that does not quite meet at high supply and low temperature, due to excess DC gain. In these corners, there is higher current in the OTA because the transistors in the constant-g_m bias circuit are not very long-channel devices. As the supply decreases or mobility decreases (with higher temperature), the effective mirror ratio drops, causing the g_m to be higher. CMRR likewise degrades with lower supply and higher temperature due to lower saturation margins on current sources.

4.2.2 Dynamic Range

The noise simulation is repeated over all the corners and the input-referred noise power is tabulated in Table 2. All corners continue to easily meet the dynamic range spec, where the noise power must not exceed 200 nV^2. The input-referred noise power spectral density is plotted in Fig. 42.

As expected, the input-referred noise is worse at lower voltages due to lower passband gain, and worse at higher temperatures due to higher thermal noise.

4.2.3 Power

The filter's power is tabulated across all corners in Table 3.

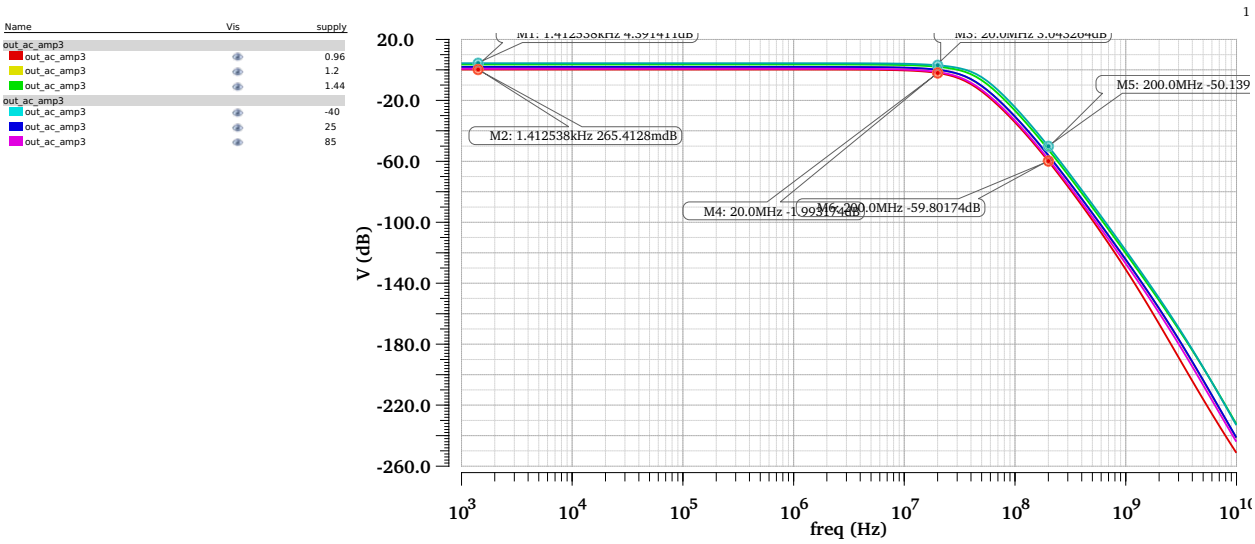

Figure 39: Filter AC response across temperature and supply

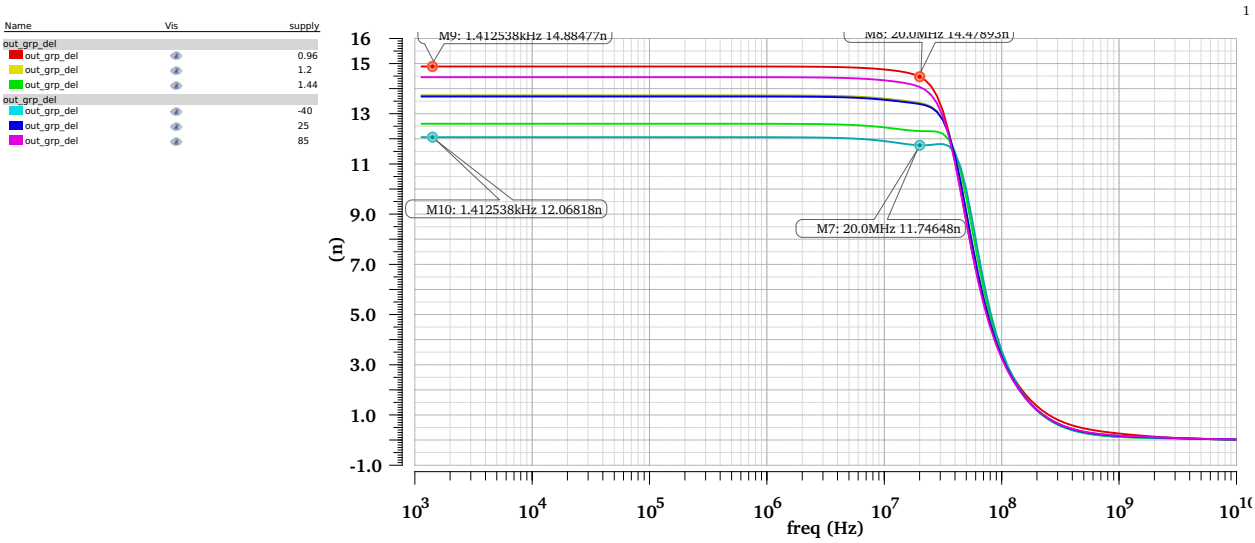

Figure 40: Filter group delay across temperature and supply

Corner	Noise (nV^2)
nominal	64.17
0.96 V	77.7
1.44 V	55.51
-40 C	39.4
85 C	87.85

Table 2: Input-referred noise power over corners

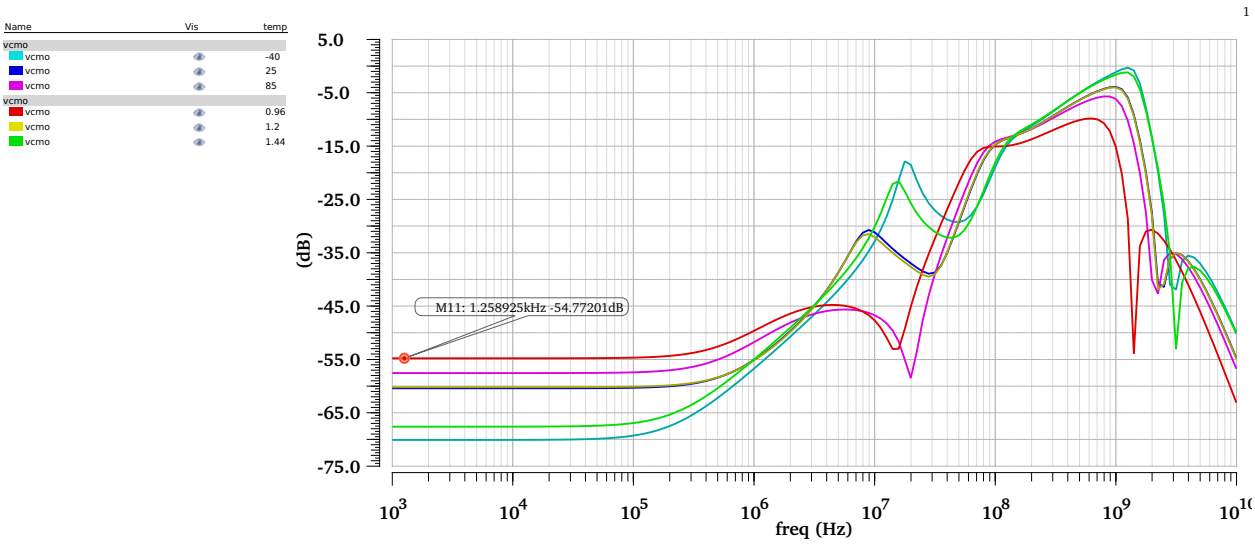

Figure 41: CMRR across temperature and supply

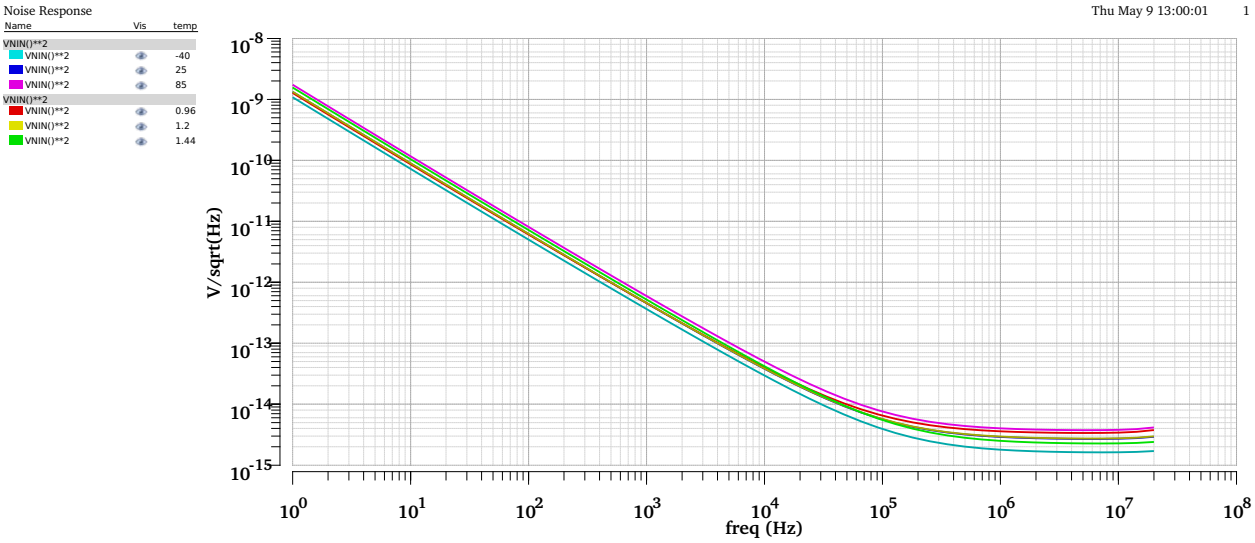

Figure 42: Input-referred noise spectral density over corners

Corner	Power (μW)
nominal	364
0.96 V	221
1.44 V	629
-40 C	629
85 C	367

Table 3: Power consumption over corners

Corner	Settling Time (ns)
nominal	7.5
0.96 V	8.4
1.44 V	5.4
-40 C	5.8
85 C	7.1

Table 4: 200mV common-mode step settling time over corners

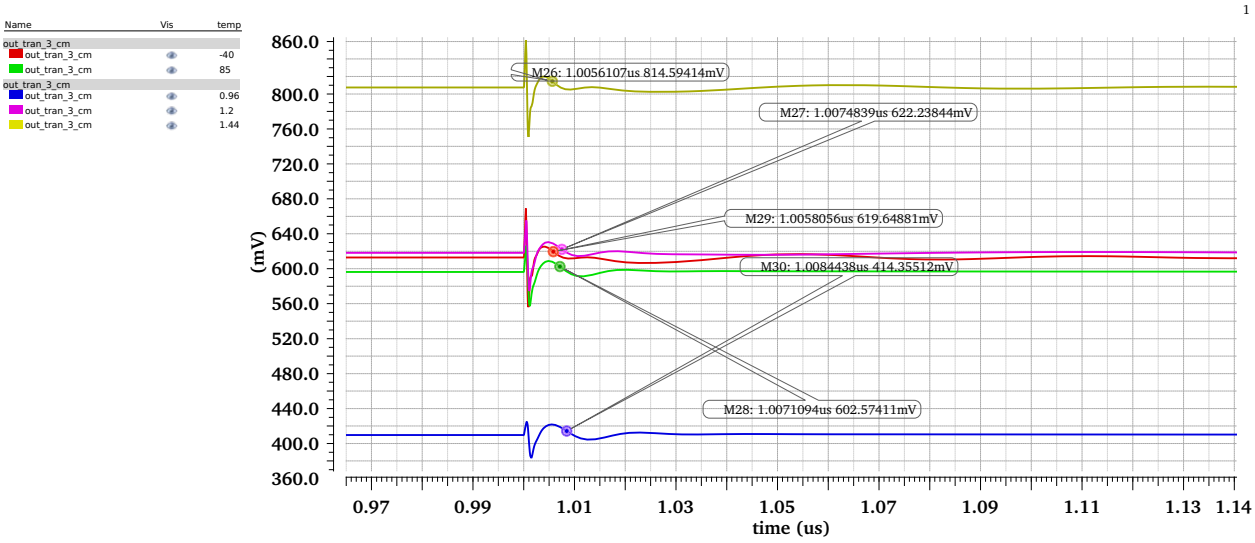

Figure 43: Settling of a 200mV CM step (with 1% points marked) over corners

4.2.4 Stability & Settling Time

The filter is stable in all corners in response to a 200mV common-mode and differential-mode step. The transient simulations are shown in Figs. 43 and 44. The settling time is calculated by finding when the voltage settles within 1% of its final value. This is tabulated in Tables 4 and 5.

We can see that across all corners, the CM settling time is well over 2× faster than the differential mode settling time.

Corner	Settling Time (ns)
nominal	37.8
0.96 V	42.7
1.44 V	31.5
-40 C	29.2
85 C	42.8

Table 5: 200mV differential-mode step settling time over corners

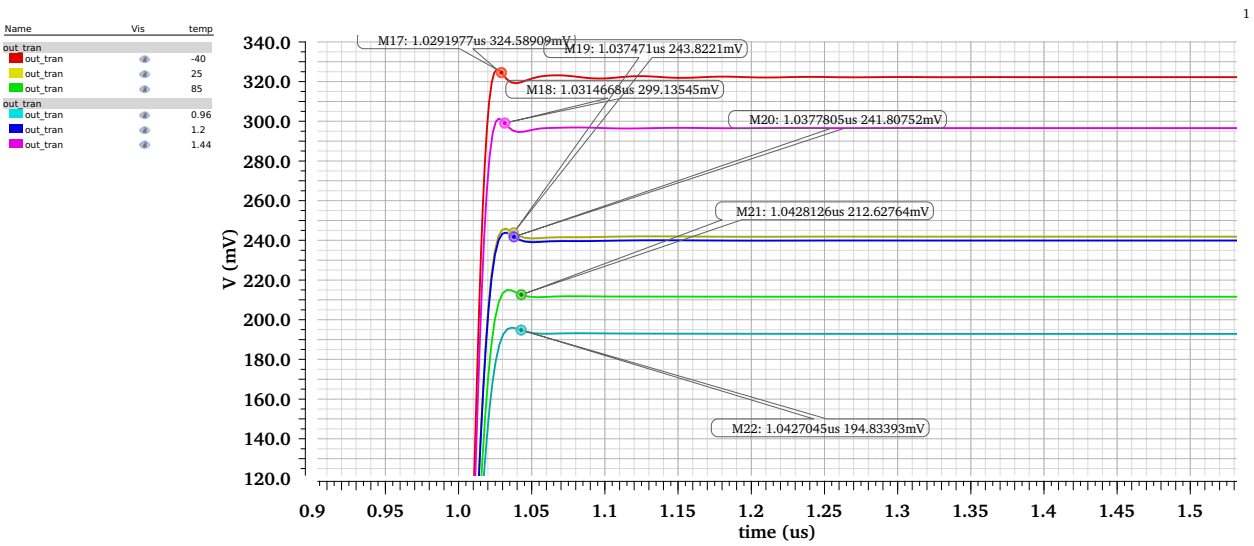

Figure 44: Settling of a 200mV DM step (with 1% points marked) over corners

Corner	THD (%)
nominal	0.966
0.96 V	1.67
1.44 V	0.451
-40 C	0.742
85 C	0.824

Table 6: THD over all corners

4.2.5 Distortion (Harmonic & Intermodulation)

The THD is tabulated for all corners in Table 6 and we sweep the input amplitude and plot the THD in Fig. 45. The THD varies from 0.00889% at -40dBc to the nominal 0.966% at 200mVpp input swing. As expected, a lower supply increases the distortion due to decreased headroom in all of the transistors.

We sweep the blocker amplitude at 40 and 60MHz and find when the input-referred IM at 20MHz exceeds the input-referred noise voltage. This occurs at approx. 145mVpp, as shown in Fig. 46.

5 References

We found the book, "Continuous-Time Active Filter Design" by T. Deliyannis et al. to be very useful in deriving simple design equations and choosing topologies. Ahkab, a symbolic Python circuit simulator, helped us greatly with more complex calculations such as noise analysis.

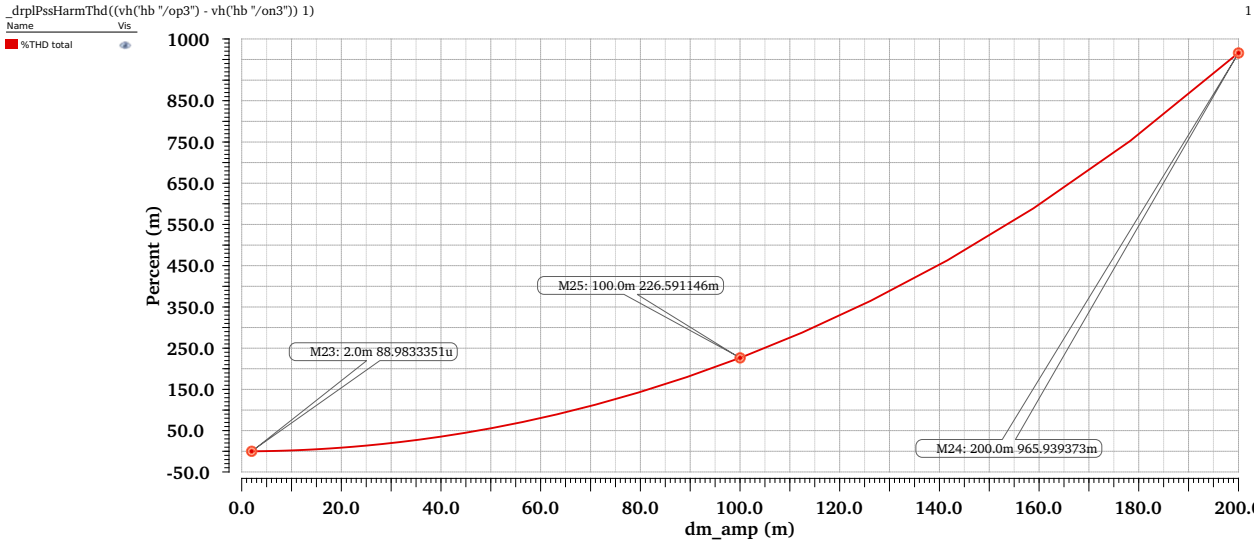

Figure 45: THD at output with varying input differential signal peak-to-peak amplitude

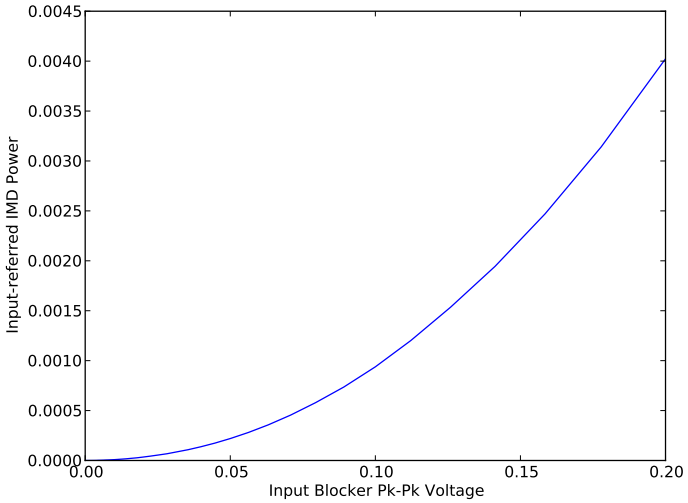

Figure 46: IMD input-referred power with swept blocker peak-to-peak amplitude