Class Project: Op-Amp RC Filter Design

EE 240B, Spring 2019
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This project is a key part of learning for this course and is required to pass the class. You may work alone or in teams of two. If working in teams, each student should submit a report (two identical submissions are allowed). There are four project checkpoints / deadlines. Please ensure on-time delivery of each project component to receive full credit. Late submissions will only receive 50% credit.

Project Description

In this project you will design an active, fully differential filter using op-amp (or OTA) RC filter stages in CMOS. You may not design a Gm-C filter. The design must be closed-loop. The specifications for the filter are summarized below:

1) Gain and BW: Gain of 0dB with a 3-dB bandwidth of 20 MHz
2) 55 dBc out-of-band attenuation at 200 MHz
3) Maximum in-band group delay variation of 3nsec
4) Dynamic Range of 50 dB (integrated over the band from 1 Hz to 20 MHz)
5) Capable of driving a load capacitance of 40 fF
6) Supply voltage of 1.2V
7) Minimum power consumption
8) Gain ripples less than 1-dB. In other words, if the transfer function can only vary by 1-dB near the passband.
9) Stable when driven by a 200mV differential step.
10) Common mode rejection of 60 dB.
11) Common-mode settling time equal to half the differential mode settling time.
12) Optional: THD < 1% when driven by a 200mV differential input 1 MHz sinusoid (peak-to-peak amplitude)

You may use design equations and tools readily available to come up with the filter design. If you are not familiar with filter design, do some background reading (not extensive, just enough to understand the specifications), for example Texas Instruments has nice applications notes. You can also consult the 142/242A filter lab, “Ladder Filter Design, Fabrication, and Measurement” and ignore the “fabrication” part.

Note: The THD spec is optional because it requires some background knowledge from 142/242A.

Checkpoint 1 (2 weeks)

Due Date: Monday March 18
Points: 25%

For your first project checkpoint, you need to answer the following questions:

1) What filter order and family best meets the desired specifications (Butterworth, Chebychev, Inverse-Chebychev, Bessel, …)?
2) Choose the filter topology. You can use Multiple Feedback, Biquads, or Tow-Thomas biquads, or others.

3) For the active stage, choose between an op-amp or an OTA. Explain your choice. You may choose to have a combination of OTA/op-amps for different stages.
4) What are the OTA/op-amp specifications in terms of gain-bandwidth, gain, output resistance, and other specifications. Specify each stage.
5) Size resistors and specify input noise requirements for the OTA/op-amp to meet dynamic range requirements.
6) Estimate the power consumption of your design based on these requirements. Do not run transistor level simulations on the entire circuit (except on a single device). Use general concepts to perform the design.

To provide these answers, you must do calculations, perform behavioral level Spice simulations, and iterate until you are satisfied with your design. Note that many applications notes prescribe a GBW about 10X the filter corner frequency. This is a very rough estimate and you can improve the power consumption of your design by being less conservative. On the other hand, you don't want the filter response to be determined to a large extent by the op-amp or OTA, so exercise some restraint in making the design too aggressive. Ultimately make a decision based on system level simulations and your calibration procedure.

You are highly encouraged, but not required, to use BAG to automate this step the design. If you take this route, you are in a good position to do the bonus project described below.

Checkpoint 2 (4 weeks)

Due Date: Monday April 8
Points: 40%

In this second phase of the project, you will be designing the OTA or op-amp to meet the specifications at the transistor level. Your design must be fully differential, and while you must provide common-mode feedback and biasing, you can use an ideal current source and an ideal CM feedback network. Please demonstrate the following performance specifications by providing schematics simulations results:

For the OTA:

1) Differential-mode step response stability in unity-gain feedback
2) Common-mode step response stability in unity-gain feedback
3) Phase margin larger than 60 degrees in unity-gain
4) Input noise and output noise spectrum
5) Comparison of the filter response at the transistor level to the ideal behavioral model, and also to the filter using an ideal op-amp.
   A. Frequency response
   B. Step response (200mV differential and common-mode step)
   C. Noise
   D. Linearity (THD for 200mV input)

Checkpoint 3 (3 weeks)

Due Date: Monday April 29
Points: 25%

In the previous period, you designed your op-amp except for the biasing and common-mode feedback. In this period, you need to design these blocks. The biasing scheme must be

supply independent. You need to show that you can tolerate a supply voltage that varies +/- 30 % without any appreciable impact on your filter design (except perhaps the swing). You may assume a single external precision 0.1% resistor if you wish. Your schematic should not have any ideal generators (dependent or independent) and all DC sources and precision resistors must be placed in the top level testbench.

The common-mode feedback should be stable (phase margin of 60 degrees). Check stability over the supply voltage variations. The common-mode rejection of a common mode 400mV (peak-to-peak) signal (transient simulation) should be demonstrated.

Checkpoint 4 (2 weeks)

Due Date: Friday May 3 but can be turned in May 10th
Points: 10%

Sketch the layout of the filter and show the detailed layout of the OTA/op-amp separately using stick figures. If you do not have access to a commercial foundry, please inquire about typical sheet resistance for poly resistors and capacitance density of a typical process capacitors.

Your complete project report should have detailed simulations (see checkpoint 2, simulations described in 1-6) using all the transistor level schematics. Show your top level testbench, and sub-circuits for the various blocks. Please do not have a flat schematic and use hierarchy, especially for the op-amp/OTA, biasing blocks, etc. In addition, run the following simulations:

- Report the performance over nominal supply and room temperature and also run simulations with the following variations: Supply +/- 20%, Temperature at -40C, 25C, and 85C.
- Run simulations when the differential input is 200mV (peak-to-peak) and at -40 dB from the peak and report the THD (total harmonic distortion).
- Find the limits of the performance due to intermodulation distortion. Insert "blocker" signals at 40 MHz and 60 MHz and check the intermodulation product at the band edge. Vary the strength of the blockers until the dynamic range is limited by interference rather than noise.

Bonus 1: (5 points on final)

Due Date: May 24

- Discuss calibration strategy and algorithms. Draw schematics, write pseudo-code (or functional verilog-A), and put together a convincing case that you can meet the specifications over process variations.

Include extensive consideration and discussion of strategies to deal with process variation. Local variations will cause the threshold to shift. Ensure that your design stable with variations. How much does the output DC vary? For global variations, assume that in your process all resistors vary by +/- 40 % (sigma) and all capacitors by +/- 20% (sigma). Assume that op-amp/OTA gain varies by 100% (sigma) due to variations in output resistance. You may assume a Gaussian distribution for all variations. Design for 98% yield with 1-dB variations in corner frequency. For simplicity, assume that R and/or C can be tuned with 6-bit accuracy. Note that all resistors and capacitors can be assumed to track each other. Since the corner frequency will vary, please suggest a tuning scheme to deal with this variation and a calibration procedure. Describe in detail how this will be implemented. Run Monte Carlo simulations and

demonstrate the efficacy of your approach. Your target should be less than 1dB variation in gain at the passband.

Bonus 2: (10 points on final)

Due Date: May 24

Now that your design is complete, note that you have done a lot of work and designed a very specific filter. What if the specifications change? It's not uncommon for these changes to occur during the design cycle and this means much of the work has to be repeated. In addition, it's likely that many more projects will require a similar filter. How much of this design can you automate? Use the BAG framework to fully automate the generation of the filter based on the specifications of the filter. You may skip the biasing part but construct an automation framework to go from filter specifications to the output circuit. You can fix the filter family to make things easier. Demonstrate that your tool works by changing the following specifications. Show three designs that meet these three specific changes:

1) Increase 3-dB bandwidth of 40 MHz
2) 46 dBc out-of-band attenuation at 200 MHz
3) Increase dynamic Range to 70 dB (integrated over the band from 1 Hz to 20 MHz)

Note that you must apply each specification change only once (not all there simultaneously).